6.6 15.247(e) Processing Gain Requirement

1. **Theoretical Processing Gain Calculation**

For Chip/symbol rate etc. see the table below:

Bit rate	Chip/symbol rate	Bit/symbol rate	Chip/bit rate
1 Mbit/sec	11	1, DBPSK	11
2 Mbit/sec	11	2, DQPSK	5.5
5.5 Mbit/sec	8	4, CCK	2
11 Mbit/sec	8	8, CCK	1

Extra Information:

(1) For 1 and 2 Mbp/s DQPSK modulation using a fixed spreading sequence the symbol rate is 1 MSymbol/s. The symbol length is 11 chips. Each chip duration is 1/11 uS. A symbol duration is 1 uS.

The chip/symbol rate is 11. The theoretical process gain is 10*LOG(11) = 10 dB.

(2) For 5.5 and 11 Mbp/s CCK where the spreading sequence is a function of the transmitted data, the symbol rate is 8/11 MSymbol/s. The symbol length is 8 chips. Each chip duration is 1/11 uS. A symbol duration is 8/11 uS.

The chip/symbol rate is 8.
The theoretical process gain is 10*LOG(8) = 9 dB. Due to the fact that only 256 code sequences out of the 65536 code sequences that are available are used, there is coding gain. Therefore the processing gain of a CCK system consists of spreading gain and coding gain together. As such a CCK system does meet the FCC requirement for a process gain of minimal 10 dB.

Explanation:

The modulation of this system is compliant to draft standard extension IEEE 802.11b for 5.5 and 11 MBit/s signaling rates. For this modulation technique the Symbol length is 8 Chips (1 Symbol duration equals 8/11 uS). However, the 8 Chips are not a fixed spreading sequence as is the case for the 1 and 2 MBit/s modulation technique. These 8 Chips, applied in a QPSK modulation, use 256 unique patterns out of the 65536 different possible patterns, whereby each pattern represents a specific data sequence (4 or 8 bits). Thus this type of modulation introduces Coding Gain, since only 256 patterns are used out of 65536 possible combinations.

Therefore it can be concluded that the system employs Coding Gain in addition to Spreading Gain.

The Processing Gain of the system is taken as the combined result of Coding and Spreading Gain, so a Processing Gain of 10 dB can be met with 8 Chips per Symbol.

Panasonic has shown by a CW jammer margin test that a SIR of 10 dB can be met, while meeting the system specified BER. It is our understanding that this is compliant with the FCC ruling.

2. Measurement of the Processing Gain

The processing gain is related to the jamming margin Mj as follows [1];

Gp = (S/N)o + Mj + Lsys

Where, Gp : Processing gain
(S/N)o : Signal to noise ratio per symbol
Mj : J/S ratio
Lsys : System losses

When the reference packet error rate PERref is the specified as 8 percents, the corresponding (S/N)o is 16.4 dB. Where, the PERref of 8 percents corresponds to the bit error rate of 10^(-5). The total losses in a system, including transmitter and receiver, should be assumed to be no more than 2 dB according to FCC Public Notice FCC 97-114.
Therefore,

Gp = 16.4dB + Mj + 2dB

The requirement of FCC 15.247 (e) is that Gp should be equal to or larger than 10dB.
When Mj > or = -8.4dB,
Gp = 16.4dB - 8.4dB + 2dB > or = 10dB
As a result the prcessing gain meets the FCC requirement 15.247(e).
The measurements are carried out in condition that the Mj ratio is always -8.4 dB and the resulted packet error rate is measured and evaluated.

3. Measurement results

The measurement procedure, the theoretical calculation for the measurement and the measurement block diagram are shown in the Appendixes A53, A54 and A55 in the submitted Test Report, respectively.
Please find attached list of used measurement equipment to Page A55 of our data.
The test results are shown in the appendixes A56 through A73.
The tests were carried out at channels 1, 6 and 11 in 11Mbps mode.
The test results show that the processing gain is equal to or larger than 10dB.

Result: PASS, based on meeting the requirement of FCC 15.247(e).

Processing Gain Test Equipment

	Instrument	Manufacture	Model No	Caribration Date
Te	Signal Generater	ADVANTEST	TR 4515	April, 2001
2	Step ATTN (1dB step)	Hewlett Packard	8494B	Nov., 2000
3	Step ATTN (10dB step)	Hewlett Packard	8496B	Nov., 2000
4	Power Devider	Anritsu	K240B	April, 2001
5	ATTN (10dB)	Hewlett Packard	8491C	January, 2001
6	Power Splitter	Hewlett Packard	11667A	April, 2001
7	Power Sensor/Meter	Hewlett Packard	438A	April, 2001
8	ATTN (20dB)	Hewlett Packard	33340C020	February, 2001