Bit rate	Chip/Symbol rate	Bit/Symbol rate		Chip/Bit rate
1Mbit/sec	11	1	DBPSK	11
2Mbit/sec	11	2	DQPSK	5.5
5.5Mbit/sec	8	4	CCK	2
11Mbit/sec	8	8	CCK	1

1) For 1 and 2 Mbit/sec mode

The theoretical prosess gain is 10*Log(11)=10dB

2) For 5.5 and 11 Mbits/sec mode

The theoretical prosess gain is 10*Log(8)=9dB

The modulation of our system is compliant to IEEE 802.11b for all signaling rates.
For 5.5 and 11Mbits/sec mode, the modulation technique is CCK (Complementary Code Keying).
For this modulation technique the symbol length is 8 chips. However, the 8 chips
are not a fixed spreading sequence as is the 1 and 2 Mbit/sec mode.
These 8 chips, applied in a QPSK modulation, use 256 unique patterns out of 65536
different possible patterns, whereby each pattern represents a specific data sequence
(4 or 8 bits).
Due to the fact that only 256 code sequences out of the 65536 code
sequences that are available are used, there is coding gain.
Therefore the processing gain of a CCK system consists of spreading
gain and coding gain together.
As such system does meet the FCC requirement for a process gain of minimal 10dB.