

APPENDIX 6
TRANSMITTER ALIGNMENT

TWO (2) PAGE ALIGNMENT PROCEDURE FOLLOWS THIS SHEET

TRANSMITTER TUNE-UP PROCEDURE
FCC ID: AAO2101825

APPENDIX 6

ALIGNMENT PROCEDURES

Important: The FCC requires that any frequency adjustment on a radiophone must be done by authorized person, who is the holder of a current first or second class radiotelephone license.

This unit has been fully aligned at the factory before shipment and does not normally require further adjustment. When necessary, however, the unit may be aligned as indicated below.

Do not adjust any circuit in this radiotelephone unless you understand the circuit operation and have experience adjusting radiotelephone. Tampering with the radiotelephone may upset the alignment and lower its performance.

Test Equipment Required

The following equipment is required for the alignment.

Regulated DC power supply, 0~12V, 1A or higher; or 4.5V, 1A

Audio signal generator, 10Hz~3KHz

Digital multimeter

Deviation meter

Frequency counter, 0~500MHz high impedance

Oscilloscope

RF power meter, 0.5W

High frequency standard generator, >500MHz

Tracking generator, >500MHz

Distortion analyzer

Audio level meter

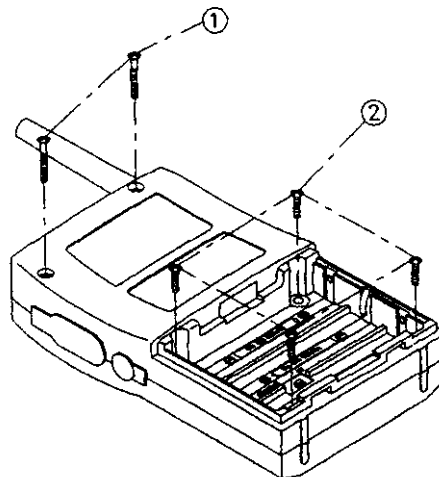
T-coupler

Alignment drivers, etc.

DISASSEMBLY INSTRUCTIONS

To remove the front and rear panels from the main chassis:

1. Remove the two screws from the bottom of the unit.
2. Remove the two screws from the battery compartment.



STEP	ADJUSTMENT	PROCEDURE
1	VC101	Adjust VC101 to obtain demanded TX frequency.
2	L113 L117 L118 L119	Adjust L117, L118, L119 obtain demanded TX power.
3	VR301	1. Inject an audio frequency (AF) -20dBm. 2. Adjust VR302 to obtain maximum TX deviation $\leq 2.5\text{KHz}$. 3. Check MIC modulation sensitivity, and it should be 2.5~10mV.
4		Check CTCSS deviation is normal.
5		Check RX sensitivity is normal.
6	L101 L102 L103 L104 L105 L106 L107 L108 L109	Adjust L101, L102, L103, L104, L105, L106, L107, L108 and L109 to obtain demanded image frequency.
7	VR101	Adjust VR101 to obtain demanded squelch sensitivity.

APPENDIX 7

CIRCUITS AND DEVICES TO STABILIZE FREQUENCY

SYNTHESIZER

A phase locked loop (PLL) circuit establishes and stabilizes operating frequency.

The data for producing necessary frequencies is established by the CPU on the digital board.

The frequency stability of the Tx/Rx is maintained by the TCXO, which generates a stable frequency of 21.25 MHz.

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