THEORY OF OPERATION

GENERAL

This product is a 40-channel, crystal controlled mobile transceiver which consists of a PLL-synthesizer circuit, a receiver circuit, a transmitter circuit. Power is supplied by a car battery (13.8 VDC). Refer to the Block and Schematic Diagrams as you read the following descriptions.

PLL SYNTHESIZER

This product uses a Phase-Locked- Loop (PLL) circuit to synthesize local-oscillator frequencies for receiving and transmitting. It employs one IC and only one crystal. IC1 is a CMOS LSI circuit containing a reference oscillator, phase detector, reference divider (1/4096) and a programmable divider.

The programmable divider directly divides the output of the VCO (voltage-controlled oscillator) circuit down to a 2.5 kHz signal. The VCO circuit consists of D15, Q16 and T6. crystal X1 provides reliable frequency standard which controls the local-oscillator frequency divider inside IC1 counts down the oscillator signal to 1/4096 (2.5 kHz) and passes it on to the phase detector, where it is compared with the 2.5 kHz signal from the programmable divider. An error voltage is generated by the phase detector which is proportional to the phase difference between the two 2.5 kHz signals.

This error voltage from pin 27 of IC1 appears at the capacity collectors of Q10 and Q11 (active low pass filter circuit), where the error voltage is integrated and harmonics and noise are filtered out. The resulting DC voltage is applied to the varicap diode D15. Its capacity varies with the applied DC voltage. Because of this capacity change, the output frequency of the VCO circuit is circuit is corrected. With proper circuit design and precise adjustments, the VCO frequency is accurate and precise when the system "locked".

This means that the phase detector senses no phase differences between the two 2.5 kHz signals, and the VCO circuit generates a frequency that is as accurate and stable as the reference crystal oscillator X1.

The VCO circuit is in the form of a Hartley oscillator and the varicap diode D15 and T6 constitute the tank circuit. The VCO circuit generates a signal ranging from 13.4825 to 16.710 MHz. IC1 also includes an unlock-signal-detector circuit. When the phase is unlocked (when the phase detector senses a phase difference between the two 2.5 kHz signals), the output at pin 18 of IC1, which is normally open, will be shorted to ground. This means that VCO frequency (1/2 carrier for transmitting) is "sunk" to pin 18 of IC1 and the transmitter circuits are inhibited.

TRANSMITTER CIRCUIT

RF Amplification

The output of doubler amp Q19 is fed through doubler tuning (27 MHz) T7 and T8 to the base of RF amp Q20. The output is then supplied through tuning circuit T9 to RF driver amp Q21. The Q21 output capacitance is divided by tuning circuit L7, C103, and C104 and passed through tuning circuit L8 to the base of final RF amp stage Q22. The Q22 output is supplied to the antenna through L13.

Suppression of Spurious Radiation

The tuning circuit (between frequency synthesizer and final amp Q22) and 3-stage "PI" network (C107, L11, C108, L12, C2, L13 and C1) serve to suppress spurious radiation. The network

serves to match Q22 impedance to the antenna and to reduce spurious content to acceptable levels. In-band spurious is reduced to acceptable levels by filtering.

Limiting Power
During factory alignment, the series base resistor (R114) of final amp Q22 is selected to limit the available power.

Modulation
The mic input is fed to mic amp Q14 and then to modulator IC3 which feeds the signal to the modulation transformer T5. The signal is stepped up at T5 and modulated by the B + voltage. Then it is fed through diode D13 to the collectors of Q21 and Q22 to modulate both these stages.

Limiting Modulation
A portion of the modulating voltages is rectified by Q12 to turn on Q13, which attenuates the mic input to mic amp Q14. The resulting feedback loop keeps the modulation from exceeding 100 percent for inputs approximately 40 dB greater than required to produce 50 percent modulation. The attack time is about 18 milliseconds and the release time is about 300 milliseconds.

RECEIVER CIRCUIT

Receiver
The receiver is a double conversion superheterodyne with the first IF at 10.695 MHz and the second IF at 455 kHz. The synthesizer supplies the first local oscillator frequency (10.695 MHz below the receiver frequency) and the second local oscillator frequency (10.240 MHz). The detector (Q7) output provides reverse AGC to all previous stages except Q6. The AGC voltage is also amplified by Q7 and used to drive RF attenuator Q1. Squelch amp and audio amp are included in IC2. IC3 functions as a speaker driver in receiving.

INDICATORS

Channel Indication
When the OUT/CH9/CH19 switch is set to OUT, the channel can be selected by the channel selector SW201 or SW202, and indicated by the 2 digits/7 segments LED LD201. LD201 lights dynamically by the outputs from IC1. The output from pin 8 of IC1 controls the lighting of the first digit through Q9, and the output from pin 9 of IC1 controls the lighting of the second digit through Q8. The outputs from pin 1 to pin 7 of IC1 control the lighting of each segment of each digit.

Ch9/ch19/PA Indication
When the OUT/CH9/CH19 switch is set to CH9(CH19), LD201 flashes and displays "9" ("19").

RX/TX Indication
LD203 (green) functions as a RX indicator during receiving and LD202 (red) functions as a TX indicator during transmission.