Datasheet
GreenPeak GP710

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1 Introduction

The GreenPeak Technologies GP710 System-on-Chip is an IEEE 802.15.4 communications controller for integration into a ZigBee RF4CE[1], ZigBee PRO[2] and/or ZigBee IP node. It is optimized for low cost while providing superior performance. The integrated RF filtering simplifies the RF design complexity enabling low cost single layer applications using simple PCB antennas requiring no shielding and a minimum number of external components. The GP710 supports dual PAN operation with two (RF4CE and ZigBee PRO/IP) protocol stacks in the host processor.

The chip is fully compliant with the IEEE 802.15.4 standard, providing robust spread spectrum data communication with a highly secure encrypted data flow. Its superior Wi-Fi interference rejection capability and antenna diversity offer additional robustness in a crowded wireless 2.4 GHz environment.

The GP710 provides a high-speed serial interface (SPI) to the host processor. The GP710 has an extreme low standby power enabling total system power consumption of less than 1 mW while allowing reception of remote control commands.

[1] For a high-level overview of RF4CE please refer to the "Understanding RF4CE" White Paper on the ZigBee website (http://www.zigbee.org/LearnMore/WhitePapers.aspx).

[2] For a description of the ZigBee PRO Feature Set please refer to the ZigBee Specification Overview on the ZigBee website (http://www.zigbee.org/Specifications/ZigBee/Overview.aspx).

Important Notices

2 Features

Radio
- ✓ 2.4-GHz IEEE 802.15.4-compliant RF Transceiver
- ✓ Excellent receiver sensitivity
- ✓ Robust to (Wi-Fi) Interference
- ✓ Preamble based Antenna Diversity, increasing the range significantly
- ✓ Packet-in-Packet resynchronization
- ✓ Integrated RF filtering limits number of external components
- ✓ Optional LNA and/or PA
- ✓ Targeting compliance with worldwide RF regulations: ETSI EN 300 328 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T-66 (Japan)

Medium Access Control
- ✓ IEEE 802.15.4-compliant MAC
- ✓ CSMA-CA
- ✓ Automatic ACK handling and Retransmissions
- ✓ Dual stack / dual PAN support

Security
- ✓ CCM* encryption and authentication with 128-bit keys

Peripherals and Interfaces
- ✓ SPI Slave serial host interface:

Power Management
- ✓ Low power standby modes:
  16 MHz standby: 600 µA
  External event standby: 250 nA
- ✓ Stand-alone RF4CE DutyCycling support and RF4CE packet filtering when the host is asleep

Dimensions and Layout
- ✓ QFN40 6x6 mm package
- ✓ Supports direct interfacing with printed antennas
- ✓ Supports single layer PCB design
- ✓ No RF shielding required

Environmental Aspects
- ✓ Meets lead-free requirements
- ✓ RoHS compliant
- ✓ Meets moisture sensitivity level 3
- ✓ Peak reflow temperature 260°C

3 Block Diagram

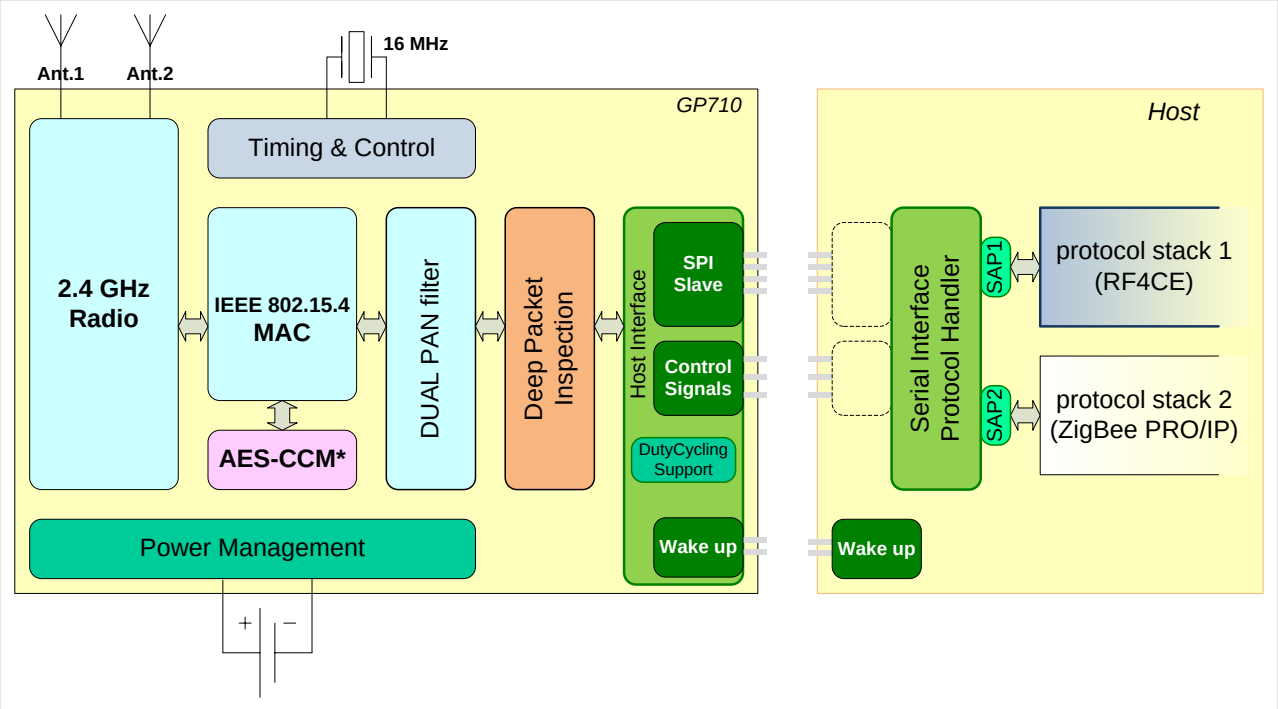


Figure 1: Block Diagram

Figure 1 shows the functional blocks of the GP710 and its signaling interfaces, including supporting software in the host.

4 Functional Description

4.1 Radio and PHY

The GP710 contains an IEEE Standard 802.15.4-2006 compliant transceiver that provides all the functionality for the Physical layer (PHY) specification. The PHY is under complete control of the Medium Access Control (MAC).

4.1.1 2.4 GHz Transceiver

The GP710 supports all the IEEE Standard 802.15.4 defined channels in the 2.4 GHz ISM license-free frequency band, including the three RF4CE channels 15, 20 and 25.

The channel number (k) and center frequency (F_c) relate as follows: $\boldsymbol{F_c = 2405 + 5(k - 11)}$ *in MHz*.

4.1.2 Radio Configurations

The GP710 supports a number of different radio configurations. It can be configured to use antenna diversity, or it can use a different receive and transmit antenna. A few different sample configurations are depicted below. For applications with an external LNA and/or PA (to increase the link budget) please refer to Application Note.

4.1.2.1 Antenna Diversity

Preamble based antenna diversity enables the PHY to choose the optimal antenna for every individual packet, and increases the performance of the receiver in environments that are dominated by multipath fading effects and interference situations. In RX mode the PHY selects the antenna based on the best signal quality (signal-to-noise/interference ratio).

For typical indoor usage in an environment with 50 ns delay-spread and 2 MHz signal bandwidth using the Rayleigh fading model, antenna diversity with 2 antennas results in a ~9 dB improved link budget (at a 1% outage probability) compared to no antenna diversity. This translates into 80% more range (using a log-distance breakpoint model[3] with path loss coefficients g1=2 (free space propagation) and g2=3.5 above the breakpoint at 10 m).

Unless configured otherwise, the GP710 will use the same antenna for transmission as the one that was used for the reception of the last packet.

[3] Refer to "T.S. Rappaport, Wireless Communications – Principles & Practice, Prentice Hall, 1996" for this model.

Sample Configuration 1 (Figure 2):

- Antenna diversity disabled
- Using antenna 1 (RF Port 1) for both RX and TX

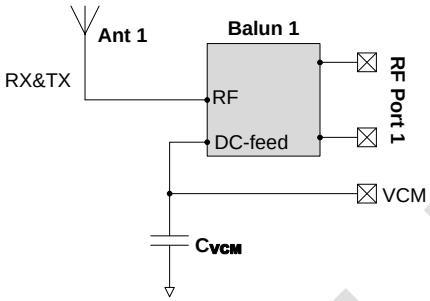


Figure 2: No Antenna Diversity

Sample Configuration 2 (Figure 3):

- Antenna diversity enabled
- TX on same antenna as was selected best by RX, or if preferred on antenna 1 only

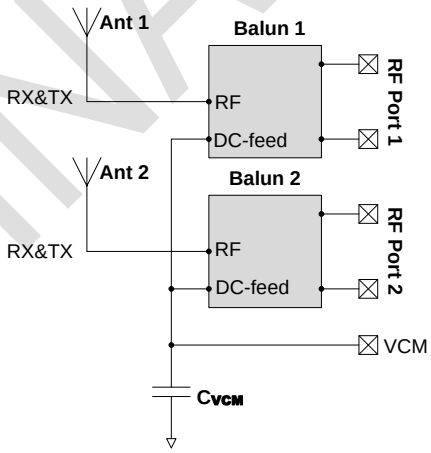


Figure 3: Antenna Diversity

Sample Configuration 3 (Figure 4):

- Antenna diversity enabled
- TX on same antenna as was selected best by RX, or if preferred on antenna 1 only
- Symmetrical antennas

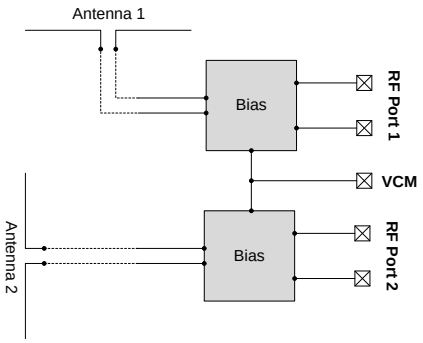


Figure 4: Symmetrical Antennas

4.1.3 Wi-Fi Robustness

When a traditional receiver is located close to a strong Wi-Fi interferer, its receiver front-end is forced into compression, resulting in a reduction of the front-end gain and desensitization of the receiver beyond the point where communication is possible. The IEEE 802.15.4 Wi-Fi rejection specification specifies the robustness against Wi-Fi interference at a distance relatively far away and does not account for nearby interference.
The GP710 is able to dynamically adapt to the presence of Wi-Fi interference and maintain communication which would otherwise have been lost.

4.1.4 Packet-in-Packet Resynchronization

If the GP710 is receiving a packet from one node and is interrupted by the reception of another stronger packet from another node, the receiver will resynchronize to the latter and continue to receive and process this packet. This allows one packet (the strongest) to be received where otherwise both packets would have been lost. Packet-in-Packet collisions can occur in situations when neighbor network packets are received at a low level and in hidden node situations where not all nodes can see each other.

4.1.5 RSSI and Link Quality Indication

The PHY's RSSI circuitry measures the received signal energy level, and the internal value is converted to dBm values. See Receiver Characteristics (5.4 below) for the range and accuracy.
For each received data packet also a link quality indication (LQI) is determined, for use at the network and application layers.

4.2 Medium Access Control (MAC)

The GP710 implements all ZigBee-required MAC features of the IEEE Standard 802.15.4-2006. The MAC provides a packet-level service and handles packet transmissions and receptions autonomously, including:

- Performing CSMA-CA to avoid collisions when transmitting packets;
- Adding CRC and Sequence number;
- Acknowledgement handling for transmitted packets, including automatic retransmissions;
- Dual Address recognition and packet filtering on received packets, including CRC checking;
- Acknowledgement handling for received packets, including automatic acknowledge transmission;

4.3 Security Engine

The GP710 is equipped with a low power Security Engine, that can work independently from the PHY and MAC.

The Security Engine is capable of:

- CCM* encryption, decryption and authentication with 128, 192 and 256-bit keys
- AES encryption with 128, 192 and 256-bit keys

However, for ZigBee protocols only the 128-bit CCM* is used.

4.4 Host Interface

Communication between the GP710 and the host processor is done via a serial interface, SPI, and some control lines. Software libraries are provided for handling the serial interface and supporting the RF4CE protocols in the host processor.

4.4.1 Dual Stack / Dual PAN Support

The GP710 provides two (2) MAC **Service Access Points** (SAPs) to the protocol stacks in the host, supporting communication over two PANs; one for each protocol stack in the host.
Note: The PANs need to be on the same RF channel.

When the host is asleep, the GP710 handles the **RF4CE duty cycling** and features RF4CE Network layer and Profile layer packet inspection.

4.4.2 Control Signals

The GP710 features the following control signals; for the Pin Assignments see chapter 6, Table 15.

- RESETn allows the host processor to reset the GP710.
- WKUP allows the host processor to wake up the GP710 from standby.
- MCU_INTOUTn line is an interrupt output to the host processor.
  The GP710 may use this signal to wake up the host processor when it requires attention from the host processor (e.g. a message from the remote node has been received, or the device has completed its initialization after power-on).

4.4.3 SPI Slave Interface

The SPI slave interface uses SPI mode 0 and supports SPI clock frequencies up to 16 MHz.

SPI is a 4-wire synchronous peripheral interface consisting of the following signals:

	Host	
SPI_SCLK	(output)	The clock signal generated by the SPI master (the host processor); used to time the reading and writing of data.
SPI_MOSI	(output)	Carries the information going from master to slave (so, to the GP710).
SPI_MISO	(input)	Carries the information sent from the slave to the master (so, to the host processor).
SPI_SSn	(output)	The slave select signal; used by the master to select the slave it wants to communicate with.

In order to communicate with the GP710, the host processor should implement a specific protocol over the serial interface. Information is exchanged in units of 8 bits (“octets”), and the first bit received or transmitted is the most significant bit (MSB).

Each transaction is initiated by the host processor sending a command. A command contains a command identifier (ID, Table 1), a register address, optionally a length field and/or data. See Table 3 for the command structure. The GP710’s response contains a synchronization code (Table 2, bit 7 = MSB), and optionally data. The data can be one byte or a block of up to 32 bytes (one byte per octet).

Table 1: Command Identifier

Command ID	Command
‘00’b (0)	Read a byte
‘01’b (1)	Write a byte
‘10’b (2)	Read a block
‘11’b (3)	Write a block

Table 2: Synchronization Code

bit	Name	Description
0	Synchronization	Always 1
1	ReadNotWrite	0 = write command; 1 = read command
2	SingleNotBlock	0 = single byte command; 1 = block command
3	Bus Error	1 = Bus access resulted in error
4	Reserved	
5	Bus Time Out	1 = Bus access timed out
6	Reserved	
7	Reserved	

Table 3: Command Structure

Command	Command Structure
Read a byte	Command ID (2 bits) – Address (14 bits)
Write a byte	Command ID (2 bits) – Address (14 bits) – Data (8 bits)
Read a block	Command ID (2 bits) – Address (14 bits) – Length (8 bits)
Write a block	Command ID (2 bits) – Address (14 bits) – Length (8 bits) – Data (n*8 bits)

Table 4: Response Structure

Command	Response Structure
Read a byte	Synchronization Code (8 bits) – Data (8 bits)
Write a byte	Synchronization Code (8 bits)
Read a block	Synchronization Code (8 bits) – Data (n*8 bits)
Write a block	Synchronization Code (8 bits)

Each transaction is initiated by the controller selecting the slave - SSn going low - and sending a command on the MOSI line. The GP710 sends its response on the MISO line. Because the MISO line stays low during the command, the first non-zero octet is the synchronization code. After the GP710 has sent its response completely, the controller ends the transaction - SSn going high. The controller should generate sufficient SCLK cycles to ensure that all available data is received from the GP710.
The timing parameters in the following timing diagrams are specified in section 5.6.

Reading a byte from the GP710

Figure 5 specifies the timing diagram when reading a single byte from the GP710. The command starts with the 2-bit command ID. Next is the 14-bit address of the data byte to be read; the 'Address0' field contains the 6 most significant bits, and the 'Address1' field contains the least significant part of the address. After the read command has been processed, the GP710 will send the 8-bit synchronization code, followed by the actual data (1 byte) that was requested to be read.

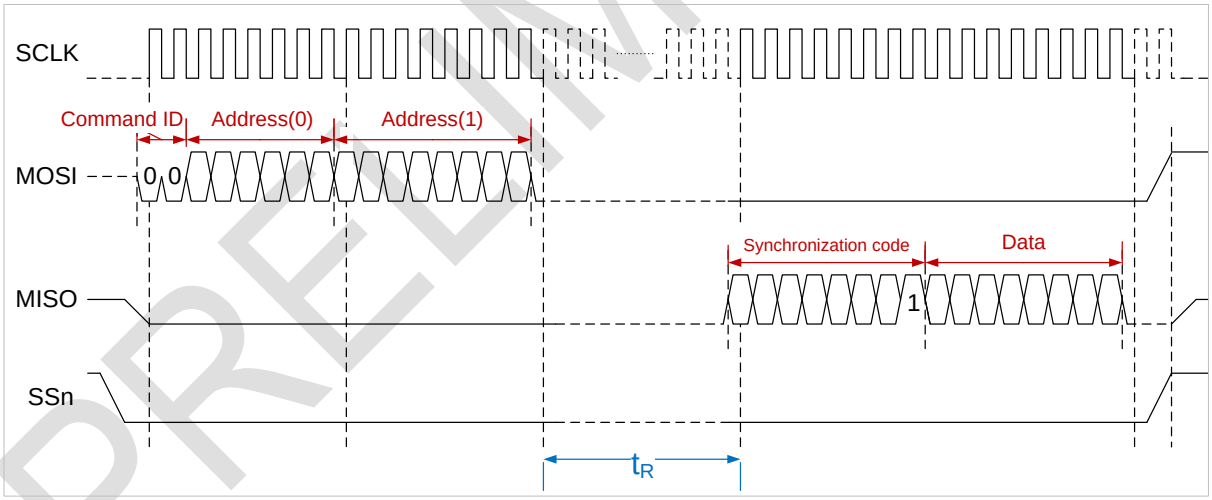


Figure 5: Read a Byte - Timing Diagram

Writing a byte to the GP710

Figure 6 specifies the timing diagram when writing a byte to the GP710. The command starts with the 2-bit Command ID. Next is the 14-bit address of the data byte to be written. The next byte is the actual data (1 byte) to be written. After the write command has been processed, the GP710 will send the synchronization code.

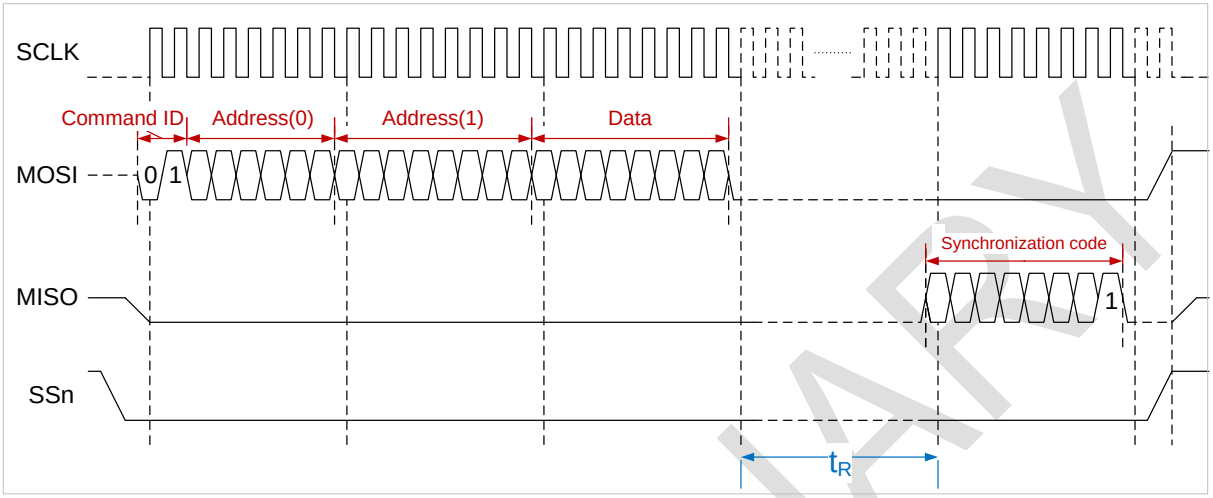


Figure 6: Write a Byte - Timing Diagram

Reading a block from the GP710

Figure 7 specifies the timing diagram when reading a block of bytes from the GP710. The command starts with the 2-bit command ID. Next is the 14-bit address of the first data byte to be read. The next octet indicates the number of bytes to be read. The data will be read from successive registers. After the read command has been processed, the GP710 will send the synchronization code, followed by the actual data (n bytes) that was requested to be read.

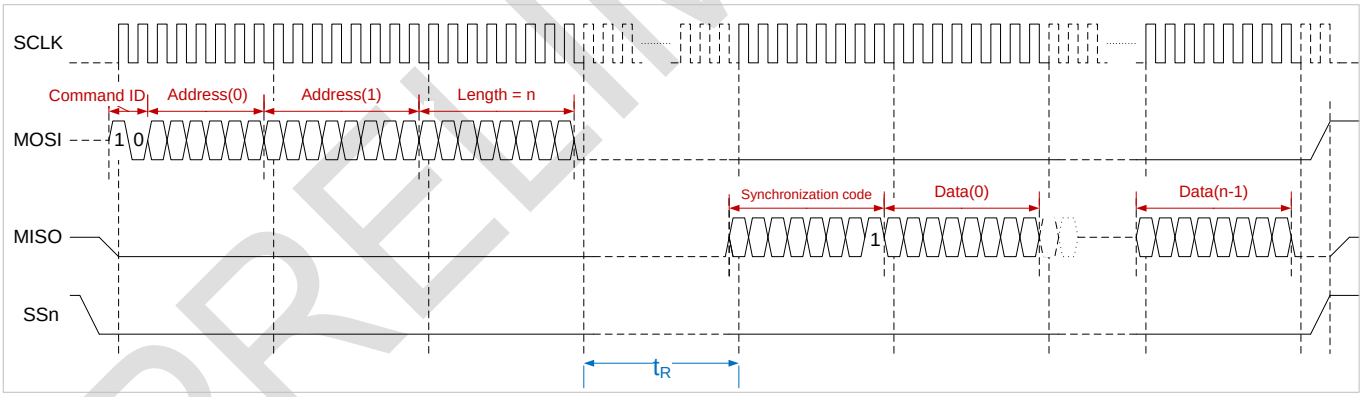


Figure 7: Read a Block - Timing Diagram

Writing a block to the GP710

Figure 6 specifies the timing diagram when writing a block to the GP710. The command starts with the 2-bit Command ID. Next is the 14-bit address of the first data byte to be written. The next octet indicates the number of bytes to be written, followed by the actual data (n bytes) to be written. The data will be written to successive registers. After the write command has been processed, the GP710 will send the synchronization code.

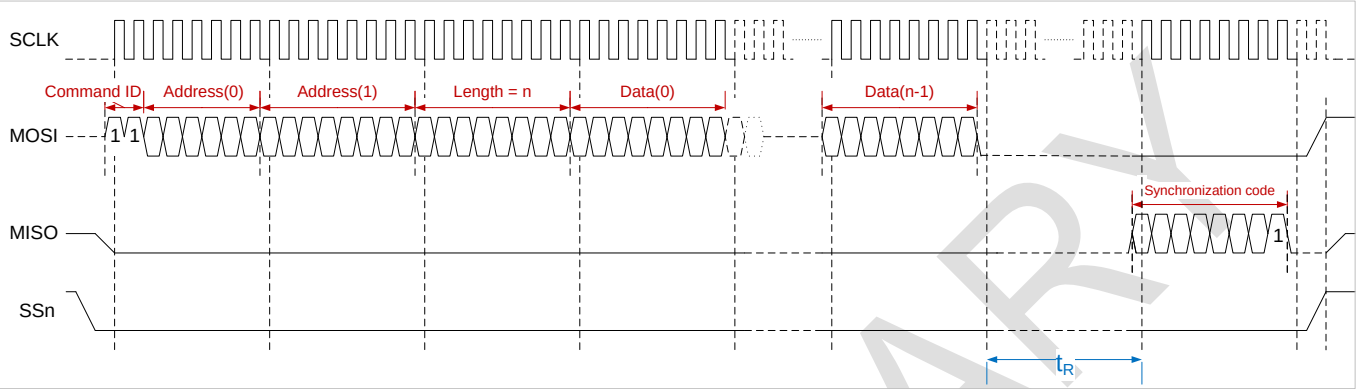


Figure 8: Write a Block - Timing Diagram

4.5 Timing and Control

The GP710 is designed to work in an environment where low power consumption is important. To achieve the low power consumption in between different receive and transmission cycles, the GP710 is put in a standby (or sleep) state.

The GP710 uses the following standby modes (see section 5.3 Table 7 for the power consumption):

Event : The GP710 can only be woken up by an external event, from the host processor. Only a small section of the chip is active, resulting in an ultra low standby current.

16 MHz : The time base is delivered by the 16 MHz crystal oscillator that is also used as the system clock for the rest of the GP710.

5 Electrical Characteristics

The GP710 characteristics are determined in the circuit shown in Figure 9 below:

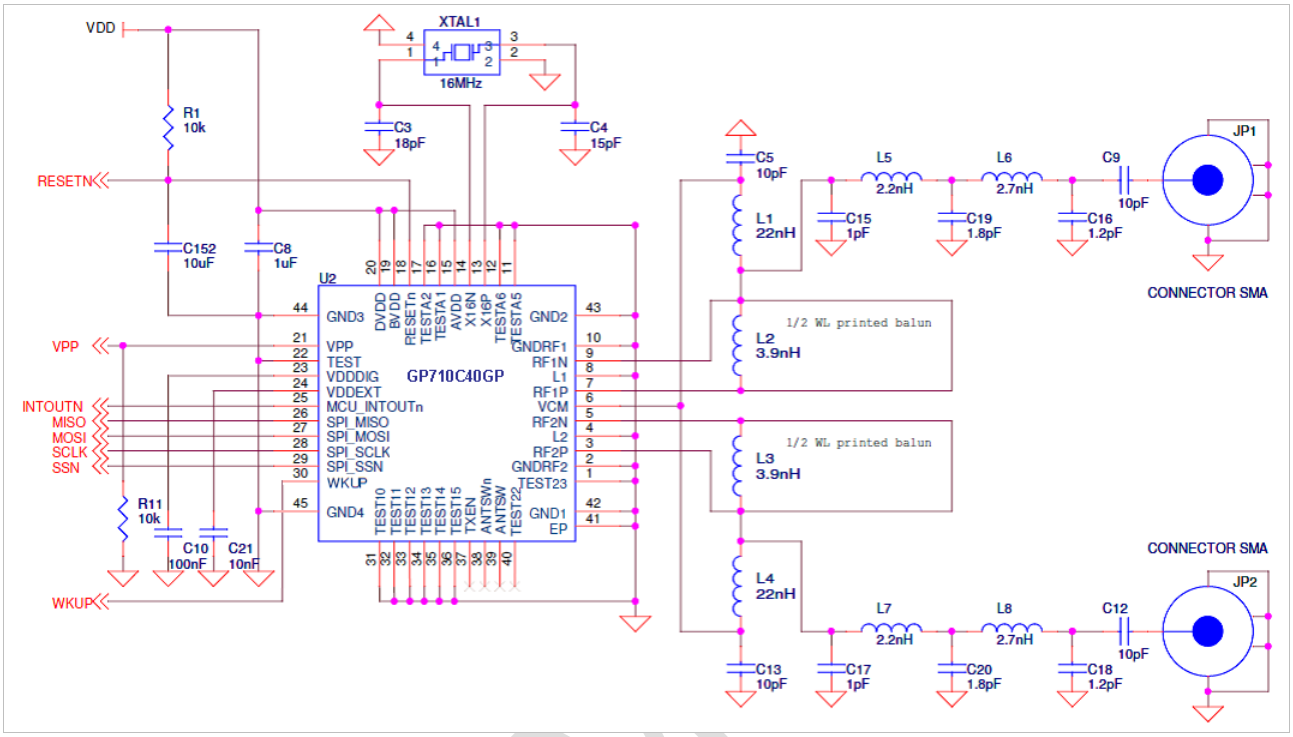


Figure 9: Parameter Evaluation Circuit

Transmit as well as receive behavior is measured in accordance with the IEEE 802.15.4 specification. Receiver characteristics are measured in normal receive mode, unless otherwise specified.

For optimum TX power efficiency and RX sensitivity the baluns should present a conjugated match to the impedance of the RF ports. The differential output impedance of these ports (on the pins of the chip) is 176 Ω in parallel with 0.9 pF.

All parameters are measured at AVDD=DVDD=BVDD=3.0V, T_A=25°C and F_{SCLK}=16MHz, unless otherwise specified.

Channel rejection is measured with the GreenPeak RD05 reference design system as interferer.

Full information on the reference design used is available from GreenPeak upon request.

The term “VDD” is used to refer to AVDD, DVDD and BVDD as a common supply.

5.1 Absolute Maximum Ratings

Table 5: Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
AVDD, DVDD, BVDD	Supply Input Voltage		-0.3 to +3.6	V
All Digital I/O pins (see Table 15)	Digital IO Voltage		-0.3 to DVDD+0.3 (Max = +3.6)	V
X16P, X16N	Analog IO Voltage		-0.3 to +2.1	V
VDDEXT	Decoupling Voltage		-0.3 to +3.6	V
RF1P, RF1N, RF2P, RF2N	RF IO Voltage		-0.3 to +2.1	V
VDDDIG, VCM	LDO IO Voltage		-0.3 to +2.1	V
VPP	OTP Program Voltage		-0.3 to +9.25	V
P_{MAX}	Input RF level		+20	dBm
T_J	Junction Temperature		+125	°C
T_{stg}	Storage Temperature		-50 to +150	°C
T_{sol}	Reflow Soldering Temperature		+260	°C
	ESD HBM (Human Body Model)	non-RF pins:	< 2000	V
		RF pins:	< 300	
	ESD CDM (Charged-Device Model)	non-RF pins:	< 750	V
		RF pins:	< 1000	
	ESD MM (Machine Model)	non-RF pins:	< 125	V
		RF pins:	< 50	

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AVDD, DVDD, BVDD	Power Supply Voltage		2.1	3.3	3.6	V
VPP	OTP Program Voltage (Non-zero voltage only applies during the programming cycle. Outside this cycle, the voltage should be removed as soon as possible; pin should be pulled low.)	The total duration of the voltage should not exceed 80 s. Overshoots should be avoided.	8.5	9.0	9.25	V
T_A	Ambient Temperature		-40	+25	+85	°C
F_{ref}	Reference Crystal Oscillation Frequency			16		MHz
V_{IL}	Input Low Voltage for all digital IO lines		GND		0.5	V
V_{IH}	Input High Voltage for all digital IO lines		VDD - 0.5		VDD	V

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{OL}	Output Low Voltage for all digital IO lines	VDD	Drive Strength	I_{OL} (*)				
		2.1 V	2 mA 4 mA 6 mA 8 mA	2 mA 4 mA 6 mA 8 mA			0.5	V
		3.3 V	2 mA 4 mA 6 mA 8 mA	3 mA 6 mA 9 mA 12 mA			0.5	V
V_{OH}	Output High Voltage for all digital IO lines	VDD	Drive Strength	I_{OH} (*)				
		2.1 V	2 mA 4 mA 6 mA 8 mA	-1.5 mA -3 mA -4.5 mA -5.5 mA	VDD - 0.5 - VDDIO_drop (**)			V
		3.3 V	2 mA 4 mA 6 mA 8 mA	-3 mA -5.5 mA -8 mA -10 mA	VDD - 0.5 - VDDIO_drop (**)			V
notes:	* I_{OL} / I_{OH} : positive value: pin is sinking current; negative value: pin is sourcing current. ** VDDIO_drop (typical, at 3V and 25°C) = 14 Ω * total I_{OH} current.							
I_{OH}	Total sourced current for all digital output lines combined						16	mA

5.3 Current Consumption

Table 7: Current Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{active}	Active Modes (Measured on AVDD+DVDD, in IEEE 802.15.4 channel 20)	RX		21	25	mA
		TX @ 0 dBm		20	25	
		TX @ -25 dBm		16		
I_{idle}		Idle		2.8	3.8	
$I_{standby}$	Standby Mode (Measured on BVDD) (Current consumption depends on crystal specification and load capacitance, see section 5.8 below)	Event standby mode		250	2000	nA
		16 MHz standby mode		600	700	µA

5.4 Receiver Characteristics

Table 8: Receiver Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
RF channels	Programmable in 5 MHz steps as defined by IEEE 802.15.4	2405		2480	MHz
Bit rate			250		kb/s
Chip rate			2.0		Mc/s
Receiver sensitivity	As defined in IEEE 802.15.4 (Measured in IEEE 802.15.4 channel 20) Nominal Test Conditions: Over temperature and voltage range:		 -93	 -88	dBm
	Antenna Diversity Gain (refer to section 4.1.2.1 for the channel model)		9		dB
RX carrier frequency offset range	Sensitivity loss < 1 dB	-220		+220	kHz
	Sensitivity loss < 0.5 dB	-150		+150	
Maximum receive level	1% PER as defined in IEEE 802.15.4		+10		dBm
IIP3	RX mode		-17		dBm
P-1dB RF front-end	RX mode		-27		dBm
Co-Channel rejection	Packet in Packet collision		-10.5		dB
	Non IEEE 802.15.4 Interference (noise)		-2.5		dB
Adjacent channel rejection	As defined in IEEE 802.15.4. IEEE 802.15.4 interferer, +/- 5 MHz		30		dB
Alternate adjacent channel rejection	As defined in IEEE 802.15.4. IEEE 802.15.4 interferer, +/- 10 MHz		45		dB
Far away channel rejection	Wanted signal at -82 dBm. IEEE802.15.4 interferer, +/- 15 MHz		50		dB
Wi-Fi IEEE 802.11g rejection	Wanted signal at -82 dBm Wi-Fi centered at +12 MHz / -13 MHz or higher offset frequency		30		dB
Bluetooth rejection (fixed carrier, rejection of FSK modulated signal with frequency deviation +/- 160 kHz, BT=0.5)	Wanted signal at -82 dBm, Bluetooth carrier at: +/-4 MHz +/-6 MHz		 25 40		dB
Blocking / desensitization (e.g. mobile phone signal rejection)	(Measured according to ETSI EN 300 440-1 V1.6.1 (2010-08). -100 MHz from lower band edge -40 MHz from lower band edge -20 MHz from lower band edge +20 MHz from upper band edge +40 MHz from upper band edge +100 MHz from upper band edge		 -15 -15 -16 -16 -15 -15		dBm
RSSI range	5 dB accuracy: 3 dB accuracy:	-92 -80		-43 -45	dBm
	Resolution:		1		dB

5.5 Transmitter Characteristics

Table 9: Transmitter Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
RF channels	Programmable in 5 MHz steps as defined by IEEE 802.15.4	2405		2480	MHz
Bit rate			250		kb/s
Chip rate			2.0		Mc/s
TX power (nominal)	Power control set to 0 dBm	-3.5	0	2.5	dBm
TX power control range	In 32 steps of 1 dB	-25		+3	dBm
	Variation over voltage and temperature range		0.5	1	dB
TX Harmonics	Conducted measurement at 0 dBm output power (1 MHz resolution bandwidth, average power and modulated carrier)			-42	dBm
TX out of band emissions < 2390 MHz > 2483.5 MHz	Measured at 0 dBm output power, modulated signal, on IEEE channels 11 to 25 (1 MHz resolution bandwidth, average power and modulated carrier)			 -42 -42	dBm
LO leakage 2.4 GHz 4.8 GHz				-47 -47	dBm
EVM			16		%

5.6 Digital Timing Characteristics

Table 10: SPI Slave Timing Characteristics

Symbol	Parameter	Reference (Figure 10)	Min	Typ	Max	Unit
	Signaling layer					
F_{SCLK}	SCLK frequency	t1	0		16	MHz
	SCLK duty cycle clock			50		%
	MOSI setup time	t2	20			ns
	MOSI hold time	t3	20			ns
	SCLK low to MISO valid time	t4			31.25	ns
	SSN setup time	t5	31.25			ns
	SSn high to MISO tri-state	t6			31.25	ns
	Protocol layer					
	Response time	t_R (see section 4.4.3)			16	µs

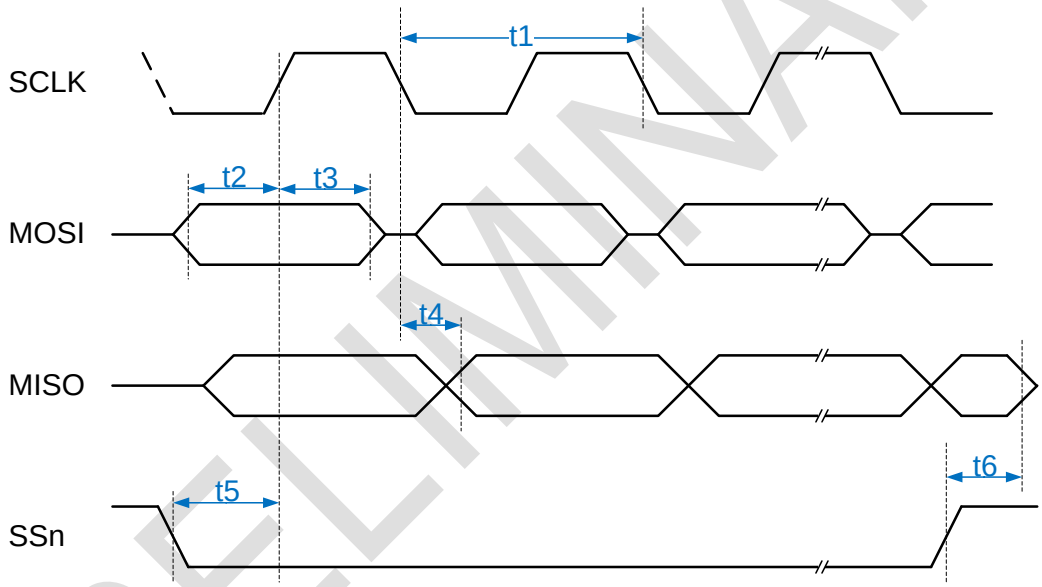


Figure 10: SPI Slave Signaling Timing Diagram

5.7 Wake-up and Standby Timing Characteristics

Table 11: Wake-up and Standby Timings

Application use cases	Activities / Remarks	Min	Typ	Max	Unit
Power On Reset, till ready for host serial interface interaction.	Assuming external Reset signal (see 5.9 below). Start up Crystal (crystal dependent; see 5.8 below) + Digital State Initialization; see Figure 11 (below)		3		ms
Go to standby, from application decision or host command.	Digital State Backup		0.4		ms
Wake up by host, from 16 MHz standby, till ready for host serial interface interaction.	Digital State Restore		0.4	0.5	ms
Wake up from 16 MHz standby to be able to receive RF packet from remote controller.	Digital State Restore + Enable RF receiver		0.5	0.6	ms
RF duty cycle during system standby.	Configurable	1.68		100	%

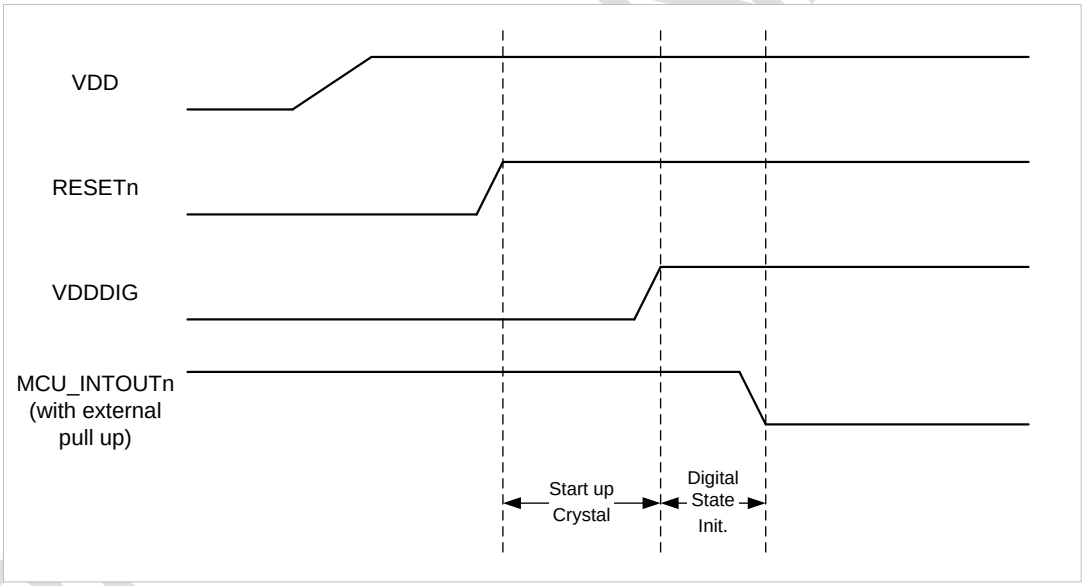


Figure 11: Power On Reset Timing Diagram

5.8 Crystal Oscillator Specifications

5.8.1 The 16 MHz Crystal Oscillator

The 16 MHz oscillator is an AGC controlled oscillator that provides a high gain at start-up, to assure fast start-up times, and low gain when running, to minimize current consumption. It generates the system clock for the GP710 and can also be used as Time-Base Generation for the Event Scheduler.
Some GP710 characteristics are crystal dependent. For reliable operation, and to meet the specified 16 MHz standby current and startup time, the crystal used should comply with the GreenPeak Procurement Specifications for the 16 MHz crystal; these Specifications are available from GreenPeak Support upon request.
Table 12 gives characteristics of two typical examples from the Procurement Specifications; other Co-ESR combinations are possible - see the Procurement Specifications. Figure 12 shows the typical configuration of the oscillator. The values of C3 and C4 are crystal type dependent and given in Table 12.

Table 12: 16 MHz Standard Crystal Characteristics

Symbol	Parameter	Nominal Value 3.2x2.5 SMD	Nominal Value HC-49/S SMD or HC-49/S leaded	Unit
Co	Shunt capacitance	1.0	2.6	pF
ESR	Effective Series Resistance	15	13	Ω
CL	Load capacitance	12	20	pF
	Temperature range	0 to +75 (-45 to +85 extended range)	0 to +50	°C
	GreenPeak Procurement Specification	GP_P004_PS_02507	GP_P004_PS_01620	
	Application information: C3 C4	18 15	33 33	pF

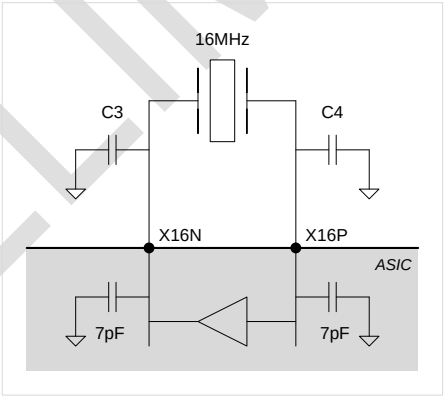


Figure 12: Typical 16 MHz Crystal Configuration

5.9 Reset Characteristics

5.9.1 Host-controlled Reset

The GP710's RESETn signal can be controlled by the host processor. In this case the host processor must keep the GP710 in reset (RESETn low) until the power supply is stable.

Table 13: Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Delay time between "power supply stable" and release of the GP710 RESETn signal		1			µs

5.9.2 Power On Reset Circuit

If the RESETn signal is not controlled by the host processor, an RC Power On Reset circuit can be used to reset the GP710 from Power on. The circuit is depicted in Figure 13 (below). The R value is specified in Table 14 (below). The C value is dependent on the power supply's rise time: the time constant must be at least twice that of the time it takes the power on BVDD to rise to its end value. (Note that the power supply rise time can be influenced by things like battery contact bounce.)

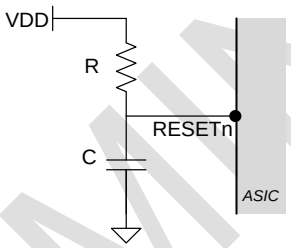


Figure 13: Power on Reset Circuit

Table 14: Power on Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset level	POR inactive	0.5	BVDD/2	BVDD-0.5	V
	Power supply rise time				R*C/2	s
	POR circuit resistor (R)			10K		Ω
	POR circuit capacitor (C)			see text above		F

6 Device Information

6.1 QFN40 Package

6.1.1 QFN40 Pin Assignments

Figure 14 below shows the pin connections top view, and Table 15 lists the pin assignments.

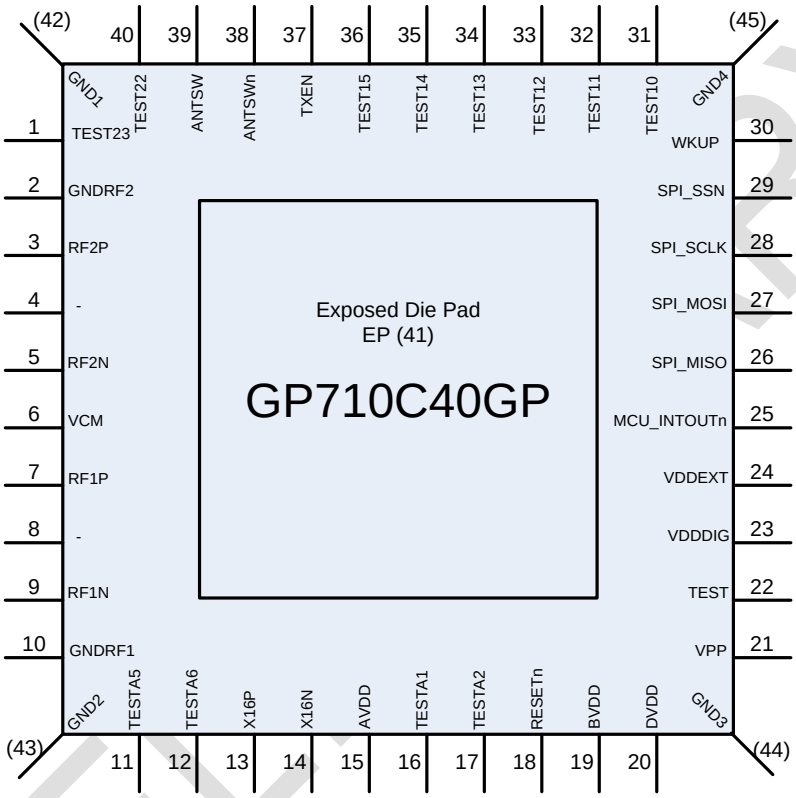


Figure 14: Pin Connections (QFN40)

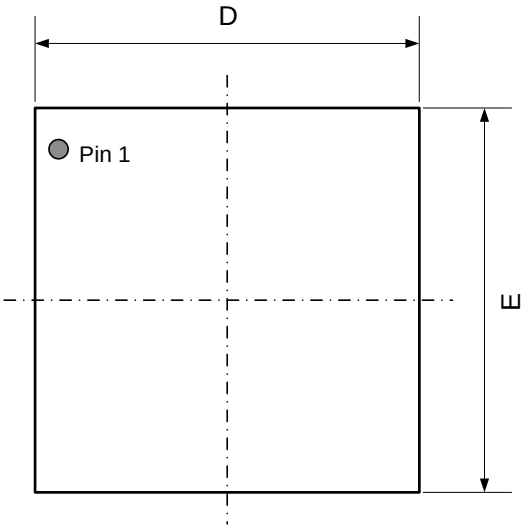
Table 15: Pin Assignments (QFN40)

Pin #	Name	Type	Description	Notes
1	TEST23	Digital IO	Test pin	Connect to exposed die pad
2	GNDRF2	Ground	Ground RF	
3	RF2P	RF IO	RF port positive for antenna 2	
4	-		Not connected internally	Suggest to connect to exposed die pad
5	RF2N	RF IO	RF port negative for antenna 2	
6	VCM	Power	RF bias supply output	VCM provides the biasing for the RF front-end for both RF port 1 and 2. Please consult the application notes for further details.
7	RF1P	RF IO	RF port positive for antenna 1	
8	-		Not connected internally	Suggest to connect to exposed die pad
9	RF1N	RF IO	RF port negative for antenna 1	

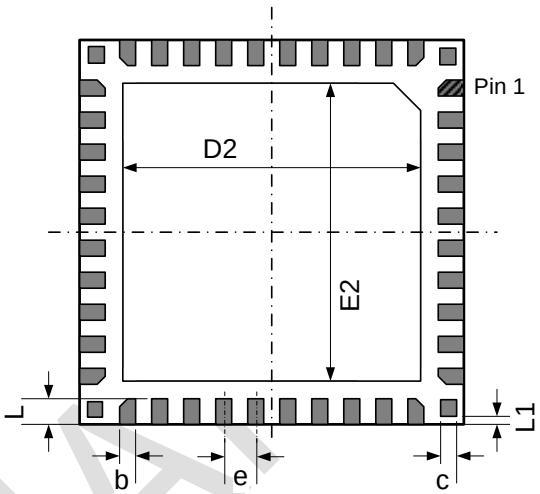
Pin #	Name	Type	Description	Notes
10	GNDRF1	Ground	Ground RF	
11	TESTA5	Analog IO	Test pin	Connect to exposed die pad
12	TESTA6	Analog IO	Test pin	Connect to exposed die pad
13	X16P	Analog IO	16 MHz reference crystal input	The GP710 does not support an external clock.
14	X16N	Analog IO	16 MHz reference crystal output	
15	AVDD	Power	Analog power supply input	
16	TESTA1	Analog IO	Test pin	Connect to exposed die pad
17	TESTA2	Analog IO	Test pin	Connect to exposed die pad
18	RESETn	Digital I	Active-low reset circuit	
19	BVDD	Power	Retention domain power supply input	
20	DVDD	Power	Digital power supply input	
21	VPP	Power	Not used	Connect to exposed die pad
22	TEST	Digital I	Test pin	Connect to exposed die pad
23	VDDDIG	Power	Power supply output for decoupling	Decoupling to ground. A 100 nF decoupling capacitor to ground is required on the VDDDIG pin.
24	VDDEXT	Power	Power supply output for decoupling	Decoupling to ground. A 10 nF decoupling capacitor to ground is required on the VDDEXT pin.
25	MCU_INTOUTn	Digital O	Interrupt to host processor	Open drain output that is pulled low when an interrupt is pending. Requires external pull up.
26	SPI_MISO	Digital O	SPI Slave data from GP710 to host	Pull-down is required (because SPI_MISO is not driven when GP710 is not selected by SPI_SSN).
27	SPI_MOSI	Digital I	SPI Slave data from host to GP710	Pull-down is required only when host SPI output is not driven active low when the host is in sleep mode.
28	SPI_SCLK	Digital I	SPI clock signal	Pull-down is required only when host SPI output is not driven active low when the host is in sleep mode.
29	SPI_SSN	Digital I	SPI slave select signal	Pull-up is required only when host SPI output is not driven active high when the host is in sleep mode.
30	WKUP	Digital I	Wake up signal from host processor	Pull-down is required only when host WKUP output is not driven active low when the host is in sleep mode.
31	TEST10	Digital IO	Test pin	Connect to exposed die pad
32	TEST11	Digital IO	Test pin	Connect to exposed die pad
33	TEST12	Digital IO	Test pin	Connect to exposed die pad
34	TEST13	Digital IO	Test pin	Connect to exposed die pad
35	TEST14	Digital IO	Test pin	Connect to exposed die pad
36	TEST15	Digital IO	Test pin	Connect to exposed die pad

Pin #	Name	Type	Description	Notes
37	TXEN	Digital O	Optional, for external LNA/PA	When TXEN is used: Pull-down is required because TXEN output is not driven when GP710 is in standby mode
38	ANTSWn	Digital O	Optional, for external LNA/PA	When ANTSWn is used: Pull-up is required because ANTSWn output is not driven when GP710 is in standby mode
39	ANTSW	Digital O	Optional, for external LNA/PA	When ANTSW is used: Pull-down is required because ANTSW output is not driven when GP710 is in standby mode
40	TEST22	Digital IO	Test pin	Do not connect
Die pad	EP	Ground	Exposed die pad; analog chip ground	RF ground
(42)	GND1	Ground	Additional ground connection	\ Connected to die pad via lead frame. /
(43)	GND2	Ground	Additional ground connection	
(44)	GND3	Ground	Additional ground connection	
(45)	GND4	Ground	Additional ground connection	

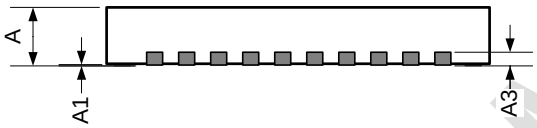
6.1.2 QFN40 Package Drawings



Top View



Bottom View



Side View

REF	Min.	Nom.	Max.	Unit
A	0.80	0.90	1.00	mm
A1	0	0.02	0.05	mm
A3		0.20 REF.		mm
b	0.18	0.25	0.30	mm
c	□ 0.18	□ 0.25	□ 0.30	mm
D, E	5.90	6.00	6.10	mm
D2, E2	4.50	4.65	4.80	mm
e		0.50 BSC.		mm
L	0.35	0.40	0.45	mm
L1	0.075	0.125	0.175	mm

Figure 15: QFN40 Package Drawings and Dimensions

6.1.3 QFN40 Package Information

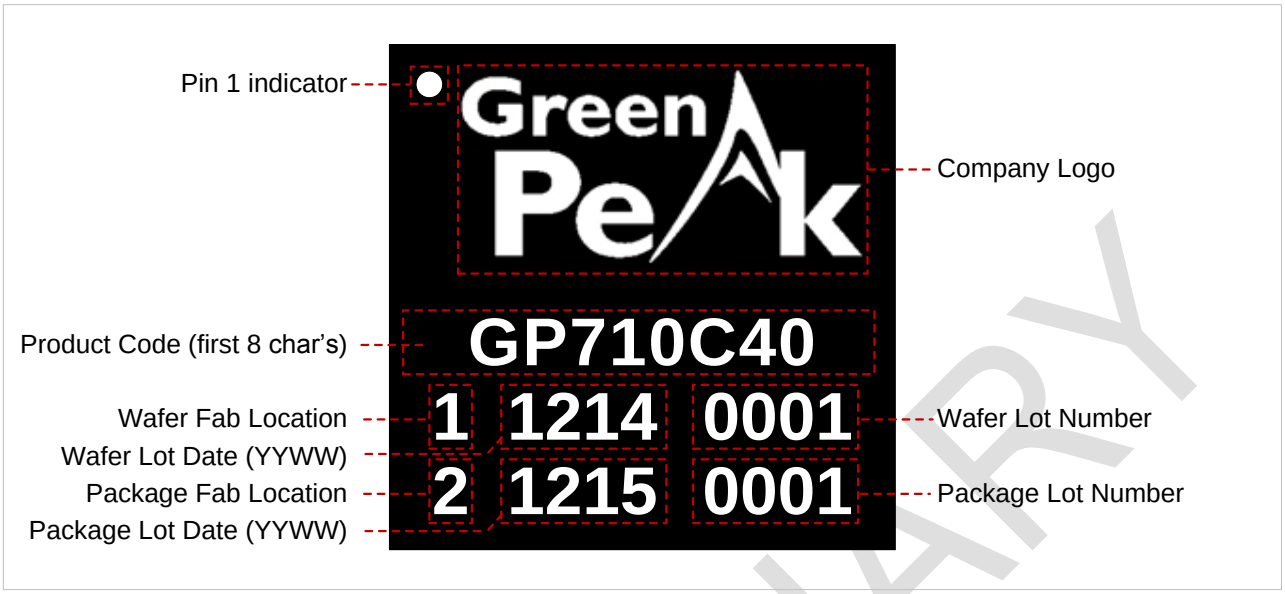


Figure 16: Information on the QFN40 Package

6.1.4 QFN40 Thermal Resistance

Table 16: QFN40 Thermal Resistance

Symbol	Parameter	Conditions	QFN40 value	Unit
Theta JA ($R_{\theta JA}$)	Thermal resistance from junction to ambient		26.7	K/W
Theta JC ($R_{\theta JC}$)	Thermal resistance from junction to case, at the exposed die pad		1.37	K/W

6.1.5 QFN40 Moisture/Reflow Sensitivity

The Moisture/Reflow Sensitivity is classified according to:
IPC/JEDEC J-STD-020D.1 (March 2008) Joint Industry Standard;
Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

Table 17: QFN40 Moisture/Reflow Sensitivity

Symbol	Parameter	Conditions	QFN40 value	Unit
	Process		Pb-free	
T_c	Peak reflow temperature		260	^oC
MSL	Moisture sensitivity level		3	

6.2 Ordering Information

Product	Package	Pins	Packaging	Unit Qty	MOQ	Packaging Dimensions
GP710C40GP_R	QFN	40	Reel	3000	3000	37 x 35 x 8 cm
GP710C40GP_T	QFN	40	Tray	490	2450	37 x 16 x 8 cm
GP710C40GP_S	QFN	40	Tray	100	100	37 x 16 x 8 cm

Abbreviations

AES	Advanced Encryption Standard
AGC	Automatic Gain Control
ARIB	(Japan) Association of Radio Industries and Businesses
CCM	Counter with CBC-MAC (ciphering), where CBC-MAC = cipher block chaining message authentication code
CCM*	extension of CCM
CSMA-CA	Carrier Sense Multiple Access with Collision Avoidance
ESD	Electrostatic Discharge
ETSI	European Telecommunication Standardization Institute
EVM	Error Vector Magnitude
FCC	(US) Federal Communications Commission
I^2C	Inter-Integrated Circuit
IIP3	Third Order Input Intercept Point
IO	Input/Output
ISM	Industrial, Scientific, and Medical (license-free frequency band)
LDO	Low Drop-Out voltage regulator
LNA	Low-Noise Amplifier
MAC	Medium Access Control layer
MOQ	Minimum Order Quantity
PA	Power Amplifier
PAN	Personal Area Network
PCB	Printed Circuit Board
PER	Packet Error Rate
PHY	Physical layer
QFN	Quad Flat No leads (package)
RC	resistor–capacitor (circuit)
RF	Radio Frequency
RF4CE	Radio Frequency for Consumer Electronics
RSSI	Received Signal Strength Indication
RoHS	Restriction of Hazardous Substances (Directive)
SAP	Service Access Point
SPI	Serial Peripheral Interface

Document History

Version	Date	Section	Changes
0.04	24 Jan 2012		Initial PRELIMINARY version.
0.05	13 Mar 2012		Updated PRELIMINARY version
		All	Changed product name to GP710
		3	Block Diagram improved
0.06	14 Mar 2012		Updated PRELIMINARY version
		6.2	Added sample order quantity packaging
0.07	14 Mar 2012		Updated PRELIMINARY version
		6.2	Correction in sample order quantity packaging ID
0.08	15 Mar 2012		Updated PRELIMINARY version
		6.2	Packaging dimensions updated
0.09	30 Aug 2012		Updated PRELIMINARY version
		5.9	(APP-319) Added host-controlled Reset.
		5.1, 6.1.1	(APP-545) RESETn is Digital and in 3V range.
		6.1.1	Updated pin descriptions; added application notes.
0.10	27 Nov 2012		Updated PRELIMINARY version
		4.1.1	Focus on all IEEE channels, not just the RF4CE ones, for ZigBee PRO.
		4.1.2.1	Clarified situation for antenna diversity. Added reference to the model.
		4.1.4	Clarified situation for Packet-in-Packet resynchronization.
		4.1.5	Changed description of the LQI.
		4.4.3	Removed paragraph on driving output signals to high in standby.
		5.1	(APP-600) Corrected “DVVD” to “DVDD”.
		5.1, 5.2, 6.1.1	(CCB-31) Removed VDDEXT load option.
		5.2	Added limitation on VPP voltage duration.
		5.2	Removed “I_{OL}” from total current specification.

Version	Date	Section	Changes
		2, 5.2, 5.3, 5.4, 5.5	(APP-670) Added characterization data.
		5.4	Removed row on CCA Threshold; is configuration.
		5.8.1	Added note that other Co-ESR combinations are possible.
		5.9.1	Clarified requirement for host during power-on reset.
		6.1.1	Pins 4 and 8 are not connected.
		6.1.3	(APP-810) Limited Product Code on marking to 8 characters.
0.11	29 Nov 2012		Updated PRELIMINARY version
		4.4.2, 5.7	(APP-908) Clarified the use of the interrupt pin during Power On Reset.