Operational Description / Schematics Note (Confidential)

FCC ID: A3LSMG390F
Model: SM-G390F
Date:2017-02-21

Please note that this Operational Description provides a complete description of the subject model. However, the chip(s) within the device may include additional capabilities that are not implemented for this device. Technical information pertaining to these additional capabilities may be shown within this document. The actual supported capabilities as implemented for this model are listed below.

Please find below the capabilities that are operational for this device:

Within USA:

- GSM/GPRS/EDGE 850 / 1900
- GPRS Multi-slot Class 33
- WCDMA 850 / 1900
- HSDPA (Rel.5) / HSDUA (Rel.6) / HSPA+ (Rel.7)
- LTE BAND 5 Rel.10, Cat.4
- 2.4GHz 802.11 (b/g/n) HT20, 802.11a/n HT20/40
- Bluetooth v4.2
- Mobile Hotspot(2.4GHz)
- Wi-Fi Direct(2.4GHz). 5GHz ch149 only
- Dual SIM / Dual Standby

Non-USA:

- GSM/GPRS/EDGE 900
- GSM/GPRS/EDGE 1800
- WCDMA/HSDPA/HSUPA 900 / 2100
- LTE BAND 1 / 3 / 7 / 8 / 20 / 38 / 40 (LTE B7/B38 does not work in US.)

Although the chipset documentation may indicate possible functions, the following have been permanently hardware disabled in this device and cannot be enabled by the end user or service provider

- FM Transmitter
- WLAN 2.4GHz 802.11n HT40
- WLAN 5GHz 802.11ac
- Mobile Hotspot 5GHz
- WiFi Direct 5GHz except ch149

Power Reduction for SAR

The wireless hotspot feature available in the device allows the end-user to tether the data connection from the Device over Wi-Fi. This is a standard feature of the OS. Upon the activation of this feature by the end-user, instructions are sent to activate the hotspot services for the end-user and also to configure the power while in hotspot mode to utilize an alternate single level output power level for certain transmission modes and frequencies. The power reduction is implemented using a single fixed level of reduction through a static table look-up algorithm for all exposure configurations. The single event trigger is only when hotspot is enabled by the end-user. The transmission modes and frequency bands that implement this reduction algorithm can be found in the tune-up procedure. The maximum allowed output power when hotspot is active and not activated is also included in the tune-up document.

Additionally, this device uses an independent single-step fixed level power reduction mechanism for WLAN operations during voice or VoIP hand held to ear senarios.

SM-G390F Operational Description

1. SM-G390F RF Circuit Desciption

1.1 RFIC : S5M925DA02-L330

1. Introduction

This document is the data sheet of SHANNON925 transceiver RFIC for multimode, multiband applications. This document provides features, detailed specifications, and package information of SHANNON925.

1.1 IC Features

- 28nm CMOS 1P8M
- Die Size: 3.94 × 3.12 mm^2 (12.3 mm^2, 11.7 mm^2 for cellular and 0.6 mm^2 for GNSS)
- Package: Flip-Chip Fine Ball Grid Array (FC-FBGA)
  - 110 balls & 120 bumps (5.09 mm x 3.96 mm, 20.2 mm^2)
- Clock: 1) shared TCXO for cellular and GNSS or 2) TCXO for GNSS, VC-TCXO for cellular
- Control interface: SPEEDY / 3-wire SPI for Cellular, SPEEDY for GNSS

1.2 S925 Cellular RF Features

- Supporting modes
  - Quad-band GSM/GPRS/EDGE (GSM 850, EGSM 900, DCS 1800, PCS 1900) with RX Diversity
  - WCDMA/HSPA: B1/B2/B3/B4/B5/B6/B8/B9/B11/B19/B21/B26
  - TD-SCDMA: B34/B39/B40
  - LTE (FDD) : B1/B2/B3/B4/B5/B6/B7/B8/B12/B13/B17/B18/B19 /B20/B21/B25/B26/B27/B28/B29/B34

- LTE (TDD) : B38/B39/B40/B41
- LTE (FDD) 2CC DL CA
- LTE (TDD) 2CC DL CA (Inter/Intra)
- Joint-CA (FDD RX/TX + TDD RX, TDD RX/TX + FDD RX)
- 4-Rx Diversity (3G/LTE) – B1/3/7 (EU), B2/4/30 (NA)
- 4x4 MIMO (3G/LTE)

- SHANNON 925 transceiver consists of 4 receiver (RX) and 1 transmitter (TX) chains
  - Primary RX (PRX): 15 RF inputs (High Band: 4, Mid Band: 5, Low Band: 6)

    Diversity RX (DRX): 6 RF inputs (HB: 2, MLB: 4) with external LNAs
  - TX: 10 RF outputs for 2G/3G/4G (HMB: 6, LB: 4)
- Direct conversion Zero-IF Receiver
  - 3G/LTE inter-stage SAW filters are not required
  - Wideband LNA options provided for DRX
  - No IQ mismatch calibration required
  - Single-ended LNA input ports
  - Optional Single-Ended I/Q output support
- Direct up-conversion transmitter
  - SAW filters are not required except for B13/B26/B11/B21/B30/B41 (Due to additional spurious emission requirement)
  - FB-Mixer: CL-DPD/AIT, fast IQ/DC calibration
  - Internal power detector
  - Class 33 compliant GPRS/EDGE
- Frequency synthesizer
  - Fully integrated Digital PLL
  - Integrated low drop regulators (LDOs) for DCO and LO buffer supplies

– Adaptive control of supply voltage using internal LDO for power optimization

1.3 S925 Cellular RF CA (Carrier Aggregation) operating Scenario

Table 1 lists the supported down-link CA scenarios. SHANNON925 supports most of the inter-band and intra-band DL cases. SHANNON925 does not support 2UL cases.

Table 1 Supported DL CA Band Scenarios

RX Mode		LB	MB	HB	Combination	S925 Support	Comments
2CC FDD	Inter-Band	B5/B8/B12/B11 B B	B1/B2/B3/B4			es	
						es	
			B1+B21/B2+B4		M+M	Yes	
			B1/B3/B4	B7	M+H	Yes	
		B5+B17/B5+B12			L+L	Yes	
	Intra-band		B	B7/B23	M+M H+H	Yes	
2CC TDD	Inter-band		B39	B41	M+H	Yes	
	Intra-band		B39	B38/B40/B41	M+M H+H	Yes	

1.4 S925 GNSS RF Features

- Simultaneous quad GNSS reception: GPS, GLONASS, Galileo, and Beidu
- Companion with Kepler GNSS baseband
- Low-IF receiver
- Single-ended LNA input and single-ended I/Q outputs

- RFIC standalone VCO calibration and IF calibration
- DCOC calibration and IP2 calibration with GNSS BB (Kepler) support

1.5 IC functions

- Cellular RF Receiver

A SHANNON925 RX consists of Primary RX (PRX) with 15 input ports, Diversity RX (DRX) with 6 input ports as shown in Figure 1. PRX and DRX combined can support 2G with RX diversity and 3G/4G RX diversity for both FDD and TDD operations.

- Cellular RF Transmitter

SHANNON925 TX outputs are designed as single-ended to be compatible with commercialized external components. TX supports 2/3/4G with 10 output ports.

- Cellular RF LO distribution

SHANNON925 has 2 frequency synthesizers for RX and 1 for TX1 (RXLO1, RXLO2, TXLO) as shown in Figure 1. The RXLOs are used to support 2CC LTE mode of operation. During 4 RX diversity mode, only RXLO1 is used. TXLO is used for TX transmission as well as for RX signal down-conversion during TDD mode and 2G mode.

- Cellular RF feedback receiver

SHANNON925 TX has an integrated feedback receiver, and the feedback receiver output is connected to both of DRX1 and DRX2 TIA inputs. The feedback receiver inputs can be muxed from the RFIC transmitter output, the external power amplifier output with the dedicated package ball (FBRX_IN), and TX ABB outputs. This feedback receiver could be used for various purpose such as the closed-loop DPD and closed-loop AIT during the power up calibration or factory calibration, fast IQ/DC calibration, and ABB bandwidth calibration.

SHANNON925 TX doesn't have the internal power detector.

1.6 Block diagram

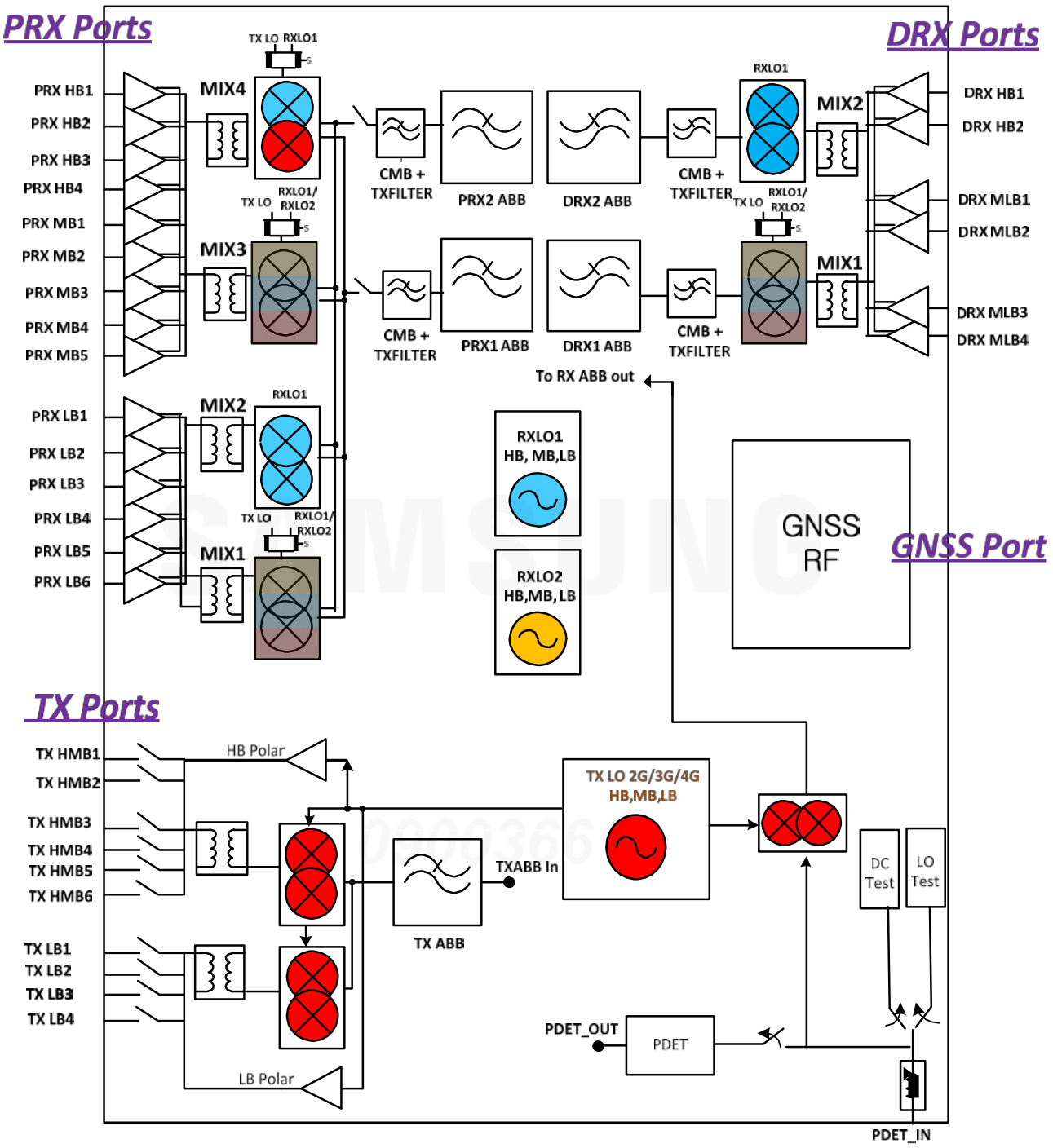


Figure 1 SHANNON925 Block diagram

1.2 HB PAM : WIPS33232-01

Description

WiPAM WIPS33232-01 is a MultiMode and MultiBand (MMMB) Power Amplifier Module (PAM) that supports 4G handsets and operates efficiently in LTE bands from 2.3 GHz to 2.7 GHz, especially FDD LTE Bands 7 and 30, TDD LTE Bands 38, 40 and 41.

The module is fully programmable through a Mobile Industry Processor Interface (MIPI®).

The PAM consists of a single 4G/ LTE high band Power Amplifier (PA) block, a PA & Switch Control logic block, and a T/R Switch block. RF input/output ports internally matched to 50 Ω to reduce the number of external components. A CMOS integrated circuit uses standard MIPI controls to provide the internal control interface and operation. Extremely low leakage current maximizes handset standby time.

The PA die, Control die, T/R switch die, and passive components are mounted on a multi-layer laminate substrate. The WIPS33232-01 is housed in a 3.0 mm x 3.0 mm x 0.8 mm, 20-pad MCM, SMT package which is a more highly manufacturable, low cost solution.

The WIPS33232-01 supports FDD LTE, TDD LTE and Uplink Carrier Aggregation (CA) for Bands 7/40/41 (up to 40 MHz)

Output power is controlled by varying the input power and V_{CC} is adjusted using a DC/DC converter to maximize efficiency for each power level.

Applications

- Multiband 4G / LTE Handsets
- FDD LTE Bands 7, 30
- TDD LTE Bands 38, 40, 41

Features

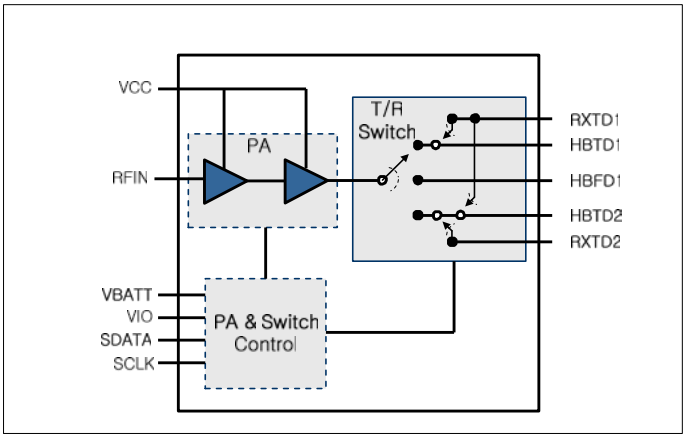
- Two T/R (Rx) Port and 3 Outputs
- Low Current Consumption
- Optimized for APT DC/DC Operation
- Fully Programmable MIPI Digital Control
- MIPI Programmable Bias Modes Optimize

  Best 4G Efficiency / Linearity Performance
- Small and Low Package Profile

  - 3.0 mm x 3.0 mm x 0.8 mm

    - 20-pad configuration

Functional Block Diagram



PIC 1. Block Diagram

1.3 LB/MB MMMB PA

- **WIPS115749-25**

Description

The WIP115749-25 is multimode multiband Power Amplifier module that supports 2.5G and 3G/4G handsets and operates efficiently in GSM, EGPRS, EDGE, WCDMA, and LTE modes. The WIP115749-25 is housed in a 5 mm x 7 mm x 0.7 mm surface mount package and optimized for premium performance.

Feature

- Separate GSM, WCDMA Paths
- MIPI Control Logic Interface
- Small Profile Surface Mount Package:
  5 mm x 7 mm x 0.7 mm (Thin Package)
  42-pad configuration
- Optimized for DC-DC Converter Operation
- Optimized for a 50 Ω System
- Green Material Package

Application

- Multiband 3G Handsets
- WCDMA/ HSDPA/ HSUPA/ LTE-modulated handsets for Bands 1, 2, 3, 4, 5, 8, 12, 13, 17, 20, 26, 28, 34, 39
- Quad - Band GSM/GPRS/EDGE
  - Class 4 GSM850 /EGSM900
  - Class 1 DCS1800/PCS1900
  - Class E2 GSM850/GSM900/DCS1800/PCS1900
  - Class 12 GPRS Compliant

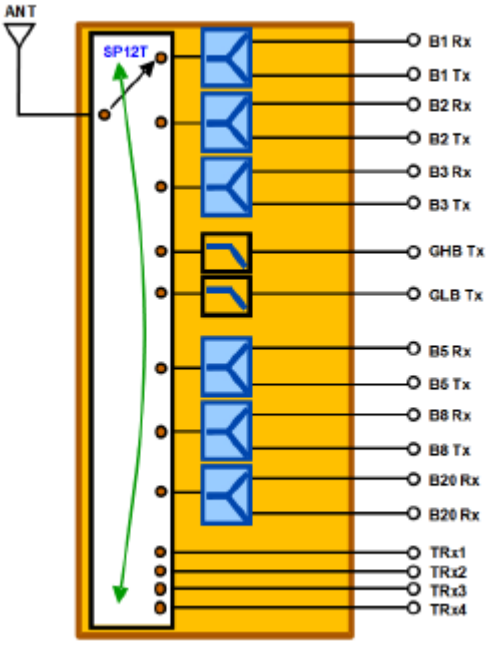
42 Pad
5 mm x 7 mm x 0.7 mm

1.4 TX MODULE : SFMD6X0G001

- Manufacture construction method : PCB + TOP component (L, C, SAW, S/W, Low pass Filter) SMT
- Package Type : Molding
- Description : FEMiD, used in mobile phone
-Demesion : 6.5(Typ.) x 4.5(Typ.) x 0.9(Max.) mm W L H
- MSL Level : 3 - ESD Level : HBM ±2KV at ANT Port, ±250V at RF Port ,

FEM integrated Duplexer (FEMiD)		
B1,B2,B3,B5,B8,B20,GLBTX,GHBTX TRX1,TRX2,TRX3,TRX4	6.5 x 4.5 x 0.9 Max.mm^3	50pin layout

<Block Diagram>



1.5 WLAN/BT/FM : S5N5C10B01-6330

This document is the data sheet of S5N5C10B01-6330, an RF IC for WLAN/BT/FM used in conjunction with SOC incorporating the Maxwell140 (MXL140) subsystem. S610 comprises a WLAN RF transceiver, a Bluetooth RF transceiver with modulator/de-modulator and an FM RF receiver with demodulator.

1.1 IC Features

• S.LSI 28 nm CMOS

• Package: Wafer level chip scale package (WL-CSP) (2.53 mm 2.92 mm, 7.40 mm^2)

- 42 balls

• Overall

- Connectivity RF chip with WLAN RF transceiver, BT radio and FM receiver
- 26MHz TCXO sharing with Cellular & GNSS system or 40MHz TCXO sharing with GNSS
- Power supply from companion PMIC chip

• WLAN

-Supports dual-band single stream 802.11ac mode (20, 40, 80MHz bandwidth)

- Highly integrated front-end eliminates external PA and LNA matching, and antenna Tx/Rx switching
- Optional external 5GHz PA for higher output power and efficiency
- Concurrent WLAN + BT reception
- Built-in calibrations for PVT variation
- No manufacturing calibration needed
- 8-wire analog baseband interface (optional 4-wire mode with Rx/Tx multiplexing)
- 2-wire WLAN dedicated digital control interface (1 x Master SPEEDY and 1 x Slave SPEEDY)

• Bluetooth

- Include RF transceiver, mixed (ADC/DAC) and baseband modem for BT 4.2 + BR/EDR + BLE
- Support for BT-WLAN coexistence operation, including concurrent receive via shared LNA with WLAN
- Support for class 1 and class 2 power-level transmissions without requiring an external PA
- No factory calibration required
- 2-wire digital baseband interface for both BT data and control (1 x Master SPEEDY and 1 x Slave SPEEDY)

• FM

- Worldwide FM band support (65 to 108 MHz) with 50 kHz channel spacing
- Digital stereo demodulator
- Full RDS/RBDS decoding supported
- Automatic antenna tuning, auto search and tuning, volume control
- Mono/Stereo blending
- Support both internal and earphone antenna
- Adaptive filter to suppress narrow band interference in the FM channel
- Single-wire digital baseband interface for both FM data and control (1 x Slave SPEEDY)

2. SM-G390F BB Circuit Desciption

2.1 AP+CP : S5E7570XU0-LA30

1.1 Introduction

Exynos 7570 is a System-on-Chip (SoC) based on the 64-bit ARMv8 processor that seamlessly supports 32-bit and 64-bit code. With a 14 nm FinFET process design, Exynos 7570 provides the best performance features such as LTE Cat4 carrier aggregation, TD-SCDMA, DC-HSPA Rel8, Cortex A53 quad CPU, and Mali-T720 GPU.

Exynos 7570 supports 64-bit code with Cortex-A53 quad-core to increase the performance over Cortex-A7. It targets 1.35 GHz frequency with LPDDR3 channel. It provides 5.3 GB/s memory bandwidth for supporting UI rich scenarios such as 720p video en/decoding, 3D graphics display, and wireless display. The dynamic virtual address mapping feature of Exynos 7570 builds up applications without hindering the memory resource.

Exynos 7570 supports LTE Cat 4 with a downlink (DL) of 150 Mbps and uplink (UL) of 50 Mbps with carrier aggregation, 3G HSPA DL42/UL11.5 Mbps, TD-SCDMA, GSM/GPRS/EDGE Rel4, dual sim, and SG-LTE. Exynos 7570 supports global navigation satellite systems such as GPS, GLONASS, and Beidou. Exynos 7570 supports WiFi 802.11a/b/g/n/ac and Bluetooth v4.2.

Exynos 7570 provides Mali-T720 GPU with a wide range of APIs such as OpenGL ES 1.1/2.0/3.1+AEP, DirectX11 FL9.3, OpenCL 1.1/1.2 Full Profile, and Renderscript.

Exynos 7570 has an integrated Image Signal Processor (ISP). Maximum camera configuration is rear camera with 13 mega pixels @ 30fps and front camera with 5 mega pixels @ 30 fps. ISP provides zero-shutter lag of camera shooting.

Exynos 7570 reduces the Bill of Materials (BOM) by integrating the IPs such as nine channels of I2C for a variety of sensors and a variety of USB derivatives (USB Host/Device 2.0). The application processor supports Double Data Rate (DDR) based eMMC 5.0 interfaces to increase the file performance of the system.

Exynos 7570 is available as a 478 FC-FBGA, which has a 0.4 mm ball pitch.

1.2 Features

Exynos 7570 supports the following features:

• ARM Cortex-A53 quad CPU with 128-bit SIMD NEON
– 32 KB (Instruction)/32 KB (Data) L1 cache and 512 KB L2 cache
– Core frequency of 1.35 GHz at OD
• 3GPP LTE Release 10 FDD/TDD
• 3GPP HSPA Release 8 FDD
• TD-SCDMA
• 2G EDGE modem
• 128-bit multi-layer bus architecture with AMBA interface
• Internal ROM and RAM for secure booting, security, operating secure OS, and general purposes
• Memory subsystem
– One port 32-bit 668 MHz LPDDR3 interface
– Dynamic clock gating and DVFS
• Multi-format video hardware codec
– 1080 p 30 fps: Decodes and encodes MPEG-4/H.263/H.264/VP8
– 1080 p 30 fps: Decodes MPEG-2/VC1/Xvid/VP8
• Image signal processor
– Maximum pixel throughput: 390 M p/s (13 Mp @ 30 fps)
– Still picture performance: 30 fps @ 13 M (4240 × 3152)

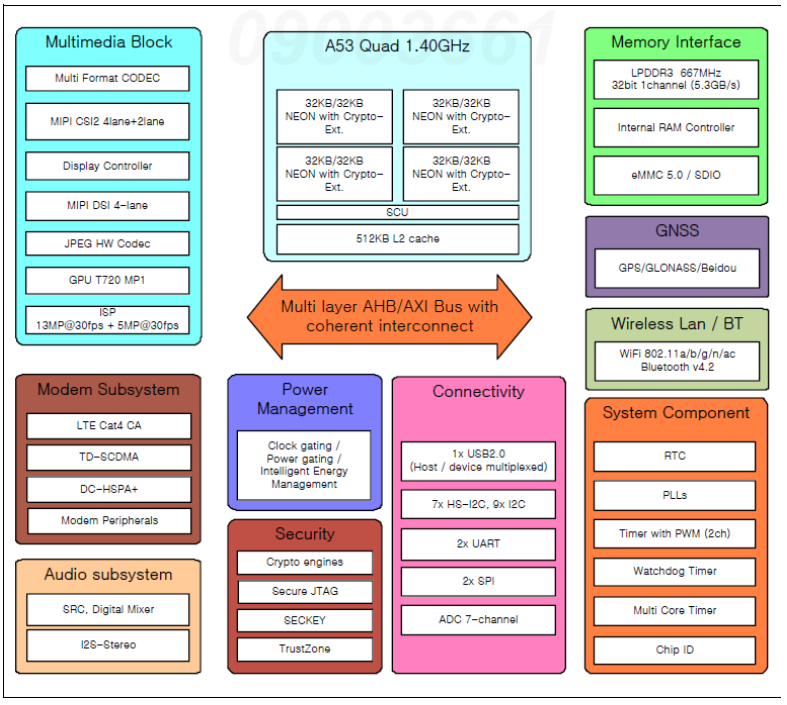
– Moving picture performance: 60 fps @ Full-HD
– Sensor defect compensation, statistics for 3A (AE/AF/AWB), demosaicing, and denoising
– Image resizing and face detection
• JPEG hardware codec
• 3D graphics hardware
– OpenGL ES 1.1/2.0/3.0
– Open VG 1.1
• LCD single display that supports MIPI
• WXGA (1280 × 800 @60 fps) LCD display
• 1 ports (4-lanes) MIPI DSI interfaces
• 2 ports (4-lanes and 2-lanes) MIPI CSI interfaces
• 6-channel I2C interface support for general-purpose multi-master
• 2-channel high-speed SPI
• 2-channel USI
• 8-channel speedy for modem and connectivity RF device and PMIC

• 2-channel high-speed UART up to 3 Mbps data rate
• USB 2.0 1-channel that supports LS/FS/HS (1.5 Mbps/12 Mbps/480 Mbps) with on-chip PHY (shared with
host/device)
• Channel SD/MMC interface that supports SD 3.0 and eMMC 5.0 DDR 8-bit interface
• Audio codec digital features such as DRC, mixer, and equalizer paired with S.LSI PMIC and ADC/DAC
• 8-channel PDMA controllers
• Configurable GPIOs
• Real time clock
• PLLs
• Timer with PWM
• Watchdog timer

• 7-channel 12-bit general purpose ADC

1.3 Block Diagram

Figure 1-1 illustrates the block diagram of Exynos 7570



2.2 Memory : KMQ310013B-B419

INTRODUCTION

The KMQ310013B is a Multi Chip Package Memory which combines 16GB e.MMC and 16Gb(8Gb*2) DDP LPDDR3 SDRAM.

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.0 which is a industry standard.
eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports 200MHz DDR – up to 400MBps with bus widths of 8 bit in order to improve sequential bandwidth, especially sequential read performance.
There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host.
Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.
The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The
FTL supports all features of the Samsung NAND flash and achieves optimal performance.

LPDDR3 devices use a double data rate architecture on the Command/Address (CAbus to reduce the number of input pins in the system. The 10-bit CA bus contains command, addres, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.
These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.
Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command.
The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.
Prior to normal operation, the LPDDR3 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

The KMQ310013B suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 221-ball FBGA Type

2.3 PMIC : S2MPU06

1.1 Introduction

S2MPU06 is an advanced Power Management IC (PMIC) designed for mobile applications. It is comprised of high efficient Buck converters, various LDOs, RTC, Switching Charger with Fuel Gauge, Flash LED Driver, Audio CODEC and APT Buck integrated into a 130-WLCSP (Wafer Level Chip Scale Package) with 4.80 mm 4.80 mm package.

S2MPU06, coupled with Multi Core Samsung Application Processors (Exynos7570), is the integrated

LTE Modem-AP solution in highly renowned Exynos products, bringing the advanced 4G LTE connectivity with a full portfolio of multiband and multimode in power-efficient platform.
The Buck Converters in S2MPU06 provide stable power to the CPU, GPU, Memory interface, CP and sub-regulators. The three Buck Converters for high load capacity on the Application Processor side also provide optimal power control using Dynamic Voltage Scaling (DVS) via Speedy interface between PMIC and SOC. Sub-regulation bucks using the constant on-time (COT) control provide the low ripple voltage and the fast transient performance. The COT regulator transitions smoothly between PWM and PFM modes with no glitches on the output.

The APT Buck Converter supplies RF PAM (Power Amp Module) power provides dynamic output voltage from 0.4V to 3.6V to improve PA efficiency over its entire operating range.

The various LDOs supply appropriate power to each I/O and functional blocks in the SOC, the camera IC and the peripherals in the system. Applying independent LDO to each I/O block helps the CPU to support various types of devices. Each block can be turned on and turned off for power optimization. Other features include a thermal regulation and an internal timer function.

The switching charger supporting 1-cell Li+ or Li-polymer battery is able to operate up to Max 5.2V and there is Boost function for USB-OTG/Flash-LED. In Boost is USB-OTG mode, Charger Register control output voltage and in Flash-LED mode, Flash-LED Register control output voltage between 3.625V to 5.2V.

Single input source is USB VBUS or TA (Travel Adaptor) and output is connected to Battery which is input source for System. Therefore, Charging current provide stable current to battery regardless of consumption current. Battery provides power to connected System. Switching charger provide several functions, such as Input current regulation and Input Voltage Regulation. In Boost mode, the source is battery and charging current is possible up to 2A.

In Flash mode, charging current is possible up to Max. 1.2A. Flash LED driver is comprised of 1-channel and can handle current up to 1.2A. S2MPU06 is sourcing type that LED is connected to ground so PCB routing is simple. By loading current and time, there are Flash mode (max. 1.2A) and Torch mode (max. 300mA). By adjusting method of output voltage, there is fixed mode.

Fuel gauge, that is voltage mode only and simple structure, calculates the SOC using battery voltage and the error must be fewer than 5%.

S2MPU06 has the Audio Hub for smart-phone, tablet applications including various functions of a stereo ADC with 3 MIC inputs and a stereo DAC with a stereo headphone driver, a mono earpiece driver, and a mono speaker driver. The ADC paths are comprised of a MIC boost amp, Programmable Gain Amplifier (PGA), mixer, analog $\Delta\Sigma$ modulator, compensation filter, FIR filter, Sinc (Comb) filter. The ADC output provides 84 dB Signal-to-Noise Ratio (SNR) over the band of interest (typically 20 kHz with sampling rate of 44.1KHz and 48 kHz and with 20dB MIC boost amp gain setting). The DAC path contains a compensation filter, a FIR filter, a Sinc (Comb) filter, a digital $\Delta\Sigma$ modulator, a multi-bit DAC, and various output drivers. The stereo headphone outputs provide 100 dB SNR for the band of interest. The speaker driver and earpiece driver delivers 97 dB and 99 dB SNR, respectively. The headphone and earpiece driver uses a negative supply. Hence, the drivers obviate a huge DC blocking capacitor. Moreover, the high power efficiency of the speaker driver can help to maximize battery life time. Accessory detector inside S2MPU06 enables to detect an Ear-jack, Headset microphone as well as Volume-Up, Volume-Down, and Send/End Buttons including voice assistant.