Operational Description / Schematics Note (Confidential)

FCC ID: A3LSMG130HN

Model: SM-G130HN

Date: 2014-06-12

Please note that this Operational Description provides a complete description of the subject model. However, the chip(s) within the device may include additional capabilities that are not implemented for this device. Technical information pertaining to these additional capabilities may be shown within this document. The actual supported capabilities as implemented for this model are listed below.

Please find below the capabilities that are operational for this device:

Within USA:

- GSM/GPRS 850
- GSM/GPRS 1900
- GPRS Multi-slot Class 12
- 2.4 GHz 802.11(b/g/n)
- Bluetooth v4.0 + EDR
- Mobile Hotspot
- FM Receiver
- EDGE Rx Only
- NFC Function

Non-USA:

- GSM/GPRS 900
- GSM/GPRS 1800
- UMTS 2100
- UMTS 900
- HSDPA (64QAM)
- HSUPA (QPSK)
- EDGE Rx Only (GSM900, 1800)

Although the chipset documentation may indicate possible functions, the following have been permanently hardware disabled in this device and cannot be enabled by the end user or service provider

- 802.11a
- FM Transmitter
- UMTS1900

Operational Description

1. SM-G130HN RF Circuit Description

1.1 Transceiver : SR3131B

SR3131B is a highly integrated, single-die radio transceiver IC that supports 3G WCDMA, HSDPA, HSUPA and GSM/EDGE (HEDGE 2.5G) operation without the need for external transmit SAW filters, baluns or LNAs. Implemented in low cost bulk CMOS, it is optimized to meet the challenges of today's small form factor, power efficient, high performance cellular handsets. The SR3131B has total of six transmit ports and six receive ports (differential). The SR3131B provides multiple bands of operation.

The SR3131B offers a cost competitive and small footprint radio solution for multi-mode, multi-band applications with the highest performance at the lowest power.

The linear transceiver architecture of SR3131B is utilized for both 2.5G and 3G systems, offering excellent performance and design margins over 3GPP requirements. For 2.5G, a direct modulation scheme is used in the transmitter and performance of 2.5G receive and transmit chains is such that no additional RF filters are required to meet out-of-band noise specifications. The output driver stage for each transmitter chain is single-ended and matched to 50Ω.

The transceiver supports analog I/Q interfaces for 2.5G and 3G with simple 3-wire bus architecture to program the radio.

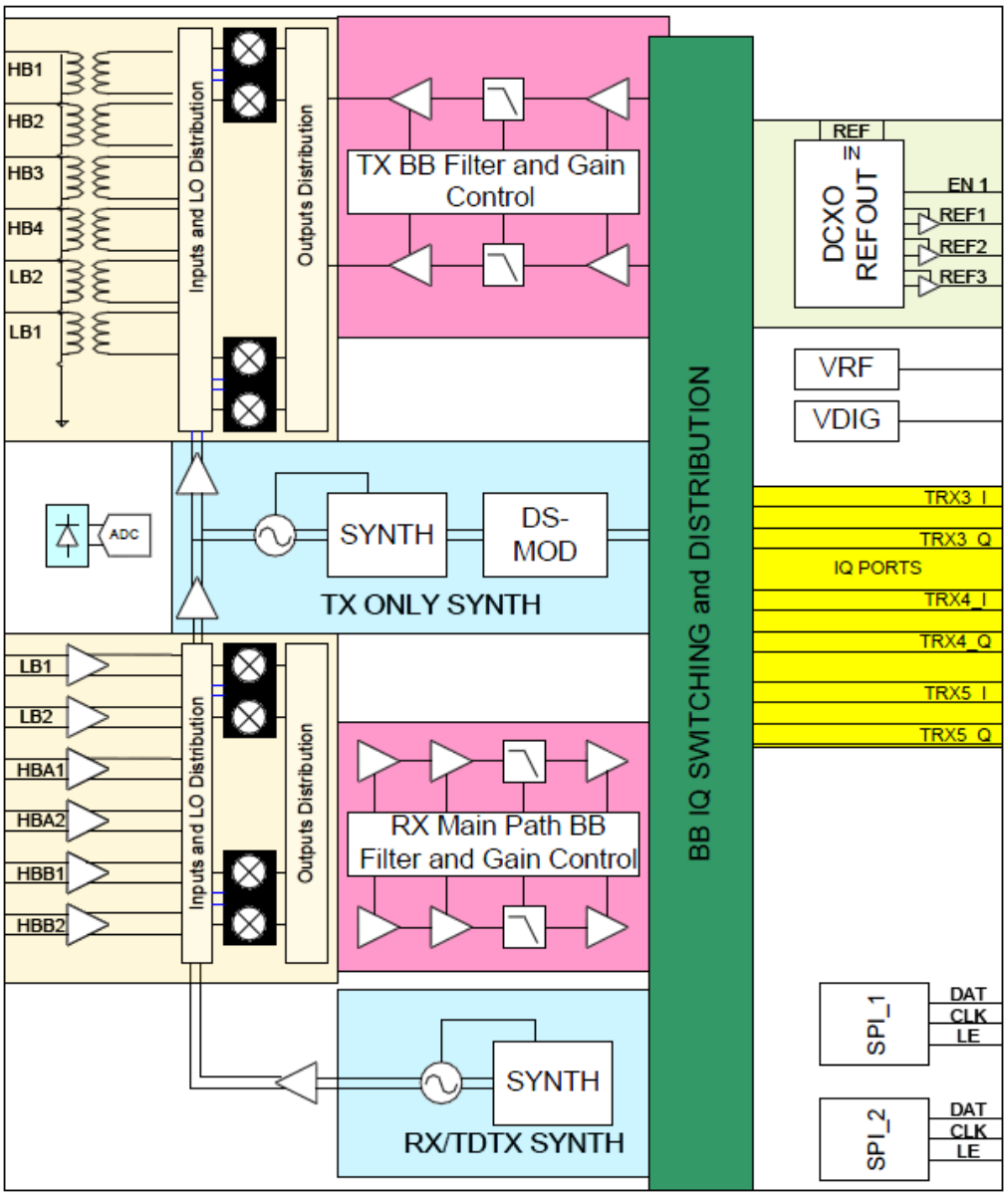
Features

- Fully integrated single chip multi-mode, multi-band HEDGE transceiver in bulk CMOS
- Quad-band GSM operation: USGSM850,EGSM900,DCS1800 and PCS1900
- Support for 3GPP Band 1to Band 6, Band 8, Band 9, and Band 10
- No off-chip RF SAW filters required for GSM
- Fully integrated LNAs in all receive bands and all modes of operation
- Completely integrated frequency synthesizer and VCO
- All TX outputs are single-ended and internally matched to 50Ω
- Analog IQ interface
- Built-in DCXO
- Ultra Low Power Consumption
- Three sets of reference outputs
- Single SPI operation
- 5.5mm x 7mm QFN 50 pin 0.4mm pitch package
- RoHS Compliance
- Halogen Free (HF) Compliance

Applications

- Dual mode 3Gand GSM Modem
- Dual mode 3Gand GSM Feature Phone

• 3G Smart Phone



1.2 WGPRS Tx Module : SKY77585-11

SKY77585-11 is a transmit and receive Front-End Module (FEM) with integrated power amplifier control designed in a low profile, compact form factor for quad-band cellular handsets comprising GSM850 / GSM900 and DCS1800 / PCS1900 operation. The SKY77585-11 offers a complete Transmit VCO-to-Antenna and Antenna-to-Receive SAW filter solution. The FEM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation and EDGE downlink.

The module consists of a GSM850/GSM900 PA block and a DCS1800/PCS1900 PA block, impedance-matching circuitry for 50 ohm input and output impedances, Tx harmonics filtering, high linearity / low insertion loss RF switch, and a Power Amplifier Control (PAC) block. One

PA block supports the GSM850 / GSM900 bands and the other PA block supports the DCS1800 / PCS1900 bands. Both PA blocks share common power supply pads to distribute current. The output of each PA block and the outputs to the four receive pads are connected to the antenna pad through an RF switch. Four broadband interchangeable receive ports provide flexibility to support multimode and multiband configurations. The GaAs die, the CMOS die, the Switch die, and passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

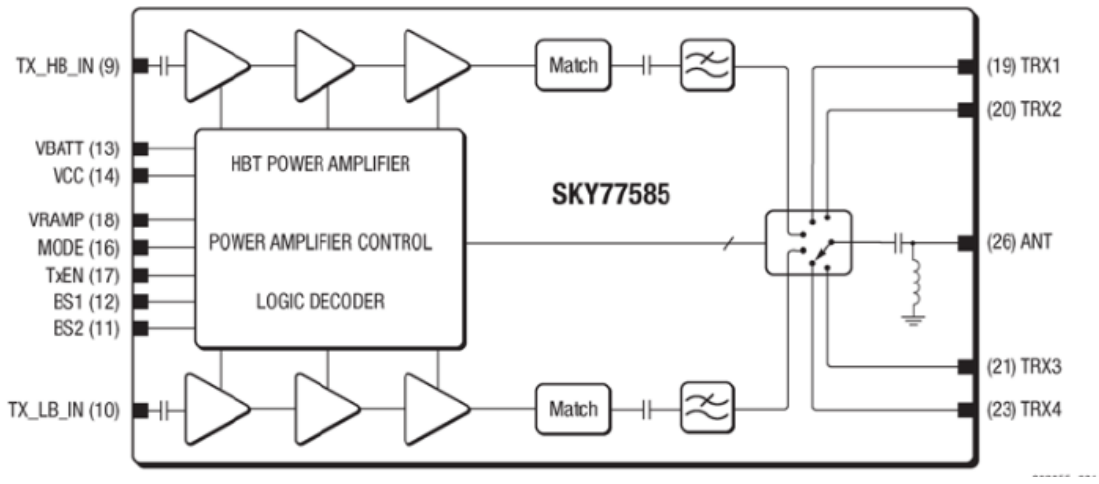
Band selection and control of transmit and receive are performed using four external control pads. Refer to the block diagram in Figure 1 below. The band select pad, BS1, BS2, Mode, and TxEN select GSM850, GSM900, DCS, and PCS modes of operation.

Transmit enable TxEN controls receive or transmit mode of the RF switch (Tx = logic 1). Proper timing between transmit enable TxEN and Analog Power Control VRAMP allows for high isolation between the antenna and Tx–VCO while the VCO is being tuned prior to the transmit burst.

The SKY77585-11 is compatible with logic levels from 1.2 V to 2.9 V for BS1, BS2, MODE, and TxEN pads.

Features

- High efficiency
  - 42% (GSM850,GSM900)
  - 39% (DCS1800)
  - 38% (PCS1900)
- Low transmit supply current
  - 1.35 A (GSM850, GSM900)
  - 0.94 A (DCS1800)
  - 0.96 A (PCS1900)
- 50 ohm matched Input/Output
- Tx-VCO-to-antenna and antenna-to-Rx-SAW filter RF interface
- RF switch affords high linearity, low insertion loss, and 0 V DC on Rx ports
- Small, low profile package : 6.0 mm x 6.0 mm x 0.9 mm, 28-pad configuration



1.3 3G PAM : SKY77758-21

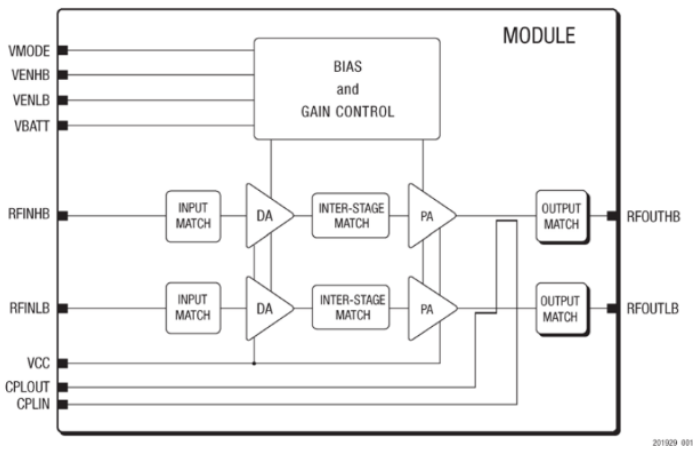
The SKY77758-21 Power Amplifier Module (PAM) is a fully matched, 14-pad, surface mount module developed for Wideband Code Division Multiple Access (WCDMA) applications. This small and efficient module packs full coverage for WCDMA Bands I, II, IV, V, VIII into a single compact package. The SKY77758-21 meets stringent spectral linearity requirements for WCDMA, HSDPA, HSUPA, HSPA+ transmission with high power-added efficiency. A directional coupler integrated into the module eliminates the need for any external coupler.

The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. Output match into a 50-ohm load is realized off-chip within the module package to optimize efficiency and power performance.

The SKY77758-21 PAM is manufactured with Skyworks' InGaP GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. No VREF voltage is required. Power down is accomplished by setting the voltage on VENHB and VENLB to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

Features

- Low voltage positive bias supply 3.0V to 4.5V
- High effiency
- Large dynamic range
- Small, low profile package : 3mm x 4.2mm x 0.9mm, 14-pad configuration
- Power down control
- InGap
- Supports low collector voltage operation
- Digital Enable
- No Vref required
- CMOS compatible control signals
- Integrated Directional Coupler



1.4 Duplexer : SAYRF1G95HJ0F0A, SFX897UZ102

Duplexer split each single operating band into receive and transmit paths

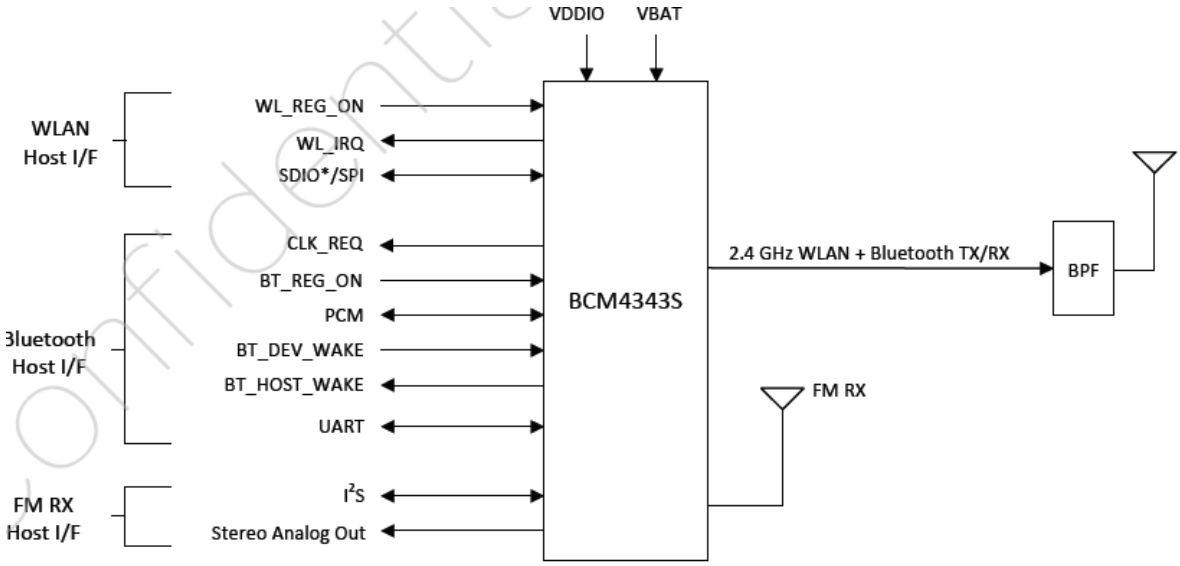
1.5 BT/WLAN : BCM4334S

The Broadcom® BCM4343S is a highly integrated single-chip solution and offers the lowest RBOM in the industry for smartphones, wearables, and a wide range of other portable devices. The chip includes a 2.4 GHz WLAN IEEE 802.11 b/g/n MAC/baseband/ radio, Bluetooth 4.1 support, and an FM receiver. In addition, it integrates a power amplifier (PA) that meets the output power requirements of most handheld systems, a low-noise amplifier (LNA) for best-in-class receiver sensitivity, and an internal transmit/receive (iTR) RF switch, further reducing the overall solution cost and printed circuit board area.

The WLAN host interface supports gSPI and SDIO v2.0 modes, providing a raw data transfer rate up to 200 Mbps when operating in 4-bit mode at a 50 MHz bus frequency. An independent, high-speed UART is provided for the Bluetooth/FM host interface.

Using advanced design techniques and process technology to reduce active and idle power, the BCM4343S is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit that simplifies the system power topology and allows for operation directly from a rechargeable mobile platform battery while maximizing battery life.

The BCM4343S implements the world ' s most advanced Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative WLAN and Bluetooth coexistence.



1.6 GPS : BCM47520

The Broadcom® BCM47520 is a Global Navigation Satellite System (GNSS) single-die receiver IC, fabricated in low-power 40 nm CMOS technology. The BCM47520 features a host-based architecture, where processing functions are split between the BCM47520 and the CPU on the host system. Demands on the host CPU are minimal and no real time requirement s are imposed. Host communication can be implemented via UART (with optional hardware flow control) or a Broadcom Serial Control (BSC) slave. The BCM47520 includes an internal low-dropout regulator to power both an external GNSS TCXO and an optional external low noise amplifier. It is available in a 0.4 mm ball pitch, 2.07 mm × 2.47 mm WLBGA package.

" • Designed for the fast-growing mass market smartphone segment, where GNSS has become pervasive. The BCM47520 enables both navigation, a feature increasingly demanded by consumers, and location services, which are demanded by emergency services such as E911, network operators, location-aware services, as well as by consumers.

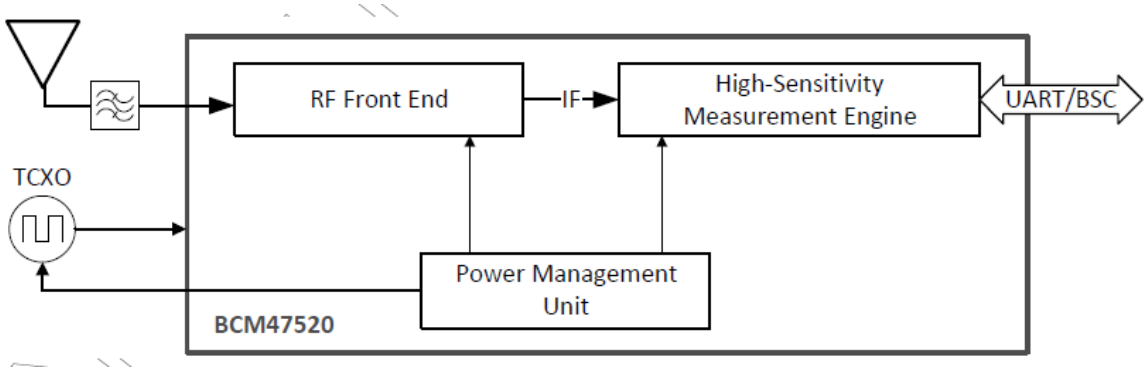
" • Optimal for mass market portable digital assistants.

" • Multi-constellation capability that simultaneously uses signals from four satellite constellations (GPS, GLONASS, QZSS and SBAS) to compute each position fix.

" • Very low current consumption. As little as 8 mA average current in low-power mode made possible by a flexible internal signal processing architecture.

" • The industry's smallest GNSS chip featuring a low bill of materials (BOM) part count, which enables a very small PCB size of 16 mm2, including external filter and TCXO.

" • Proven firmware package with advanced multiconstellation assistance data:
- Always maintains fresh multi-.constellation assistance data thanks to Broadcom's Location Based Services (LBS) client/server solution



1.7 NFC : S3FWRN5

1.7.1 Introduction

S3FWRN5 is a controller that is used in contactless communication at 13.56 MHz. It is based on the SC000 microcontroller core.

The operation modes that S3FWRN5 hardware supports are:

- ISO/IEC 18092 peer-to-peer (Active/Passive initiator and target)

- ISO/IEC 14443 A (NFC-A) Reader/Writer
- ISO/IEC 14443 B (NFC-B) Reader/Writer
- ISO/IEC 15693 (NFC-V) Reader/Writer
- Sony FeliCa (NFC-F) Reader/Writer (NOTE)
- Topaz Reader/Writer
- KOVIO(RF Barcode) Reader

- ISO/IEC 14443 A (NFC-A) card emulation
- ISO/IEC 14443 B (NFC-B) card emulation
- Sony FeliCa (NFC-F) card emulation (NOTE)
- Type B' card emulation
- ISO/IEC 15693 (NFC-V) card emulation

1.7.2 Features

The features of S3FWRN5 are:

- ARM SC000 processor
- 128 KB flash code memory
- 8 KB SRAM data memory
- Timer
- Two 16-bit timers with 8-bit prescaler
- 16-bit watchdog timer
- Host interface
- UART
- SPI (Slave)
- I2C (Slave)
- Includes four GPIO
- GPI0: NFC wake-up
- GPIO1: Host wake-up
- GPIO2: Clock request
- GPIO3: SE interrupt
- Contactless interface modem
- ISO/IEC 18092 Active/Passive communication (Active/Passive initiator and target)
- ISO/IEC 14443 A and B Reader/Writer
- ISO/IEC 15693 Reader/Writer
- Sony FeliCa Reader/Writer
- Topaz Reader/Writer

- KOVIO(RF Barcode) Reader
- ISO/IEC 14443 A and B card emulation
- Sony FeliCa card emulation
- Type B' card emulation
- ISO/IEC 15693 card emulation
- RF level detector:
- Configurable polling loop for automatic device discovery

- Secure element interfaces:
    - Two SWPs
    - SPI (Master)
    - I2C (Master)

- Flexible clock supply concept for CPU
- External crystal (27.12 MHz)
- PLL (13.56 MHz)
- Power supply: 2.3~4.8V Battery Connection
- Flexible interrupts that uses IRQ pin GPIO
- Uses automatic host wakeup through HCI/NCI
- Highly integrated demodulator and decoder

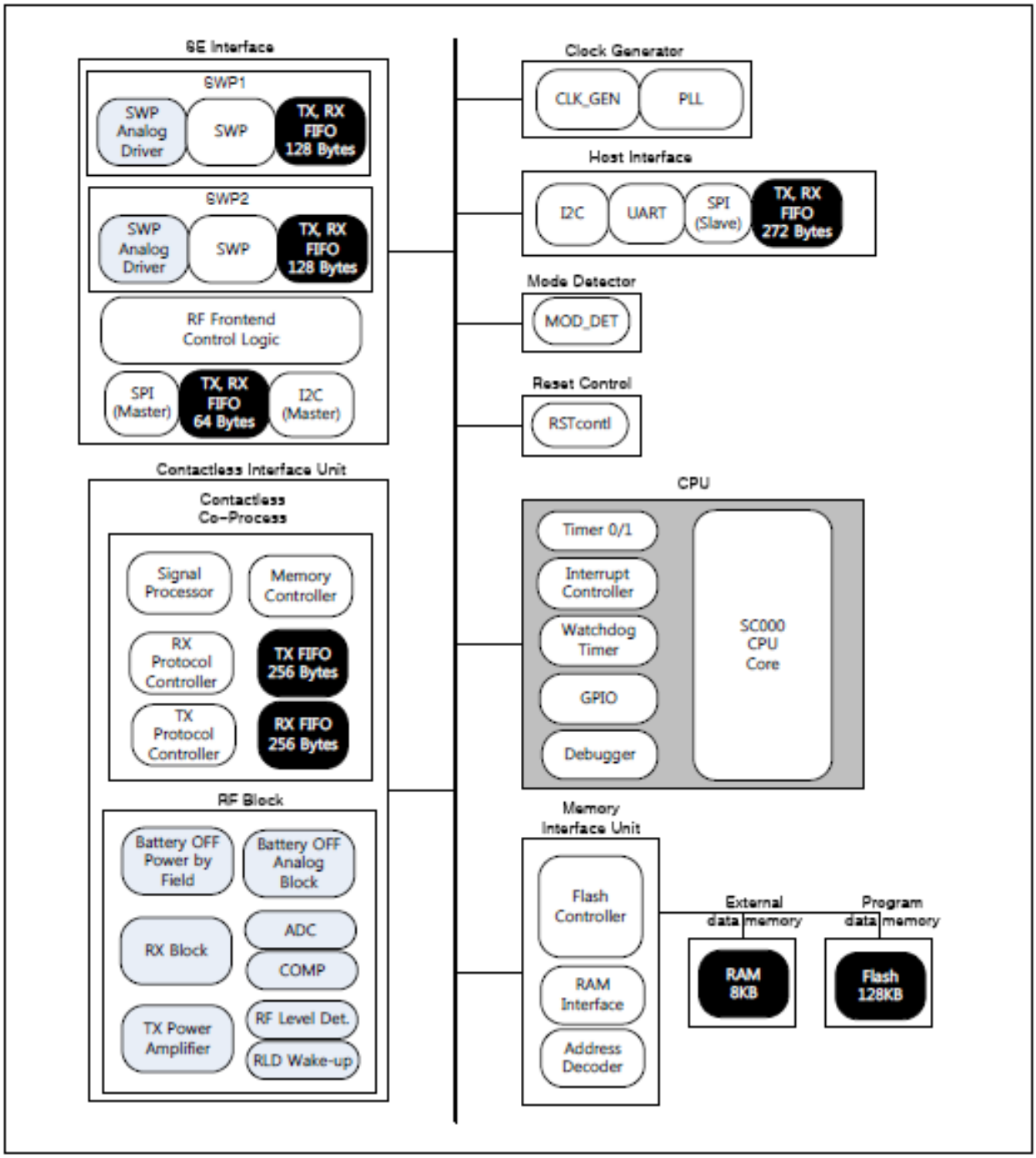


Figure 1 Block Diagram of S3FWRN5

2. SM-G130HN BaseBand Circuit Description

2.1 Application Processor + PMU : SC7715A

The SC7715A is a highly integrated application processor with embedded GSM/EDGE/Bluetooth/WiFi/FM/GPS modem and PMU. It consists of single core ARM Cortex -A7 core as application processor, which includes a NEON multimedia processing engine, single-core ARM mali400 as 3D graphics accelerator, multi-standard multi-media accelerators and advanced audio subsystem. It integrated GSM/GPRS/EDGE baseband, Bluetooth, WiFi, FM,GPS. The specially optimized architecture can achieve high performance and low power for a lot of applications. Proprietary architectures and algorithms were developed for low power ASIC design and power management. Unique techniques are used for noise/offset calibration and cancellation. Overall, this chipset presents a high cost-effective platform for Android mobile devices

Platform Features

MCU subsystem

- signle-core ARM Cortex$_{TM}$ A7 processor, up to 1.0GHz
- 32 KB L1 I-cache and 32 KB L1 D-cache, 256KB L2 cache
- 52 KB on-chip SRAM
- NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
- High performance multi-layer AXI bus system and low power APB system
- Support 32-bit ARM and 16-bit Thumb instructions
- 32 KB on-chip ROM for laboratory or factory programming and system boot
- Support boot from NAND, USB, UART, eMMC
- Support memory re-mapping mechanism
- Dedicated DMA with 32 logical request channels
- General purpose RTC timers for task schedule and system timing recording
- System timer with 1 ms counting scale
- Watchdog timer for system crash recovery
- Bus monitors for MCU system debug or performance analysis
- JTAG port for in-circuit emulation
- Support UID and secure boot
- DVFS/AVFS technology with adaptive operating voltage from 0.9V to 1.2V

Note:
- ARM Cortex$_{TM}$ is a registered trademark of Advanced RISC Machines Limited.

External memory interface

- Support NAND flash

- Support eMMC 4.5
- Support LP DDR1, LP DDR2, DDR3
- Supporting the following memory combinations:

  NAND + LP DDR1 or Nand + LP DDR2, or Nand + DDR3

  eMMC + LP DDR1 or eMMC + LP DDR2, or eMMC + DDR3

  SPI-NAND + LPDDR2 or SPI-NAND +DDR3L
- NAND flash is supported by NAND controller, with the following features:

  Support address cycle of 3 / 4 / 5 or more

  Support nand density of no limited

  Support SPI Nand

  Support 2 chip select

  Support 8 bit and 16 bit devices

  Support 1.8 V and 3.0 V devices

  Support multi-bit ECC, ECC bit number can be 1/2/4/8/12/16/24/40/60 bit s

  Support page size 512bytes/2K/4K/8K/16K

  Support sequential read or write at most 256 pages at once

  Support Randomizer 4 polynomials or 1 polynomials

  Support Randomizer polynomials coefficient configurable

  Support Randomizer polynomials depth configurable from 3 ~ 32
- eMMC flash is supported by eMMC controller, with the following features:

  Support 1.8V I/O

  Support 1.8 or 3.0V VCC

  Support 1/4/8-bit device

  Compliance to eMMC4.5
- LP DDR1 is supported by DDR Controller, with the features list below:

  Support only 1.8 V devices

  Support 16 bit and 32 bit devices

  Support up to 2 chip select channels (2 CS)

  Support up to 4G Bit devices

  Clock up to 200 MHz
- LP DDR2 is supported by DDR Controller, with the features list below:

  Support only 1.2 V devices

Support 16 bit and 32 bit devices

Support up to 2 chip select channels (2 CS)

Support up to 8G Bit devices

Clock up to 333 MHz

 DDR3 is supported by DDR Controller, with the features list below:

Support 1.35 or 1.5 V devices

Support 16 bit and 32 bit devices

Support up to 2 chip select channels (2 CS)

Support up to 8G Bit devices

Clock up to 333 MHz

Peripheral and connectivity interfaces

 Support upto tri-SIM cards, both 1.8 V and 3.0 V devices
(At this model, SM - G130HN, it supports only one SIM card)

 Support 2 SDIO 2.0 and 1 SDIO 3.0

 Support USB 2.0

 Four UARTs

 Three SPIs, support both master and slave, support 3-wire SPI, 4-wire SPI and synchronous SPI

 Two IISs(PCM)

 Support 3-column x 3-row keypad with internal pull-up resistors

 Six I2C interfaces

 More than 100 GPIO pins

 Four PWM outputs

Modem Features

GSM/GPRS/EDGE baseband

 Compatible with GSM/GPRS/EDGE Release 1999, GSM850, GSM900, DCS1800, and PCS1900 recommendations

 Complete in-phase and quadrature (I/Q) component interface between the Digital Signal Processor (DSP) and RF module

 EGPRS class12，type B (MCS1-9 in downlink and MCS1-9 in uplink)

 Cryptographic Algorithms: A5/1 A5/2 A5/3,GEA1，GEA2，GEA3

Voice and audio codec

 Quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), half rate (HR), and full rate (FR)

 Dial tone generation

- Voice memo
- Noise reduction
- Echo suppression/echo cancellation
- Digital sidetone generator with programmable gain
- Support ClassAB/D/G
- Support dual MICs

Multimedia Features

3D Graphics

- Support OpenGL ES1.1/1.2 3D graphic
- Support OpenVG 1.1
- Up to 33M Tris/s, 312MPix/s @ 312Mhz

LCD display

- Integrated display controller (Dispc), support MCU IF, RGB IF
- Supports panel resolution up to FWVGA(854x480)
- Support 2 layers, one is image and another is OSD
- Support YUV422/YUV420/YUV400/RGB888/RGB565/RGB666/RGB555/PACK data format in image layer;
- Support RGB888/RGB565/RGB666/RGB555/PACK data format in OSD layer
- Support dithering, RGB888->RGB666, RGB888->RGB565

Image Sensor Interface

- Support JPEG image sensor sizes up to 5M pixels
- Support YUV image sensor sizes up to 2M pixels
- Support image sensor data YCbCr, and JPEG format, support both CCIR601 and CCIR 656

Image signal processor

- Support scaling down/up functions, scaling factors from 1/4 to 2
- Support hardware rotation
- Support JPEG decoder baseline profile, as defined in ISO/IEC 10918-1, with sizes up to 5M pixels, and color format YUV444, YUV422/YUV422R, YUV420, YUV411/YUV411R or gray scale
- Support JPEG encoder baseline profile, as defined in ISO/IEC 10918-1, with sizes up to 5M pixels, and color format YUV422 or YUV420
- Support PNG, GIF decoder

Video codec

- H.264 encoder for Baseline Profile upto Level 3.1 720p 30fps
- MPEG4 encoder for Simple Profile upto 720p 30fps

 H.264 decoder for Baseline Profile, Main Profile and High Profile upto Level 4.1 720p 30fps

 MPEG4 decoder for Simple Profile, Advanced Simple Profile upto 720p 30fps

 H.263 decoder for Baseline profile upto 720p 30fps

 VC1 decoder for simple profile, main profile upto high level 720p 30fps

 VP8 decoder upto 720p 30fps

 Multiple codec: supports up to 1 decoding and 1encoding processes simultaneously, each process can have a different format

Graphic Signal Processor

 Support 2 mode of 2 layer alpha blending and color key.(layer1 is bottom layer,layer2 is uppermost layer),

 Support image and OSDs blending; OSDs blending;

 Support clipping;

 Support 90,180 and 270 degree rotation, flip horizontal and flip vertical in each layer.

 Support layer1 scaling from 1/4~4, and in fetch phase, implement 1/2, 1/4 down sample before scaling. No support scale up and down in different direction synchronously

 Support alpha scaling.

 Support BitBlt

 Support command queue mode for BitBlt (only for layer2)

 Support dithering RGB888 to RGB565;

 Support endian configures.

Audio codec

 Wavetable synthesis up to 64 tones

 Support MP3/AAC/AAC+/WMA/DRA/AMR-NB decoding

 PCM record and playback

 Digital audio playback

Connection Features

Blue tooth

 V2.1+EDR/V4.0LE

 On-chip TX/RX Switch to simple external hardware design

 Support standard HCI specification

 Support WiFi-BT coexistence

WiFi

 Compliant to IEEE 802.11b/g/n

 Support 802.11e/i/h/j

- Support both Access Point and STAtion
- Support WEP, WPA-TKIP, AES, WPA2
- Support 802.11e QoS
- Support A-MPDU, A-MSDU and Block-ACK
- Support WiFi-BT coexistence

GPS

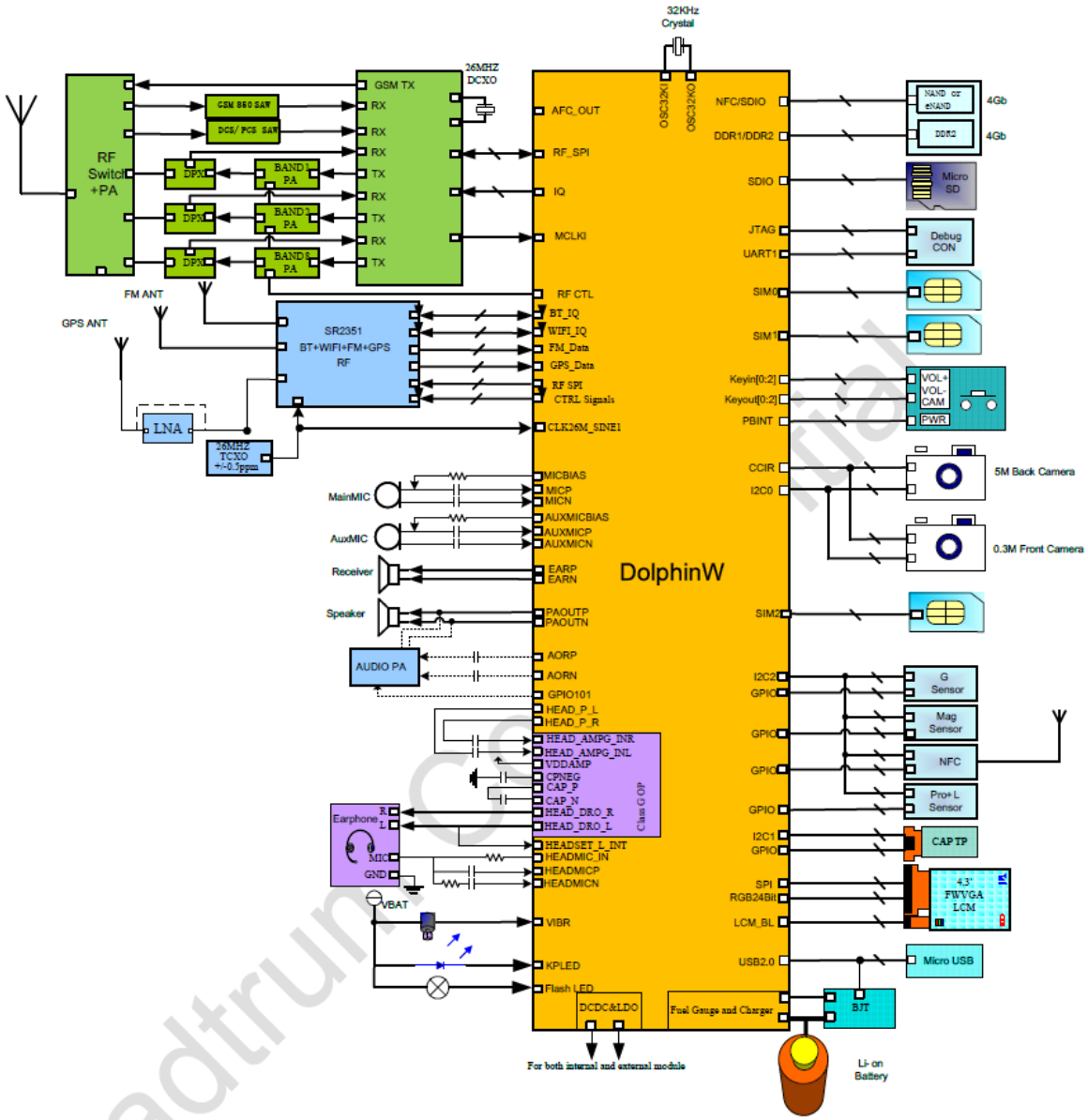
- Acquistion -160dBm, tracking -145 dBm
- Suport SUPL1.0

FM

- Support US/Europe band (87.5~108MHz)
- Support Radio Data System demodulator

PMU feature

- Integrated 5 DC-DCs and 22 low dropout regulators (LDOs), supplying power for internal chip or external devices. All such DC-DCs and LDOs can be powered down and up with software management.
- Support standby mode with small deep-sleep current.
- Integrated Li-ion battery charger, support charging from USB or external adaptor. The charger voltage can be measured with auxiliary ADC.
- Integrated whiteLED driver, keypad driver, flash driver, vibrator.
- Integrated charger detect support BC1.2.
- Integrated coloumb counter.


32KHz Crystal
26MHZ DCXO
GSM TX
RX
RX
RX
TX
RX
TX
RX
TX
GSM 850 SAW
DCS/ PCS SAW
RF Switch +PA
DPX
DPX
DPX
BAND1 PA
BAND3 PA
BAND8 PA
FM ANT
GPS ANT
SR2351 BT+WIFI+FM+GPS RF
LNA
26MHZ TCXO +/-0.1ppm
AFC_OUT
RF_SPI
IQ
MCLKI
RF CTL
BT_IQ
WIFI_IQ
FM_Data
GPS_Data
RF SPI
CTRL Signals
CLK26M_SINE1
OSC32K
OSC32KO
MICBIAS
MICP
MICN
AUXMICBIAS
AUXMICP
AUXMICN
EARP
EARN
PAOUTP
PAOUTN
AORP
AORN
GPIO101
HEAD_P_L
HEAD_P_R
HEAD_AMPG_INR
HEAD_AMPG_INL
VDDAMP
CPNEG
CAP_P
CAP_N
HEAD_DRO_R
HEAD_DRO_L
Class G OP
HEADSET_L_INT
HEADMIC_IN
HEADMICP
HEADMICN
VIBR
KPLED
Flash LED
DCDC&LDO
Fuel Gauge and Charger
DolphinW
MainMIC
AuxMIC
Receiver
Speaker
AUDIO PA
Earphone
R
L
MIC
GND
VBAT
NFC/SDIO
DDR1/DDR2
SDIO
JTAG
UART1
SIM0
SIM1
Keyin[0:2]
Keyout[0:2]
PBINT
CCIR
I2C0
SIM2
I2C2
GPIO
GPIO
GPIO
GPIO
GPIO
I2C1
GPIO
SPI
RGB24BIT
LCM_BL
USB2.0
BJT
For both internal and external module
Li-on Battery
NAND or eNAND
4Gb
DDR2
4Gb
Micro SD
Debug CON
VOL+
VOL-
CAM
PWR
5M Back Camera
0.3M Front Camera
G Sensor
Mag Sensor
NFC
Pro+L Sensor
CAP TP
4.3" FWVGA LCM
Micro USB

2.2 Memory : KMN5X000ZM-B209

The KMN5X000ZM is a Multi Chip Package Memory which combines 4GB e·MMC and 4Gbit LPDDR2 S4 SDRAM.

The SAMSUNG e·MMC is an embedded MMC solution designed in a BGA package form. e·MMC operation is identical to a MMC card and therefore is a simple read and write to memory using MMC protocol v4.41 which is a industry standard.
e·MMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF) whereas 1.8V or 3V dual supply voltage (VDD) is supported for the MMC controller. Maximum MMC interface frequency of 52MHz and maximum bus widths of 8 bit are supported.

There are several advantages of using e·MMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host.

Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash mangement software or FTL(Flash Transition Layer) of e·MMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

LPDDR2-S4 uses a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. LPDDR2-S4 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins.

A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.Prior to normal operation, the LPDDR2 must be initialized.

The KMN5X000ZM is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 162-ball FBGA Type.