Operational Description / Schematics Note (Confidential)

FCC ID: A3LSMA536V

Model: ***SM-A536V***

Date: 2022-01-03

Please note that this Operational Description provides a complete description of the subject model. However, the chip(s) within the device may include additional capabilities that are not implemented for this device. Technical information pertaining to these additional capabilities may be shown within this document. The actual supported capabilities as implemented for this model are listed below.

Please find below the capabilities that are operational for this device:

Within USA:

- GSM/GPRS/EDGE 850/1900, GPRS/EDGE Multi-slot Class 12
- WCDMA 850/1900, HSDPA/DC-HSDPA (Cat.24, 64QAM), HSUPA (Cat. 6, QPSK), HSPA+ (DL Only)
- 3GPP Rel.15, LTE DL UE Cat.18 (QPSK, 16QAM, 64QAM, 256QAM), UL UE Cat.16 (QPSK, 16QAM, 64QAM, 256QAM)

  BAND2: 1.4/3/5/10/15/20 MHz BW
  BAND4: 1.4/3/5/10/15/20 MHz BW
  BAND5: 1.4/3/5/10MHz BW
  BADN7: 5/10/15/20MHz BW
  BAND12: 1.4/3/5/10 MHz BW
  BAND13: 5/10MHz BW
  BAND46: 10/20MHz BW (TDD) (DL Only)
  BAND48: 5/10/15/20MHz BW (TDD)
  BAND66: 1.4/3/5/10/15/20 MHz BW

- 3GPP Rel.16, 5G NR FR1 UL/DL, Non-Standalone & Standalone

  CP-OFDM: QPSK, 16QAM, 64QAM, 256QAM,
  DFT-s-OFDM: π/2-BPSK(UL Only), QPSK, 16QAM, 64QAM, 256QAM

  n2: 5/10/15/20 MHz BW
  n5: 5/10/15/20 MHz BW
  n66: 5/10/15/20 MHz BW
  n77(3450-3550, 3700~3980MHz): 10/15/20/25/30/40/50/60/70/80/90/100 MHz BW

  As for n77, For LTE / 5GNR User equipment (UE) will not initiate transmissions and will only transmit after receiving the Node B (Base Station) device transmissions containing the Master Information Block (MIB) and System Information Block (SIB) necessary for it to join the network. Therefore transmissions on non-allocated US bands cannot occur because there cannot be a Node B device operating on non-US bands in the USA / US Territories. Similar protocols are followed for 2G and 3G to ensure that the device will not transmit on bands it supports but are not covered by US allocation.

  The failsafe mechanism to ensure 5G NR n77 always operates within 3450-3550, 3700-3980 MHz FCC Part 27 operation, and not the entire 3GPP range, is that the DUT will be hard limited by the chipset to operate only within the C-Band 3450-3550, 3700-3980 MHz regardless of the device operating in the US or not. This cannot be modified by any end-user or third-party to disable this mechanism.

- 3GPP Rel.16, 5G NR FR2 UL/DL (CP-OFDM: : QPSK, 16QAM, 64QAM,
  DFT-s-OFDM: π/2-BPSK(UL Only), QPSK, 16QAM, 64QAM), Non-Standalone Only

  n260: 50/100 MHz BW
  n261: 50/100 MHz BW

- WLAN 2.4GHz 802.11(b/g/n) (20MHz)
  WLAN 5GHz 802.11a
  WLAN 5GHz 802.11n(HT20, HT40)
  WLAN 5GHz 802.11ac(VHT20,VHT40, VHT80)

- Bluetooth v5.1 BDR + EDR + LE
- Mobile Hotspot
- GNSS, GPS, NFC
- LTE UL Carrier Aggregation
- S.LSI TAS Algorithm: Please see on page 21.
- This device support carrier voice calls over 5GNR (VoNR / Vo5G).

Non-USA:

- GSM/GPRS/EDGE 900/1800
- UMTS B1 / B8
- LTE Band FDD 1, 3, 20, 28
- 5G NR FR1 n78

Although the chipset documentation may indicate possible functions,
the following have been permanently disabled in this device and cannot be enabled by
the end user or service provider:

- All CDMA/EVDO Bands not listed above
- All WCDMA/ HSDPA/ HSUPA/ HSPA+ Bands not listed above
- All GSM/GPRS/EDGE Bands not listed above
- All LTE Bands not listed above
- 5G NR Bands not listed above

1. RF Circuit Description

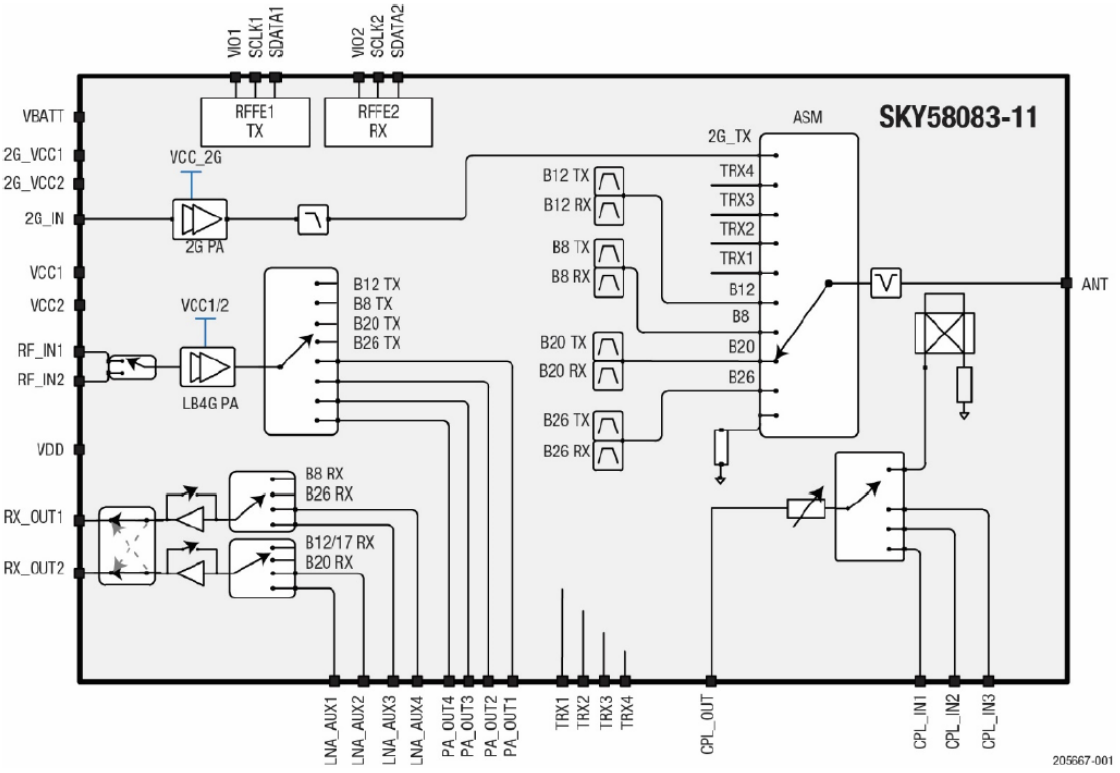
1.1 LPAMID : SKY58083-11

1) General Description

The SKY58083-11 is a multimode multiband (MMMB) Tx-Rx front end module (FEM) with integrated Low Noise Amplifiers (LNAs) which supports 2G / LTE / 5G NR handsets. The SKY58083-11 includes the SkyOne® platform, a highly configurable, integrated connectivity solution enabling next generation mobile devices with the most advanced wireless architectures. The SKY58083-11 is part of our Sky5® product portfolio.

The module consists of a 4G PA block operating in the LTE low bands, a 2G PA operating in GSM850/900 bands, a Si logic block controlling multiple power levels and enable band selections. RF I/O ports internally matched to 50 ohms minimize external components. Extremely low leakage current maximizes handset standby time. The InGaP/GaAs die and passive components are mounted on a multi-layer laminate substrate and the assembly encapsulated in plastic overmold.

2) Block Diagarm



1.2 OMH LPAMID : QM77098

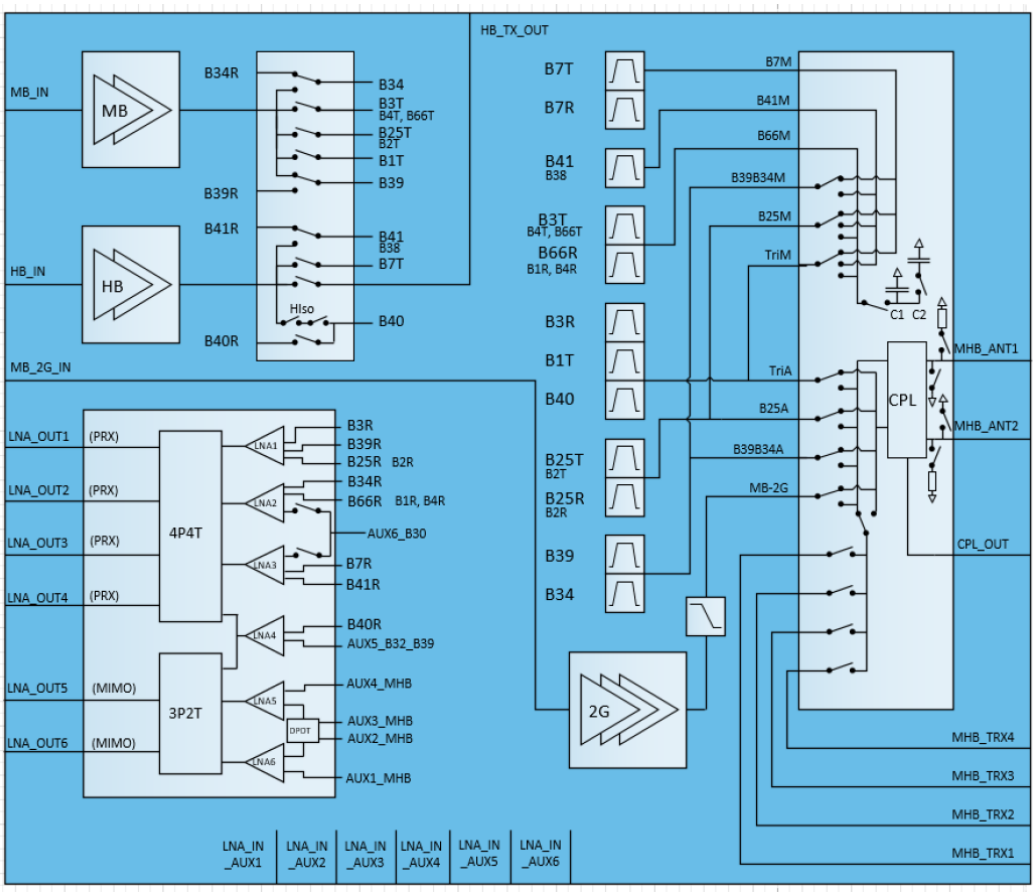
1) General Description

The Qorvo® QM77098 is a highly integrated Mid and High Band L-PAMiD compliant to 2G(MB), 3G, 4G and 5G standards targeted for complex flagship and premium TDD and FDD smartphones and data devices. The high efficiency L-PAMiD module consists of separate Mid and High Band PA paths, six LNA paths, distribution switches, filters, and antenna switches for multi-band coverage. The QM77098 supports Average Power Tracking (APT) for application versatility combined with higher system efficiency across a wide range of power levels. The QM77098 is packaged in a RoHS-compliant, compact 56-pin, 6.2 x 7.4 x 0.7 (max) mm surface-mount leadless package.

2) Key Features

- Integrated MB and HB LNAs
- Multi-Mode and Multi Band Capabilities
- 2G MB/WCDMA/CDMA2000/ FDD-LTE/TDD-LTE / NR
- Integrated Band 1, 2/25, 3, 66, 4, 7, 34, 39, 40 and 41(38) Filters for Transmit and Receiver
- Additional Bands Through External AUX Paths
- Intra-Band Uplink and Downlink Carrier Aggregation (CA): B1, B3, B7, B39, B40, B41
- Inter-band Downlink Carrier Aggregation (DL CA) functionality: B1+B3+B7, B1+B3+B40, B1+B3+B41, B25+B66+B7, B25+B41+B66, B3+B1+B41, B3+B1+B40, B3+B1+B7, B66+B25+B41, B66+B25+B7, B7+B25+B66, B7+B1+B3, B7+B40 and B41+B39+B34
- Designed and Optimized for Use with DC-DC Converter
- Support of Average Power Tracking (APT) for High System Efficiency and Versatility
- Supports 5G NR bands n1, n25, n3, n4, n7, n40, n41, n66 and n30(AUX)
- Supports Multiple MIMO bands with internal DPDT
- Module Configuration Programmable with MIPI RFFE V2.1
- Applied Microshield™, self-shielded technology

3) Block Diagram



1.3 N77 PAM : QM78078

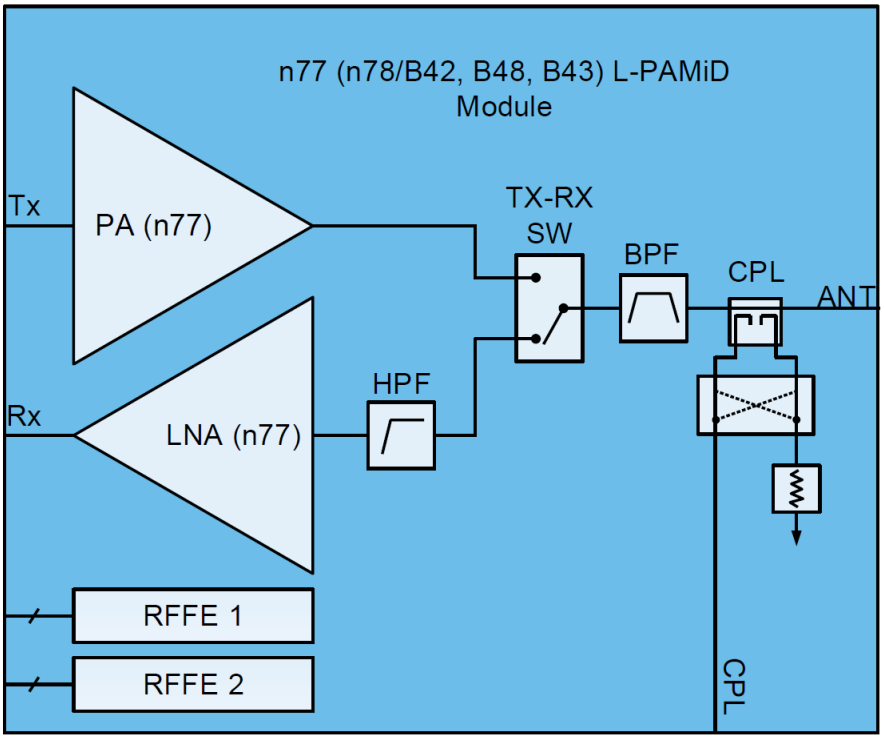
1) General Description

The Qorvo® QM78078 is a highly integrated Sub-6GHz UHB L-PAMiD compliant to both 4G-LTE and 5G-NR standards targeted for advanced RF devices including flagship/premium smartphones and data devices. The module consists of Ultra-High Band PA, LNA, Filter, directional coupler and TxRx Switch for TDD operation. QM78078 supports Envelope Tracking (ET) as well as Average Power Tracking (APT). An integrated LNA provides low noise figure, high linearity, and optimal system sensitivity with support for high order carrier aggregation. The QM78078 is packaged in a RoHS-compliant, 5mm x 3mm package.

2) Key Features

- 5G-NR Bands n77, n78.
- 4G LTE Bands B42, B48, B43.
- Integrated UHB LNA and filtering
- Global CA Platform
- Forward and reverse coupler
- Dual core MIPI RFFE
- Switchable Vcc Capacitance to reduce loading on other wideband ET PAs when not in active

3) Block Diagram



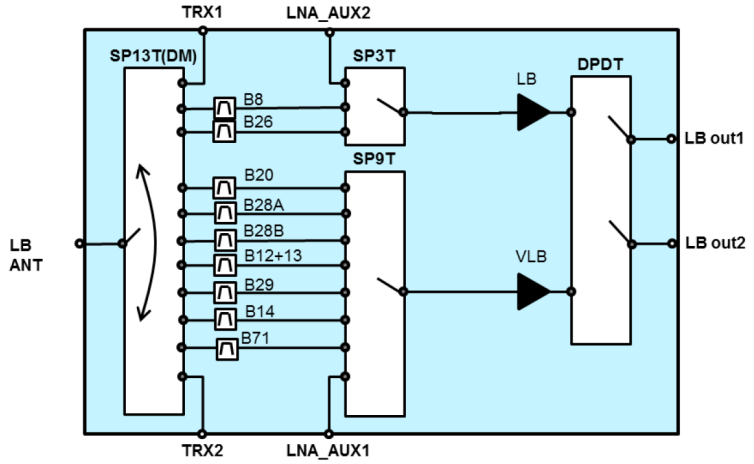
1.5 DRX LB LFEM : HFQRX4WJB-451

1) Electrical Specification

Specifications	Test conditions	Notes	HF-451			Units
			Min	Typ	Max	
Supply Voltage	Vdd		-0.3		2.4	V
Control Voltage	VIO		-0.3		2.4	V
Input RF Power	Aux - LNA out	880~915M, 824~849MHz			30	dBm
		1710~1785MHz, 1850~1910MHz			25	dBm
		@ RX Freq.(G0~G4)			20	dBm
		@ TX Freq.			23	dBm
	Ant-TRx port	LB(NR PC2)			30	dBm
		MB, HB(NR PC2)			30	dBm
	Ant-LNA out	880~915M, 824~849MHz			25	dBm
		1710~1785MHz, 1850~1910MHz			25	dBm
		@ RX Freq.(G0~G4)			20	dBm
		@ TX Freq.			23	dBm
DC Voltage MAX	All RF ports				1.0	V
ESD	HBM	All ports	-2000		2000	V
	CDM	All Ports	-1000		1000	V
	ESD-IEC61000	All Ports	-6000		6000	V
Storage Temperature			-55		125	°C

Specifications	Test conditions	Notes	HF-451			Units	Notes
			Min	Typ	Max		
Supply Voltage			1.5	1.8	2.1	V	
Supply Current	OFF State			0.4	5.0	uA	
Digital control signals (SDATA, SCLK), output low voltage			0		0.2*VIO	V	
Digital control signals (SDATA, SCLK), output high voltage			0.8*VIO		VIO	V	
Control voltage	VIO		1.65	1.8	1.95	uA	
Control Current	VIO/SDATA/SCLK	Idle State			110.0	uA	
Start Up Time	All Gain State, Within 0.1dB				5.0	us	Within 0.5dB
Gain Setting Time	All Gain State, Within 0.1dB				1.0	us	Within 0.5dB
Band Switching Time	All Gain State, Within 0.1dB	Ant-Output			2.0	us	Within 0.5dB
Operating Temperature			-30.0		85.0	°C	
Stability	k		1.0				
Impedance				50.0		Ω	
Phase Discontinuity	All Gain State		-20.0		20.0	deg	
Noise Figure (LNA Only)	G0(Gain Mode0)	Nf, All Bands		1.2		dB	G0 Bias4
	G0(+Tx Jamming=-25 dBm)	Nf, All Bands		1.3		dB	G1 Bias4
	G1(Gain Mode1)	Nf, All Bands		1.3		dB	G1 Bias4
	G2(Gain Mode2)	Nf, All Bands		3.7		dB	G2 Bias4
	G3(Gain Mode3)	Nf, All Bands		11.5		dB	G3 Bias4
	G4(Gain Mode4, Bypass, Option)	Nf, All Bands		3.0		dB	G4 Bias0
Power Gain (Include the switches and Splitter)	G0(Gain Mode0)	All Bands		19		dB	G0 Bias4
	G1(Gain Mode1)	All Bands		15		dB	G1 Bias4
	G2(Gain Mode2)	All Bands		9		dB	G2 Bias4
	G3(Gain Mode3)	All Bands		-3		dB	G3 Bias4
	G4(Gain Mode4, Bypass, Option)	All Bands		-3		dB	G4 Bias0
Additional NF & Decremental Gain	2CA	All Bands		1.0		dB	
Return Loss	LB	ANT, Non CA	2.5	6.5		dB	
Reverse Isolation (1/|S12|²)	LM	All Low Bands	24.0	35.0		dB	
Inband input 1dB compression point	G0(Gain Mode0)	All Bands	-23	-16		dBm	G0 Bias4
	G1(Gain Mode1)	All Bands	-21	-16		dBm	G1 Bias4
	G2(Gain Mode2)	All Bands	-17	-11		dBm	G2 Bias4
	G3(Gain Mode3)	All Bands	-6	-1		dBm	G3 Bias4
	G4(Gain Mode4, Bypass, Option)	All Bands	6	11		dBm	G4 Bias0
Inband input 3rd-order intercept point	G0(Gain Mode0)	All Bands	-16	-3		dBm	G0 Bias4
	G1(Gain Mode1)	All Bands	-13	-2		dBm	G1 Bias4
	G2(Gain Mode2)	All Bands	-10	1		dBm	G2 Bias4
	G3(Gain Mode3)	All Bands	-2	10		dBm	G3 Bias4
	G4(Gain Mode4, Bypass, Option)	All Bands	15	35		dBm	G4 Bias0
Isolation(Internal Switch, Antenna to any off Rx port)	LM	All Low Bands	30	33		dB	
Isolation(Output Switch or Splitter)	LNA Out1-Out2	All Bands	25			dB	
Power handling(Internal BPF)	DC impedance to ground		10			MΩ	
RSE Case2	See RSE Case2				-40	dBm	
DC Leakage	All RF Ports				0	V	
Shield Resistance					15	Ω	

2) Block diagram



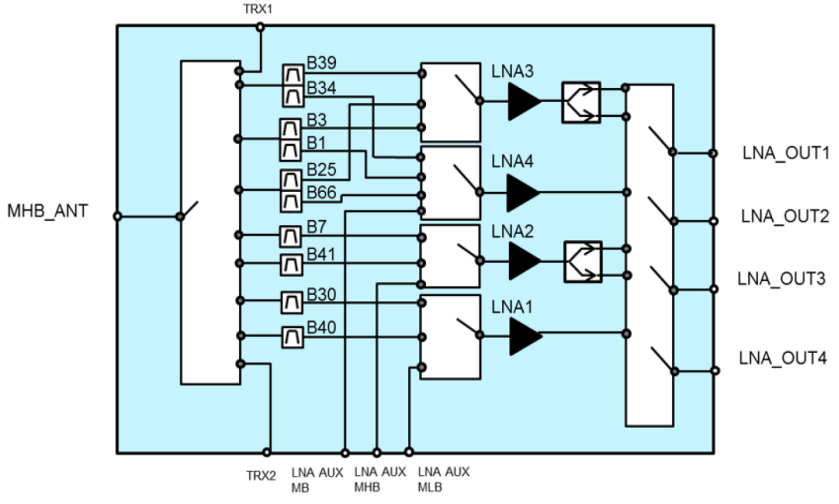
1.6 DRX MHB LFEM : HFQRX4WJB-452

1) Electrical Specification

Specifications	Test conditions	Notes		Min	Typ	Max	Units
Supply Voltage	Vdd			-0.3		2.4	V
Control Voltage	VIO			-0.3		2.4	V
DC Voltage	Apply DC voltage to RF port	All RF ports, no leakage				5	V
Input RF Power	ANT-LNA_OUT (#4)	880~915M, 824~849MHz (#2)				30	dBm
		1710~1785MHz, 1850~1910MHz	B3 (#3)			21	dBm
			B25 (#3)			25	
			B1,66,40,7,30,41,34,39 (#2)			25	
		@ RX Freq. (#1)	B41			19	dBm
			B1,66,3,25,40,7,30,34,39			20	
		@ TX Freq. (#1)	B3			18	dBm
			B25			20	
			B7			21	
			B30			22	
			B1,66			23	
	LNA_AUX-LNA_OUT (#4)	880~915M, 824~849MHz (#2)				30	dBm
		1710~1785MHz,1850~1910MHz (#2)				25	dBm
		@ RX Freq. (#1)				20	dBm
		@ TX Freq. (#1)				23	dBm
	ANT - TRX	1.4~2.7GHz				30	dBm
	TRX - ANT	1.4~2.7GHz				30	dBm
ESD	HBM	All ports		-2000		2000	V
	CDM	All Ports		-1000		1000	V
	IEC61000	ANT Port, w/56nH		-6000		6000	V
Operating Temperature				-30		85	°C
Storage Temperature				-55		130	°C

Specifications	Test conditions	Notes	HF-452			Units	Notes
			Min	Typ	Max		
Supply Voltage			1.5	1.8	2.1	V	
Supply Current	OFF State				5.0	uA	
Digital control signals (SDATA, SCLK), output low voltage			0.0		0.2 X VIO	V	
Digital control signals (SDATA, SCLK), output high voltage			0.8 X VIO		VIO	V	
Msel Low voltage			0.0		0.2 X VIO	V	
Msel High voltage			0.8 X VIO		VIO	V	
Control Voltage	VIO		1.65	1.8	1.95	V	
Control Current	VIO/SDATA/SCLK	Idle State			160.0	uA	
Start Up Time	All Gain State, Within 0.1dB				5.0	us	Within 0.5dB
Gain Setting Time	All Gain State, Within 0.1dB				1.0	us	Within 0.5dB
Band Switching Time	All Gain State, Within 0.1dB	Ant-Output			2.0	us	Within 0.5dB
Operating Temperature			-30.0		85.0	°C	
Stability	k		1.0				
Impedance				50.0		Ω	
Phase Discontinuity	All Gain State		-20.0		20.0	deg	
Noise Figure (LNA Only)	G0(Gain Mode0)	Nf, All Bands		1.6		dB	Bias4
	G0(+Tx Jamming=-25 dBm)	Nf, All Bands		1.7		dB	Bias4
	G1(Gain Mode1)	Nf, All Bands		1.8		dB	Bias4
	G2(Gain Mode2)	Nf, All Bands		3.5		dB	Bias4
	G3(Gain Mode3)	Nf, All Bands		11.5		dB	Bias4
	G4(Gain Mode4, Bypass, Option)	Nf, All Bands		4.9		dB	Bias0
Power Gain (Include the switches and Splitter)	G0(Gain Mode0)	All Bands		19.1		dB	Bias4
	G1(Gain Mode1)	All Bands		13.8		dB	Bias4
	G2(Gain Mode2)	All Bands		6.2		dB	Bias4
	G3(Gain Mode3)	All Bands		-4.2		dB	Bias4
	G4(Gain Mode4, Bypass, Option)	All Bands		-3.0		dB	Bias0
Power Gain (Non-Contiguous CA, Split, LNAout port)	G0(Gain Mode0)	All Bands		18.1		dB	Bias4
	G1(Gain Mode1)	All Bands		12.8		dB	Bias4
	G2(Gain Mode2)	All Bands		5.2		dB	Bias4
	G3(Gain Mode3)	All Bands		-5.2		dB	Bias4
	G4(Gain Mode4, Bypass, Option)	All Bands		-4.0		dB	Bias0
Additional NF & Decremental Gain	2CA	All Bands		0.3		dB	
	3CA	All Bands		1.6		dB	
	4CA	All Bands		2.0		dB	
Return Loss	MB	ANT, Non CA	3.0	4.8		dB	
Reverse Isolation (1/|S12|²)	LM	All Low Bands	24.0	41		dB	
	MB	All Mid Bands	24.0	33		dB	
	HB	All High Bands	24.0	40		dB	
Inband input 1dB compression point	G0(Gain Mode0)	All Bands	-27.0	-22.3		dBm	Bias4
	G1(Gain Mode1)	All Bands	-23.0	-15.8		dBm	Bias4
	G2(Gain Mode2)	All Bands	-17.0	-8.0		dBm	Bias4
	G3(Gain Mode3)	All Bands	-8.0	-1.2		dBm	Bias4
	G4(Gain Mode4, Bypass, Option)	All Bands	8.0	21.1		dBm	Bias0
Inband input 3rd-order intercept point	G0(Gain Mode0)	All Bands	-18.0	-12.4		dBm	Bias4
	G1(Gain Mode1)	All Bands	-13.0	-4.9		dBm	Bias4
	G2(Gain Mode2)	All Bands	-7.0	2.5		dBm	Bias4
	G3(Gain Mode3)	All Bands	2.0	15.3		dBm	Bias4
	G4(Gain Mode4, Bypass, Option)	All Bands	15.0	30.6		dBm	Bias0
Isolation(Internal Switch, Antenna to any off Rx port)	LM	All Low Bands	30.0	44.0		dB	
	MB	All Mid Bands	25.0	41.0		dB	
	HB	All High Bands	20.0	38.0		dB	
Isolation(Output Switch or Splitter)	LNA Out1-Out2	All Bands	15.0	26.0		dB	
Power handling(Internal BPF)	DC impedance to ground		10			MΩ	
RSE Case2	See RSE Case2				-40	dBm	
DC Leakage	All RF Ports			0.0		V	
Shield Resistance					15	Ω	

2) Block diagram



1.9 mmW Antenna Module : SGB5640X01-M040

1.9.1 Key Features

☐ Process: 28 nm CMOS

☐ Package: Wafer level chip scale package (WL-CSP)

☐ Control Protocol: PSpeedy or Hspeedy

☐ Two IF interfaces at ~9 GHz connecting to S5720

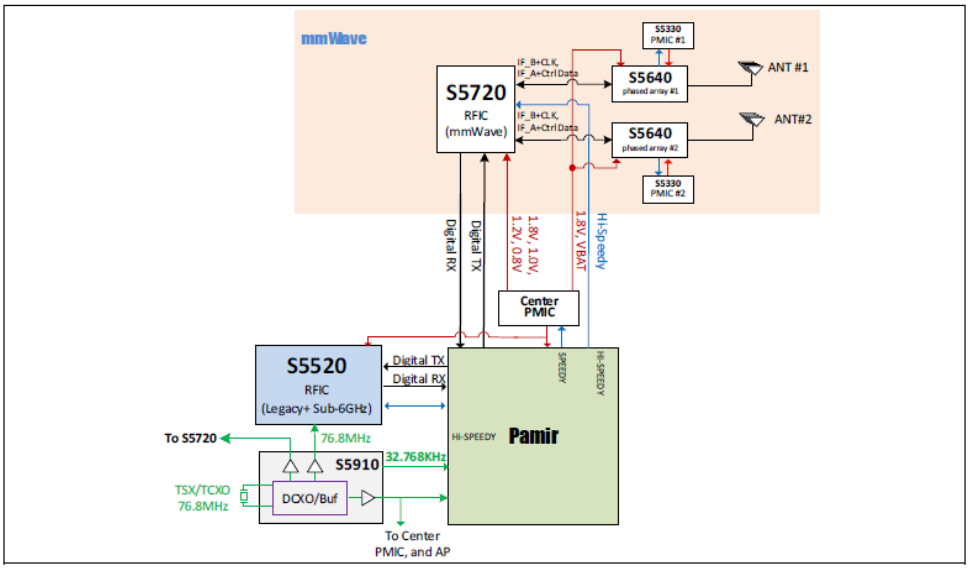
☐ Supports 5 TRx chains per IF (total 10) for low band, and 5 TRx chains per IF (total 10) for high band

☐ Supports N257/258/260/261 5G NR mm-wave bands

☐ Sliding IF up and down conversion architecture

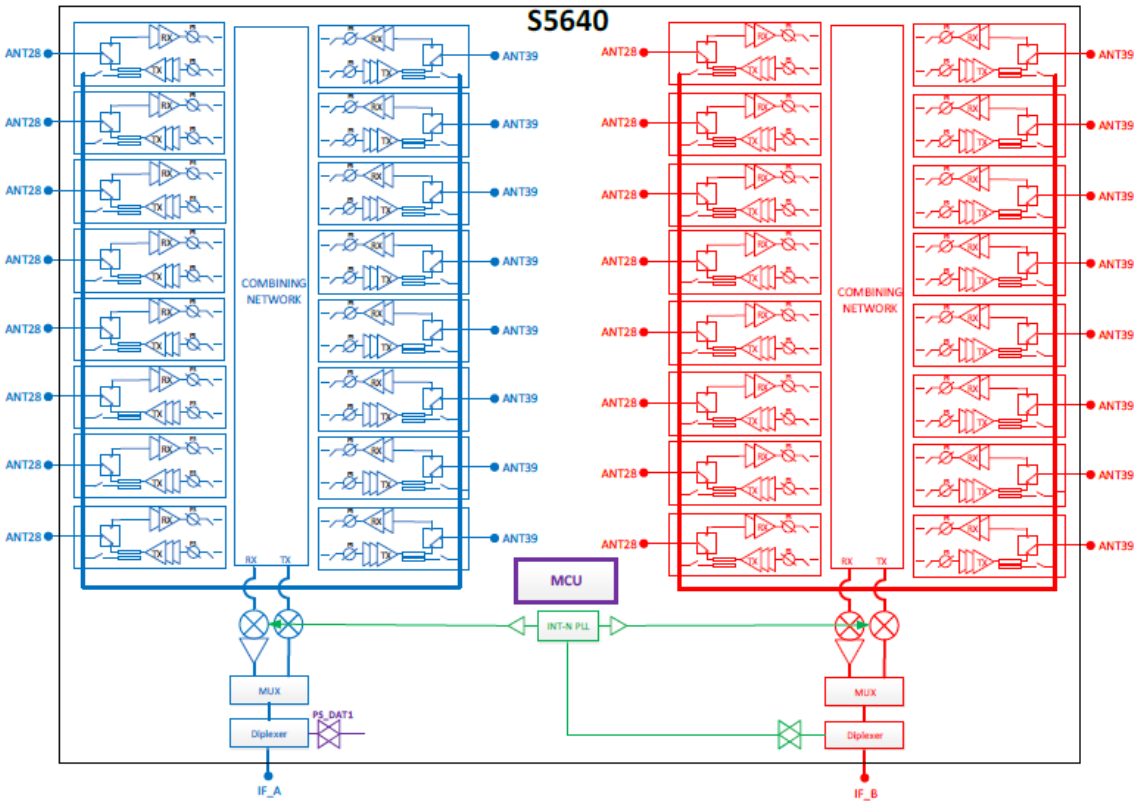
1.9.2 System Diagram

Figure 1-1 shows one 5G NR solution for cellular handsets. It consists of one S5720, one modem chip (Pamir) and two separate phased array chips (S5640). The modem uses digital interface for communication to S5720 (both receive and transmit). Inside the S5720 in the transmitter mode, these signals are filtered and up-converted to an intermediate frequency (IF) and sent via the four IF ports to the two phased array chips. These IF ports also allow control data and clock, and 560MHz reference clock to be sent from S5720 to the phased array chips. Note that the S5720-to-S5640 IF interconnection loss at the clock frequency must not exceed 1dB, so that the clock input power at the S5640 clock input is at least -8 dBm. S5720 can connect to two phased array chips but only one phase array can work in the transmitter mode, and two can be operating concurrently in the receiver mode. Note that S5640 supports two types of control interface: PSpeedy and HSpeedy. The configuration shows the use of PSpeedy, where both clock and data are multiplexed along with the IF signals.



1.9.3 Chip Block Diagram

The block diagram of S5640 is shown in Figure 1-2. There are totally 20 antenna ports in S5640: 10 for 28GHz band, and 10 for 39GHz band. A0~A4 are driven by the IF_A port, and B0~B4 are driven by the IF_B port. An integer-N PLL is added to generate the LO clock at ~18GHz for the RF mixers. Any antenna ports are built with identical circuitry with same performance. Selecting which ports to use is totally up to module designer's plan. Both reference clock at ~560MHz of the PLL and PSpeedy data will be generated from S5720 and transmitted through the IF cables. IF_B port has both IF signal plus reference clock, and IF_A port has both IF signal plus data information.



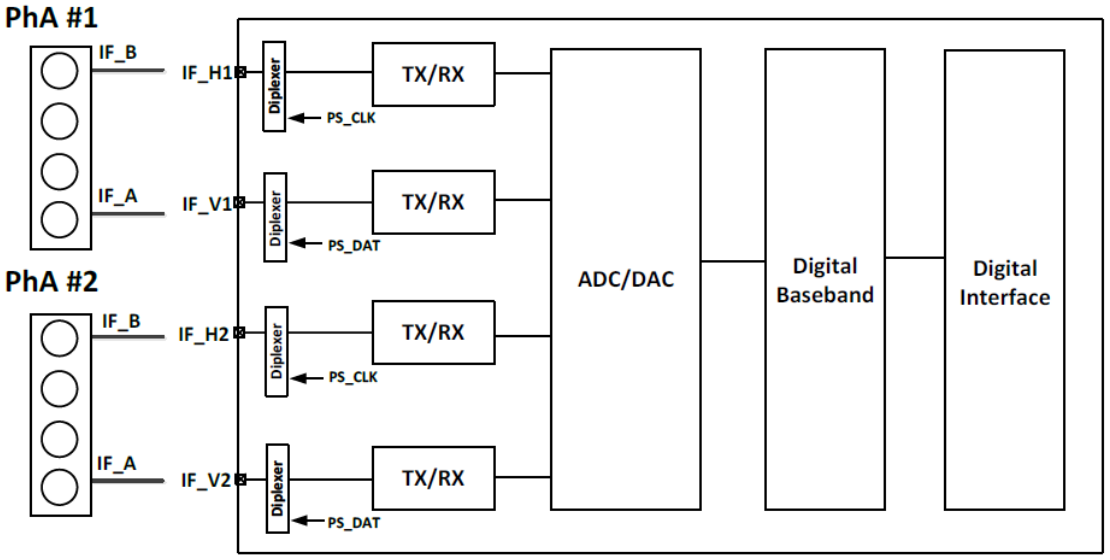
1.10 mmW IFIC : S5M5720X01-7030

1.10.1 Key Features

- Process: 14nm CMOS 1P9M
- Package: Wafer level chip scale package (WL-CSP)
- Supports two phased array chips each with two IF interfaces, with both phased array chips concurrently active in receiver mode
- 9GHz signal + 560MHz LO + register access and control to phased array modules
- Integrated PLL
- Downlink path supports up to 800 MHz on each IF chain, and 1.4GHz RF BW (when split between two IF chains)
- UL path supports up to 800 MHz.
- Integrated ADC/DAC Digital filter and digital interface to modem chip (S5123)
- Integrated MCU and memory for calibration and control

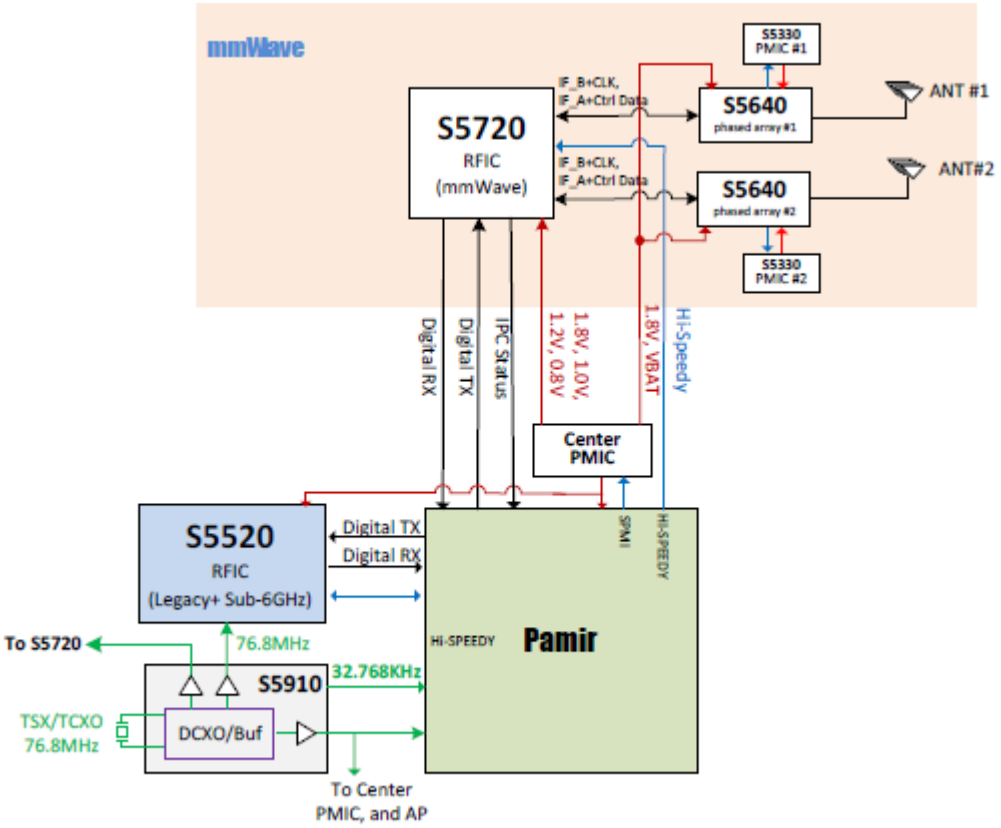
1.10.2 Chip Block Diagram

The block diagram shows the S5720 internal architecture. It has four IF ports that can connect to two phased array chips, providing two independent IF paths for each, indicated by IF_H and IF_V in the figure. Each IF_V and IF_H pair uses the same LO frequency, but the LO frequency of the two pairs can be different. The chip has four receiver (Rx) and four transmitter (Tx) chains. The transmitter chain filters the analog baseband signal coming from the DAC, up-converts it to 9GHz IF with its IQ modulator, and drives it to the RF output through the driver amplifier (DA) and the T/R switch. In the receiver mode, the IF input coming from the phased array chip passes through the diplexer and T/R switch, and gets amplified (if necessary) and then down-converted to the base band using IQ demodulators. The signal is then filtered by low-pass filters in the base band, and sent to ADCs. S5720 controls the phased array modules via PSpeedy interface. PSpeedy requires two signals: reference clock at ~560 MHz, PS_CLK, and control data, PS_DAT at 140MHz. On the IF_H, a diplexer is used to combine 9-GHz IF_H with PS_CLK so that they can be multiplexed over one signal line. Similarly, another diplexer is used on IF_V to combine the IF signal and PS_DAT. PS_CLK is also used as reference clock for PLL in the phased array chip.



1.10.3 System Diagram

The block diagram shows one 5G NR solution for cellular handsets. It consists of one S5720, one modem chip (Pamir) and two separate phased array chips (S5640). The modem uses digital interface for communication to S5720 (both receive and transmit). Inside the S5720 in the transmitter mode, these signals are filtered and upconverted to an intermediate frequency (IF) and sent via the four IF ports to the two phased array chips. These IF ports also allow control data and clock, and 560MHz reference clock to be sent from S5720 to the phased array chips. Note that the S5720-to-S5640 IF interconnection loss at the clock frequency must not exceed 1dB, so that the clock input power at the S5640 clock input is at least -8 dBm. S5720 can connect to two phased array chips but only one phase array can work in the transmitter mode, and two can be operating concurrently in the receiver mode. Note that the shown solution is an example with the 76.8 MHz reference clock, but the chip can also work with 52 MHz reference clock.



1.11 Grip Sensor : SX9380

1.11.1 General Description

The SX9380 is a smart capacitive sensor for SAR (Specific Absorption Rate).

The resulting detection is used in portable electronic devices to reduce and control radio-frequency (RF) emission power in the presence of a human body, enabling significant performance advantages for manufacturers of electronic devices with electro-magnetic radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards.

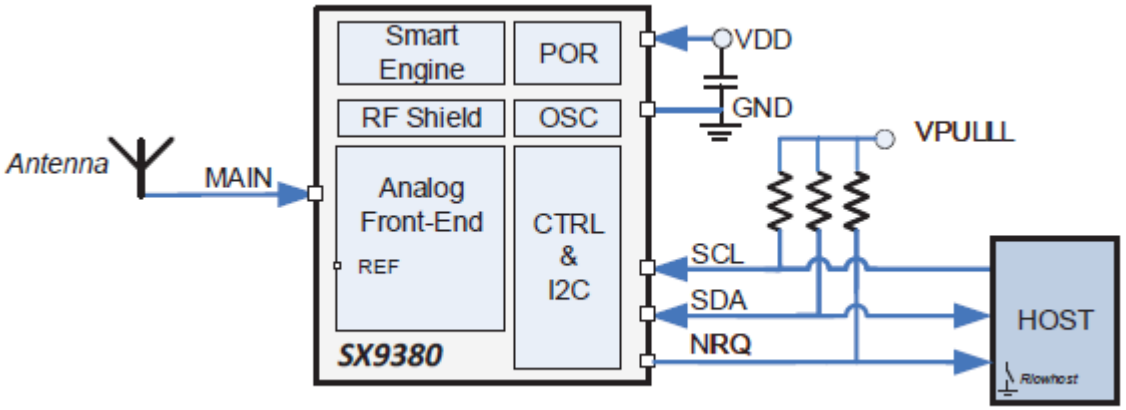
Operating directly from an input supply voltage of 2.7-3.6V, the SX9380 outputs its data via I2C serial bus. The I2C serial communication bus port is compatible with both 1.2V and 1.8V host control to report body detection/proximity and to facilitate parameter settings adjustment. Upon proximity detection, the NIRQ output asserts, enabling the user to either determine the relative proximity distance, or simply obtain an indication of detection.

The SX9380 includes an on-chip auto-calibration controller that regularly performs sensitivity adjustments to maintain peak performance over a wide variation of temperature, humidity and noise environments, providing simplified product development and enhanced performance.

1.11.2 Key Features

- ☐ 2.7-3.6V Input Supply Voltage
- ☐ High Performance Analog-Front-End
- ☐ Capacitance Resolution down to <1.5aF
- ☐ Capacitance Offset Compensation up to 400pF
- ☐ RF Shield (Patented)
- ☐ Smart Features
- ☐ Reference Correction (Patented)
- ☐ USE Filter (Patented)
- ☐ Ultra Low Power Consumption

1.11.3 System Diagram



2. LOGIC Circuit Description

2.1 AP/CP : S5E8825 (EXYNOS1280)

1) Description

S5E8825 is a System-on-Chip (SoC), which is based on a 64-bit RISC processor. It also contains a 5G communication processor (modem), which is compliant with 5G NR features and all legacy features. S5E8825 targets high-end smart phones and tablet products. S5E8825 is based on the 5 nm low-power process and it provides the following features:

☐ Octa-core CPU (Dual-core ARM Cortex-A78 (Big CPU), and Hexa-cores ARM Cortex-A55 (Little CPU)

☐ 17.1 GB/s of LPDDR4 bandwidth

☐ WQHD embedded display

☐ 4K 30-frame video decoding (H.264/HEVC) and FHD 30-frame video decoding/encoding hardware (MPEG4/H.263/VP8)

☐ 3D graphics H/W

☐ Image Signal Processor (ISP)

☐ Neural Processing Unit (NPU)

☐ ABOX (Audio Sub-System)

☐ High-speed interfaces, such as UFS 2.2 and USB 2.0 DRD

☐ Embedded communication processor (5G NR FR1 FR2, 4G LTE, 3G FDD/TDD, 2G GSM/CDMA)

☐ GNSS and WiFi/BT

☐ Context HUB (CHUB)

S5E8825 adopts ARM Cortex-A78 dual -core (Big CPU) for high performance computing. S5E8825 also supports ARM Cortex-A55 hexa-core processor for energy-efficient computing. S5E8825 provides 3D graphics functionalities with wide range of APIs, such as Vulkan 1.0/1.1, OpenGL ES 1.1/2.0/3.2, and OpenCL up to 2.2. The native single display supports the WQHD resolution LCD display. S5E8825 supports a neural network with NPU, which has Convolutional Neural Network (CNN), Recurrent Neural Network (RNN), and Long Short-Term Memory (LSTM). S5E8825 contains an integrated ISP engine ISP supports the following functionalities:

☐ Dynamic Range Control (DRC)

☐ 3-dimentional noise reduction (3DNR)

☐ Video Digital Image Stabilization (VDIS) and Rolling Shutter Compensation (RSC)

☐ Optical distortion correction

☐ AWB/AF/AE (3AA)

☐ Zero shutter lag of camera during shooting

S5E8825 tries to decrease the Bill of Materials (BOM) by integrating the following IPs:

☐ Embedded ISP

☐ Multiple channels of USI for various sensors

S5E8825 is available as 11.0 by 11.0 FCFBGA SCP with the bottom ball pitch of 0.35 mm.

2)Key features

S5E8825 supports the following features:

☐ Big CPUs known as ARM Cortex-A78 includes the following.

☐ 64 KB/64 KB I/D L1 cache

☐ 256 KB private L2 cache

☐ 1 MB shared L3 cache, which is shared with big/little octa processor

☐ Little CPU known as ARM Cortex-A55 as a power-efficient performance processor, which includes the following.

☐ 32 KB/32 KB I/D L1 cache

☐ 64 KB private L2 cache

☐ 1 MB shared L3 cache, which is shared with big/mid/little quad processor

☐ 128-bit multi-layer TREX architecture

☐ DRAM access through two channels of 16-bit LPDDR4 interface

☐ 128 KB ROM for secure booting and 100 KB internal RAM for security function

☐ Multi-core timer and generic interrupt controller/combiner for multi-core CPU system

☐ DMA controllers (1 x 8-channel PDMA and 1 x 4-channel PDMA for security purpose)

☐ Real-Time Clock (RTC)

☐ Highly structured power management system for mobile applications

☐ Flexible clock management system with system PLLs

☐ 3D graphic accelerator that supports OpenGL ES 1.1/2.0/3.0/3.2, OpenCL 1.2/2.1 full profile, OpenVG 1.1, and Vulkan 1.0 and 1.1

☐ JPEG codec for various compression formats

☐ Three on-the-fly scalers, one post scalers, on-the-fly rotator, and one write-back for display

☐ One memory-to-memory scaler

☐ 16/32 bpp RGB format and NV12, NV21 YUV420 format for display DMA

☐ LCD display through MIPI DSI interface and DSC with FHD+ and WQHD+ resolutions

☐ Customized image enhancer for display

☐ Six channels of MIPI CSI interface for six cameras

☐ Combo D-PHY/C-PHY for rear/front camera

☐ High performance ISP engine with DRC, 3DNR, VDIS, RSC, and 3AA features

☐ Ultra-low-power audio decoding co-processor with internal SRAM

☐ Unified Audio Interface (UAIF)☐ Host controller for high-speed storage interface of UFS 2.2 1-lane (6 Gbps)

☐ SD 3.0 interface (1-channel, 4-bit, and wide-range)

☐ USB 2.0 DRD (1-channel) with Type-C support

☐ USI with high-speed I2C/SPI and UART

☐ I3C I/F

☐ Context HUB with 3ea USI I/Fs

☐ DTRNG hard macro for a key generation session

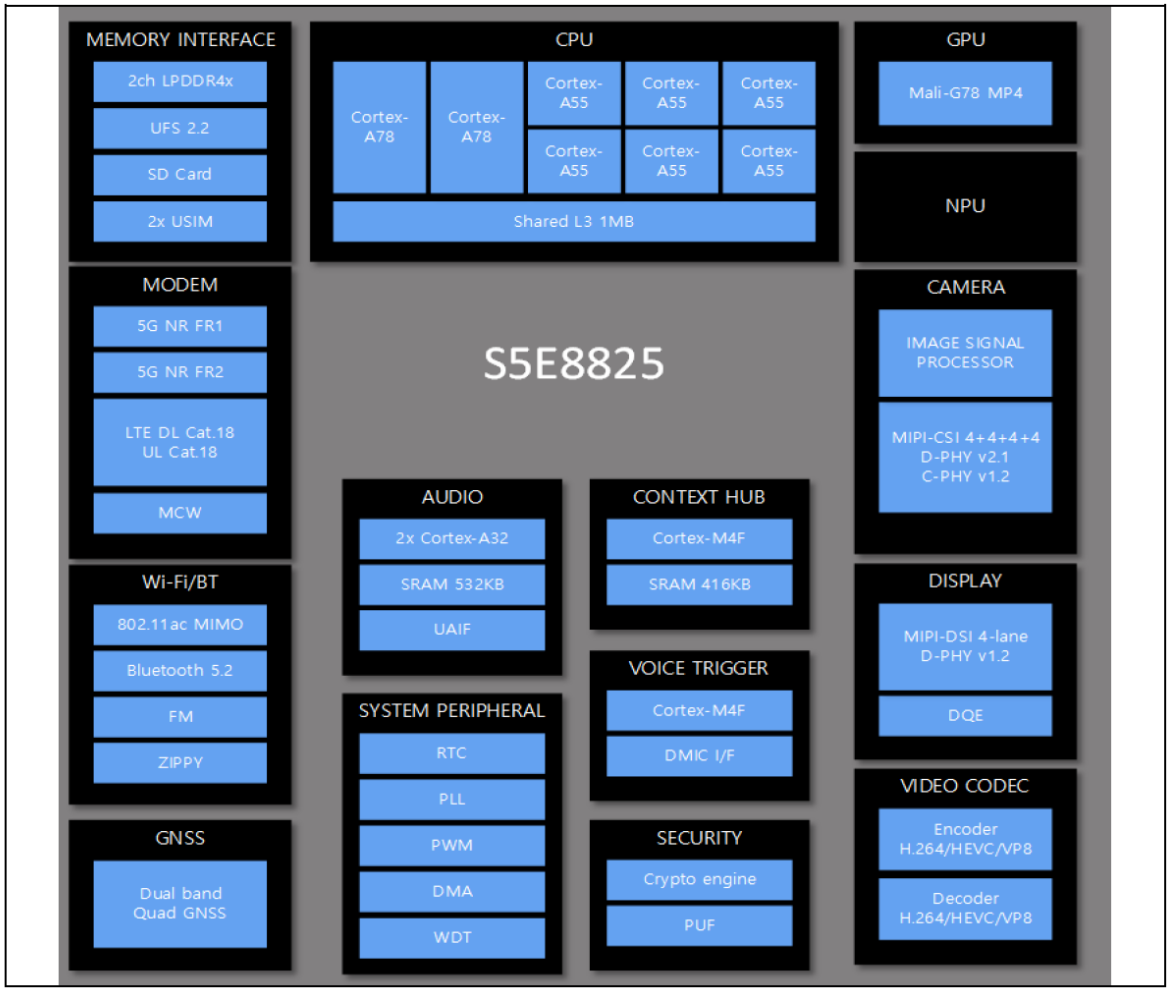
☐ Embedded communication processor (5G NR FR1 FR2, 4G LTE, 3G FDD/TDD, 2G GSM/CDMA)

☐ Bluetooth 5.2

☐ 802.11ac MIMO with Dual-band (2.4/5G) Wifi support

☐ Dual-band quad-GNSS (GPS L1 C/A , GLONASS L1, Beidou B1, B2a , Galileo E1, E5a)

3) Block Diagram



2.2 PMIC : S2MPU13X01-6330

1) Description

S2MPU13 is an advanced Power Management IC (PMIC) designed for mobile applications. It is comprised of high efficient buck converters including dual/single-phase buck converters, various LDOs, and RTC which are integrated into a 225-Wafer Level Chip Scale Package (WLCSP) with 5.50 mm × 5.50 mm package. S2MPU13 (Main PMIC) and S2MPU14 (Sub PMIC), coupled with Multi Core Samsung Application Processors (E9815), are the integrated LTE Modem-Application Processor (Modem-AP) solution in highly renowned Exynos products. This brings the advanced 5G connectivity with a full portfolio of multiband and multimode in power-efficient platform. The buck converters in S2MPU13 provide stable power to the CPU, NPU, internal logic, memory, and sub-regulators. The buck converters for high load capacity on the Application Processor (AP) provide optimal power control using Dynamic Voltage Scaling (DVS) through I3C interface between PMIC and AP. The various LDOs supply appropriate power to each I/O and functional blocks in an AP and the system. Applying independent LDO to each I/O block helps the CPU to support various types of devices. Each block can be turned on and turned off for power optimization. Other features include a thermal regulation and an internal timer function.

2) Key features

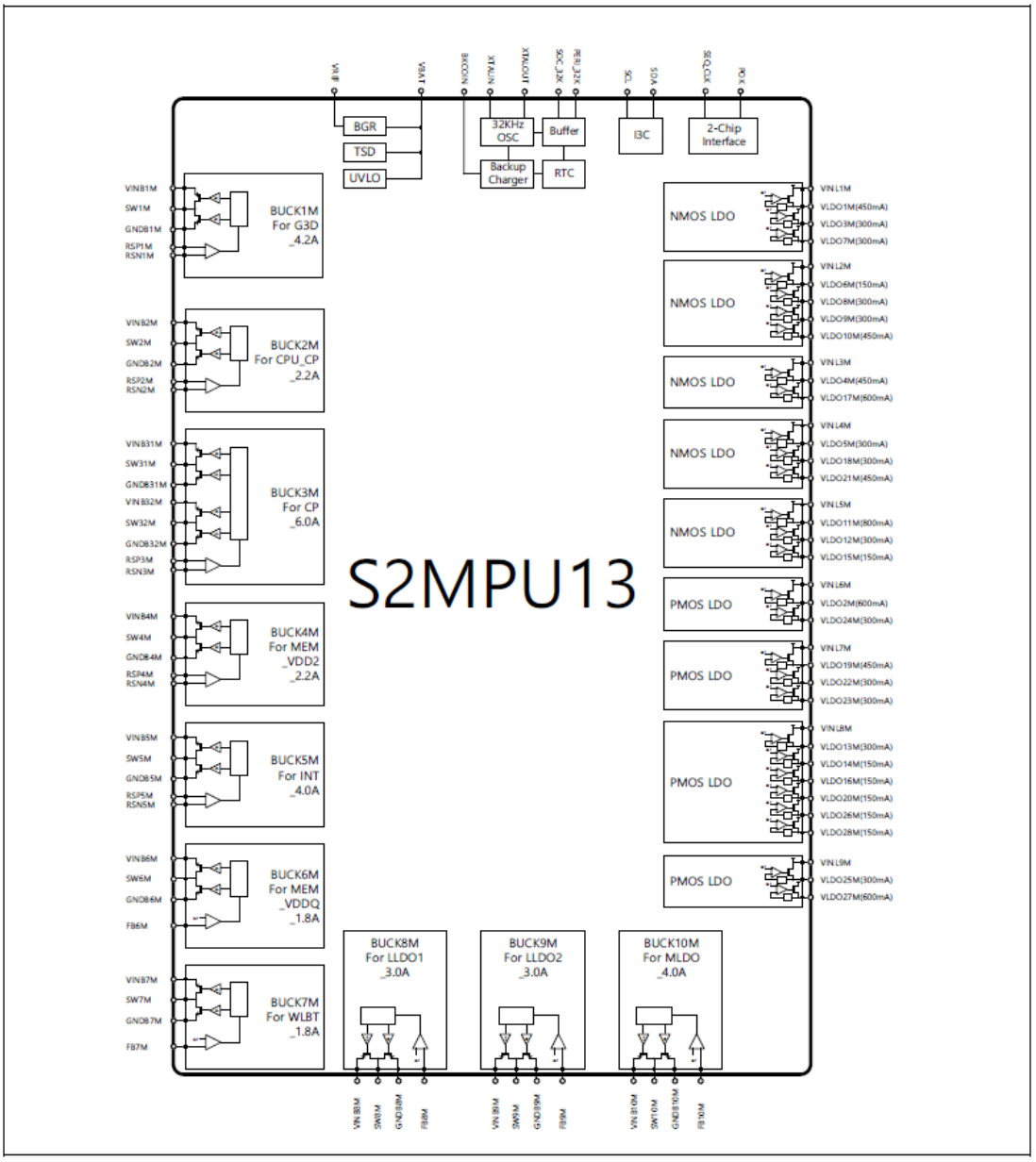
Regulators

S2MPU13 (Main PMIC) supports the following regulators:

- 10 high-efficient programmable buck converters
  - Buck1M (VDD_G3D) : 4.2 A (0.40 V to 1.30 V, 6.25 mV step, default on, 0.75 V, DVS)
  - Buck2M (VDD_CPU_CP) : 2.2 A (0.40 V to 1.30 V, 6.25 mV step, default on, 0.75 V, DVS)
  - Buck3M (VDD_CP) : 6.0 A (0.40 V to 1.30 V, 6.25 mV step, default on, 0.75 V, DVS)
  - Buck4M (VDD_MEM_VDD2) : 2.2 A (0.40 V to 1.30 V, 6.25 mV step, default on, 1.1 V, DVS)
  - Buck5M (VDD_INT) : 4.0 A (0.40 V to 1.30 V, 6.25 mV step, default on, 0.75 V, DVS)
  - Buck6M (VDDQ_MEM_VDDQ) : 1.8 A (0.40 V to 1.30 V, 6.25 mV step, default on, 0.60 V, DVS)
  - Buck7M (VDD_WLBT) : 1.8 A (0.40 V to 1.30 V, 6.25 mV step, default on, 0.75 V, DVS)
  - Buck8M (VDD_LLDO1) : 3.0 A (0.40 V to 1.40 V, 6.25 mV step, default on, 0.90 V, DVS)
  - Buck9M (VDD_LLDO2) : 3.0 A (0.90 V to 1.40 V, 6.25 mV step, default on, 1.00 V, DVS)
  - Buck10M (VDD_MLDO) : 4.0 A (1.75 V to 2.15 V, 12.5 mV step, default on, 2.00 V, DVS)

- 28 LDO regulators (13 PMOS LDOs, 15 NMOS LDOs; N:NMOS type LDO, P:PMOS type LDO)
  - LDO1M (N) : 450 mA (0.50 V to 1.1875 V, 12.5 mV step, default on, 0.75 V)
  - LDO2M (P) : 600 mA (1.60 V to 1.95 V, 25.0 mV step, default on, 1.80 V)
  - LDO3M (N) : 300 mA (0.50 V to 1.1875 V, 12.5 mV step, default on, 0.60 V)
  - LDO4M (N) : 450 mA (0.40 V to 1.30 V, 25.0 mV step, default on, 0.85 V, DVS)
  - LDO5M (N) : 300 mA (0.40 V to 1.30 V, 25.0 mV step, default on, 0.80 V, DVS)
  - LDO6M (N) : 150 mA (0.40 V to 1.30 V, 25.0 mV step, default on, 0.80 V, DVS)
  - LDO7M (N) : 300 mA (0.40 V to 1.30 V, 25.0 mV step, default on, 0.75 V, DVS)
  - LDO8M (N) : 300 mA (0.50 V to 1.1875 V, 12.5 mV step, default on, 0.75 V)
  - LDO9M (N) : 300 mA (0.40 V to 1.30 V, 25.0 mV step, default on, 0.75 V, DVS)
  - LDO10M (N) : 450 mA (0.40 V to 1.30 V, 25.0 mV step, default on, 0.75 V, DVS)
  - LDO11M (N) : 800 mA (0.725 V to 1.30 V, 12.5 mV step, default on, 0.85 V)
  - LDO12M (N) : 300 mA (0.725 V to 1.30 V, 12.5 mV step, default off, 0.80 V)
  - LDO13M (P) : 300 mA (1.60 V to 1.95 V, 25.0 mV step, default on, 1.80 V)
  - LDO14M (P) : 150 mA (1.60 V to 1.95 V, 25.0 mV step, default on, 1.80 V)
  - LDO15M (N) : 150 mA (0.725 V to 1.30 V, 12.5 mV step, default off, 0.80 V)
  - LDO16M (P) : 150 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO17M (N) : 600 mA (0.725 V to 1.30 V, 12.5 mV step, default on, 0.85 V)
  - LDO18M (N) : 300 mA (0.725 V to 1.30 V, 12.5 mV step, default off, 0.80 V)
  - LDO19M (P) : 450 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO20M (P) : 150 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO21M (N) : 450 mA (0.40 V to 1.30 V, 25.0 mV step, default off, 0.80 V, DVS)
  - LDO22M (P) : 300 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO23M (P) : 300 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO24M (P) : 300 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO25M (P) : 300 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO26M (P) : 150 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO27M (P) : 600 mA (1.60 V to 1.95 V, 25.0 mV step, default off, 1.80 V)
  - LDO28M (P) : 150 mA (1.60 V to 1.95 V, 25.0 mV step, default on, 1.80 V)

3) Block Diagram



2.3 IF PMIC : SM5714

1) General Description

The SM5714 is a highly-integrated interface power management IC that integrates Type-C and non MCUbased PD, 3:1 USB switches, a max. 3.5 A switch-mode charger with Adaptive Fast Charge (AFC), QC2.0, nechannel source-type flash LED driver and a very accurate fuel gauge for handheld applications. The device features Type-C with non MCU based PD and advanced water detection scheme, 3:1 switches for managing switching signals multiplexing between an application processor, a communication processor and its accessory through a Type-C connector. The single-input switch-mode charger with a very low R_{DS_ON} resistance reduces thermal dissipation and allows the charger to operate in a stable switching operation, which results in a shorter charging time. The function of the VBUS supply voltage limit, also called AICL, is able to make the most of the maximum power from a Travel Adapter (TA). The high-side flash driver features an easy PCB layout, and the built-in sophisticated algorithm for the fuel gauge measures the State-Of-Charge (SOC) of the 1-cell battery. The SM5714 is available in 3.72 mm x 3.72 mm, 81-Bump WLCSP package.

2) Key Features

☐ Type-C with Non MCU-based PD and Water Detection

- Super Speed Polarity Indicator

☐ 3:1 MUX Switches with Built-in BC1.2 Scheme and TA Hiccup control

☐ Max. 3.5 A Switch-Mode Charger with Dual-output and Embedded AFC and QC2.0 Protocol

☐ Programmable Charge Parameters via I^2C

- Fast-Charge Current
- Top-Off (end of charge)
- Battery Floating (regulation) Voltage
- Trickle-Charge Current
- Adaptive-Input Current Limit (AICL)
- VBUS Input Current Limit

☐ Fuel Gauge with Flexibility in Current Sensing Resistor

- External High-Side Current Sensing
- 5 mΩ or 2 mΩ Selectable Sensing Resistor

☐ A nVBUSPOK pin for Touch Sensor

☐ 1.5 A Flash LED Driver

☐ Protections

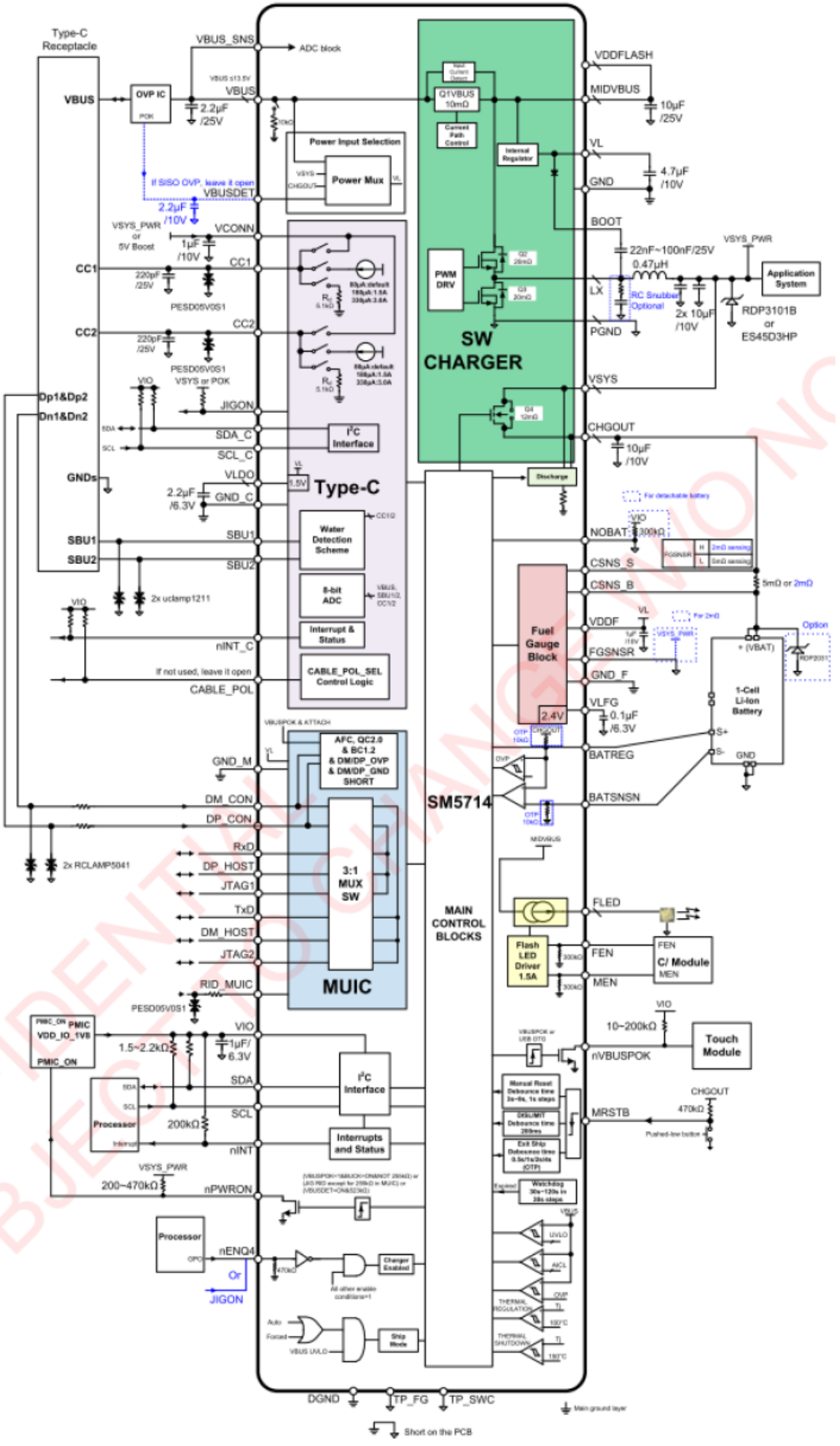
- Thermal Protection
- Thermal Regulation
- VBUS Overvoltage Protection
- Battery Overvoltage Protection
- VSYS OVP
- Discharge Overcurrent Protection
- Charger Safety Timers
- Reverse Leakage Blocking
- Charger = Off (or PWM = OFF) in DP / DM OVP
- CC1, CC2 Overvoltage Protection
- SBU1, SBU2 Overvoltage Protection
- Water Detection with 8-bit ADC
- DP_CON / DM_CON Short Detection

☐ Ship Mode to Minimize Leakage Current during System OFF

☐ Up to 400kHz Full-Speed I^2C Interface

☐ 81-Bump, 3.72 mm x 3.72 mm WLCSP Package

3) Block Diagram



2.4 MEMORY : KM2L9001CM-B518

1) General Description

The KM2L9001CM is a Multi Chip Package Memory which combines 128GB UFS and 48Gb(16Gb*3) TDP LPDDR4X SDRAM.

UFS (Universal Flash Storage) is an embedded Flash storage for mobile systems which consists of NAND Flash and Flash controller. UFS has a high speed serial interface which supports up to HS-GEAR3 with 2lane. UFS basically supports Flash-friendly eMMC features such as partitions for boot and RPMB, security of write protect and Purge, several Flash managements like background operation, power off notification. Also, UFS has SSD-like command queue feature which is based on SCSI architecture model to enhance responsiveness for better user experience. Samsung UFS is based on industry-leading specifications from MIPI Alliance to support high performance and is optimized with Samsung's cutting edge NAND Flash memory technology.

LPDDR4X-SDRAM is a high-speed synchronous DRAM device internally configured with 2 channels. Dual channel is comprised of 8-banks with from 2Gb to 16Gb per channel density. The configuration for channel density that is greater than 16Gb is still TBD1).

This device contains the following number of bits:
Dual-channel SDRAM devices contain the following number of bits:
16Gb has 17,179,869,184 bits

LPDDR4X devices use a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. See command truth table for details. These devices use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4X SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR4X SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read, Write or Mask Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the Bank and the starting column location for the burst access.Prior to normal operation, the LPDDR4X SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

The KM2L9001CM suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 254-ball FBGA Type.

2) Block Diagram

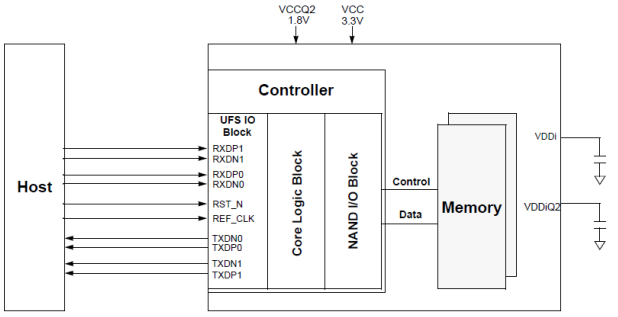
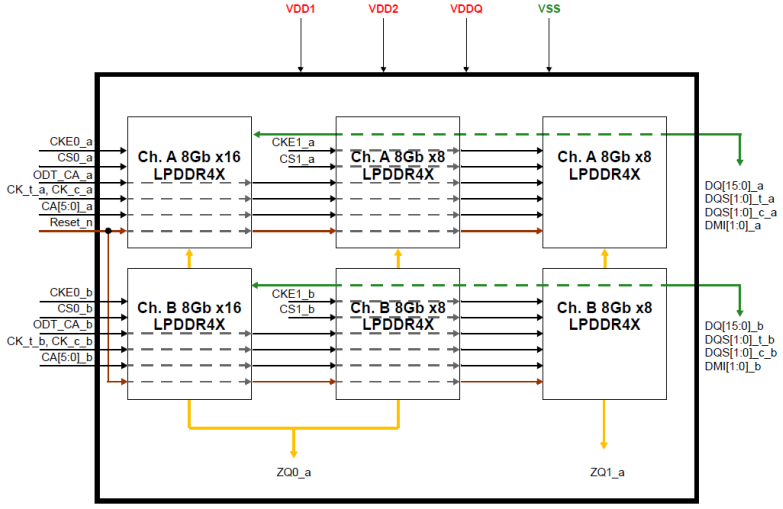


Figure 1. UFS Device Block Diagram



Time Average SAR Algorithm Description

1 Introduction of SAR/PD compliance test with TAS algorithm

FCC RF exposure limits are comprised of SAR (Specific Absorption Rate) and PD (Power Density) limits depending on frequency of operation. Both SAR and PD regulatory specifications are defined over certain measurement duration allowing for time-averaging. The Samsung S.LSI proprietary TAS (Time Average SAR) algorithm has been designed to meet the compliance limits over the required duration, while still allowing dynamic control of transmit power for meeting system performance.

The device under the test (DUT) with S.LSI chipset will contain the following RATs (radio access technologies):

- mmWave module supporting 5G FR2 NR
- RFIC and modem supporting 2G/3G/4G/FR1 NR technologies
- Operation of Wi-Fi and BT

This document consists of TAS algorithm description, algorithm parameters, validation methodology, test cases, test procedures and test results. In order to demonstrate that TAS algorithm meets FCC requirements for SAR/PD exposure, we can define multiple steps as summarized below.

1. SAR/PD baseline characterization data using non-signaling tests
2. Signaling test case definition and associated SAR compliance evaluation methodology
3. Test results and analysis to explain SAR compliant behavior

2 TAS algorithm description

2.1 High-level algorithm concept

The RF exposure limit is defined based on time-average exposure during a certain amount of time window. Basically, the length of time window is adjustable in current TAS algorithm implementation. As representative values, following time window sizes are introduced in the report. Time window size 100 seconds, 60 seconds and 4 seconds are used for SAR (below 3GHz), SAR (3~6GHz) and PD (Above 6GHz) respectively in this evaluation report aligning with the FCC requirement. TAS algorithm ensures the DUT can meet the FCC compliance at all times over test duration. As we will establish via lab characterization, both SAR and PD are directly proportional to terminal Tx(transmitter) power, so TAS algorithm scales transmitter power level dynamically to meet compliance.

Samsung S.LSI proprietary TAS algorithm considers 4G and 5G NR cellular RAT, and connectivity technologies such as Wi-Fi and BT (Bluetooth) because the DUT should keep the total amount of radiation below the level defined by regulations. To do this, modem controls transmitter power in real time. Because FR2 systems can have different PD impacts depending on beam index and module selection, operation scenarios that change those are considered as well.

At a very high level, the TAS algorithm consists of the following:

- Maximum Tx power limit for a particular RAT is calculated considering SAR/PD compliance using some pre-characterization data.
- Instantaneous Tx power can go over Tx power limit but average value during any measurement

window will be maintained below the Tx power limit. This operation is depicted in Figure 2.1-1.

- In a simultaneous multi-RAT scenario, TAS algorithm also has to meet TER (Total Exposure Ratio), which is sum of actual SAR/PD to the compliance limits across all RATs. TER of the DUT will be equal to or less than 1 at all time.
- To preserve the radio link quality and call connection, TAS algorithm provides the concept of priority of each RAT's transmit power. For instance, a certain minimum value of max transmit power limit will be ensured for anchor RAT such as LTE in EN-DC.

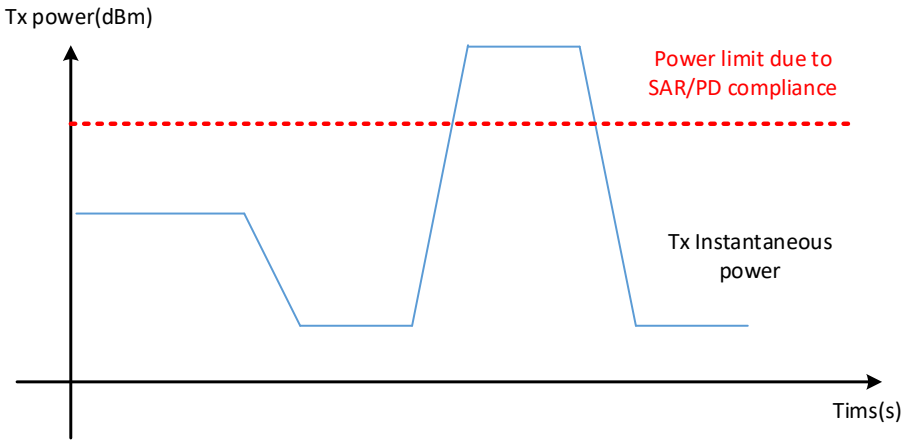


Figure 2.1-1 TAS algorithm concept

2.2 Algorithm operation and configurable parameters for each RAT

Samsung S.LSI proprietary TAS algorithm operates as follows.

- Define the minimum duration of SAR/PD calculation. This duration is the 'SAR/PD average window' consists of N slots. Any measurement duration or time-averaging duration as specified by FCC for the particular RAT will then consist of M such windows. The product of FCC limit of SAR/PD limit (or equivalently the Tx power for this limit as used in the algorithm) and M is then defined as a SAR budget for such measurement durations.
- For a particular window, calculate the amount of average SAR consumed during the window duration by computing average of instantaneous transmit power value per slot. Because SAR value isn't given directly, Tx power value is used to calculate consumed SAR value.
- Estimates the total SAR consumed during the SAR/PD measurement duration in the past which includes the above window. This value will be the sum of SAR/PD consumed by all windows in the measurement duration.
- Monitor the remaining SAR budget continuously for every window and control the maximum Tx power for the next window to comply with SAR/PD regulation

Below figure illustrates the detailed operation of the TAS algorithm. Please keep in mind the unit of TAS/PD

evaluation is average power (unit: Watt) during the measurement duration. Then total SAR budget can be defined as required average SAR * measurement duration to comply with FCC requirements. So, 'SAR Budget' is defined as an integrated SAR value during measurement duration. To monitor the risk of test failure with fine granularity, the measurement duration is divided into fine sub-time blocks called 'window's, and a maximum power limit is imposed for each window. TAS algorithm updates consumed SAR in the current window and remaining budget exploiting moving average window concept. As mentioned above, we don't know SAR value directly, so Tx power is used for calculation. Whenever N slots have passed, TAS algorithm discards a past window and adds a new window to update SAR status. From the result, TAS algorithm calculates permissible max Tx power (Tx MaxPower) for next window to meet SAR compliance test. By ensuring that the DUT does not transmit higher power than this max Tx power, we are guaranteed that the consumed SAR/PD for any measurement duration will not exceed the SAR/PD budget. Because slot (TTI) is very short time interval and fine enough granularity, DUT can handle various events and respond promptly. The reason why N is defined is for flexibility of implementation. If N=1, budget will be updated every slot. It can reflect Tx power change promptly, but too frequent updates can increase CPU software processing burden when TAS algorithm is implemented in modem software.

In this implementation, the length of each window needs to be small enough to respond promptly to various event scenarios. For instance, allowed SAR consumption limit may need to be adjusted by events. Hence proper value of window size is applied for each RAT to comply with this requirement.

By considering remaining SAR budget, maximum SAR for next window is determined. It could be larger or smaller than SAR_design_target as instant power. Figure 2.2-1 shows the overall concept of TAS measurement duration and window. In each consumed SAR is saved in each window, and window size is fixed in same RAT. If RAT is changed the window size could be changed.

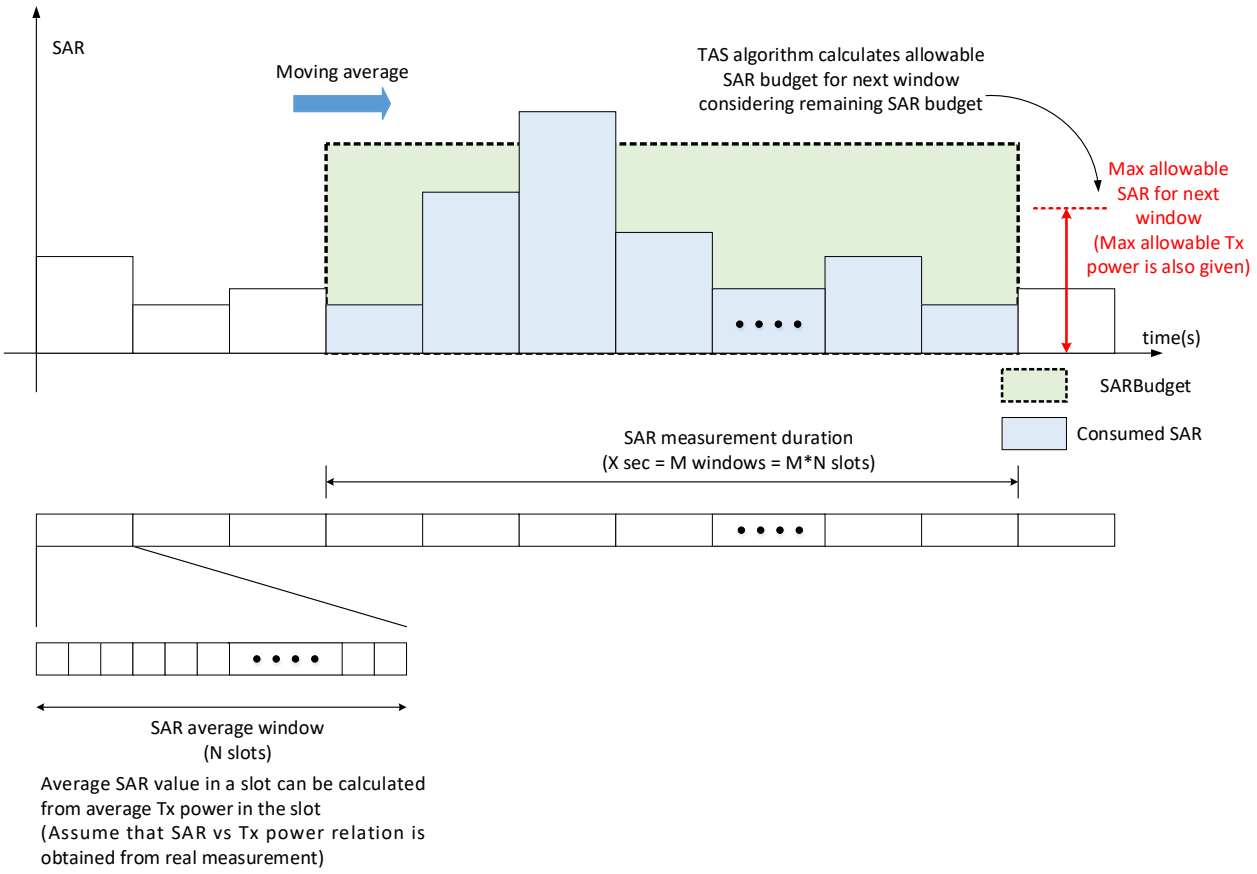


Figure 2.2-1 SAR measurement from Tx power using block-wise processing

LTE/FR1 and legacy transmitter should follow SAR requirements for sub6GHz. On the other hands, FR2 transmitter has to follow MPE (Maximum Permissible Exposure) requirements or PD limit. But EN-DC and other various cases should be supported in real usage as well as other NR combinations. For these cases, total exposure ratio (TER) criteria is defined as follows.

- For sub-6 transmissions only:

$$\sum_{l_{SAR}=0}^{L_{SAR}-1} \frac{SAR_{avr,l_{SAR}}}{FCC\ \ SAR_{limit}} \leq 1 \tag{2.2.1}$$

- For both sub-6 and mmWave transmission:

$$\sum_{l_{SAR}=0}^{L_{SAR}-1} \frac{SAR_{avr,l_{SAR}}}{FCC\ \ SAR_{limit}} + \sum_{l_{PD}=0}^{L_{PD}-1} \frac{PD_{avr,l_{PD}}}{FCC\ \ PD_{limit}} \leq 1 \tag{2.2.2}$$

where SAR represents sub6GHz average power, PD stands for power density of MPE regulation, L_{SAR} is the number of fixed, mobile or portable RF sources using SAR-based formula and L_{PD} is the number of fixed, mobile or portable RF sources using PD (MPE)-based formula. Please keep in mind that each carrier can be regarded as a transmitter.

Considering a whole platform terminal, Wi-Fi and BT should be counted in as well. Real time information sharing between a cellular CP (Communication Processor) and Wi-Fi/BT processor isn't feasible due to

communication interface delay in most cases. More proper way is assigning normalized SAR budget to Wi-Fi and BT if they are on the enabled state. The AP (Application Processor) can let modem software know if Wi-Fi or BT transmission is enabled or not. Then the equation above is given like follows.

- For sub-6 transmissions only:

$$\sum_{l_{SAR}=0}^{L_{SAR}-1} \frac{SAR_{avr,l_{SAR}}}{FCC\ \ SAR_{limit}} \leq 1 - SAR_{WiFi,Norm} - SAR_{BT,Norm} \quad (2.2.3)$$

- For sub-6 mmWave transmission:

$$\sum_{l_{SAR}=0}^{L_{SAR}-1} \frac{SAR_{avr,l_{SAR}}}{FCC\ \ SAR_{limit}} + \sum_{l_{PD}=0}^{L_{PD}-1} \frac{PD_{avr,l_{PD}}}{FCC\ \ PD_{limit}} \leq 1 - SAR_{WiFi,Norm} - SAR_{BT,Norm} \quad (2.2.4)$$

$SAR_{WiFi,Norm}$ is the normalized SAR value of Wi-Fi and $SAR_{BT,Norm}$ is the normalized SAR value of BT and these can be figured out by lab characterization tests at highest allowed powers for Wi-Fi/BT. (These values are zero if the transmitter of these technologies are disabled) We can keep the simple TER criteria considering all components in a platform in this way.

To measure TER, measure method of SAR and PD should be defined. Most important parameter is the required average time. The average time for SAR measurement for FCC is 60 or 100 seconds depends on carrier frequency (whether higher or lower than 3GHz, respectively). On the other hands, 4 seconds can be considered for PD measurement average duration. The value of measurement duration in the algorithm can be flexibly adjusted based on the actual requirement of SAR/PD compliance even if they are changed later. In legacy and FR1 cases, measured time for one window is considered as 500ms. There are N slots in one window, and all power used in each slot is averaged and stored in one window.

2.3 The concept of time average SAR/PD algorithm

Section 2.2 presented the important concept of TAS algorithm. This section describes the concept of algorithm. This algorithm is applied both for sub6GHz SAR and above 6GHz PD control.

SAR/PD values are accumulated for every slot in one measurement window. At the end of every window measurement time, TAS algorithm check the amount of current remaining SAR/PD. If remaining SAR/PD is enough, use maximum power by considering the remaining SAR/PD. If remaining SAR/PD is not enough, algorithm goes to restore stage. In restore stage, there are several ways to saving SAR/PD budget. Through this stage, SAR/PD budget would be increased. After then, if remaining SAR/PD is still not enough, the algorithm would enter restore stage again. If enough, the algorithm would use maximum power.

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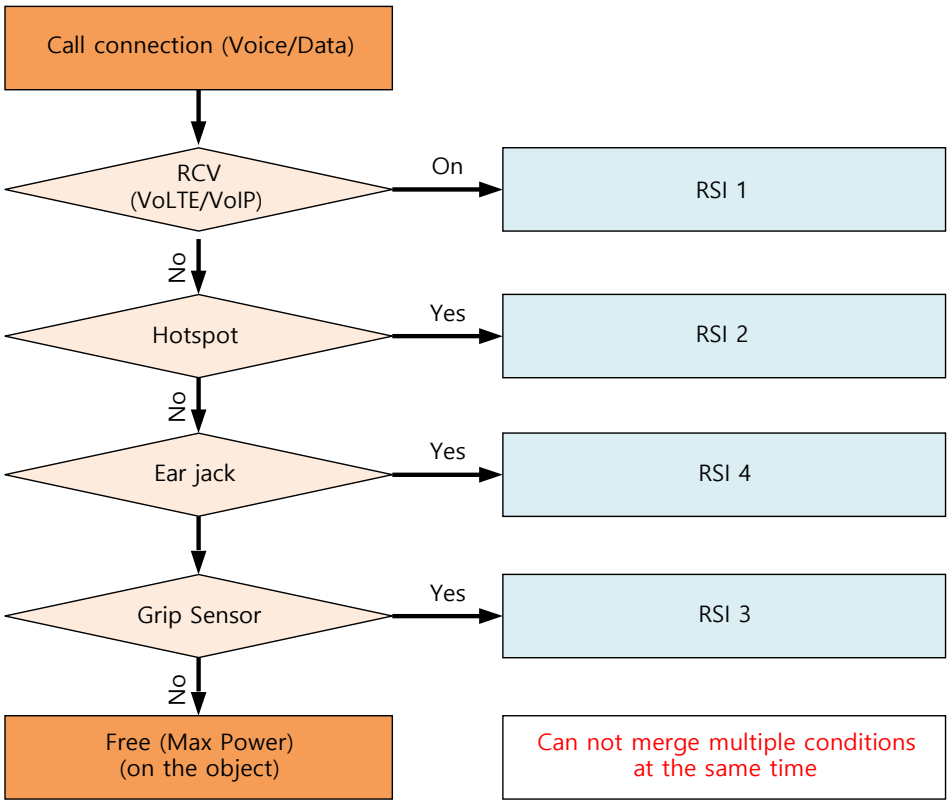
FCC Documentation for RSI

RSI Configuration

This device configures RSI for the time-averaging implementation for standalone and for TER (Total Exposure Ratio)compliance. The CP decides the maximum output power based on the RSI from the audio receiver state, capacitive sensor circuit, the hotspot activation state through the UI and the state of the headphonejack.

It is first determined if it's in a voice or VoIP call using the audio receiver. When it is activated, the power is always configured to the output power levels specified as RSI 1.
If audio receiver is not activated, it will be determined if the user has activated Hotspot through the UI. When it is activated, the power is always configured to the output power levels specified as RSI 2. If hotspot is not activated,it will be determined if the earjack is being used. If earjack/headphones are inserted, the power will configured to thesettings in RSI 4. Then, it will be determined if the grip sensor is activated. If the capacitive grip sensor is activated (for example, when the device is being used in the hand), the output power is configured to the parameters of RSI 3.



SAMSUNG ELECTRONICS

FCC Documentation for RSI

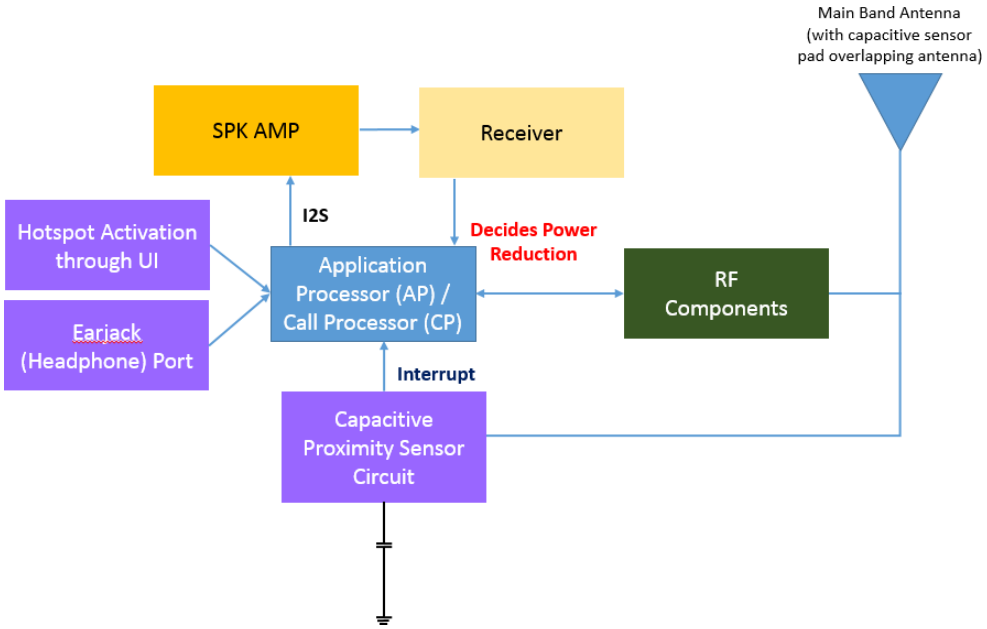


Figure 2
Power Reduction Block Diagram

Hotspot Triggering Mechanism

The Wireless Hotspot feature available in the device allows the end-user to tether the data connection from the device over Wi-Fi. This is a standard feature of the OS. Upon the activation of this feature by the end-user, instructions are sent to not only activate the Hotspot services for the end-user but the instructions also notify the CP that the hotspot state has been activated. For wireless modes that can operate simultaneously with voice/data sharing a single channel, when a voice call comes in hotspot mode stays enabled. There is no change in the allowed maximum output power and it will stay configured to the appropriate RSI until it is deactivated. For wireless modes that cannot support simultaneous voice/data operations, when a voice call is received and hotspot mode is ON, hotspot mode is disabledautomatically by the device's SW. When the call ends, the user must reactivate hotspot manually to continue using the hotspot services (the device does not automatically return to hotspot mode).

Capacitive Sensor Triggering Mechanism

Additionally, the power level of EUT is configured by the sensor (Capacitive Proximity sensor). When capacitive proximity sensor is active in the hand, the power level of EUT is configured by activation of the capacitive proximity sensor by the CP.

Below is the operation description of the capacitive proximity sensor activation. The capacitive proximity sensor is the same metallic component as the main antenna (not spatially offset). If an object close to the antenna (i.e. capacitiveproximity sensor) and distance is below the threshold distance, the capacitive proximity sensor chipset is aware of a change of capacitance. From there, the capacitive proximity sensor chipset reports to the CP that the capacitive sensor state is active.

FCC Documentation for RSI

In the first case of normal, if the antenna is active without the capacitive sensor activation, the capacitive proximity sensor does not generate sensing frequency, at that time interrupt signal doesn't occur (See Figure 2). But, if an object (ex. human hand) approaches to the capacitive sensor (capacitive sensor is activated), the capacitive proximity sensorgenerates sensing frequency and interrupt signal is occurred. At that time, the CP recognizes the interrupt signal (capacitive sensor is active) and the CP configures the RSI.

In the rare case of capacitive sensor failure, although the object is in the range of sensing distance of the capacitive sensor, the capacitive sensor doesn't work. Then CP cannot recognize a change of voltage (1.8V -> 0V), the interrupt signal of capacitive proximity sensor. However, the capacitive proximity sensor periodically checks (every 200ms) thedifference of capacitance between reference capacitance and input capacitance that in order to determine the normal or abnormal operations of capacitive sensor. Therefore, if there is a difference in capacitance between input capacitance and reference capacitance, interrupt occurs and CP recognizes the interrupt signal. Additionally, if there is no response from the capacitive proximity sensor (High: 1.8V or Low: 0V), CP will forcibly configure the RSI. In either of these cases, the CP forcibly configures the proximity sensor state as active.

Earjack/Headphone Triggering Mechanism

This device has a USB Type-C earjack which allows the user to insert headphones. Upon insertion of the headphones, instructions are sent to direct audio through the earjack port to notify the AP/CP that the earjack is active. Then, the AP/CP reduces the maximum allowed power until the headphones are removed.

Receiver Mechanism

A RSI is configured when the device is called when the earpiece is active while in a held-to-ear voice/ VOIP call and the active audio receiver. Therefore, when earpiece is active in a held-to-ear user scenario, the output power level is configured to a specific RSI. The maximum allowed output powers in all conditions are included in the maximum power document.

The Application Processor (AP) coordinates logic components (sensors, cameras, audio, etc) of the device. The AP controls the audio components of the device through the audio codec. When a call is placed or received, the AP sends the audio output through the earpiece. When the audio earpiece is activated, the AP uses pre-programmed instructions to configure the RSI. The output power stays reduced until the audio through the earpiece is disabled, for example, when the user ends the call or uses Bluetooth. Figure 2 shows an operational block diagram of the power reduction mechanism. The speaker amplifier is connected to the AP with I^2S lines. If Speaker Amplifier is enabled by AP, Speaker amplifier controls earpiece during held-to-ear voice/VOIP call. At that time, AP sends pre- programmed basic instructions, like providing feedback to the RF block to configure the RSI for head condition

SAMSUNG ELECTRONICS

FCC Documentation for RSI

Hotspot, Ear jack, Grip (Capacitive) Sensor, and Receiver Power Reduction – SAR Test Configuration

Receiver Active?	Hotspot State	Earjack/ Headphones Inserted	Capacitive Grip Sensor State	RSI State	Proposed SAR Test Configurations for the SAR Report
On	On/Off	On/Off	On/Off	RSI 1	Head SAR
Off	On	On/Off	On/Off	RSI 2	Hotspot (10mm)
Off	Off	On	On/Off	RSI 4	Body-Worn Accessories (15mm) with Headphones[3]
Off	Off	Off	On	RSI 3	Hand SAR (0mm)[1]
Off	Off	Off	Off	RSI 0	Body-worn Accessory (15mm)[2] Hand SAR (Triggering Dist. -1mm)[1]

1 - For device sides/edges that utilize a proximity sensor. Sides/Edges that do not trigger the proximity sensor will be evaluated at 0mm at maximum output power. Triggering distances and configurations will be evaluated per the procedures in FCC KDB 616217

2 – Body-worn accessory tested at maximum power without headphones inserted per FCC KDB 648474

3 – If required per FCC KDB 648474 Procedures

Note: The output powers when Hotspot is active (RSI 2) will always be the same or less than the output powers when only the earjack or grip sensor is active (RSI 4 and RSI 3). For this device, the Plimit implemented for RSI 4 and RSI 3 are the same. Additionally, for this device, the Plimit values for RSI 2 are greater than the Pmax values. Therefore, head SAR was evaluated at Pmax.

FCC Documentation for Power Class2 and Class3 operations

NR n77 Power Class 2 and Power Class 3 operations

1. HPUE (High Power User Equipment) Overview

For NR n77, UE Power Class 3 is defined as having a maximum output power of 23 dBm ± 2 dB and UE Power Class 2 is defined as having a maximum output power of 26 dBm ± 2 dB, as defined in 3GPP TS 36.101 and 38.101. This device is capable of operating as a UE Power Class 2 or UE Power Class 3 device for NR n77, as determined by network signaling. The specific output powers and tolerances implemented in this device can be found in the tune-up.

i. Power Class 2 (PC2) is applicable only if all of the following conditions prevail
   A. NR n77
   B. In all other bands/networks, UE needs to operate as Class 3 UEs; that is, FDD, TDD UL/DL FC 0/6 or non-n77
   C. UE Power Class 2 support is communicated as part of RRC signaling (that is, ue-PowerClass-N-r13 in UE-EUTRA-Capability)
   D. UE will support RF requirements for HPUE feature per TS 36.101 and TS 38.101

ii. UE behavior

i. Cell reselection
   A. UE assumes tdd-config is the same if NeighCellConfig = either 00, 01 or 10 in SIB5
   B. PC2 (e.g. 26 dBm) is used in computing Srxlev on target cell if serving cell allows for PC2

ii. RRC_CONNECTED mode
   A. Power Headroom Report (PHR) computation
   B. UE computes PHR based on PC2 (e.g. 26 dBm) when PC2 is used.
      In all other cases, PC3 is used.
   C. Mid-call mobility cases when power class changes
   D. Handover (e.g., FDD ←→ TDD)
   E. RLF(Radio Link Failure) → Connection Re-establishment on NR n77

iii. MPR/ A-MPR
   A. UE supports MPR/A-MPR tables for Power Class 2 and Power Class 3 based on PC2 and PC3 usage respectively

iv. PowerClassSignaling - ue-PowerClass for NR n77
   A. If PC2 is enabled in specified MCCs (that is, this IE is sent as part of UE-EUTRA-Capability in specified networks)

NR Checklist

NR FR1 Operational Information	
Form Factor	Portable Handset
Frequency Range of each NR transmission band	NR Band n2 (PCS) (1850 MHz - 1910 MHz)
	NR Band n5 (824 MHz - 849 MHz)
	NR Band n66 (1710 MHz - 1780MHz)
	NR Band n77(3450-3550, 3700 - 3980MHz)
Channel Bandwidths (MHz)	NR Band n2 (PCS): 5/10/15/20 MHz
	NR Band n5 : 5/10/15/20 MHz
	NR Band n66 : 5/10/15/20 MHz
	NR Band n77(C-Band): 10/15/20/25/30/40/50/60/70/80/90/100 MHz
Subcarrier Spacing (kHz)	NR Band n2, n5, n66 : 15 kHz
	n77: 30 kHz
Total Number of Supported CCs(SISO)	NR Bands limited to 1CC
Total Number of Support 터 CCs(MIMD)	UL MIMO not supported
Modulations Supported in UL	CP-OFDM: QPSK, 16QAM, 64QAM, 256QAM, DFT-s-OFDM: π/2-BPSK(UL Only), QPSK, 16QAM, 64QAM, 256QAM
LTE Anchor Bands for NR Band n2 (PCS)	LTE Band 2/5/13/48/66
LTE Anchor Bands for NR Band n5 (Cell)	LTE Band 2/5/48/66
LTE Anchor Bands for NR Band n66 (AWS)	LTE Band2/5/13/48/66
LTE Anchor Bands for NR Band n77	LTE Band 2/5/7/13/48/66

NR Checklist

NR FR2 Operational Information	
Form Factor	Portable Handset
Frequency Range of each NR transmission band	NR Band n261
	NR Band n260
Channel Bandwidths (MHz)	NR Band n261: 50MHz, 100MHz
	NR Band n260: 50MHz, 100MHz
Subcarrier Spacing (kHz)	120
Total Number of Supported UL CCs (SISO)	2 (DFT-s-OFDM, CP-OFDM)
Total Number of Supported UL CCs (Tx Diversity)	2 (DFT-s-OFDM, CP-OFDM)
Total Number of Supported UL CCs (MIMO)	2 (CP-OFDM Only)
Modulations Supported in UL	DFT-s OFDM: π/2-BPSK, QPSK, 16QAM, 64QAM CP OFDM: QPSK, 16QAM, 64QAM
LTE Anchor Bands (n260)	LTE Band 2/5/13/48/66
LTE Anchor Bands (n261)	LTE Band 2/5/13/48/66
Duplex Type (mmWave)	TDD

FCC Documentation for MCC based A-MPR Power Reduction Mechanism

MCC based A-MPR Power Reduction operations

3GPP standards allow for certain bands to apply Additional Maximum Power Reduction (A-MPR) based on Network Signaling (NS). A-MPR is implemented commonly to address design challenges with components such as power amps, filters, basebands, etc and also for standardized power reduction across devices.

System LSI has designed an algorithm that forces the use of A-MPR for certain MCC codes. The device is programmed with the country codes and bands that will apply A-MPR independent of network signaling. When the device attaches to the network, the device reads the MCC. If the device is operating with the subject band and MCC, the A-MPR setting will be used, regardless of NS setting from the base station. This algorithm is permanently implemented and cannot be changed by any end-user or third party.

1. Feature to Force A-MPR Use per Country

- ✓ Device manufacturers program MCC codes where A-MPR is mandatory, regardless of the LTE network's signaled NS value
- ✓ Feature can be validated through RF testing
- ✓ The goal is to enable a mechanism on the UE to comply with FCC regulation in the US

2. Operational Description

- ✓ To handle the scenario more efficiently, System LSI has made changes to the LTE software
- ✓ LTE Radio Resource Control (RRC) obtains MCC/ band specific NS_NON_CA and NS_CA values from the A-MPR Tune List file and stores the same.
- ✓ Before UE camps on a band present in A-MPR Tune List, if SIB1 PLMN MCC matches with the one in A-MPR Tune List, LTE RRC queries RF for all supported NS values for that band. If RF supports the NS value in A-MPR Tune List, then apply the same. If not, apply the network signaled value.
- ✓ To summarize, device manufactures must configure their devices with the following parameters, for this feature to work:
  1) Country codes that force A-MPR regardless of NS
  2) Bands impacted
  3) A-MPR values applied (default values are based on 3GPP 36.101)

3. Implementation in this device

- ✓ This A-MPR MCC Based mechanism only applies to LTE ULCA 48C operations when the device is operating with Power Class 3
- ✓ A-MPR is implemented per the CA_NS_10 Settings in 3GPP 36.101 Table 6.2.4A.10-1
- ✓ This mechanism applies for all US based MCC that operate with Power Class 3: 310~316

FCC Documentation for Uplink Carrier Aggregation operations

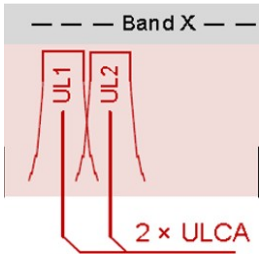
Uplink Carrier Aggregation Implementation and Limitation

1. Implementation in this device

- ✓ This device supports Uplink Carrier Aggregation for LTE 48C.
- ✓ Uplink Carrier Aggregation is limited to two intra-band contiguous carriers on the uplink with the maximum aggregate bandwidth defined by each CA Bandwidth class.
- ✓ The total aggregate power measured across both component carrier will never exceed the single carrier scenario.

2. Intra-band CA – the two or more carriers are in the same band

- ✓ Contiguous – carriers are adjacent to each other



PCC and SCC UL TX power is not balance always in real network conditions, there are complex algorithm and specification definition to describe the PCC and SCC behavior. Simply saying, PCC and SCC TX power could be balance if there is no PDCCH. Therefore, when the device is configured so that PCC and SCC DL RB number is 0, the PCC and SCC UL Tx Power is balanced for max power test scenarios.

3. UL timing advance

- ✓ PCC and SCC are time-synchronized, therefore, a single timing advance command is needed for both.

4. UL power control

- ✓ UL power (Maximum power per Power Class) cannot exceed the aggregated power of PCC and SCC. The maximum power can be found in the tune-up procedure.
- ✓ UL power control works independently for each PCC and SCC. However, the aggregated power across both carriers will never exceed the value in the tune-up.
- ✓ Power level of each CC is defined by bandwidth, number of RB and RB allocations since these configurations set different MPR.
- ✓ TPC (Transmit Power Control) commands are applied to a CC granted by base station.
- ✓ Path loss estimates are individually on the CCs.
- ✓ Each PCC and SCC power is controlled and correlated by modem using transmit power feedback algorithm.

FCC Documentation for 4x4 Downlink MIMO

(for USA Only)

4x4 Downlink MIMO operation

– LTE B2/4/48/66, NR n2/n66/n77

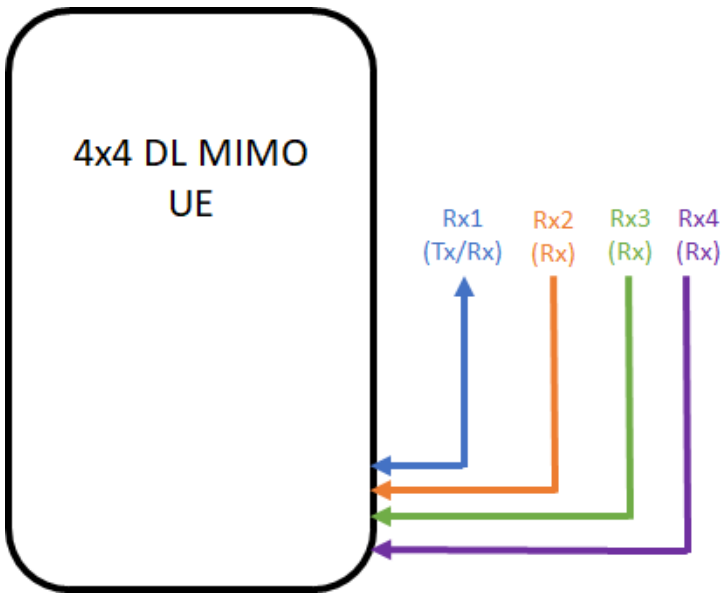
1. 4x4 MIMO Overview

- ✓ Definition
  - ■ Four separate, simultaneous data streams flowing from a base station to four receiving antennas on a device

2. Implementation in this device

- ✓ Supports up to 4 DLCA up to 80MHz across five bands
- ✓ Implements up to five interband downlink Rx carrier aggregation including LAA(LTE Band 46) DL
- ✓ Support interband 3CC 4×4 MIMO and 1CC 2x2 MIMO
- ✓ Capability of five 4-way HO-RxD concurrently

3. 4×4 MIMO Conceptual Diagram



4x4 Downlink MIMO Conceptual Diagram

FCC Operational Description for SRS Operations

FCC ID: A3LSMA536V
Models: SM-A536V

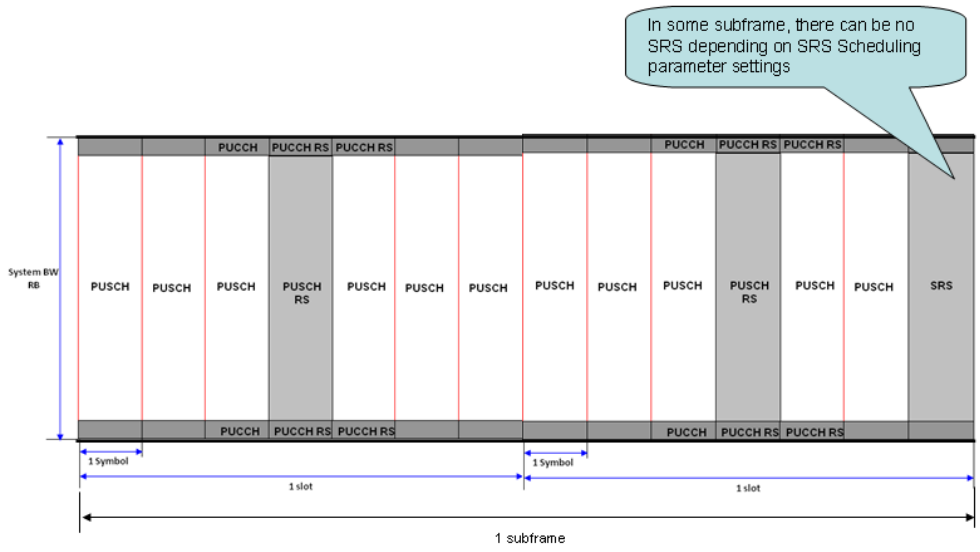
SRS (Sounding Reference Signal) Operational Description

SRS stands for Sounding Reference Signal. The purpose is antenna switching for Downlink (Rx) CSI (channel status information) acquisition to enhance Downlink (Rx) MIMO allocation and improve Rx performance. This device supports SRS operations for n77 operations only.

It is a reference signal for eNodeB to figure out the best channel quality. It is transmitted by the UE at the end of some subframes.

For NR, eNodeB often allocates only a partial section of full system bandwidth for a specific UE and at a specific time. The motivation for the SRS is so that the section with the best channel quality across the overall bandwidth can be determined. Once known, the network can allocate the specific frequency region which is the best for each of the UEs.

For this device, SRS can transmit when the device is in NSA or SA mode.



FCC Operational Description for SRS Operations

Duty Cycle Information

The frequency of the SRS signal is determined by the configuration set by the signaling message (SIB2, RRC Connection Setup, RRC Connection Reconfiguration etc) from the eNodeB. The range of intervals are such that the UE can transmit SRS every two subframes at the most and every 32 frame (320 subframe) at the least. The 10 bit signaling parameter srs-ConfigIndex tells UE of the periodicity of SRS transmission and the period can be 2,5,10,20,40,80,160,320 ms. Additionally, the eNodeB can be configured such that there is no SRS signal sent from the UE.

SRS is transmitted at the last symbol of UL slot with full system band area and it is transmitted by a certain interval.

Calculations for n77, SCS= 30 kHz Duty Cycle
SRS can theoretically be transmitted maximum 1 time per 0.5ms slot. (varying by network configuration.)

1 frame = 10 subframe = 20 slots = 10ms; 1 subframe = 2 slots = 1ms; 1 slot = 14 symbols = 0.5ms

SRS can be up to 4 symbols out of 14, per 0.5ms slot.

Tx Duration in 1 slot = 4/14 * 0.5ms = 0.143ms.

Therefore, max theoretical Duty cycle of SRS is 28.6%.

Output Power

Target powers are same or lower than current tune-up levels for n77. Tune-up procedure includes target powers for each antenna for n77. Additionally, the SRS tx operations can't exceed time-averaged power level that is controlled by Smart Transmit.

Antennas Operations

The device has 1 Tx antenna for n77 data (Ant H) and 3 Rx antennas (Ant E, K, D). With SRS operations, all 4 antennas can transmit the SRS signal to check for the channel quality of n77. The antennas cannot simultaneously transmit. Only the single TX/RX antenna is used for Data transmission.

Beamforming – n261

The mmWave operations in this device use beam-forming. The below beams are used in this device (no other beams or combinations of beams are supported.)

	Patch/Dipole	SISO/MIMO & Polarization	Beam ID	
ANT L	Patch	Single beam / V-pole	0	
			1	
			2	
			3	
			4	
			5	
			6	
		Single beam / H-pole		7
				8
				9
				10
				11
				12
				13
		Paired beam / MIMO	0	7
			1	8
			2	9
			3	10
			4	11
			5	12
			6	13

Beamforming – n260

The mmWave operations in this device use beam-forming. The below beams are used in this device (no other beams or combinations of beams are supported.)

	Patch/Dipole	SISO/MIMO & Polarization	Beam ID	
ANT L	Patch	Single beam / V-pole	0	
			1	
			2	
			3	
			4	
			5	
			6	
		Single beam / H-pole		7
				8
				9
				10
				11
				12
				13
		Paired beam / MIMO	0	7
			1	8
			2	9
			3	10
			4	11
			5	12
			6	13

3.3. Beamforming

Device description

The Left (Ant-L) modules consists of 1x5 array structure with patch antenna. The total number of beams for both modules are shown in below table:

# of beams for each modules and polarizations

	Patch/Dipole	SISO/MIMO & Polarization	Beam ID	
ANT L	Patch	Single beam / V-pole	0	
			1	
			2	
			3	
			4	
			5	
			6	
		Single beam / H-pole		7
				8
				9
				10
				11
				12
				13
		Paired beam / MIMO	0	7
			1	8
			2	9
			3	10
			4	11
			5	12
			6	13

For the beams, the number of enabled antenna element is as follows: 1 element-enabled antenna, 1 element-enabled array antenna, and 5 element-enabled array antenna.

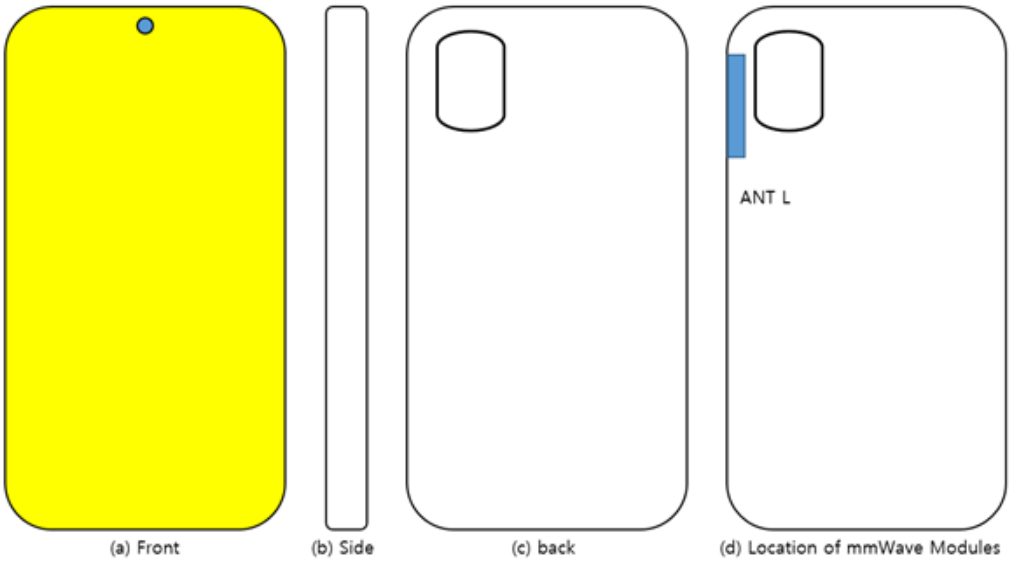
Key features

- Process: 28 nm CMOS
- Package: Wafer level chip scale package (WL-CSP)
- Control Protocol: PSpeedy or HSpeedy
- Two IF interfaces at ~9 GHz connecting to S5720
- Supports 5 TRx chains per IF (total 10) for low band, and 5 TRx chains per IF (total 10) for high band
- Supports N257/258/260/261 5G NR mm-wave bands
- Sliding IF up and down conversion architecture.

mmWave Array Antenna

■ Antenna Configuration

- 5 patches only, placed on the left side
  - Dimension: 23.8mm x 3.5mm x 2.14mm rectangular



- Patch antenna elements has feeds to excite vertically polarized and/or horizontally polarized.
- Only one array antenna active at a time
- Only one mmWave band at a time