Digital Imaging's integrated product development process

Abstract: *The evolution of Digital Imaging (DI) from research and development to a product-oriented organization required additional discipline and focus on business processes. The high-level business map was defined to flow information from the marketplace requirements into the final product delivered to the customer. One of the critical pieces of the process flow was the product development process–translation of market and customer requirements into physical form.*

The product development process needed to be a dynamic document that met the needs of the organization. It needed to tightly couple the market requirements with the final product and ensure alignment to DI's business strategies. A cross-functional team evaluated processes from inside and outside TI to limit the amount of effort the team would need to expend. The phase-gate process documented by DI covers product life cycle from concept to closeout in seven phases. The gates are business-focused reviews that evaluate progress, the project's value proposition and alignment with DI strategy. The latest improvement activity added details to the early phases, enabled use of Intranet access and increased consistency of product documentation and storage.

Digital Imaging (DI) began as a technology development program in 1992. The purpose was to find a use for the Digital Micromirror Device™ (DMD™) and develop demonstration products that would attract customers to DI. Since the products were not intended to go into production, little or no attention was paid to business process related to documenting requirements, verifying producibility or validating functionality. When it became evident that DI was a viable business in 1994, teams were established to define a business process model and a product development process.

DI's business process model

The business process team was not interested in "reinventing the wheel" and began searching for successful existing models applicable to DI's needs. TI's Semiconductor Group (SC) model provided the basic structure for a non-end item product driven by market requirements. The TI calculator model provided the concept of a multi-layered market element. The DI team integrated the two models and released the Digital Imaging business process model in October 1994.

As shown in *Figure 1*, business management and strategy development for DI's products are driven by the needs of the market. The primary market interface is coordinated through the original equipment manufacturer (OEM). Demand assumptions are generated on end-user needs. A product business model and work-share allocation between OEM and DI are established. Integrated product development efforts are coordinated to achieve full realization of market requirements and timely entry into the market. Sales and operations provide planning and support for product manufacturing and order fulfillment. To support product design and build, a materiel team establishes and manages supplier relationships and alliances. DI's core technologies, driven by product strategy, have both evolutionary and revolutionary paths. Technology development is intended to lead product development to lower the risk of new technology insertion into DI's products.

There are several enablers to this business model. Assessment of DI's product quality, reliability and product safety are provided by an independent Quality Reliability Assurance (QRA) organization. Staffing and training of all DIers is handled through division-based Human Resources (HR) services. Legal Support Services manage all intellectual property and contractual issues. Information technology provides computer and tool infrastructure support

Alice Parry, Bob Stoddard and Ron Barry

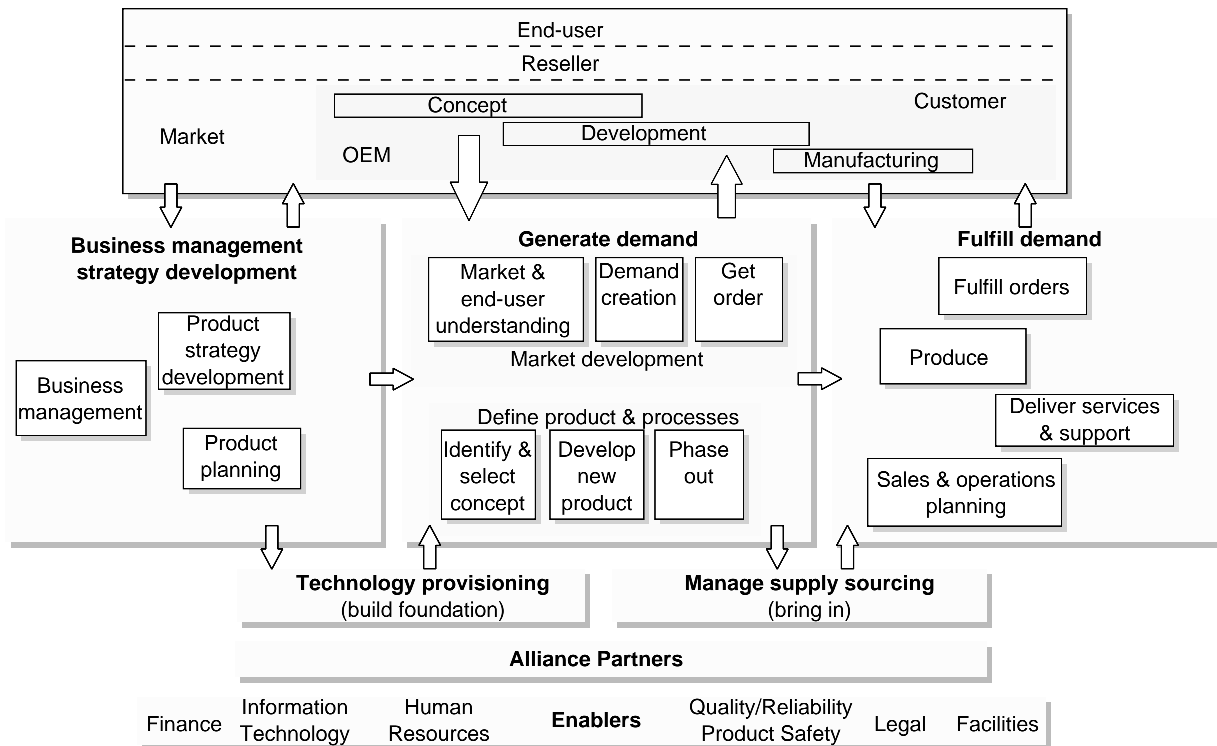

Figure 1. Digital Imaging's business process model.

and a networked environment to facilitate information sharing. Finance reports current status and forecasts upward into TI's corporate structure. It also provides support for financial risk assessments at the product level.

Key business objectives drive process

The business process model made it clear that the product development process must be driven by and aligned with DI business objectives. The product development team used the business model to clarify how development facilitated this flow and to help meet DI's business objectives. With this process the customer is the center of DI's focus.

Customer satisfaction is the primary focus for DI. Part of the satisfaction quotient includes product-related business objectives such as:

- Market driven product requirements
- Meeting customers' needs
- Meeting time-to-market targets
- Reducing product costs
- Reducing product development cycle time
- Improving product quality.

Figure 2 shows a general information flow between customers and various DI organizational and functional entities.

During the early phases of DI's product development process, Marketing is responsible for identifying customer careabouts and translating them into market requirements. Systems Engineering creates the product specification and design requirements from the market requirements. Target product costs and time-to-market requirements also are established by Marketing.

Proper market and systems analysis are critical to this process. Product Marketing's presence as an integral part of the product development team helps focus the development effort toward these objectives. The product development team, which includes manufacturing, tailors the process to meet the time-to-market window without sacrificing product quality. Product quality and reduction of product costs and cycle time are the responsibility of all functions including engineering, operations and QRA. Concurrent engineering during the requirements and design phases by engineering, manufacturing and customers, help to reduce the amount of rework nec-

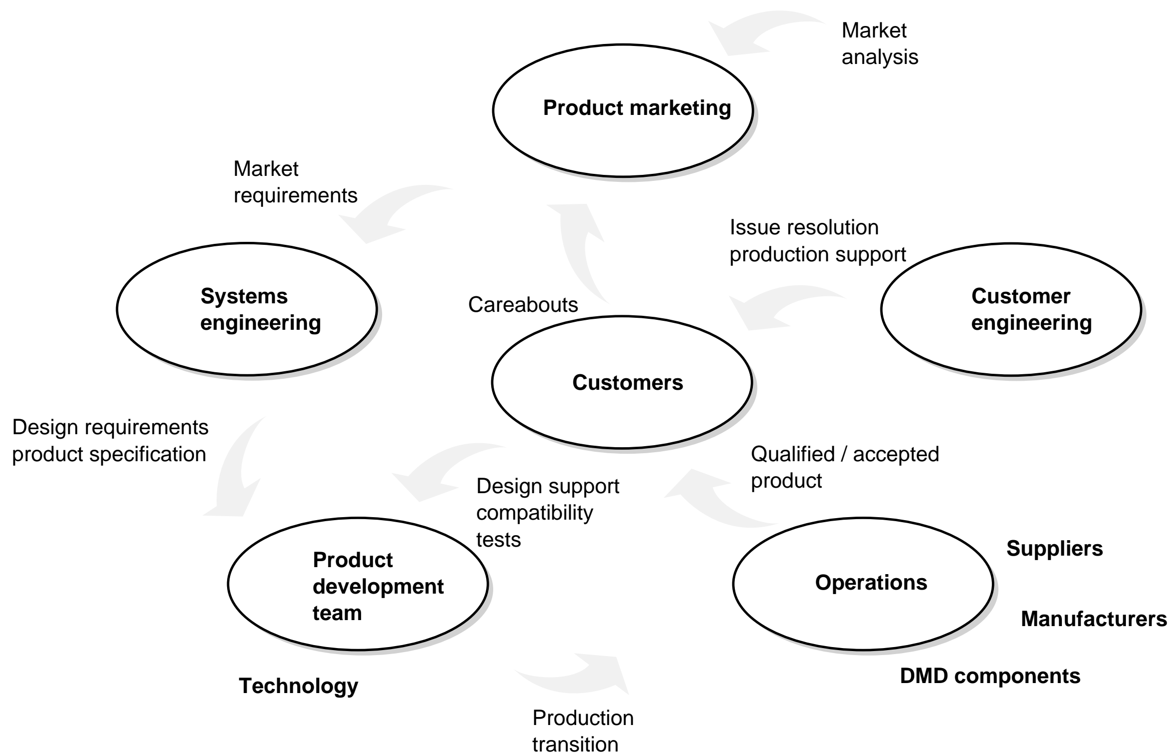

Figure 2. Information flow model.

essary as the development moves toward production. Emphasis is placed on design for manufacturability and design-to-cost. The concurrent efforts provide the basis for reducing cycle time and keeping overall product costs in line. Solid design practices, engineering, management and testing activities ensure product quality and customer satisfaction are achieved.

Issues management and production support are important to the customer satisfaction equation. Customer Engineering, within the Marketing organization, is responsible for technical interface with customers to document and resolve problems and complaints.

DI's business-focused product development process

A cross-functional team was established in 1994 to define a product development process. This team used the approach of reviewing existing processes internal to TI to identify a process appropriate for DI's needs. The highly successful process that was defined by Systems Group to meet government requirements was large and complex and would have been difficult to scale down to meet DI's entrepreneurial, quick-turn product cycle need. SC's process carefully defined the component development, but did not include the product assembly and customer integration issues that were critical to DI's success. The process used in TI's former Information Technology Group (ITG) was the closest fit for DI's requirements. It was modified to expand beyond the traditional product development life cycle that begins after product specifications are defined *(Figure 3)*. The DI team added detail to document concept definition (Phase 0) and market analysis (Phase 1) that lead to the product specifications and to clarify product phaseout (Phase 7 [not shown]).

The integrated process flow

Product development is market-driven, integrated and phase-gated. Each phase has a predefined, but tailorable set of tasks followed by a Decision Point Review (DPR). Collaborative multidiscipline teams are established early in the overall process to ensure all aspects of product development, including manufacturing, are addressed during these phases. Marketing drives the first two phases (0 and 1). A business case and high-level market requirements are established and approved. System Engineering ana-

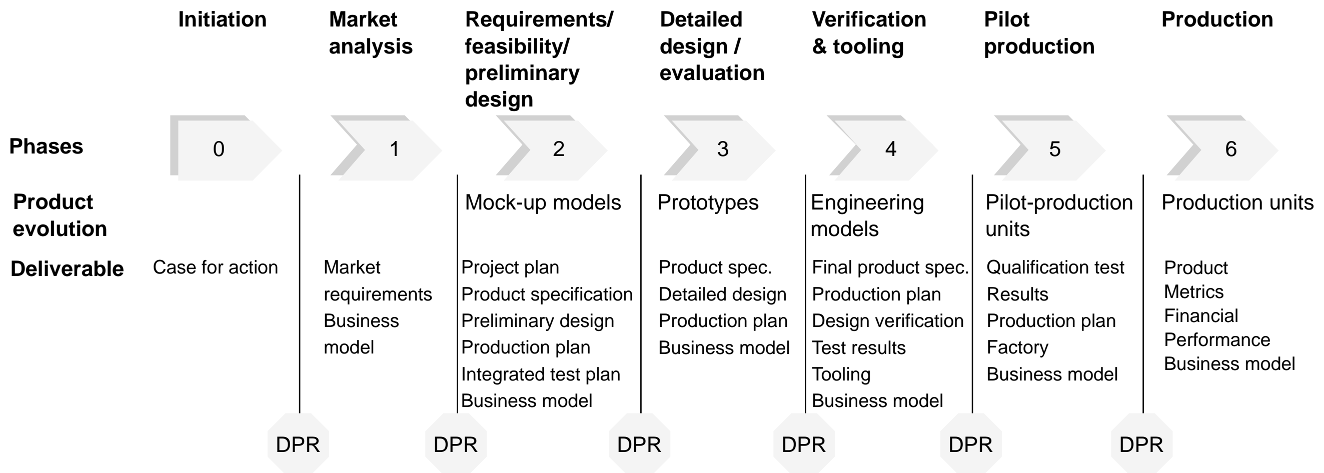

Figure 3. Phased product development process.

lyzes the market requirements to establish their feasibility and provide an initial assessment of technical risks.

At the beginning of Phase 2, Marketing and Systems Engineering agree to a set of requirements that will drive product design. Systems Engineering continues the trade-off and technical analysis effort to establish architecture and detailed requirements. The detailed requirements are provided to the designers for initial prototyping efforts. A preliminary design is reviewed and mock-up models are built.

The product specification, a contractually binding document between the customer and DI, is initially developed during Phase 2 and finalized before the end of Phase 4. This document describes the expected product performance and is the basis for product qualification.

Activities within Phase 2, such as feasibility studies, trades, risk assessments, test, production planning and development of mock-up models set the stage for a rapid thrust into production. Discontinuance of a product development effort could come as early as Phase 2 if critical business objectives established by Marketing are not met.

In Phase 3, detailed design and evaluation of prototypes begins. Coordination with customer designers, manufacturers and suppliers is critical during this phase.

Engineering models are developed within Phase 4. Design verification tests are executed during this phase to ensure all product requirements are met. Preparation for production including tooling, regulatory compliance certification and build planning begins in Phase 4. Production readiness reviews are used to ensure that the engineered product is prepared for product manufacturing.

Testing and additional tool refinement continues in Phase 5, Pilot Production. Production begins in Phase 6 and is managed by production engineering. Phase 7 (not shown) is the closeout of a product. This phase entails lifetime buys, inventory planning and closeout communications.

DI's product development process improvement

In 1997 another team was given the task of updating the DI product development process to incorporate lessons learned and to remove barriers to effective process use. The team held focus group meetings with Engineering and Marketing and searched benchmark databases to identify process improvements.

The team determined that the basic process was adequate. The SC market analysis process was adapted to add detail to activities in Phases 0 and 1. The former Personal Productivity Products division provided the basis for an electronic project notebook in Lotus Notes.™

To simplify use of the process documentation, the team established access and links through the TI Intranet. The current process is an electronic document with a tailoring matrix, document templates that are hot-linked to the project management notebook, an integrated corrective action item system and a "lessons-learned" database. *Figure 4* shows a few pages from the electronic project notebook as seen through TI's Intranet.

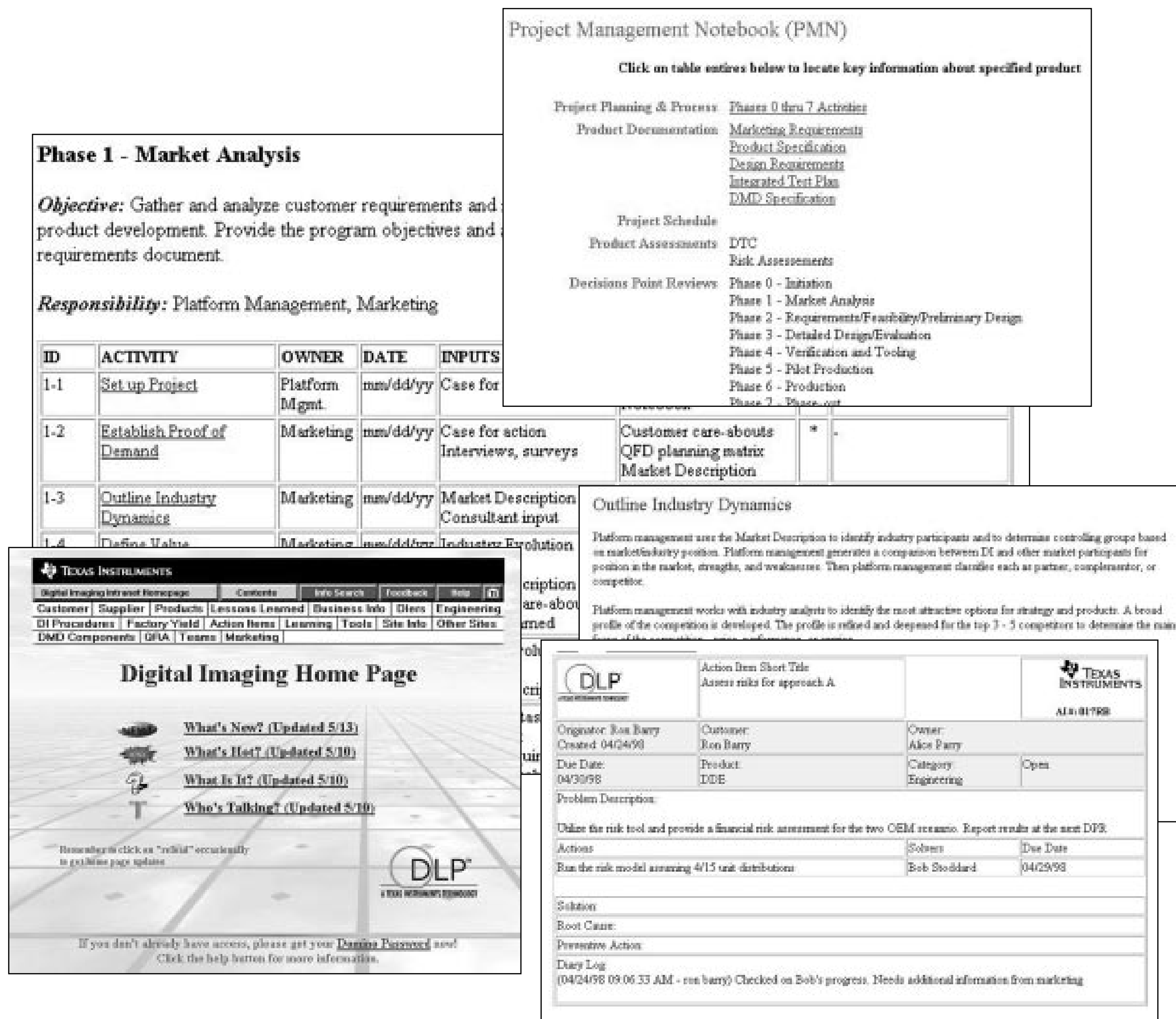

Figure 4. Excerpts from electronic project notebook.

High value aspects of the process

There are five aspects of the DI product development process that provide the greatest value.

Business focus. The product development process is focused on generating a product that meets market needs and is aligned with the DI business strategy. Phases 0 and 1 are concentrated on identifying the requirements of the market place. Platform managers have profit and loss responsibilities for a given area of the business and are responsible for these two phases. They are accountable for the product strategy and alignment with DI's business strategy.

The business focus is supported through all seven phases of the product life cycle by the gating process. At the end of each development phase, a decision point review is held. At the review, the business case and technical progress are reevaluated to ensure that the product is consistent with market requirements and business strategies. This process step helps eliminate wasted investment by identifying problems early in the development cycle.

Risk analysis and modeling. Risk analysis occurs throughout all product life cycle phases for each project team. The goal is to translate risks into financial impacts on revenue, profit from operations, gross

margin and discounted cumulative cash flow at the Digital Imaging project and platform level. A risk team, including Marketing, Project Management, Systems Engineering and Manufacturing (design-to-cost) is established. The team is responsible for following the risk analysis process shown in *Figure 5*.

Digital Imaging developed a financial risk management tool that leverages information in the traditional financial income statement (such as revenues, gross margin, profit and cash flow) and supports analysis of the combined uncertainty of various factors shown in Figure 5. A member of the DI Finance team facilitates the risk team and coordinates use of the tool and process. Members of the risk team monitor inputs and identify significant changes which trigger updates to the risk analysis.

The results of running the risk tool on "what if" alternatives are compared and presented at the decision point reviews. Business decisions to proceed or stop the development are based, in part, on the analysis. Risk management implemented by an experienced team using the financial risk tool enables the team to manage project risks and identify the impact to the financial bottom line.

Team based. A cross-functional development team is established at the end of the market analysis phase. Every attempt is made to move intact teams with domain expertise from project to project. Team members are involved in the activities described in the product development process across all phases (*Figure 6*). Engineering functions, such as producibility, reliability and quality assurance, are active participants in the development teams.

Responsibility for the product begins the transition to production engineering with the kick-off of the production readiness activities in Phase 4 (verification) and completes with the handoff at the end of Phase 5 (pilot production). The use of cross-functional teams throughout the development effort ensures that a quality design enters the factory and that a robust product is delivered to DI's customers.

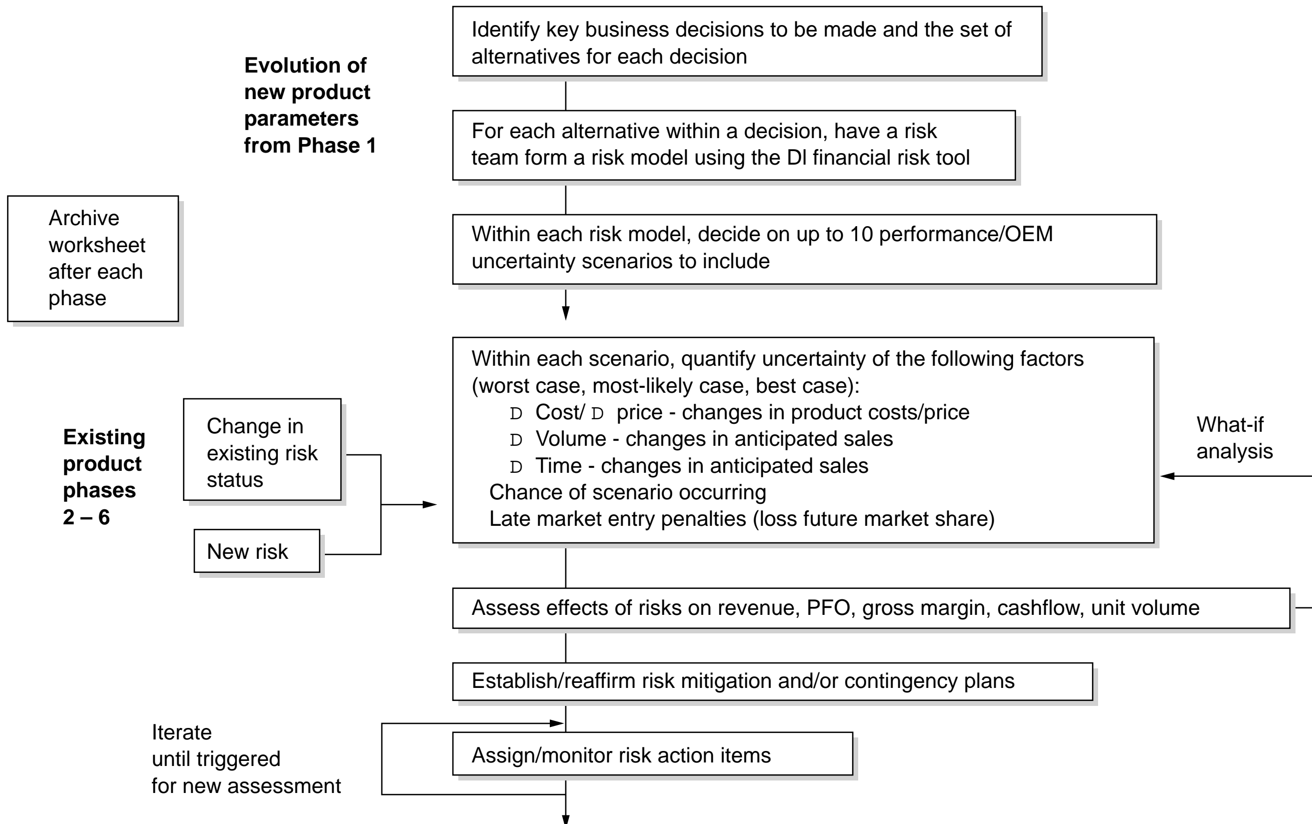

Figure 5. DI's risk analysis process.

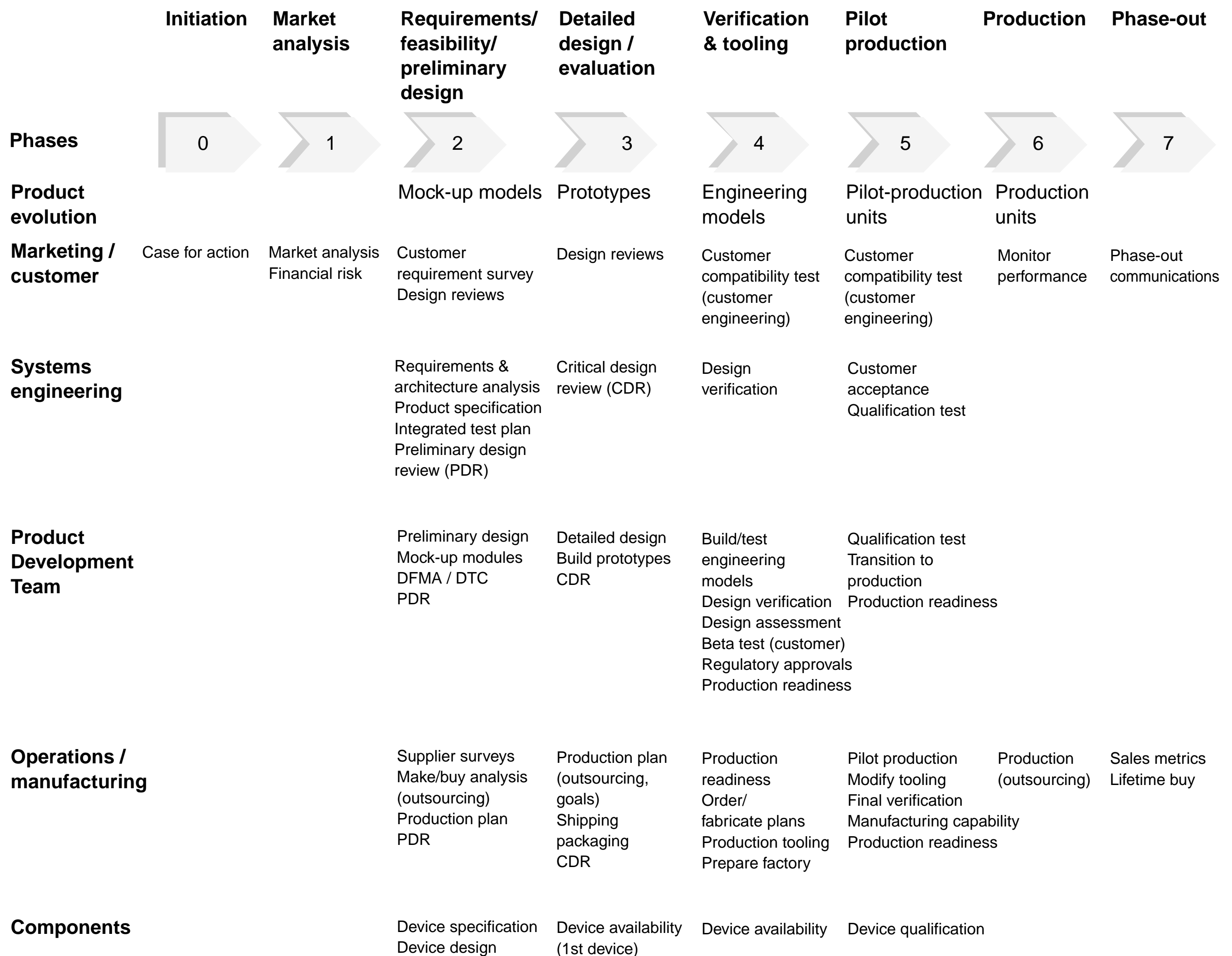

Figure 6. Cross-function activities during product development.

Tailoring. The product development process activities describe a robust generic product development. However, each development effort is unique. The product can vary from an entirely new platform design to a relatively simple upgrade of an existing product. The cross-functional development team needs the flexibility to define a process that specifically addresses their requirements. At the start of Phase 2, the product team uses the high-level requirements (defined in Phases 0 and 1), schedule, financial model and cost goals to evaluate the process activity matrix. Each activity is evaluated for applicability to the project. Tailoring allows the team to select the most cost-effective and value added activities to be performed during the development. The results of the tailoring are one of the major inputs to the planning process.

Phase synchronization. In preparation for the decision point review, platform management conducts a "phase synchronization." The phase synchronization has two elements. First, the development team evaluates the past phase and documents lessons learned that address technical, product, market or process issues. The lessons learned are documented in an electronic project notebook. The second element is planning the next phase. The team reviews their tailored process activity matrix and "retailors" the next phase activities, as necessary. The lessons learned database is searched for applicable topics from other projects. The phase synchronization ensures sharing

of lessons learned across project teams and allows the team to replan the project to address significant changes to technical requirements, cost, schedule, change in market conditions, etc.

Process contribution to business metrics

The product development process definition cannot be an end in itself. The purpose must be to increase Digital Imaging's performance in key business metrics. The business metrics are measurements that provide a barometer for judging DI's performance and setting thresholds for identifying improvement opportunities. Three metrics were selected for engineering and operations focus in 1998.

- **Customer satisfaction.** Measured by six-month customer surveys. The goal is to increase the overall satisfaction by 13% by Fall 1998. An improved and successfully deployed product development process can contribute to customer satisfaction by helping to reduce time to market and increase quality of the products as configured and delivered.
- **Integrated first pass yield.** Measured by factory output. The goal is to improve integrated yield at production release by 20%. The product development process calls out specific activities that directly impact integrated yield.
  - Clarifying, documenting and negotiating customer and market requirements
  - Involving customer and critical suppliers as early as possible during design, implementation and test
  - Initiating production planning (including yield goals) during preliminary design
  - Planning for all levels of test during requirement allocation
  - Requiring the use of design guides and formal/informal design reviews
  - Starting production readiness activities immediately after the critical design review
- **Bull's-eye.** Measured by the percent of projects on schedule. The 1998 goal is to increase project's on time to bull's-eye by 20%. The flexibility of tailoring the product development process allows each project team to focus on specific value added activities. The teams can leverage from the disciplined use of lessons learned documented by previous developments to decrease time spent in recreating methods or in following unprofitable paths.

The next step

The updated product development process has completed extensive review by functional organizations and has been released for use. Based on the limited deployment and implementation of the previous release, the update team has identified two process goals for 1998.

- Successful and widespread application of the process
- Continuous improvement

The team has identified four approaches, taken from standard concepts of successful change management which will increase the probability of successful process deployment.

- Request sponsorship from the DI Leadership Team to communicate expectations regarding use of the process
- Generate training presentation for all DI employees
- Establish process level metrics integrated with process progress reviews
- Perform selective compliance audits

The goal of continuous improvement will be met by disciplined use of lessons learned and by incorporating information received from compliance audits.

Benchmarking data indicates that companies with well-defined product development and project management processes can have significantly better performance than their competitors:

- Cycle time (40% faster time to market)
- Revenue (25% higher growth)
- Effective use of resources (200% more efficient per dollar invested)

A flexible process that is tightly coupled to customer and market requirements will help propel high quality Digital Imaging products into the marketplace earlier than the competition—yielding benefits in revenue, growth, customer satisfaction and shareholder value.

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Alice Parry

Alice Parry is the Process Development and Configuration manager in the Digital Imaging Quality and Reliability Assurance organization. She has been in DI since 1993 and set up software and hardware configuration management systems. She was a member of the teams that established the business process model and the product development process. She is a member of the software and systems engineering process improvement teams and is currently formulating a configuration management solution in SAP.

Alice joined TI in 1978 and received her B.S. in computer science from the University of Texas at Dallas in 1984, taking advantage of TI's Engineering Development Program. She received her M.S. in software engineering from Southern Methodist University in 1996.

Prior to her DI assignment Alice spent 14 years working with TI's former Systems Group (now Raytheon Systems Company) in configuration management and software quality. She has been active in the TI software process improvement effort (SofTware Engineering Process and Software Core Competency Teams) for six years.

As a member of the Dallas Business and Professional Women's organization, Alice taught the Leadership Skills and Development class. She views her experience and personal networks as strengths that have enabled her to identify and select best practices from defense and commercial communities.

Bob Stoddard

Bob Stoddard is currently the Software Assurance manager within the TI Digital Imaging Quality, Reliability Assurance (QRA) organization. Bob is responsible for assessing software process, technology and tools and also serves as a statistical coach for DI facilitating the activities of the DI Sigma Black Belt team. Bob is active in the process improvement activities of the DI Systems Engineering, Electrical Engineering, Software Engineering, Risk Management and Design-to-Cost teams. In these capacities, Bob has developed a Monte Carlo simulation financial risk analysis tool, a statistically-based design-to-cost tool and a tool to implement the analytic hierarchy process supporting the subjective evaluation of DI image quality.

Bob has an undergraduate degree in finance and accounting from the University of Maine and a master's degree in systems management with the University of Southern California. Most recently, Bob completed coursework in a doctoral program with the University of Maryland at College Park in the area of software reliability and applied statistics.

Bob is an active member of the IEEE and the American Society for Quality and is the program chair and deputy chair of the Dallas/Fort Worth Software Process Improvement Network (SPIN)—known locally as the Association for Software Engineering Excellence (ASEE). Bob holds ASQ certifications in reliability, quality, software quality and auditing.

Ron Barry

Ron Barry is currently the engineering manager within DI's Systems, Engineering and Operations organization. He is responsible for the development and improvement of engineering processes for software, electronics and systems engineering. Ron is the lead facilitator of the teams supporting each of these disciplines. He also is the facilitator of the Risk Management, Test, Design-to-Cost and Intranet teams. Ron coordinates staffing activities and engineering tool evaluation and acquisitions. He is a member of DI's People Development Team and assists in the coordination of specialized learning development coursework. He is also a member of DI's Technical Council and TI's Technical Communications Committee.

Ron is a Senior Member, Technical Staff and a Technical Award for Excellence recipient from TI's former Systems Group. He joined TI in 1979 after receiving his master's degree in computer science at West Virginia University. Prior to DI, Ron served in both the Systems and Industrial Automation Groups. ❑

From ICs To DMD™s

Abstract: *This article describes the process of the DMD™ and how it compares to standard IC and MEMS processing. The processes and device architecture will be described from CMOS through assembly test. A key goal for this device is to have similar processes and processing equipment as in the semiconductor industry. Packaging and electro-optical testing are two areas where this device does not follow mainstream IC components. The complete process flow, including package assembly and test are performed in a cleanroom environment due to the particle sensitivity of this mechanical device. Our lowest and highest resolution products in production have more than one-half and one million moving elements, respectively. Today, the majority of units we ship are defect free. The DMD has demonstrated capability of meeting customer performance and reliability expectations. Our technology and manufacturing capability can support current resolution and future, higher resolution products.*

Over 40 years ago bulky vacuum tubes and wires made up the piece-by-piece assembly of electronics. The invention of the transistor and the integrated circuit began a technological revolution—the miniaturization of electronics. Mechanics is now poised on the verge of similar revolution with its own miniaturization.[1] The driving force for the miniaturization of mechanical systems is cost, size, speed, weight and precision, while providing an effective interface between the macro and the microdynamic world. The terminology for these small mechanical systems is microelectrical mechanical systems (MEMS).

The majority of MEMS products being produced today are targeted to replace existing products. Replacement alone, however, is not sufficient—the new device must provide more functions with better performance at a reduced cost. Silicon gas chromatographs, mass flow sensors, tactile sensors, optical fiber alignment guides, pressure sensors (automobile, medical, and industrial), electrostatically driven micromotors, microactuators, chemical microsensors, microtubing and microvalving are just a few examples of miniaturized mechanical systems.[2,3] The Digital Micromirror Device™ (DMD) is a MEMS device that uses the miniaturization advantages of both IC and mechanical systems.

Fabrication of the DMD comprises several major operations. These include SRAM CMOS circuitry, DMD superstructure (i.e., the structure built on top of the CMOS) fabrication, window assembly fabrication, packaged component assembly and device test and characterization. To build the DMD, a broad spectrum of technologies, including semiconductor, packaging, optics, materials and test expertise, were brought together.[4]

The DMD is a reflective, passive, spatial light modulator composed of an array of rotatable aluminum mirrors currently targeted for the projection displays market. It offers performance far exceeding liquid crystal display (LCD) and cathode ray tube (CRT) projection display technologies. *Figure 1* illustrates the micromirror element, which is compromised of an aluminum mirror suspended over an air gap by two thin, post-supported, mechanically compliant torsion hinges that permit a mirror rotation of ±10°. As a digital light switch, the DMD operates

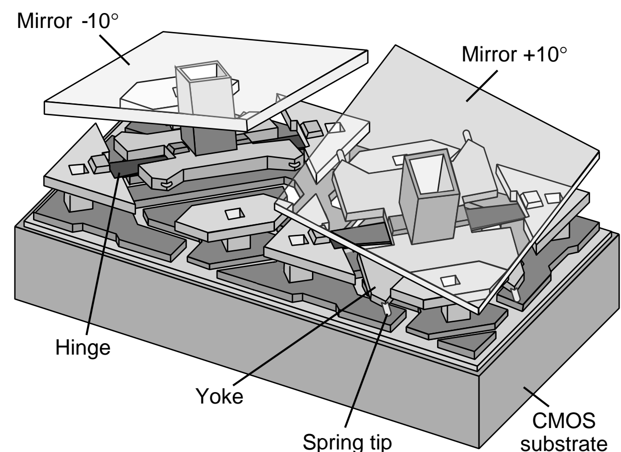

Figure 1. DMD pixel (transparent mirror, rotated).

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under dark field projection optics to direct light from a projection source into or out of the pupil of a projection lens (*Figure 2*).

Unlike most MEMS devices, the DMD is fully integrated and monolithically fabricated on a mature SRAM CMOS address circuitry. The drive circuitry for most MEMS devices is either off-chip or on the chip but outside the active mechanical element region.

The birth of this technology occurred within TI's Central Research Laboratories under the direction of Larry Hornbeck (the inventor), Ed Nelson and Jeffrey Sampsell. The ability to transfer this technology into a high reliability, yielding- and performance-based product was not realized until the formation of the Digital Imaging business.

The immense level of development and production effort to fabricate the DMD is equally divided into thirds: the DMD superstructure, package assembly and electro-optical test. Although the tangible product produced in Texas Instruments is the DMD itself, of interest to our end customer is the projected image with optical performance being the most critical metric.

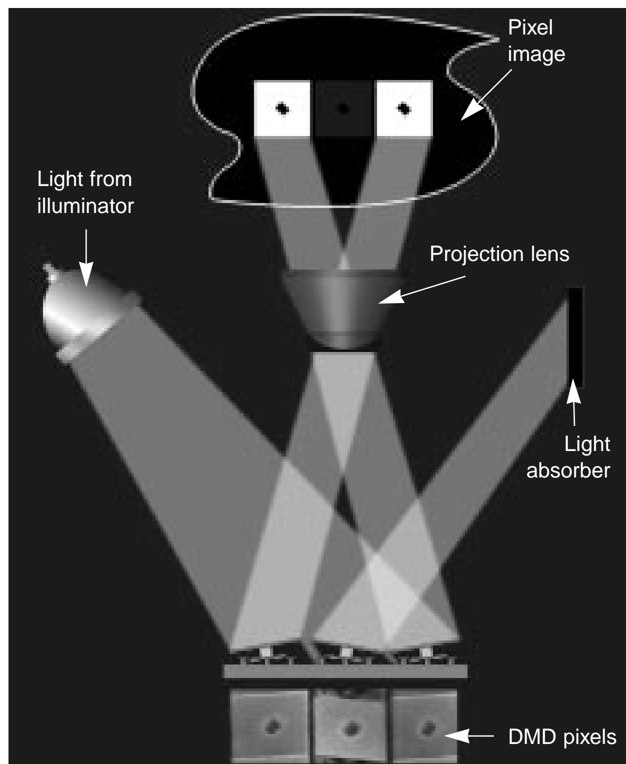

Figure 2. Dark field projection of a DMD.

A major goal set during the early days of Digital Imaging was to fabricate this technology using standard semiconductor processes and equipment tools as a means of efficient asset utilization. In keeping this goal, in February of this year we transferred the wafer portion of the processing to the DMOS-IV fabrication facility. This truly demonstrates the ability for this technology to be fabricated in a mature wafer fab using similar semiconductor processes and equipment tools.

The DMD is currently in volume production for SVGA (super video graphics adapter, 848 x 600 pixels) and XGA (extended graphics adapter, 1024 x 768 pixels) resolution display formats. It is a high performance display device that can be manufactured with high yield at marketable cost.[5] This publication provides an overview of key details of the development and production effort of the DMD manufacturing process and how it compares to the integrated circuit (IC) industry as well as other MEMS components.

CMOS fabrication

The DMD mechanical element (commonly referred as a "pixel", for picture element, or "mirror") is processed over the CMOS architecture. Our CMOS is processed in DMOS-IV and consists of conventional SRAM cells. The SRAM underlying each mirror is a six-transistor circuit or storage cell fabricated using a twin-well CMOS, 0.8 µm, double-level metallization process. *Figure 3* shows the layout of the integrated DMD structure. The SRAM cell provides addressability to each individual mirror. The mirror for each device is 16 µm square on a pitch of 17 µm. The size of the mirror is determined by both the optical system and the minimum geometry achievable for the CMOS SRAM cell.

Once the double-level metallization is complete, a final interlevel dielectric is applied. This dielectric level is the surface on which the DMD pixel architecture is fabricated. It is critical that this level is locally flat. That is, differences in topography as little as 800 angstroms across the landing surface of a pixel can negatively impact the projected image in certain systems. The human eye is extremely sensitive to very low contrast changes. For this reason, chemical-mechanical polishing (CMP) is required for adequate planarization. Once CMP is complete, vias are generated in the dielectric. For each pixel there is a pair of address electrodes connected to the complementary sides of the underlying SRAM cell (Figure 3). Each pixel has two vias within the cell. Depending on the

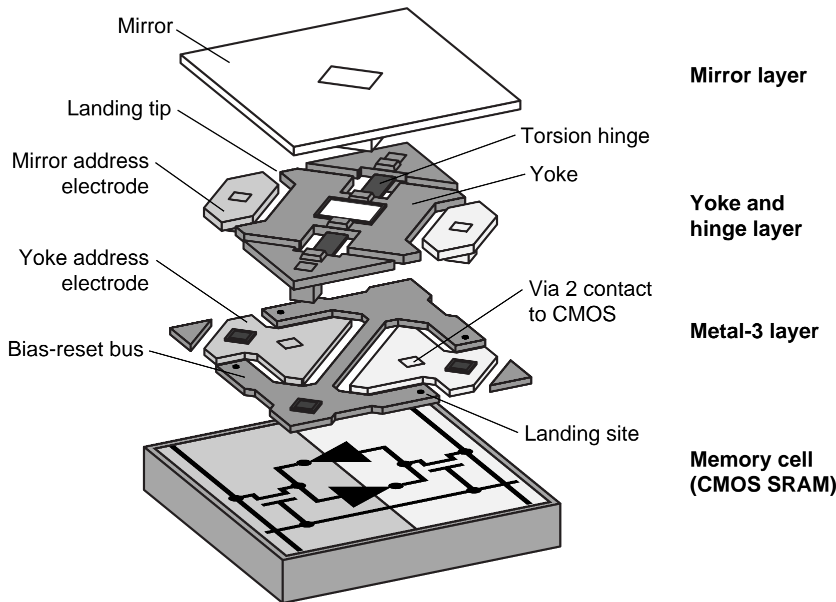

Figure 3. DMD pixel electrical schematic.

SRAM state, a combination of bias and address voltages electrostatically attracts each pixel element to one of the two address electrodes. One address side represents the "off-state" while the other side represents the "on-state" of the pixel.

Superstructure fabrication

IC fabrication employs surface micromachining layering techniques involving repetitive deposition, pattern and removal processes.[6] The DMD as well as many MEMS components use surface micromachining layering techniques. Other MEMS components can be fabricated using bulk micromachining, bonding or high-aspect ratio (or LIGA, Lithografie, Galvanik, Abformung) techniques.[7] Six metal layers make up an entire pixel cell—two metal layers of the CMOS SRAM cell and four additional metal layers that define the pixel superstructure. *Figure 4* provides a simplified process flow of the superstructure, test and assembly operations.

An attractive feature realized in the processing of the DMD superstructure is its outgrowth from the IC industry and its fabrication sequence. Many of the processes and equipment tools used in the superstructure fabrication (or front-end) are common with the semiconductor industry.

After contact openings (i.e., the vias) the address circuit electrode is formed on top of the CMOS dielectric layer. The aluminum address electrode film is sputter-deposited onto the dielectric, lithographically patterned and plasma etched. An organic sacrificial planarizing layer is then spun over the electrode and patterned with vias, which subsequently forms the support posts. These posts provide not only mechanical support but also serve as electrical contacts.

Two proprietary metal alloy layers are employed for the buried hinge process. The hinge alloy is sputtered on top of the sacrificial layer, followed by a plasma-deposited masking oxide that is patterned to define the hinges. A typical semiconductor metal deposition occurs on an inorganic dielectric (e.g., SiO_2) rather than an organic dielectric as is done with the DMD. Deposition of a second alloy layer buries the hinge oxide and forms the beam. This, in turn, is followed by still another plasma-deposited masking oxide, which is patterned to form the beam. A single metal plasma-etching step forms the hinges and beam. The support posts consist of both the hinge and beam metals. Standard IC technology tightly controls the critical dimensions in both x and y directions. However, the z-axis dimension (i.e., thickness) must also be tightly controlled. Both sacrificial layer and hinge thickness tolerances are precisely controlled to achieve reproducible, uniform mirror tilt angles and addressing voltages, respectively.

A second sacrificial planarizing layer is spun over this hinge-beam level with the process essentially repeated. In this second layer, only one metal layer is deposited—a highly reflective aluminum mirror

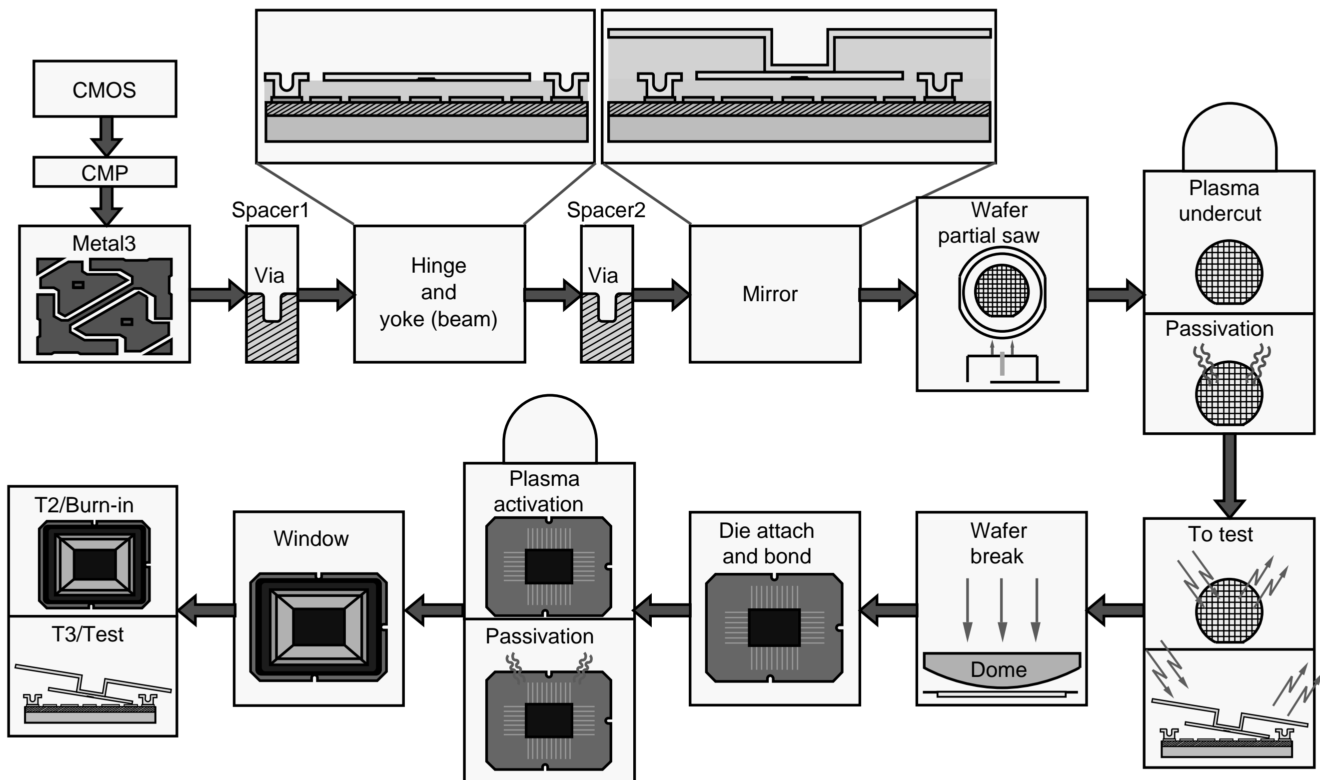

Figure 4. DMD process flow.

level. The completed superstructure is called the "hidden hinge" since the hinge is literally hidden by the mirror. This hidden hinge structure is Digital Imaging's fourth generation design. The impetus for this new design was driven mainly by performance requirements to improve the optical efficiency of the device. Figure 1 depicts an exploded view of the pixel.

At this point of DMD fabrication, the superstructure process is complete. This is essentially the demarcation between the front end and back end of the process. The individual pixels, however, have not been released, so mechanical motion of the pixels is not yet possible.

Particle control throughout the superstructure process is critical. Besides causing electrical failures, particles can also cause mechanical failure of the pixel itself. A defective pixel is typically visible on a projected image. Since the DMD is a three-dimensional component with mechanical movement, particle control involves both intralevel and interlevel monitoring. The smallest spacing at the intralevel is on the order of 1 μm. However, the interlevel gap can approach spacings as small as 0.2 μm during mechanical operation of the DMD pixel. For this reason, particle control well into the submicron range is critical. Our equipment and process engineering teams have done a superb job in achieving defect density levels that are unprecedented in the semiconductor industry. Similar to IC design, development activities are under way to make the DMD architecture less sensitive to these submicron particles.

Die separation and pixel release

Die separation is typically the first step where the MEMS industry (and the DMD technology) deviates from that of the IC industry. For silicon-wafer applications, the IC industry can employ three die separation techniques, which include laser scribing, diamond scribing and diamond-wheel sawing.[8] Sawing is the common die separation technique. Due to the expense of most MEMS packages, it is imperative that only functional devices meeting our specifications are assembled. Therefore, the MEMS mechanical element must be released for functionality testing prior to assembly. As with any high volume process,

batch or single wafer processing is the preferred manufacturing strategy. Processing individual die is typically a time-consuming and labor-intensive process—even with established automation tools. The separation of DMD die on a silicon wafer and subsequent packaging of those die was a significant core challenge for the DMD program.[4]

The DMD manufacturing strategy is to release all pixels at the wafer level rather than the individual die level (as was initially done in TI's Central Research Laboratories and the early days of Digital Imaging). It is not feasible to first release the DMD pixels and then saw the wafer. The amount of water flow through the saw would destroy the superstructure. Instead, a protective layer is placed on top of the mirror level, followed by the wafer being partially sawn and then cleaned to remove saw debris. The release process involves an organic isotropic ash process that removes both sacrificial layers from the DMD pixel using a single wafer asher. An air gap has now been created under the mirror. These steps, including the saw process, occur within the Class 10 (less than ten 0.3 μm particles per cubic foot of air) cleanroom environment. The wafer can now be presented to the wafer tester as described below.

Once wafer level test is complete, separation of the functional die from the wafer is the next crucial process step. TI has a proprietary process that breaks the wafer along the partially sawn scribe kerfs (Figure 4). This process must also be an extremely clean process since any silicon debris generated during the break process can cause mechanical failure to the pixel. Similar to standard sawing of IC components, the separated die remain on saw frames (with dicing tape) so the entire wafer can be presented and processed on a die attach assembly tool.

Package assembly

Most MEMS technologies consider packaging as their Achilles heel of manufacturing.[6] The DMD package is an integral part of the DMD. The package not only provides signal and power lead connections to the chip, but also provides protection from external environments and is a critical component in the optics system. The DMD package is application specific, which is true for most MEMS packages as well. Again, the manufacturing strategy for DMD assembly is to harmonize with standard SC equipment. The DMD, however, cannot rely on conventional packaging technology. Within the MEMS industry (and unlike the IC industry) there is no MEMS packaging infrastructure, accumulated MEMS experience base or significant MEMS depository of assembly knowledge.

Due to the application specific nature of the DMD package, the optical lid for the DMD had to be designed by the packaging development team. Requirements for the optical lid include minimal light losses, optical flatness/parallelism, an optical aperture and a frame to support package welding (*Figure 5*). The window was first fabricated at TI's Defense Systems and Electronics Group. Attached to the internal region of the optical lid is a getter to control contaminants (including moisture). Stiction mitigation is the primary driver for the inclusion of the getter: Moisture (i.e., capillary attraction) can cause the pixel to stick upon landing.

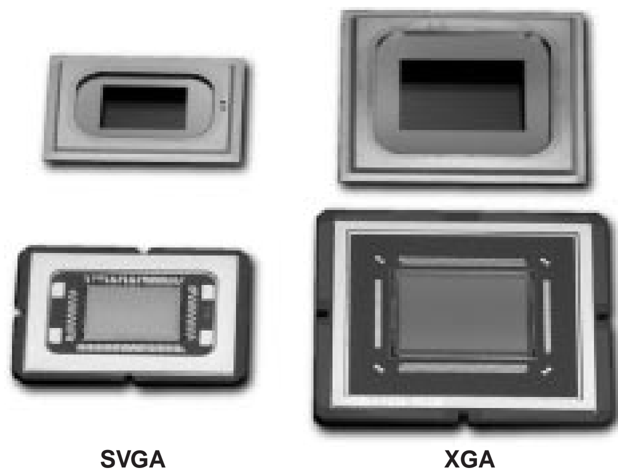

Figure 5. DMD ceramic headers and lids.

Most IC assembly areas are performed in non-cleanroom environments. Since the DMD pixels are exposed to ambient conditions prior to lid attachment, the entire assembly process is performed in our Class 10 cleanroom. Once the optical lid is hermetically sealed by seam welding to the DMD package, the device can be removed from the cleanroom environment after it is helium leak checked.[4] Although an IC-familiar sequence of assembly operations (i.e., die attach, wire bond, window seal and final test) is employed for the DMD, the product nevertheless requires special handling. Most assembly equipment has been modified to function within a cleanroom environment. Front-side, pick-and-place contact collets were carefully designed so as not to damage the DMD pixels. Die attach adhesives were chosen with low outgassing, low cure temperature and thermal

conductivity qualities—mirror stiction, mirror planarity and hinge compliance are the main image quality concerns, respectively.

Particulate control is a top effort in the assembly area. Scrapping a DMD due to particle contamination at this stage in the process flow is very costly. *Figure 6* shows an example of particulate contamination and its potential effect on mirror functionality. All packaging machines are commercially available semiconductor tools, but each has been modified for low particulate operation. In addition, a proprietary cleaning processes has been developed. Like the wafer portion of a semiconductor process, cleaning steps are used in the assembly process. A process has been developed to clean the device of particle contamination at the package level without damaging the released pixels.[4]

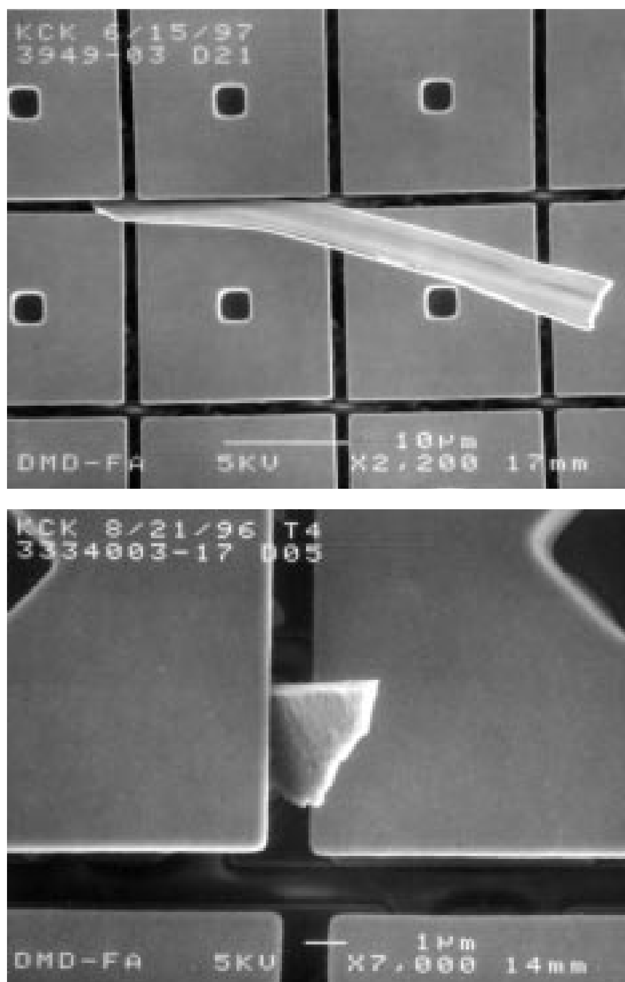

Figure 6. DMD pixels with particle defects.

As with any mechanical system, friction is a chief concern. Since the DMD is a mechanical component and the DMD pixels make surface contact, yet another TI proprietary process was developed to mitigate pixel stiction. This process is performed at the package level just prior to placement of the optical lid. During the early stage of DMD development, stiction was a primary focus. The DMD pixel must land millions of times over the life of the product.

Other MEMS products do not make surface contact or the surface contact is very limited during the life of the product. For instance, one accelerometer design, a MEMS component that is used as a sensor for automotive air bag systems, is a component that does not make surface contact during use. Accelerometers, however, are sensitive to stiction during shipping and handling. With a number of key process and design improvements, we have overcome the stiction hurdle.

Similar to processing equipment, the individual package piece parts must also be particle free. For instance, a mechanical and/or electrical failure occurs if a loose particle on the optical lid falls onto an active DMD pixel. A particle that is not loose on the optical lid can still cause a projection system defect. In this case, an optical lid defect can cast a low contrast defect (e.g., a shadow) on the projection screen. To avoid this, special handling and attention to particle control is placed upon processing of the optical lid.

As is typical with most MEMS devices, a significant portion of the total device cost is in the package. In the semiconductor industry the die dominates the cost of the component; however, for the DMD, the package dominates the cost. The biggest challenge for the DMD package development team is to develop a low-cost package that is more in line with what is typical in the IC industry while still meeting our system level optical quality goals and specific device requirements. Likewise, a huge effort is currently underway within the MEMS community to identify low cost hermetic packages that can be used for a large number of MEMS components.

Wafer, package and projection level testing

Mature parametric test structures are used on production IC components to monitor the health of the semiconductor process. Such parametric test structures have yet to be developed, characterized and implemented for most MEMS components.[6] The DMD does use standard CMOS test parametric structures for electrical characterization such as resistance

and capacitance. Mechanical parametric test structures are not yet established to monitor such things as residual stress of deposited films. Currently, the DMD pixel itself is our best parametric monitor.

Since released pixels are very sensitive to particles, the DMD probe area must remain in a cleanroom environment (typical IC wafer probe areas are outside of this environment). Like any IC component, there are a number of wafer-probing tools commercially available to perform electrical testing. The DMD, however, requires electrical, mechanical and optical testing. The SRAM CMOS functionality can certainly be tested on most electrical testers. The read-write function of the SRAM, however, does not guarantee that pixels are operational. Each pixel must be tested for its opto-mechanical functionality.

Herein lies a major challenge—electrical opto-mechanical testers are not off-the-shelf tools. This challenge is similar to many MEMS products—the tester needs to be somewhat application specific. The DMD test development group did an exemplary job building a low-cost, high-speed, low-particle-generating test set that performs our SRAM CMOS evaluations while also determining the functional state of each mirror on a device. For a typical SVGA product, the tester determines the functionality for over one half million pixels per device. The tester output indicates the number of single bit fails in the SRAM circuitry as well as the pixel array thus determining which die are selected for assembly. This test output also provides process engineering with valuable mechanical parametric information—hinge compliance and mirror stiction in particular.

After package assembly is complete, the device is ready for a mechanical burn-in and final package test. The intent of burn-in is to mechanically stress each pixel to uncover any process problems related to stiction mitigation and hinge deposition. Besides testing for similar characteristics as mentioned during the wafer level test, pixel reflectivity, contrast ratio and tilt angle are also measured. Again, valuable mechanical parametric information is provided to product and process engineering. A projector test is the final test performed prior to shipment. This test uncovers problems that are mostly related to the optical lid such as blemish and border problems. As with any IC test area, the DMD test group has a continous effort in test time reduction.

Device reliability

Eliminating defective pixels is currently our main device quality objective. DMD reliability means having all pixels remain functional over time, while ensuring each device works over a wide range of operating conditions. The DMD product could not solely depend on U.S. Department of Defense Military Specification reliability standards as used in the IC industry. A number of specialized reliability tests had to be developed to identify failure causes and validate the effectiveness of corrective actions. As with most MEMS devices, reliability tests are application specific. To date we have identified and eliminated all life-limiting failure modes. Future failure rate improvements will result from continued particle reduction efforts currently underway.

Summary

Having a rich collection of core competencies of CMOS, DMD, window and projector engine fabrication in close proximity has allowed very rapid product development and maturation. The DMD is currently in volume production for both SVGA and XGA display formats. It is highly unlikely that the remaining specialized (i.e., one-of-a-kind) DMD processing equipment will significantly influence any semiconductor equipment manufacturers. Therefore, it is Digital Imaging's responsibility to continue developing processes that are within the mainstream of the IC industry. Compared to other high volume MEMS companies, we are producing a more complex device. For instance, we produce more moving elements on one DMD wafer than most high volume MEMS manufacturers produce in a year.

Our manufacturing team has continually demonstrated increased shipping rates each month to meet rising business needs for Digital Imaging. A very significant percentage of SVGA and XGA devices we ship today are defect free. The demonstrated ability to transfer this technology to a mature wafer fab like DMOS-IV clearly meets our business and technology objectives as we align ourselves with the semiconductor industry. This transfer further enables our business strategy by avoiding a capacity limited situation. We have the technology and manufacturing capability to fabricate devices configured for other applications, including higher resolution (SXGA—1280 x 1024) displays, currently in initial production. The DMD is meeting our customer performance and reliability expectations as well as our business yield and cost goals.

Trademarks

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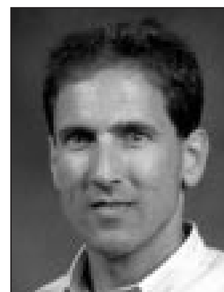

Michael A. Mignardi

Michael A. Mignardi is a Senior Member, Technical Staff (Emeritus) responsible for DMD product development, product engineering, test and design. Current responsibilities involve the delivery of new high resolution DMDs with improved optical performance.

Michael joined TI and the DMD group when it still resided in TI's Central Research Laboratories. His responsibilities at that time were process integration and development. Before joining TI, he worked in the Defense Analytical Labs at Southern Research Institute in Birmingham, Alabama. This work involved the controlled destruction of chemical warfare munitions around the world.

He holds a B.S. and a Ph.D. in chemistry from the University of Florida. He also holds a number of patents related to DMD processing.

Outside of work, Michael enjoys spending time with his wife, Marcy, and two children, Landon and Lauren. He also enjoys any activity or sport that involves being outdoors.

DMD™ pixel mechanics simulation

***Abstract:** Great strides in Digital Imaging's (DI) theoretical simulation of Digital Micromirror Device™ (DMD™) pixel mechanics have occurred over the past two years, culminating in a customized TI-proprietary DMD Pixel Simulation Tool (DMDPST) that is on the leading edge of microelectromechanical-systems (MEMS) modeling. This publication covers the following topics as they pertain to the DMDPST: development history, requirements for effective simulation, experimental-theoretical calibration methods, critical roles in DI and detailed illustrative examples of some of its capabilities.*

The field of theoretical mechanics is a branch of physical sciences concerned with the state of rest or motion of bodies subjected to the action of loads (forces and torques) of various types. Effective application of theoretical DMD pixel mechanics modeling was already an established precedent in DI prior to the development of the DMDPST.[1] This early modeling work used a combination of linear and nonlinear finite element models, closed-form solutions and simple pixel mechanics simulation software codes. These analytical methods aided in the development of many of the innovative concepts still found in current DMD products.

Development history of the DMD pixel simulation tool (DMDPST)

Work on the DMDPST began in February 1996 with the highly aggressive goal of developing a prototype of a full-featured pixel mechanics simulation code by midyear. Within a month the complete differential equations of motion for the pixel were derived. By March 1996 these equations were codified into software and the first working simulator version was under beta test. During this time the simulator underwent experimental calibration and was cautiously used to evaluate existing design concepts. By June 1996 a full-featured prototype was deemed mature enough for inclusion in an external technical publication.1 By the end of 1996 the 22nd major revision of the simulator (building on prior extensive experimental corroboration) was depended upon to evaluate and optimize pixel designs. Currently this TI-proprietary simulation code, recently renamed the DMD pixel simulation tool (DMDPST)[2] is on its 65th major revision with more improvements and further experimental corroboration planned. (Reference 3 provides additional DMDPST pixel mechanics modeling information).

Robert E. Meier

To illustrate the great strides in pixel simulation capability achieved over the past two years, one can use the metric of software complexity. Earlier attempts at a basic pixel simulator contained roughly 200 lines of code and half a dozen functional modules. Only a few input variables were required and the mirror flight trajectory (angle versus time) was the single output. By comparison, the current version of DMDPST contains 6500 lines of code and 52 functional modules, with 128 input variables and 84 selectable output variables plotted as a function of time. Two output array mapping options for critical design metrics concerning operational robustness and surface wear also are available. Another optional user-callable module (500 lines of code) manages a separate three-dimensional electrostatics boundary element algorithm (including fringing effects) called FastCap.[4-7] FastCap is a public-domain code funded by the Defense Advanced Research Projects Agency (DARPA) and developed by the Massachusetts Institute of Technology. The front and back ends (not the core solution algorithms) of the DI version of FastCap have been customized to interface directly with DMDPST.

Requirements for a highly effective DMD pixel mechanics simulation tool

To develop a highly effective DMD pixel mechanics simulation tool, certain critical requirements must be met. The simulator must:

- Have very fast execution times
- Produce stable, precise and repeatable results that are corroborated against experimental data

- Use realistic manufacturing geometries and process tolerances
- Be customized directly for the specific kinds of inputs/outputs and design metrics required for comprehensive pixel design evaluation

DMDPST has achieved great strides in all of these areas simultaneously. It far exceeds what is commercially available for DMD pixel mechanics modeling.

DMDPST's competitive edge stems largely from aggressive customization of computational algorithms to fit the specific, bounded physics of the digital micromirror. High-speed adaptive solution algorithms also were implemented. They refine themselves during highly volatile periods of pixel behavior. They also relax their precision during more stable or quiescent periods. This has led to fast, stable, precise and repeatable results.

Currently, DMDPST averages about 2-3 seconds of clock time per full time history simulation of a typical mirror flight trajectory under normal operating conditions. This includes nonlinear loadings and three-dimensional electrostatics with fringing effects using a Hewlett-Packard HP9000 J282 machine with 256 megabytes of random access memory. This can be compared to most commercial MEMS modeling codes, which might require (depending on the level of precision, degree of fidelity to the nonlinear physics and type of solution algorithm) minutes to hours to days on a comparable machine. A conservative statement can be made that DMDPST is at least an order of magnitude faster (if not several orders) in simulating DMD pixel mechanics than most commercial MEMS modeling codes available today. A critical benefit of DMDPST is that it reduces turnaround time on comprehensive pixel evaluation from weeks to hours.

The time required to simulate new design concepts also has been significantly reduced by customizing the front and back ends of DMDPST to interface directly with TI-developed modeling pre- and post-processors.[8, 9] In addition, a direct interface to a TI-developed linear static/dynamic finite element solution code enables the modeling of structural vibration modes of the DMD pixel and analysis of static loads for calibration purposes.[10]

Experimental calibration of DMDPST

It is critical that a simulation code accurately describes the physics being modeled. DMDPST has undergone continuous aggressive comparison to experimental data. This data includes dynamic structural modes (resonant frequencies) of the pixel, mirror flight trajectories under various parameter settings, operational robustness maps and static applied loadings for calibration. It is not uncommon to validate DMDPST results using experimental data for a given pixel design and discover later that new experimental data no longer correlates strongly with the simulation results. Investigative work is then conducted to determine the cause of the anomaly, which is usually resolved quickly. Sometimes an error or weakness in the simulation algorithms may be uncovered, while in other cases a purposeful or unintended change in the manufacturing process is often the root cause. This ongoing dialogue between theoretical simulation and experimental characterization has made DMDPST a trusted, powerful tool that DI is aggressively applying to a variety of critical technology development paths.

The critical roles DMDPST plays in Digital Imaging's operations

DMDPST plays a number of critical roles in DI including:

- Development, analysis and optimization of pixel designs or voltage waveforms to generate increasingly innovative and competitive products with reduced time-to-market and higher probability of first time fabrication success
- Screening out ill-conceived design or waveform changes to prevent unwarranted expenditures of engineering time and resources which could be devoted to more worthwhile critical path endeavors
- Assessing parameter sensitivities and centering their value ranges in a planned design of experiment (DoE) to focus the experiment on yielding the most useful data possible
- Sizing mechanical compliances or pixel geometry to adjust for manufacturing changes or custom design changes (such as dielectric isolation)
- Elucidating the physics behind (sometimes anomalous) experimental data
- Training Digital Imaging staff in the basic physics underlying normal operation of the DMD device, its critical design issues and typical failure mechanisms

It has been estimated that DMDPST achieves semi-annual savings in excess of $100,000 for each major

design revision whose fabrication is prevented due to a simulated low probability of success.

The training value of DMDPST in describing the basic physics of the DMD has become an unexpected value-added aspect of the simulation effort. For training purposes, DMDPST can map the time-varying mirror trajectory motion (as well as the corresponding electrostatic pressure distribution) onto a three-dimensional solid model. Pixel mechanics animation movies can then be created using the TI-developed modeling code in Reference 8. *Figure 1* shows a typical model used for these purposes. Pixel mechanics training using DMDPST animations has been widespread throughout DI using this readily understood medium, thereby elevating the knowledge of basic DMD physics across all technical levels of the organization.

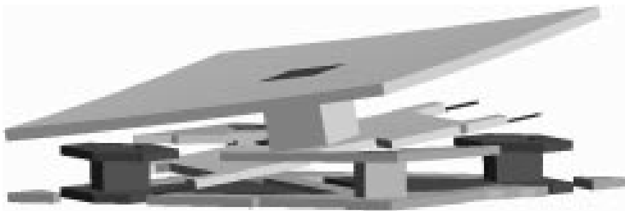

Figure 1. Typical 3D pixel mechanics solid model used for training animations.

The following section contains a detailed example of how DMDPST results can help clarify basic pixel physics. This example walks through a typical mirror trajectory time history to explain how applied voltages produce loads that control the mirror's motion in a very precise, well-engineered manner.

Using DMDPST to elucidate the physics: walking step-by-step through time

The DMD unit cell (comprising the mirror, superstructure and underlying CMOS circuitry) is a complex dynamic micromechanical system. To meet the stringent speed requirements for video applications, the cell must drive the mirror from one extreme landing position to the other at very high speed as incoming video data dictates. This must be done while angular transition time and impact energy are minimized and operational robustness and reliability are maximized. Key to achieving these optimization goals is effective drive voltage waveform design, which aims to elicit desired dynamic angular responses from the mirror through the application of time-varying electrostatic torque (dynamic addressing). This section contains a top-level discussion of a typical DMD dynamic addressing scheme, using the theoretical results of DMDPST. It should be noted that most of the waveform concepts and dynamic mirror transition terminology contained in this section are based on a long history of innovative experimental characterization and well-engineered waveform design.[11-14]

To control a DMD mirror, a bias voltage is applied to the mirror, while an address voltage is applied to one of the landing side conductors (the zeroed address complement is loaded on the opposite landing side conductor). The potential difference between the bias and address voltages on one side of the mirror versus the other will determine which side the mirror rotates toward. *Figure 2* shows two mirror angular trajectories as well as the bias voltage waveform applied to both mirrors and the address voltage waveform on the nonzero (high) side. In both trajectories the starting angle is roughly –10 degrees. In one case the mirror transitions quickly from one side (–10 degrees) to the other (+10 degrees) for what is called a “crossover transition.” In the other case the mirror undergoes dynamic perturbation, but remains on the same (–10 degree) side for what is called a “stay transition.” From an operational standpoint either of these trajectories may be dictated by incoming video data, which commands the mirror to be optically on or off.

Figure 3 shows the same mirror trajectories as those in Figure 2, along with the applied electrostatic torque acting on the mirror. The electrostatic torque (T_e) (ignoring fringing fields) is given by:

$$T_e = * x(dF/dA)dA$$

where dF/dA is the electrostatic force per unit area exerted on an elemental area dA of the yoke or mirror, which is a distance x from the torsion axis. The integral is performed over the electrostatically active portions of the yoke and mirror. The value dF/dA is given by:

$$dF/dA = (1/2)\varepsilon_o (\Delta V/\Delta Z)^2$$

where ΔV is the potential difference across the air gap, measured between the mirror/yoke and address electrodes. ΔZ is the size of the air gap at a given elemental area dA location.

Therefore, the electrostatic torque (T_e) is proportional to the square of the voltage difference across the air gap and inversely proportional to the square

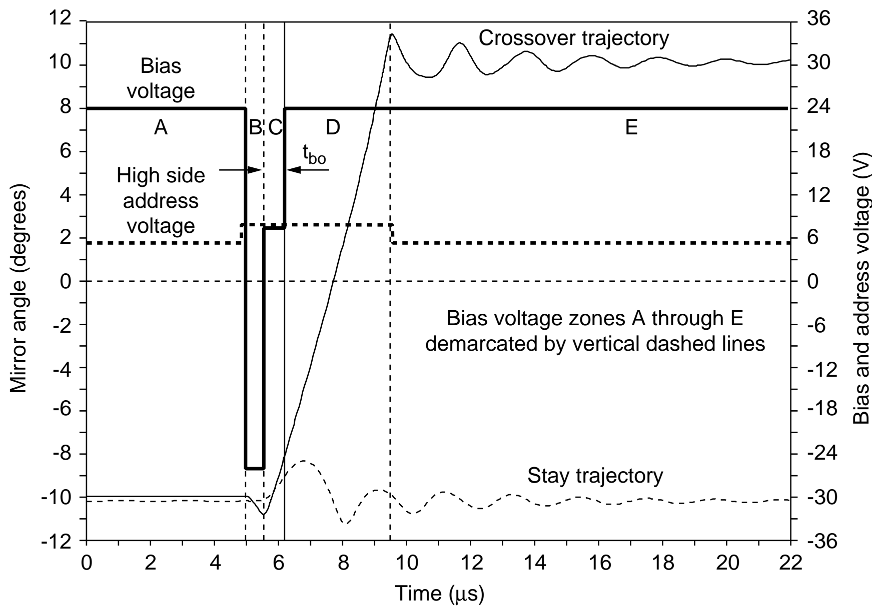

Figure 2. Mirror angle (left axis) and bias and address voltage (right axis) versus time. Vbias, high side address profile, typical pixel crossover and stay trajectories are shown.

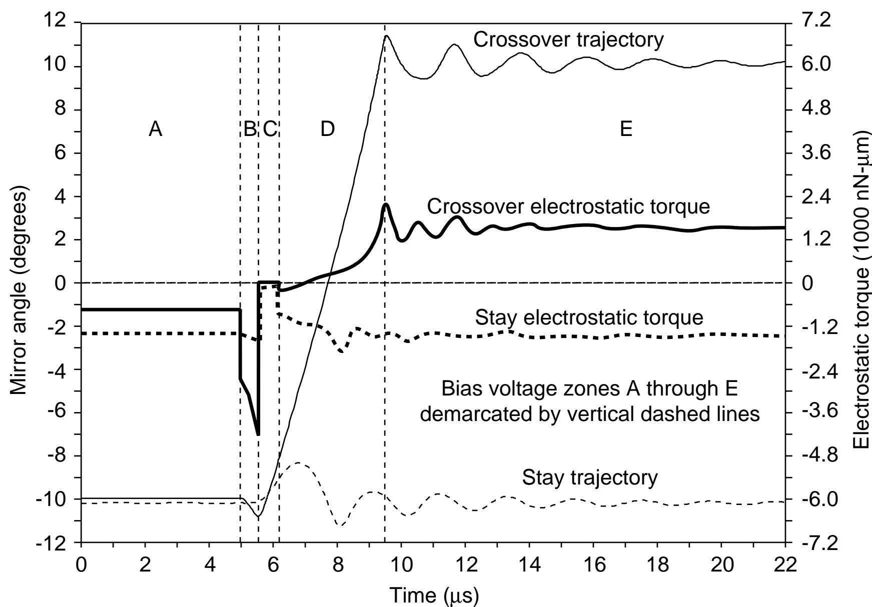

Figure 3. Mirror angle (left axis) and electrostatic torque (right axis) versus time. Crossover and stay trajectories with corresponding electrostatic torque.

of the air gap size. This gap size varies as the mirror rotates through its range of angular positions. Thus, for the purely theoretical case where ΔV is held constant and mirror angular position is varied, a mirror in a landed position (small air gap) will experience much more intense electrostatic torque than a flat state mirror (large air gap). The greatest electrostatic pressure contributions originate from the elemental areas (dA) that are in closest proximity to the address electrodes.

In both crossover and stay transitions, the same bias voltage is applied to the mirror, yet the dynamic angular responses are radically different. This is because address voltages for one transition are the complement of the other. To explain the differences in dynamic angular response, the bias voltage waveform is divided into five zones, labeled A through E, so that the bias and address voltages (and corresponding potential differences) can be described in detail. The values of these quantities for each mirror transition and zone are listed in *Figure 4*.

The portion of bias voltage waveform going from Zones A (+24V) to B (–26V) to C (+7.5V) is called the "bipolar reset pulse"[13] since it abruptly changes the sign of the bias voltage for the pulse duration of Zone B. The address voltage levels include not only 0 and 5V, but also a "stepped address"[14] or "stepped V_{DD}" value of 7.5V in Zones B, C and D. The combination of bipolar reset and stepped address has significant, but distinctly different, dynamic effects on the crossover and stay transitions, as shown in the discussion below.

Zone A is a setup time before dynamic excitation. The nominal V_{bias} level is set high enough to keep the mirror electromechanically latched so that it is not "upset" from its desired landed state by low-level dynamic disturbances. These are typically caused by loading the video data into memory at the onset of each DMD data load cycle. The address voltages are 0 and 5V, while the crossover and stay transitions have complementary values. The effect of this can be seen by the slightly reduced mirror angle for the crossover transition due to the smaller potential difference on the landed side in comparison to that of the stay transition. This becomes even clearer when one compares the electrostatic torque plots of the two transitions, where the crossover torque is significantly less than the stay torque. This reduced crossover torque causes less preload in the spring tips just before the reset pulse sequence, allowing greater spring tip deflection when the pulse excites the dynamic response of the mirror in Zone B. (See Reference 15 for the origin of the spring tip innovation.)

Zone B is critical to an understanding of the crossover and stay transitions. In this zone the V_{bias} waveform executes the bipolar reset pulse while the address voltage is simultaneously stepped to 7.5V. (Note: The most recent implementation of this waveform actually steps to 7.5V, a small fixed time interval ahead of the onset of the reset pulse. This was a solution to address concerns about waveform slew rates

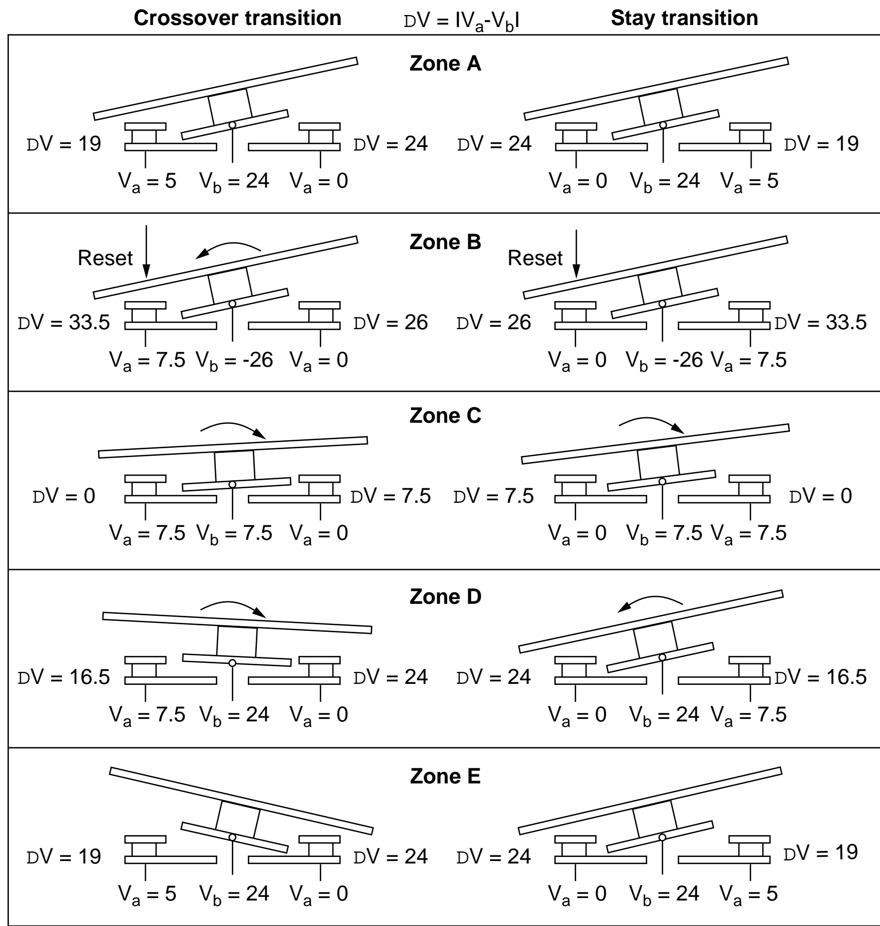

Figure 4. Applied voltages and potential differences for each zone of crossover and stay transition.

and propagation delays through the device during data load. The concern was that these factors might cause the address voltage to actually step high some period of time after the onset of the reset pulse, causing a loss of dynamic efficiency during crossover transitions.)

For the crossover transition, the sharp increase in electrostatic torque due to the combination of bipolar reset with stepped address draws the mirror forcefully down toward the address electrode on the landed side. This stores elastic strain energy in the compliant spring tips and hinge in preparation for a Zone C release of stored into kinetic energy. A comparison of the increase in landed-side potential difference, going from Zones A to B for the crossover and stay conditions, shows the former increasing from 19 to 33.5V and the latter only increasing from 24 to 26V (*Figure 4*). Thus, while the combination of bipolar reset and stepped address greatly amplifies the electrostatic loading for the crossover transition, it is basically unchanged for the stay transition.

The goal of Zone C is efficient release of stored elastic strain energy from Zone B as kinetic energy for crossover trajectories, without seriously upsetting the landed state of stay trajectories. For the crossover transition, the bias voltage on the mirror and address voltage on the landed side are set equal so the potential difference is zero. This causes the electrostatic torque on the launching side to be zeroed out. This is desirable for the crossover case because the instantaneous release of stored Zone B energy into angular kinetic energy has already propelled the mirror off the surface. Any electrostatic torque generated by the address electrodes at the launching side would only inhibit the mirror's departure.

By contrast, for the stay transition, the bias voltage on the mirror and the address voltage on the landed side are not equal. Going from Zone B to C, the stay transition experiences a significant drop-off in electrostatic torque that unloads the hinge and spring tips, causing the mirror to leave the surface momentarily. However, the angular speed with which the stay mirror leaves the surface is significantly less than that of the crossover mirror. The combination of the lower initial angular kinetic energy and the small retarding electrostatic torque toward the landed surface causes the mirror to be easily recaptured in Zone D when the bias voltage is set high once again.

The purpose of Zone D is the same for both stay and crossover transitions. It is to increase the potential difference and resultant electrostatic torque on the intended landing side so the mirror completes its transition to the desired optical state. Using stepped address loaded to the non-landed side reduces the counteractive torque component from that side. This helps the mirror favor the desired landing surface even more strongly.

The purpose of Zone E is to let the dynamic transients from the previous zones settle out, preparing the mirror for the next set of video data and resultant stay/crossover commands. In Zone E, the address voltage is lowered from 7.5V back to 5V. The lower voltage helps prevent upset of mirrors from their latched state when the address voltage is suddenly changed during the next address cycle. The bias and address voltages in Zone E are identical to those for Zone A, thus completing the logical cycle for dynamic addressing.

Using DMDPST to generate theoretical solution space maps

DMDPST can automatically simulate crossover and stay trajectories for a specified range and resolution of V_{bias} and Zone C time period (tbo) values. A pass/fail designation can be assigned as to whether a given trajectory's final destination is in agreement with the state commanded by incoming video data. This generates a theoretical "goodness" map for operational robustness called the "solution space" for a given design.[12] This solution space is the most critical design metric for grading pixel operational robustness. (Please refer to the DMD Superstructure Characterization article on page 75 of this issue for further information.)

A comparison of an experimental solution space map (for a typical pixel that has undergone little operational wear) versus the theoretical DMDPST-generated version is shown in *Figure 5*. The experimental version is generated by totaling the number of fails counted on a section of the device containing 12720 mirrors for which all trajectory transition types are tested. This statistical count is shown in each Vbias-tbo cell. If 127 mirrors fail to complete the correct transition, a failure rate of 1% is realized. The 0% and 1% experimental failure rate boundaries are delineated in Figure 5 with solid and bold dashed lines, respectively.

By contrast to the statistical count of the experimental map the theoretical version is made up of the resultant outcome of a single mirror (whose geometry and compliances are described by nominal fab process values). This single mirror undergoes stay

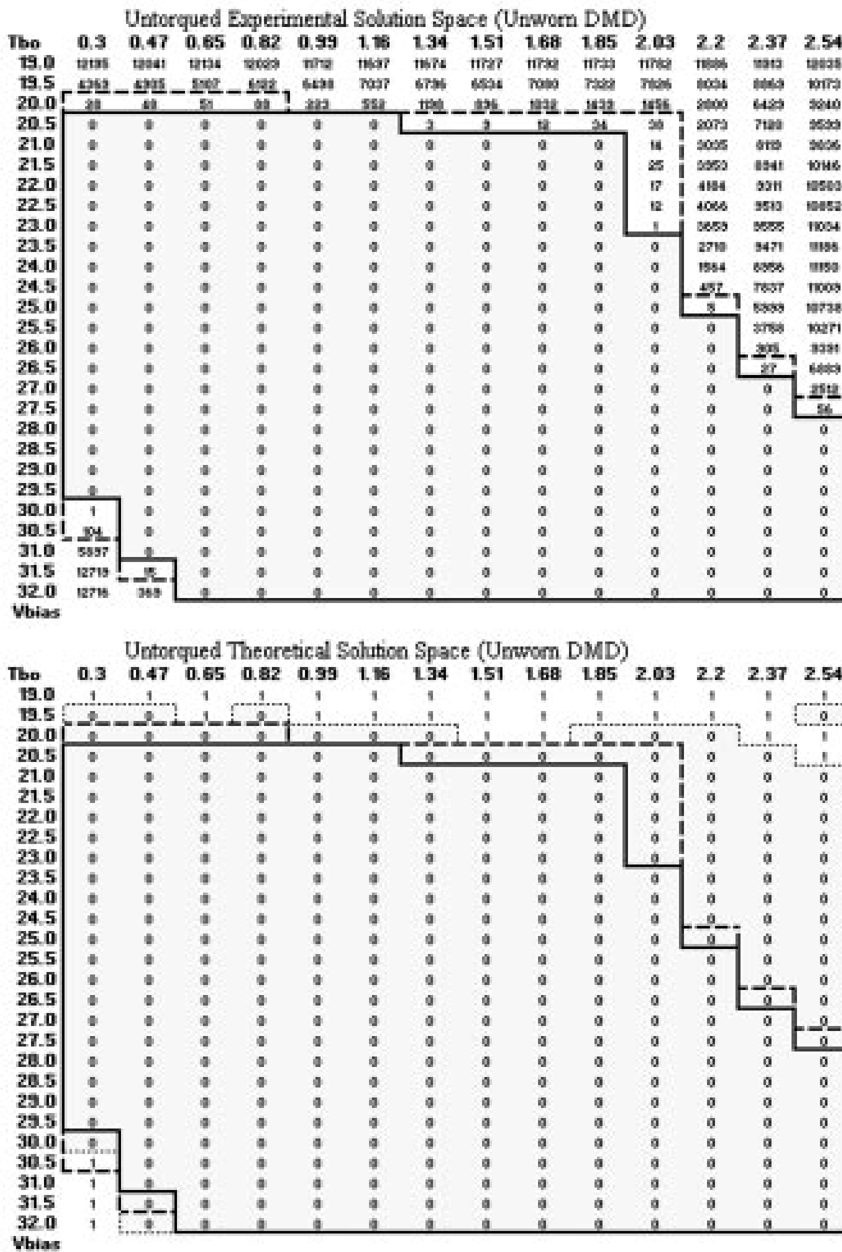

Figure 5. Experimental versus theoretical solution space map for unworn DMD (bold dashed boundary is 1% experiment failure rate).

and crossover trajectories tested under high and low surface adhesion at the spring tip landing sites. So the “failure rate” can only be described in terms of “1s” (fail) and “0s” (succeed). The 0% and 1% failure rate boundaries from the experimental case are superposed on the theoretical case for comparison purposes. It can be seen that upper and lower left solution space boundaries are in fairly close agreement for the theoretical and 1% experimental failure boundaries. This is important because these are the two most critical boundaries for assessing pixel operational robustness. There is some error in the theoretical version at the rightmost boundary. The likely cause of this lack of correlation has already been identified and a DMDPST improvement is in development. This boundary is also the least critical for assessing operational robustness of the pixel.

If a DMD pixel undergoes overly severe operational conditions in the presence of atypically high temperature environments, the pixel may become

heavily worn. This refers to a condition called “hinge memory,” whereby the torsion hinge takes on a permanent angular set to one side or the other when unloaded, thus changing the zero torsion load reference point. If hinge memory grows large enough it can result in an asymmetric, potentially resistive torsional load which “fights” the desired trajectory of the mirror. The experimental-theoretical comparison of the same DMD (previously shown in the unworn solution space map) after it is purposefully driven into a heavily worn state is shown in *Figure 6.* This is shown along with the 0% and 1% experimental failure rate boundaries superposed on the theoretical map. It can be seen that the upper boundary of the theoretical case lines up well with the experimental 0% failure rate boundary, while the lower left theoretical boundary lines up with the experimental 1% failure rate boundary. Again, the theoretical case compares rather poorly with the extreme right edges of the experimental boundaries of solution space.

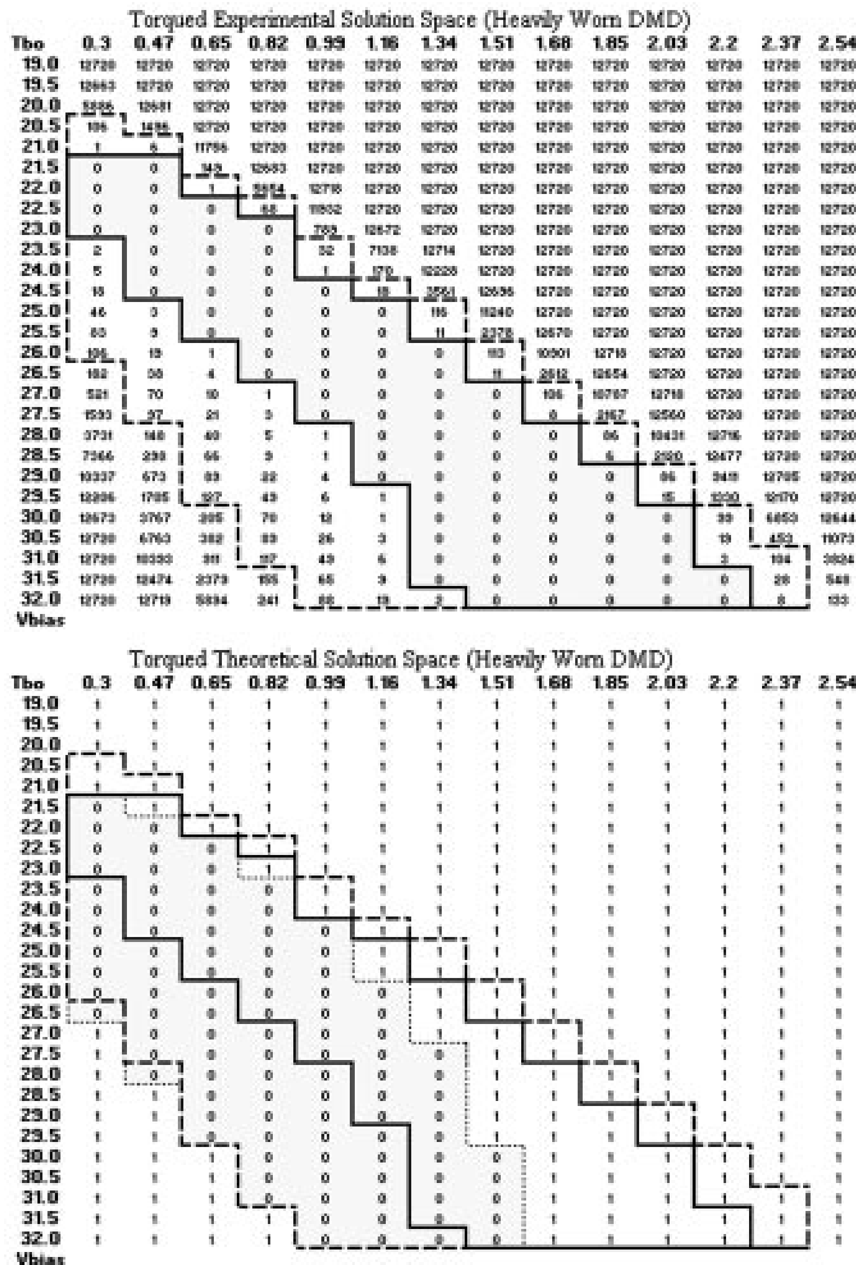

Figure 6. Experimental versus theoretical solution space map for heavily worn DMD (bold dashed boundary is 1% experimental failure rate).

In general, the quality of theoretical-experimental solution space correlation has been consistently strong in terms of the general range of Vbias and tbo values for which operation is deemed acceptable (i.e., general width of the space, its centering, triggering voltages for its boundaries and the types of failure mechanisms that occur on the boundaries of the space). However, as already noted, improvements to DMDPST have been identified to improve its correlation further.

The theoretical solution space maps shown in Figures 5 and 6 required 3024 total mirror trajectories (of the type discussed in the mirror dynamics section above) to build the resultant maps. The clock time for DMDPST's complete simulation of both maps (using the computer cited previously) was a total of 2.4 hours. No commercially available MEMS modeling code of which the author is aware is even close to achieving aggressive run times of this small magnitude without wholly compromising the fidelity of its results.

Using DMDPST to elucidate the physics: failed mirror trajectories

Many challenges must be overcome to ensure optimization goals of minimum angular transition time and impact energy, as well as maximum operational robustness and reliability, are met in a given unit cell design. (A detailed discussion of these challenges is outside the scope of this article. Hinge memory and stuck mirrors are discussed in Reference 3. Further discussion of these and other issues may be found in Reference 1.)

For illustrative purposes, a few examples of failed mirror trajectories (and one undesirable trajectory) are shown in *Figure 7.* Two stay trajectories have a Zone C time period (tbo) that is 33 and 63 longer than typical. The 63 case leads to a failed trajectory (wrong optical state) and the 33 case can lead to undesirable contrast ratio degradation as the mirror approaches the flat state.

Several cases of abnormal bias levels are shown in Figure 7 as well. Crossover and stay trajectories with bias voltages 10V below typical are illustrated. In the crossover case, low-level dynamic perturbation (loading the video data into memory at t = 0) causes the mirror to unlatch immediately because of extremely low bias voltage and become "upset" to the wrong optical state. In the stay case the post-reset Zone C unloading of the spring tips and hinge causes the mirror to leave the desired landing surface and its recapture is prevented by the reapplication of a Zone D bias level that is far too low. Finally, a crossover transition with bias levels 10V above typical is shown. In this case, the large compressive preload in the spring tips (which prevents them from storing much additional elastic energy during bipolar reset), combined with the very large electrostatic torque toward the launching surface applied just after release, forces the mirror to return to the launching side.

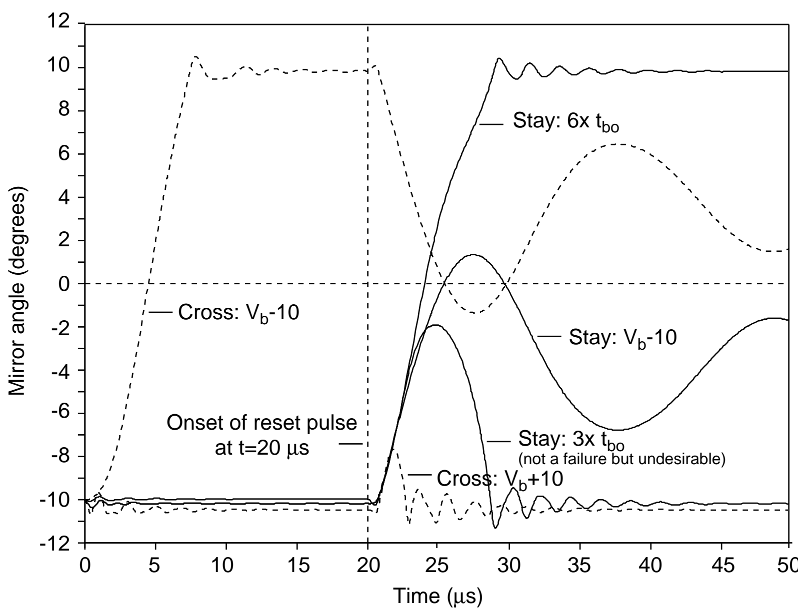

Figure 7. Mirror angle versus time. Examples of failed and undesirable stay and crossover trajectories.

Multidisciplinary impact on the DMDPST

A final characteristic of DMDPST's successful implementation is the degree to which it was influenced by many multidisciplinary interactions with DI staff throughout the organization. Numerous input/output variables, internal solution algorithms and future pixel design concepts have been developed to specifically address the concerns arising from these different technical areas. These include process development, manufacturability, yield improvement, low voltage electrical design, optimized mechanical layout, contrast ratio enhancement, waveform optimization, image quality assessment, low cost system design and integration. This has enabled the DMDPST to make more effective and wide-ranging contributions to Digital Imaging's current and potential success with Digital Micromirror Device applications.

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He received a B.S. in mechanical engineering from Bradley University in 1983 and an M.S. in mechanical engineering from Southern Methodist University in 1990. He joined TI in 1984, spending the bulk of his career prior to Digital Imaging performing structural dynamics modeling for a wide variety of defense programs in the Applied Mechanics section, as well as helping to develop customized dynamic analysis software and training other modelers in its use. Prior to his mechanical engineering education he received B.A. degrees in psychology and philosophy. He is a member of ASME and SPIE and is a registered professional engineer in Texas. ❑

Identifying and eliminating Digital Light Processing™ failure modes through accelerated stress testing

Abstract: *Reliability is a critical aspect of any commercial or consumer product. The challenge of developing reliable high technology products in a rapid-paced, highly competitive marketplace is discussed. Specific examples of accelerated stress tests applied to the Digital Micromirror Device™ (DMD™) and other Digital Light Processing™ (DLP™) components are reviewed.*

Delivering reliable products is always a challenge. Further constraints on product development include low cost, rapid time-to-market and limited samples for evaluation. To meet these challenges, innovative and aggressive reliability development techniques must be implemented. The approach implemented by Texas Instruments Digital Imaging program is referred to as "accelerated stress testing" or AST.

Although this is not a new concept, many people are unfamiliar with it. Similar techniques are known as accelerated life testing, highly accelerated life testing (HALT℠), step stress testing, reliability growth testing, and test, analyze and fix (TAAF), among others. Each of these reliability development techniques has the common goal to find potential failure modes as rapidly as possible providing opportunities to eliminate the failure mode prior to product delivery.

This article describes the Digital Imaging reliability development approach, provides examples of stress testing and summarizes the reliability of Digital Light Processing (DLP) products.

Introduction

DLP-based products consist of six major components including a light source, optics, color filters, a Digital Micromirror Device (DMD), electronics and a projection lens, as illustrated in *Figure 1.* The DMD consists of an array of micromirrors. Each micromirror is 16 microns square on a 17-micron pitch. *Figure 2* provides an exploded view of a micromirror. Micromirrors are individually addressable and rotate ± 10 degrees when an electrostatic field attracts the micromirror toward the underlying address electrode. Detailed information about DMD fabrication and operation is provided in reference 1.

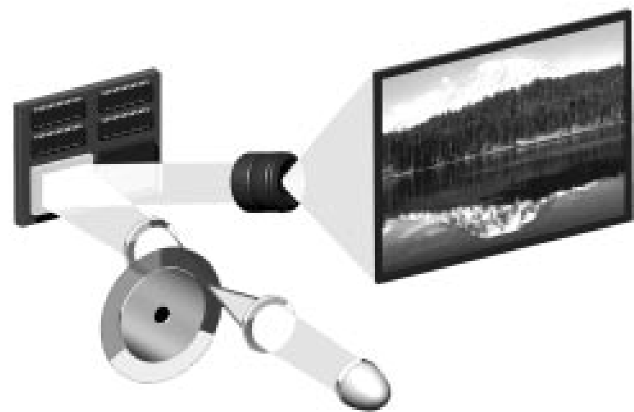

Figure 1. Illustration of a DLP system.

Accelerated stress testing approach

In its simplest form the accelerated stress testing (AST) approach implemented by Digital Imaging consists of five (5) steps:

1) Identify potential product weaknesses
2) Increase test stresses in order to force weaknesses to failure
3) Investigate the root cause of the failure
4) Implement appropriate corrective actions

Mike Douglass and Andrew Sontheimer

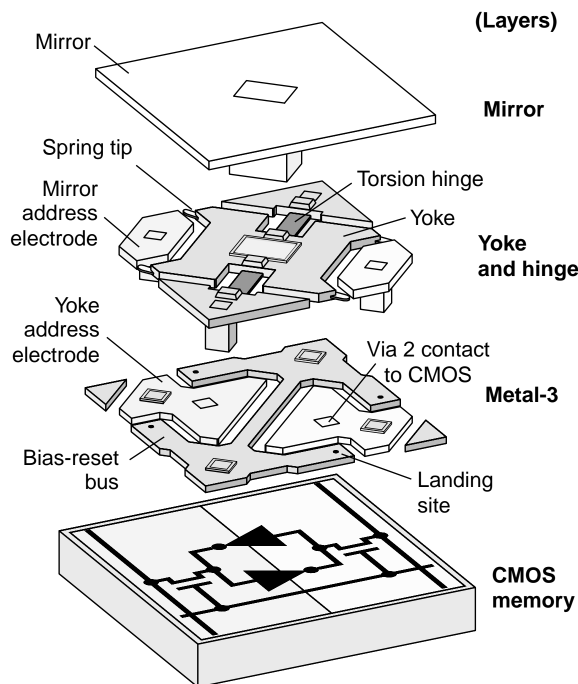

Figure 2. Exploded view of a DMD micromirror.

5) Repeat items two through four for each weakness until it is no longer cost-effective to implement additional corrective actions

At this point, the inherent design weakness of the product is usually well beyond the products' operating limits.

The following paragraphs describe some of the stress tests used to improve, verify and demonstrate DMD reliability. The sections following the discussion about DMD reliability address the AST approach to other levels of DLP electromechanical subassemblies.

Identifying and accelerating potential DMD failure modes

The first application of accelerated stress testing by Digital Imaging occurred with the DMD. In 1992, when the DMD was still under development, little was known about DMD reliability. The reliability department organized an informal failure mode and effect analysis (FMEA) by bringing together a group of DMD experts. Since the DMD materials and processes were (and still are) similar to other semiconductor devices[1], the group was joined by semiconductor experts from throughout Texas Instruments. These experts brainstormed possible ways a DMD could fail, identifying several dozen potential failure modes that included:

- Hinge fatigue (mirrors wearing out due to metal fatigue in the hinges)
- Mirrors breaking (due to handling, shock and vibration)
- Hinge memory (mirrors becoming nonfunctional due to metal creep)
- Nonfunctional mirrors (mirrors that stick or otherwise fail due to billions of landings)

For each failure mode identified during the FMEA, a test was designed to measure its potential risk. The tests varied in duration, ranging from hours to several years before confirming results would be available. There was not enough time to use normal operating stress levels, resulting in waits ranging from months to years for results. The program also needed to produce rapid results to help establish priorities for the emerging Digital Imaging business, including answering whether the DMD was reliable. If it was not reliable, what were the reasons? Could design and/or process changes improve device reliability? For these reasons it was imperative to apply acceleration factors to several tests. Accelerated stress testing contributed essential information to address these important issues.

Rapid mirror switching—hinge fatigue

One of the most critical failure modes identified during the FMEA review was the possibility of mirrors breaking due to hinge fatigue as a result of the hinges twisting and bending. Normal operation in a DLP application switches the micromirrors once every 200 to 300 microseconds. To achieve a five-year lifetime (assuming only 1000 operating hours per year), the micromirrors would need to switch over 90×10^9 times. No known microelectromechanical system (MEMS) had ever achieved such lifetimes.

To address this concern a simple accelerated stress test was designed. The test cycled DMD micromirrors on and off every 20 microseconds, accelerating this failure mode by a factor of 10. Within several weeks the test had already surpassed 90×10^9 cycles and eventually reached 1 trillion cycles without failure.

More recently, this test was repeated. The devices again surpassed 1 trillion cycles and continued beyond 1.7 trillion cycles without failure. This test has demonstrated at least 10 years of normal use in *any* application and over 50 years in *most* applica-

tions. Interestingly, the devices on this test have accumulated over 2 x 10^{18} (two quintillion) mirror cycles and are still on test with no evidence of hinge fatigue!

The results of this accelerated stress test were critical to our understanding of DMD reliability. Although a failure was not identified nor accelerated, the test was able to quickly demonstrate that hinge fatigue was not a concern for reliable device operation. This allowed Digital Imaging to focus on other priorities and concerns.

Shock and vibration—handling and package integrity

Considering the microscopic size of the micromirrors, the FMEA questioned if mirrors could easily break during assembly, handling or use in a DLP product. To address this concern a sequence of mechanical tests was extracted from the Texas Instruments Semiconductor Qualification Procedure. The test consisted of mechanical shock (1500g, 0.5 millisecond pulses), vibration (20g peak, 20 to 2000 hertz), and acceleration (10,000g centrifugal force).

With the exception of some early package integrity failures and an occasional loose particle inside the device package, all micromirrors were undamaged and unaffected by this series of testing. To further investigate the mechanical integrity of the DMD, a mechanical shock test was designed to increment shock levels to the point of failure. Shock levels of 1500g, 3000g, and 5000g resulted in no damage to the micromirrors or the package. At 10,000g, package damage was evident and the test was stopped. Similar robust performance was confirmed through repeated vibration and acceleration testing.

This series of accelerated stress tests demonstrated that the micromirrors were mechanically robust. The package damage occurred at stress levels well above the design requirement. A particle reduction program addressed random loose particles in the package. This sequence of stress tests provided rapid feedback to the DMD process engineers resulting in a dramatic reduction of particles.

High temperature operation—hinge memory and nonfunctional (stuck) mirrors

During early development testing it was observed that devices failed more rapidly at high temperatures. This was noted as a potential failure mode during the FMEA. DMDs were characterized at various temperatures ranging from 0C to +85C and nonfunctional micromirrors were strongly correlated with high operating temperature. The root cause of the failures was attributed to metal creep in the hinge material and was referred to as “hinge memory.” For example, a micromirror continually addressed toward the offside (that is, when the micromirror appears dark in a projected image) will exhibit a small amount of residual tilt toward the offside when all electrostatic fields are removed. The micromirror will continue to operate properly until the residual tilt accumulates and exceeds approximately 35 to 40% of the 10-degree rotation angle. At this point, the micromirror will only rotate to the offside and appear as a dark pixel on a projected image.[3, 2]

Once the correlation was found between hinge memory and high temperature, accelerated stress tests were designed to take advantage of this knowledge. A life test at high temperature and high duty cycle (the micromirrors always addressed toward one side) forced DMDs to fail within a few hours. This allowed rapid evaluation of a series of new materials and processes. Within several months tests identified hinge materials exhibiting less metal creep and therefore longer lifetimes due to hinge memory. Additional testing helped develop improved material processes and a more effective way to dynamically control the micromirrors. In a relatively short development period, hinge memory lifetime increased dramatically, exceeding 100,000 hours.

DMD reliability demonstration

References 2, 3, and 4 provide more detail on the failure modes discussed above as well as other DMD failure mechanisms. Accelerated stress tests greatly increased our learning cycles by shortening the time required to realize experimental results. We also were able to make rapid decisions about proposed design and process changes. Consequently, the DMD entered the commercial marketplace with great expectations for high reliability. To date over 100,000 DLP systems are in use throughout the world and the DMD is proving to be even more reliable than expected. Recent calculations demonstrated a DMD mean time between failures (MTBF) of over 119,000 hours. Life tests, as discussed in reference 2, have demonstrated lifetimes exceeding 100,000 hours under normal operating conditions.

Application of accelerated stress testing to DLP systems

The success of AST on DMD reliability lead to its application on other DLP assemblies. Early testing on

prototype DLP engines indicated very promising product reliability.[5] The following sections describe examples of follow-on stress testing activities as well as lessons-learned on a variety of products.

Mechanical shock

One of the first stress tests applied to a DLP product was mechanical shock. There was concern that the critical alignment of DLP components (light source, optics, color filter, DMD, electronics and projection lens) would degrade during assembly, handling and use.

To *simulate* severe handling and *stimulate* any mechanical weaknesses, a series of mechanical shocks (illustrated in *Figure 3*) were applied to the original VGA (640x480-resolution) design. The tests started with pulses of 5G, 11 milliseconds in all six axes and progressed to 25G, 11 milliseconds with no failures or indications of degraded operation. At 30G the test caused a glass color wheel filter to chip. (This DLP projector with one DMD used a spinning color wheel with red, green, and blue filters to create sequential color.) Further investigation found the color wheel assembly improperly supported and free to move when excited in the Y-axis.

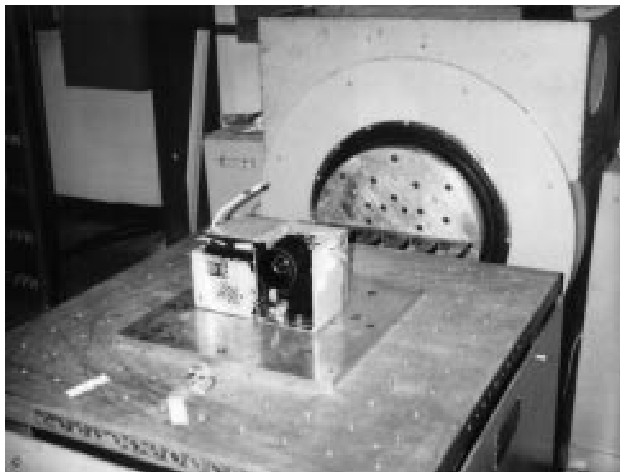

Figure 3. DLP engine on an electrodynamic vibration table for mechanical shock testing.

Shortly after the investigation started, customers reported a small number of their products exhibited chipped color wheel filters upon receipt of the DLP engine. Apparently, the units were being subjected to mechanical forces equivalent to 30G, 11 milliseconds in the shipping process. Fortunately, Digital Imaging engineers had already identified the source of failure through AST and had corrective actions nearly implemented. The support structure of the color wheel assembly was improved and the shipping containers redesigned to provide better protection. Customer failures attributed to chipped color wheels were eliminated and overall mechanical robustness of the product was enhanced.

To obtain fundamental information about DLP mechanical integrity, mechanical shock AST was continued with a goal of reaching 50G. The testing identified additional weaknesses resulting in further design modifications. The testing continued through 50G, 8 milliseconds with no failures or degradation. This series of testing was stopped when it eventually achieved 105G, 5 milliseconds in all six axes. The product remained fully functional through 105G although the zoom lens was slightly deformed. The test was ceased due to the limitations of the mechanical shock table being used.

Several essential lessons-learned from mechanical shock AST include:

- Earlier testing would have highlighted weaknesses prior to shipping products
- Test results correlated well with reported customer failures
- Using AST, rapid feedback was provided to the Digital Imaging design team resulting in rapid corrective action and closure
- AST-based mechanical shock improved the mechanical integrity of follow-on DLP products and designs

Power cycling

Another early example of stress testing DLP systems was the application of rapid power cycling. Early prototype systems were placed on life tests to simulate actual operation. This test consisted of a power cycle (the system was automatically turned off, then on again) once every three hours. A computer controlled the power cycling and also recorded failure codes when a system failed to turn on. A review of life test data indicated that there were some intermittent failures but no trends were apparent. There were so few power cycle attempts that no statistically significant conclusions could be drawn.

To learn more about possible power cycling failures the life test was redefined and modified. Its new purpose was to *stimulate* failure modes, not *simulate* possible operating scenarios. Instead of a power cycle once every three hours (eight times per day), the new

life test performed a power cycle once every minute. Within the first day, the test accumulated 1440 power cycle attempts on each system under test. The data clearly showed that there was one failure for every thirteen power-on attempts. In addition, the data was statistically significant and demonstrated numerous causes of failure originating from firmware errors, power supplies, lamps, miscellaneous electronics, and test equipment.

With this detailed information available, the Digital Imaging design team was able to assign detailed actions and systematically eliminate the root cause of each failure. The rate of failure was rapidly reduced to one intermittent failure for each 800 attempts and eventually reached the point where the tests consistently accumulated thousands of power cycles with no failures.

The lessons learned from the previously discussed mechanical shock AST are also applicable to the power cycling stress testing. By stimulating and eliminating failure modes, production failures can be minimized, customer failures avoided, and learning cycles increased, resulting in a more reliable product available to the market sooner. In this example and subsequent development efforts, power cycling AST has resulted in DLP products with more robust electrical designs.

Temperature stress testing

A very common stress test uses temperature as an acceleration factor. Digital Imaging used a modified version of the typical temperature-based life test to more rapidly accelerate and identify product weaknesses. Temperature stress testing is performed at the engine, subsystem or assembly level during the development process to identify and eliminate design weaknesses. It is performed in three steps.

Step 1—High temperature step stress

The test sample is operated in a temperature chamber where it is subjected to increasing ambient temperatures until failure is observed. Dwell and transition times are modified based on time estimates needed to reach thermal stability and the capabilities of the temperature chamber. A typical test scenario is:

- Operate the unit in a temperature chamber at +40°C (maximum specified operating temperature) for two hours allowing the chamber and unit under test to achieve thermal equilibrium
- Perform an operational test (acceptance test) at the end of the thermal soak
- Increment the temperature by 5°C to +45°C
- Dwell at this temperature for 10 minutes and perform an operational test
- Continue testing until a failure is observed
- When a failure occurs, a team determines the cause of failure and takes appropriate action
- If the failure is due to a device that provides protective thermal shutdown, the shutdown function is disabled and testing continues

Step 2—Low temperature step stress

This test is performed much like the high temperature step stress test except the test is started with a soak at the lower operating temperature limit (typically 0°C or 10°C). The temperature then decrements by 5°C with each successive test.

Step 3—Extreme temperature cycling

The test sample is operated in a chamber with the temperature rapidly cycling between two extremes. Performance is monitored throughout testing and temperature cycling continues until a failure is observed. Temperature extremes are based on results from the previous step stress tests. They are chosen to be slightly less stressful than temperatures resulting in failures during high and low temperature step stress tests. For instance, if the high temperature tests resulted in failure at +80°C, then a high temperature extreme may be set at +70°C. Similarly, if the low temperature tests resulted in failure at -50°C, then the low temperature extreme may be set at -40°C.

An application of temperature stress testing

Temperature AST was recently applied to a new DLP product in the large-venue product line. A projector engine with XGA (1024x768) resolution included three DMDs to achieve superior brightness and image quality. The engine development program employed temperature stress testing during system development to verify and gain confidence in system performance over temperature. The development effort was for a drop-in replacement of the 500W 3-DMD SVGA (800X600) engine with XGA (1024X768) resolution. The 500W engine consisted of a base plate, lamp power supply, 3-DMD light tube assembly and flex cables connecting the DMDs to the formatter memory and control boards, image processor, signal converter and motherboard. *Figure 4* shows an engine ready to be tested in a temperature chamber. Temperature stress testing was performed on a sample of one unit. The observations are listed in *Table I.*

Figure 4. Large-venue XGA 500W engine installed in temperature chamber for temperature testing.

The results of these tests showed that the design had very good margin with regard to system temperature specifications. All anomalies occurred outside of the +10°C to +40°C specification limits. Noise on the image was observed while operating the unit at +65°C. These results formed the basis for a design change necessary to increase noise margin on a phase locked loop (PLL) clock circuit. The high temperature step stress test was discontinued after a lamp power supply failure occurred at +75°C, which is 35°C above the upper system operating temperature limit of +40°C. The low temperature step stress test resulted in no failures until a lamp power supply would not stay energized at –50°C, 60°C below the lower operating specification of +10°C! A single failure was observed in the second cycle of extreme temperature cycling from -40C to +50C due to a lamp power supply shut down. The lamp power supply was replaced and an additional 6 temperature cycles were completed without failure. A second unit completed an additional 24 temperature cycles from -40C to +50C with no failures. The testing also verified successful operation of thermal protective devices shutting down the system in case of over- heating.

Following completion of temperature stress testing, the engine passed a rigorous image quality evaluation, requiring only minor adjustments to converge the three DMDs. While a DLP product will not encounter these temperature extremes in real life applications, the results provide a high degree of confidence that the system will work under the more benign conditions expected in the actual use environment.

Voltage stress tests

Voltage stress testing is a method used to determine a design's tolerance to fluctuations in power supply voltages. The testing employed by Digital Imaging consisted of:

- Verification that the unit under test met performance requirements under any combination of power supply voltages (within specification limits)
- Testing to determine operational limits of critical supply voltages (beyond specification limits)

For the first test, a matrix of system-level power supply voltages could be compiled to evaluate each

Table I. Observations from 3-DMD XGA temperature stress testing.

Test	Temp.	Finding	Resolution
High temperature step stress	+55°C	Lamp power supply shut off	Verified protection circuit function. Disabled to continue test
High temperature step stress	+65°C	Noise on image	Changed design to improve filtering on formatter PLL clock circuit
High temperature step stress	+70°C	Parked mirrors	Verified protection circuit function. Disabled to continue test
High temperature step stress	+75°C	Lamp power supply shut off	Showed good margin to +40°C specification limit – discontinued test
Low temperature step stress	-10°C	Parked mirrors	Verified protection circuit function. Disabled to continue test
Low temperature step stress	-50°C	Lamp power supply shut off	Showed good margin to +10°C specification limit – discontinued test
Extreme temperature cycling	+50°C	Lamp power supply shut off	Survived numerous temperature cycles

combination of minimum and maximum voltage tolerances. A test would then be performed for each combination of voltages. If the unit under test had only a few supply voltages (i.e., +3.3 VDC, +5 VDC and +12 VDC), testing every combination of limits could be done with 2^3 settings of the supply voltages as in *Table II.*

Table II. Matrix to test every combination of high and low specification values on three power supply voltages.

Test run	+3.3 VDC ± 5%	+5.0 VDC ± 5%	+12 VDC ± 10%
1	+3.135	+4.75	+10.8
2	+3.135	+4.75	+13.2
3	+3.135	+5.25	+10.8
4	+3.135	+5.25	+13.2
5	+3.465	+4.75	+10.8
6	+3.465	+4.75	+13.2
7	+3.465	+5.25	+10.8
8	+3.465	+5.25	+13.2

Systems or subsystems that are more complex may use a large number of supply voltages. Verification of full system performance should also include performance over a variety of temperature conditions. Exhaustive testing of every combination of voltage and temperature would require a significantly large number of tests. If the system had five DC supply voltages, testing every combination requires 2^5 or 32 settings of supply voltages. Performing these tests at room, hot and cold temperature would increase the total number of tests to 96. If exhaustive testing were too time-consuming, the concept of orthogonal arrays may be used to reduce the number of tests. For example, if a system had five supply voltages, operation over the supply voltage tolerances may be verified with only 16 settings using a half-factorial orthogonal array as in *Table III.*

Testing within the specified voltage tolerance range of the system power supply is inadequate to ensure performance when production variation is introduced. To address this, voltage stress testing beyond specification tolerances may be applied. One method is to increase and decrease a single supply voltage until failure occurs while other supply voltages are held constant (usually at nominal values). When a failure is observed, the design team analyzes the cause of failure and either implements corrective actions to increase margin or concludes that adequate margin has been demonstrated to meet performance requirements. Voltage stress tests are often repeated over temperature or combined with accelerated temperature stress testing to further enhance the reliability of the system.

Timing margin improvements realized through accelerated stress testing

Voltage stress testing was applied during the 3-DMD

Test run	+5.0 VDC Digital +0.25 V, -0.1 V	+5.0 VDC Analog ± 5%	-5.0 VDC Analog ± 5%	+3.3 VDC Digital +0.165 V, -0.1 V	+12 VDC Analog ± 10%
1	+4.9	+4.75	-5.25	+3.2	+13.2
2	+4.9	+4.75	-5.25	+3.465	+11.8
3	+4.9	+4.75	-4.75	+3.2	+11.8
4	+4.9	+4.75	-4.75	+3.465	+13.2
5	+4.9	+5.25	-5.25	+3.2	+11.8
6	+4.9	+5.25	-5.25	+3.465	+13.2
7	+4.9	+5.25	-4.75	+3.2	+13.2
8	+4.9	+5.25	-4.75	+3.465	+11.8
9	+5.25	+4.75	-5.25	+3.2	+11.8
10	+5.25	+4.75	-5.25	+3.465	+13.2
11	+5.25	+4.75	-4.75	+3.2	+13.2
12	+5.25	+4.75	-4.75	+3.465	+11.8
13	+5.25	+5.25	-5.25	+3.2	+13.2
14	+5.25	+5.25	-5.25	+3.465	+11.8
15	+5.25	+5.25	-4.75	+3.2	+11.8
16	+5.25	+5.25	-4.75	+3.465	+13.2

Table III. Half-factorial orthogonal array for applying five DC supply voltages over their tolerance ranges.

XGA development program to accelerate failure mechanisms early in the design process. The 3-DMD XGA electronics use five DC supply voltages: +5 VDC and +3.3 VDC for digital logic, ± 5 VDC for analog video signal processing and +12 VDC for cooling fans and DMD reset voltage generation. A half-factorial orthogonal array was selected to investigate the effects and interactions of voltage tolerances.

The array summarized in Table III includes combinations of high and low specification limits on DC power supply voltages. The system passed acceptance tests performed for each combination of supply voltage settings in Table III and passed at low and high system temperature specifications (+10C and +40C). However, the design team was not satisfied with just performance to specification, and applied AST methods to discover the limits of the design. Each supply voltage was individually varied while the others were held constant.

System performance was continuously monitored as in *Figure 5.* During one such test of the +3.3 VDC digital logic supply voltage operating at +40C, a noise pattern was observed on the image with the +3.3 VDC slightly below specification at +3.1 V. While this is below the system specified minimum voltage of +3.2 VDC, the design team concluded that it did not provide adequate margin for production variation. An analysis of the problem found that a timing parameter was being violated at these conditions. The formatter assembly was modified to provide additional timing margin. This simple modification significantly improved margin on the +3.3 VDC supply voltage while providing confidence the system will tolerate power supply variation in production.

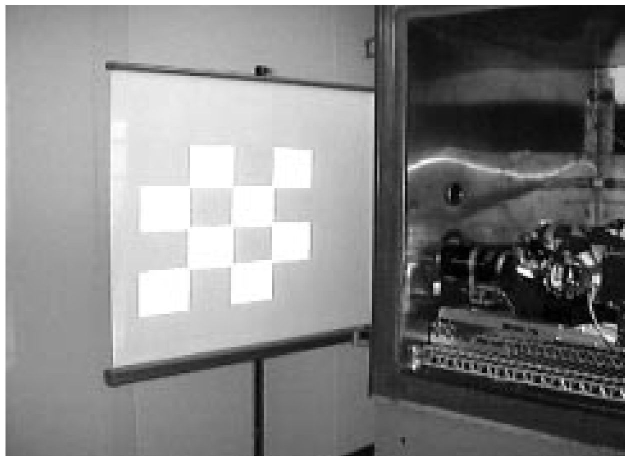

Figure 5. System performance continously monitored during temperature and voltage tests.

Conclusion

The use of stress testing beyond specification levels provides significantly more information than just whether a design passes or fails. By testing designs to the point of failure, Digital Imaging can better understand how systems fail and implement designs that are more robust. In addition, once failure modes are identified through stress testing, designs can be readily evaluated by using the stress test to accelerate the known failure mode.

This article provided several examples of how AST was applied to DMDs and DLP technology. There are numerous other AST examples addressing other failure modes. Using AST, DMD reliability has been improved dramatically. DMD lifetimes are estimated at over 100,000 operating hours and over 1.7 trillion mirror cycles. The successful implementation of AST on DMD development lead to a similar approach on other DLP systems with equally successful results.

Several important findings and conclusions from the DLP accelerated stress testing program include:

- Development testing needs to *stimulate* failures not *simulate* use
- Early testing is capable of highlighting design weaknesses prior to shipping products
- Testing correlates well with customer failures
- Using AST, rapid feedback was provided to the Digital Imaging design engineers resulting in faster corrective action implementation
- AST deployment has improved mechanical integrity, thermal robustness, electrical performance stability and overall reliability of DLP products.

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