Exhibit 4

Brief Description of Circuit Functions

1. Video pre-amplifier:

The TDA4886 (7301) is a monolithic integrated RGB pre-amplifier for colour monitor system with I2C bus control and OSD mixer. In addition to bus control beam current limiting. The signal are amplified in order to drive output driver LM2439 (7701. Individual black level control (pin 17/20/23 0f 7301) with positive feedback for cut-off control.

The RGB input signals with nominal signal amplitude of 0.7Vb-w are capacitively coupled (2308/2310/2311) into TDA4822_COSMIC IC (7302) from a 75 Ω (3301/3302/3303) source and output from pin19/21/23 of 7302 into TDA4886 actively clamped to an internal DC Voltage during signal black level by CLBL (pin 5) signal from deflection controller.
A fast signal blanking is driven by CLBL signal.

The input signal related to the internal reference black level can be simultaneous adjusted by contrast control via I2C bus with 6 bits DAC. For white point adjustment the individual for three channels gain control are driven by I2C bus with 6 bit DAC too.

In the output stage the nominal input signal will be amplified to 2.8Vb-w output color signal at nominal contrast and maximum gain. Individual out put clamping is to set the reference black level of the signal output to a value which corresponds to the extend cut-off voltage of the CRT cathodes, all feedback reference are driven by I2C bus.

The output signal from pre-amplifier R (pin19), G (pin16) and B (pin22) are sent to LM2439 to have around 40Vp-p amplitude, which are AC coupled to the CRT and need to be clamped to cut-off level. These are achieved by the black level clamp circuits 7721, 7722, 6721, 6722, 2724, 3723, 3724, 3725, 3726, 3727, 3786 for Red channel, the rest channel are identical to it and all of three channels are control by TDA4886 (R: pin 19, .G: pin16, B: pin 22).

The OSD signal are inserted during fast blanking active period, the OSD and fast blanking signal are generated by OSD IC MTV018-27.

Actually, the COSMIC IC TDA4822 just only by-pass the RGB video signal and it will enhance the gain of video around 40% while allp the lighfram function.

2.0. Micro controller:

The micro controller WT62P2(7801) is monitor micro controller with DDC interface to the PC host. The internal built in hardware can detect sync. presence for the VESA DPMS standard of various display mode with separated (pin 40: H 41; V) . The output pin33/34 can be used to control the video and deflection function of the monitor.

Besides to control two bus driven IC TDA4841 and TDA4886 via I2C bus , micro controller output still handle the rest function as V-DC shift, rotation, brightness, power management , degaussing, LED color, H-unlock detector, ABL, s-cap switch, H-Dc shift, and H-linearity. After alignment the data are stored at EEPROM 7804.

3. Deflection controller:

The TDA4841 is a high performance and efficient solution for autosync monitors. All functions are controllable by I2C bus. TDA4841 provides synchronization processing,

horizontal and vertical with full autosync capability, it provides extended function e.g. as a flexible B+ control. and extensive set of geometry control facilities.

The HSYNC (pin15) is the input for horizontal synchronization signal which can be TTL separate or composite sync with positive or negative polarity. The horizontal oscillator capacitor at HCAP (pin 29) for optimum jitter performance the value of 10nF must not be changed. The given value is widely synchronised from 30KHz to 86KHz.

PLL1 phase detector compares the middle of horizontal sync with a fixed point on the oscillator sawtooth voltage. The PLL1 loop filter is connected to HPLL1 (pin 26). Via register HPOS the I2C bus allows a linear adjustment of the relative phase between horizontal sync and oscillator sawtooth (in PLL1 loop). Via registers HPARAL and HPINBAL correction of pin unbalance and parallelogram is done by modulating the phase between oscillator sawtooth and horizontal flyback (in loop PLL2).

The PLL2 phase detector is similar to PLL1 detector and compares the line flyback pulse at HFLB (pin 1) with the oscillator sawtooth voltage. The control currents are independent of horizontal frequency. The PLL2 detector thus compensates for the delay in the external horizontal deflection circuit by adjusting the phase of HDRV (pin8) output pulse.

EWDRV (pin 11) provides a complete EW drive waveform. The components horizontal pincushion, size, corner correction, and trapezium correction are controlled by the registers HPIN, HSIZE, HCOR and HTRAP.

The VSYNC (pin14) is the input for vertical synchronization signal it can be TTL separate or extract from composite sync. with positive or negative polarity. The widely synchronization range from 50 to 160Hz.

The amplitude of the differential output currents at VOUT1 and VOUT2 can be adjusted via register VSIZE. Register VPOS provides a DC shift at the sawtooth output VOUT1 and VOUT2 (pin 13 and pin 12) and the EW drive output EWDRV (pin11) in such a way, that the whole picture moves vertically while maintaining the correct geometry.

The horizontal moiré (also known as video moiré) can be cancelled by controlling register HMOIRE and cancelled vertical moiré (scan moiré) by controlling register VMOIRE.

The B+ function block cab be used for buck converter in feed forward mode. It provides a frequency independent pulse width to control the deflection circuit.

4. Horizontal deflection:

The horizontal output signal 7501 pin 8 (limited at very low amplitude around 1.4Vp-p) directly fed to driver stage 7605, after boost to about 80Vp-p and amplifies current drive capability it drives output transistor 7606 to reach expected deflection current. The horizontal linearity correction circuits is composed by 4 segment S-cap. switch (7262, 7263, 7264, 7266) and one controllable linearity coil 5601 to get optimised linearity

The B+ control output signal is modulated with geometry control and size control signal together, it directly fed to buck converter 7603 via buffer stage 7601, 7602 to supply an adequate deflection voltage to output stage. The horizontal raster position control circuits is composed by 5612, 6604, 6605, 7607, 7608, 3606, 3604 from MCU H-DC shift pin2 pwm control 7617 to reach right center position. To correct the tilt symptom while monitor facing

the different direction or operating at various place, the rotation coil (plus control ckt. 7621-A, 7683, 7682…) is need to against the magnetic field changing.

5.0 EHT generator and Vertical output stage:

The EHT generator supplies 25KV anode voltage to picture tube. The generator is fully combin from the horizontal deflection input from 7501 pin6 B+ control.
Pass through 7601/7602 and DC/DC converter 7603 180v voltage source driver the LOT to get the needed EHT /G2 and G1 voltage.
The generator is protected against over beam current (over load) and over voltage (x-ray), over load protection, it is activated if anode voltage exceed 27.5 - 29.5 KV, the x-ray protector will be triggered and switched off the B+ control output of 7501 immediately.

EHT generator also supply tertiary voltage for concern circuits like:

-178 Vdc	: for spot killer
+320Vdc	: for vertical dynamic focus
+600Vdc	: for VG2 control.

TDA 4841 vertical differential output pin 12/13 fed to 7401 TDA8172 input pin1/7 and boost to expected deflection current around 1.5Ap-p.

6.0 Power supply:

The power supply works at a fixed frequency about 57KHz in flyback mode and suitable for universal line input 90-264Vac. The proper PTC for the degaussing part, it working automatically at switch on for about 6 seconds or pushing an external button via OSD under PTC cold condition.

The mains voltage, rectified 6101 and filtered 2106 (150μF/400V), is applied to the power transformer 5113 which switching the power transistor 7101, transfer the energy to secondary side. Besides, an auxiliary voltage is obtained from the primary side to supply the power controller TEA1504.

The hard start current is supply by rectified mains. The power transformer secondary side rectified and filtered out defined voltages : +190V, +78V, -6.3V, +12V, -12V,(+8V, +5V are drop out from +12V).
+190V is sensed and subtracted to a stabilized reference voltage; the error signal is amplified and send to TEA1504 via phtocoupler, where it is compare with ramp waveform to keep constant voltage output by modulating duty cycle.

The primary current is sensed by the resistor 3121,3138, when current increase to over current threshold point then power shut down immediately. When a short circuits occurs on the outputs voltage (+190V, +78V,±12V …), the primary current increase in such a way that the power supply turns off and secondary will into burst-mode.

Power management off mode is directly short circuits 7116 turn onand let power supply enter burst mode, it delivery out very low power (less than 5 watt).