BCM43235

2.4 GHz 802.11n MAC/PHY/Radio Chip

GENERAL DESCRIPTION

The BCM43235 is a single-band (2.4 GHz) IEEE 802.11n-compliant MAC/PHY/Radio complete system-on-a-chip with a 2.4 GHz internal PA. The device enables the development of USB 2.0- or HSIC-based 802.11n WLAN client and router subsystem solutions. The BCM43235 is targeted for all WLAN markets that can take advantage of the high throughput and extended range of Broadcom's second generation MIMO solution. With MIMO, information is sent and received over two or more antennas simultaneously using the same frequency band thus providing greater range and increasing throughput, while maintaining compatibility with legacy IEEE 802.11b/g devices. This is accomplished through a combination of enhanced MAC and PHY implementations including spatial multiplexing modes in the transmitter and receiver and advanced digital signal processing techniques to improve receive sensitivity.

The BCM43235 architecture with its fully integrated single-band radio transceiver supports 2 × 2 antennas for Layer 2 throughput of over 200 Mbps.

State-of-the-art security is provided by industry standardized system support for WPA™, WPA2™ (802.11i), and hardware accelerated AES encryption/decryption, coupled with TKIP and IEEE 802.1X support. Embedded hardware acceleration enables increased system performance and significant reduction in host-CPU utilization in both client and access point configurations. The BCM43235 also supports Broadcom's widely accepted and deployed WPS for ease-of-use wireless secured networks.

FEATURES

- IEEE 802.11n-compliant
- 2.4 GHz internal PA
- Two-stream spatial multiplexing up to 300 Mbps
- Uses on-chip OTP (One-Time Programmable) memory instead of SROM for substantial RBOM savings.
- Supports MCS 0–15 and MCS 32 modulation and coding rates.
- Supports 20 MHz and 40 MHz channels with optional SGI.
- Support for STBC in both TX and RX
- Greenfield, mixed mode, and legacy modes supported
- Full IEEE 802.11b/g legacy compatibility with enhanced performance.
- Supports one USB 2.0 host port or one 480 MHz HSIC port.
- UART and JTAG interface, up to eight GPIOs.
- Supports up to 32 MB of serial flash memory.
- ARM® Cortex-M3™ CPU core plus 256 KB ROM and 448 KB RAM.
- Supports Broadcom's OneDriver™ software.
- Supports WHQL certified drivers for Windows® Vista 32- and 64-bit, Windows XP, and Windows 2000 operating systems for client applications.
- Supports Linux® and VxWorks® for access point and router applications.
- Comprehensive wireless network security support that includes WPA, WPA2, and AES encryption/decryption coupled with TKIP and IEEE 802.1X support.
- BCM43235 package: 10 mm x 10 mm 88-pin QFN

APPLICATIONS

- USB 2.0 dongles
- HSIC media modules

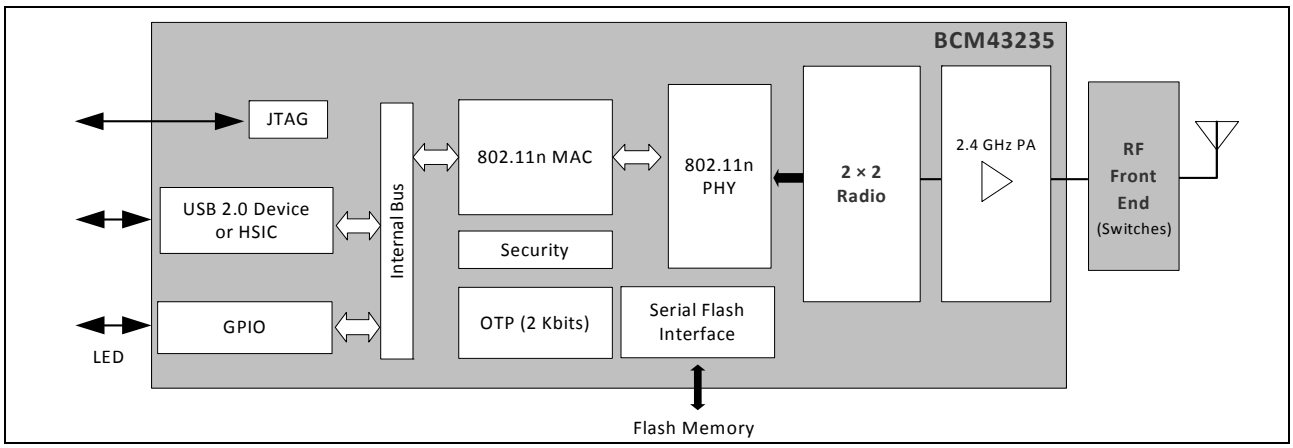

Figure 1: BCM43235 Block Diagram

Revision History

Revision	*Date*	*Change Description*
43235-DS02-R	8/13/2010	**Updated:** • Section 1: "Introduction," on page 7 • Figure 7: "BCM43235 88-Pin QFN Package," on page 17 • Table 2: "Pin Assignments," on page 18 • Table 3: "Signal Descriptions," on page 19 • Table 5: "Absolute Maximum Ratings," on page 24 • Table 9: "HSIC Characteristics," on page 26 (added) • Table 17: "88-Pin QFN Thermal Characteristics," on page 33 • "Junction Temperature Estimation and PSIJT Versus ThetaJC" on page 33 • Table 18: "Ordering Information," on page 35
43235-DS01-R	6/14/2010	**Updated:** • "rcal_res_ext_core" signal description on page 19.
43235-DS00-R	5/10/2010	Initial release

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Section 1: Introduction

The BCM43235 is the latest innovative chip from Broadcom® based on 802.11n. The chip is designed to take current WLAN systems to the next level of higher performance and greater range with Multiple Input Multiple Output (MIMO) technology as shown in Figure 1. The 802.11n standard more than doubles the spectral efficiency compared to that of current IEEE 802.11b/g WLANs.

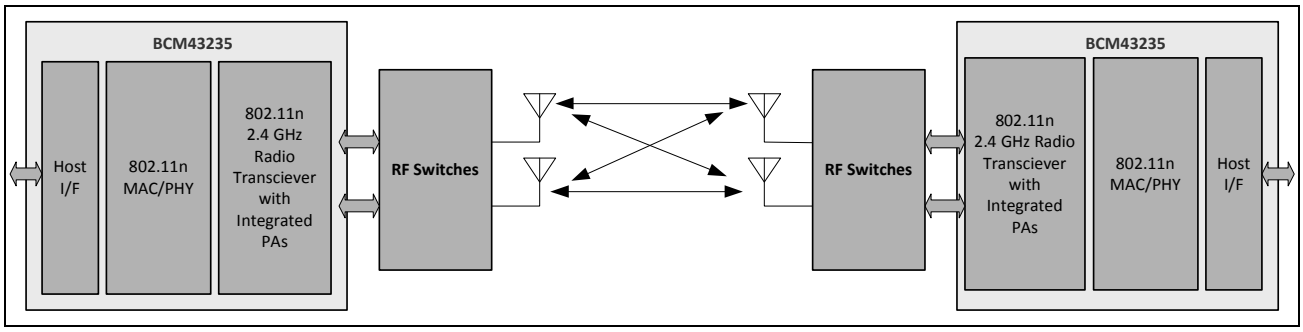


Figure 1: MIMO System Diagram Showing 2 × 2 Antenna Configuration

Employing a native 32-bit bus with Direct Memory Access (DMA) architecture, the BCM43235 offers significant performance improvements in both transfer rates and CPU utilization and flexible support for USB 2.0 devices.

Figure 2 on page 8 shows a block diagram of the device.

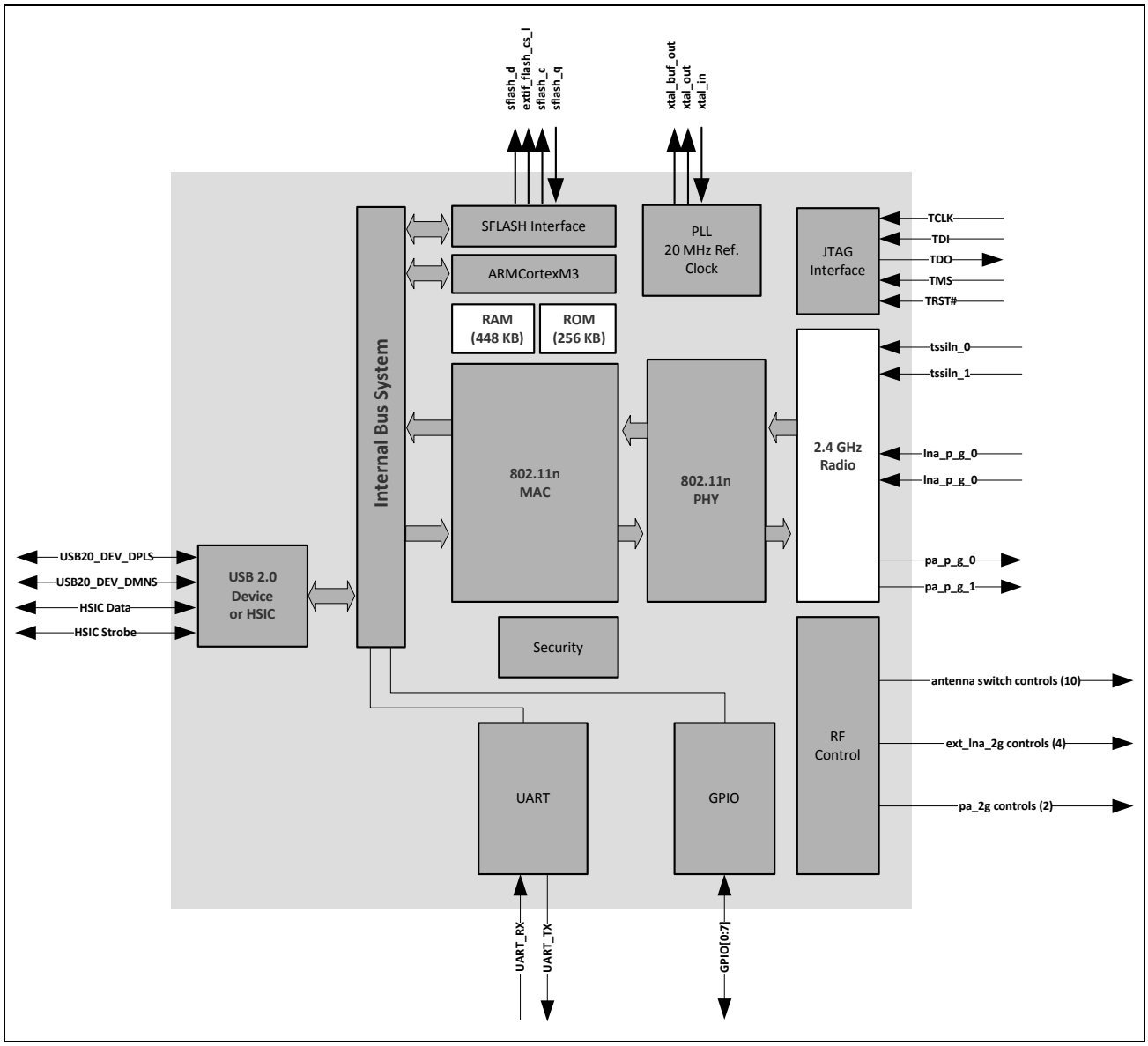


Figure 2: BCM43235 Functional Block Diagram

Section 2: Functional Description

Global Functions

Power Management

The BCM43235 has been designed with the stringent power consumption requirements of battery-powered hosts in mind. All areas of the chip design were scrutinized to help reduce power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages.

Additionally, the BCM43235 includes an advanced Power Management Unit (PMU). The PMU provides significant power savings by putting the BCM43235 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters in the PMU are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

Voltage Regulators

Three Low-Dropout (LDO) regulators and a PMU are integrated into the BCM43235. All regulators are programmable via the PMU.

Reset

Resets are generated internally by the BCM43235. An optional external power-on reset circuit can be connected to the active-low Ext_por input pin. A 50 ms low pulse is recommended to guarantee that a sufficiently long reset is applied to all internal circuits, including integrated PHYs. The initialization process loads all pin configurable modes, resets all internal processes, and puts the device in the idle state. During initialization, the clock source input signal must be active, and the 3.3V power supply to the device must be stable. The external power-on reset overrides the BCM43235 internal reset.

GPIO Interface

There are eight General-Purpose I/O (GPIO) pins provided on the BCM43235. They are multiplexed with the control signals. These pins can be used to attach to various external devices. Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. A programmable internal pull-up/pull-down resistor is included on each GPIO. If a GPIO output enable is not asserted, and the corresponding GPIO signal is not being driven externally, the GPIO state is determined by its programmable resistor.

Bluetooth® Coexistence Interface

A 5-wire handshake interface is provided to enable signalling between the device and an external Bluetooth® device host to manage sharing of the wireless medium for optimum performance. The signals provided are:

- btcx_tx_conf
- btcx_rf_active
- btcx_status
- btcx_prisel
- btcx_freq

Note: These five pins are muxed with the JTAG interface.

OTP

The BCM43235 contains an on-chip One-Time-Programmable (OTP) area that can be used for nonvolatile storage of WLAN information such as a MAC address and other hardware-specific parameters. The total area available for programming is 2 Kbits.

JTAG Interface

The BCM43235 supports the IEEE 1149.1 JTAG boundary-scan standard for testing the device packaging and PCB manufacturing.

UART Interface

One UART interface is provided that can be attached to RS-232 Data Termination Equipment (DTE) for exchanging and managing data with other serial devices. The UART interface is primarily used for debugging and development.

Serial Flash Interface

Serial Flash™ is available regardless of whether USB 2.0 operation is enabled or disabled. The Flash interface is an STMicroelectronics®-compatible, 4-pin interface.

USB/HSIC Interface

The BCM43235 USB/HSIC interface can be set to operate as a USB 2.0 port or a High-Speed Inter-Chip (HSIC) port. Features of the interface are:

- USB 2.0 protocol engine:
  - Parallel Interface Engine (PIE) between packet buffers and USB transceiver
  - Supports up to nine endpoints, including Configurable Control Endpoint 0
- Separate endpoint packet buffers with a 512-byte FIFO buffer each
- Host-to-device communication for bulk, control, and interrupt transfers
- Configuration/status registers
- The HSIC port can communicate with an external HSIC host, such as the BCM5357 and BCM5358.

The various blocks in the USB 2.0 device/HSIC core are shown in Figure 3.

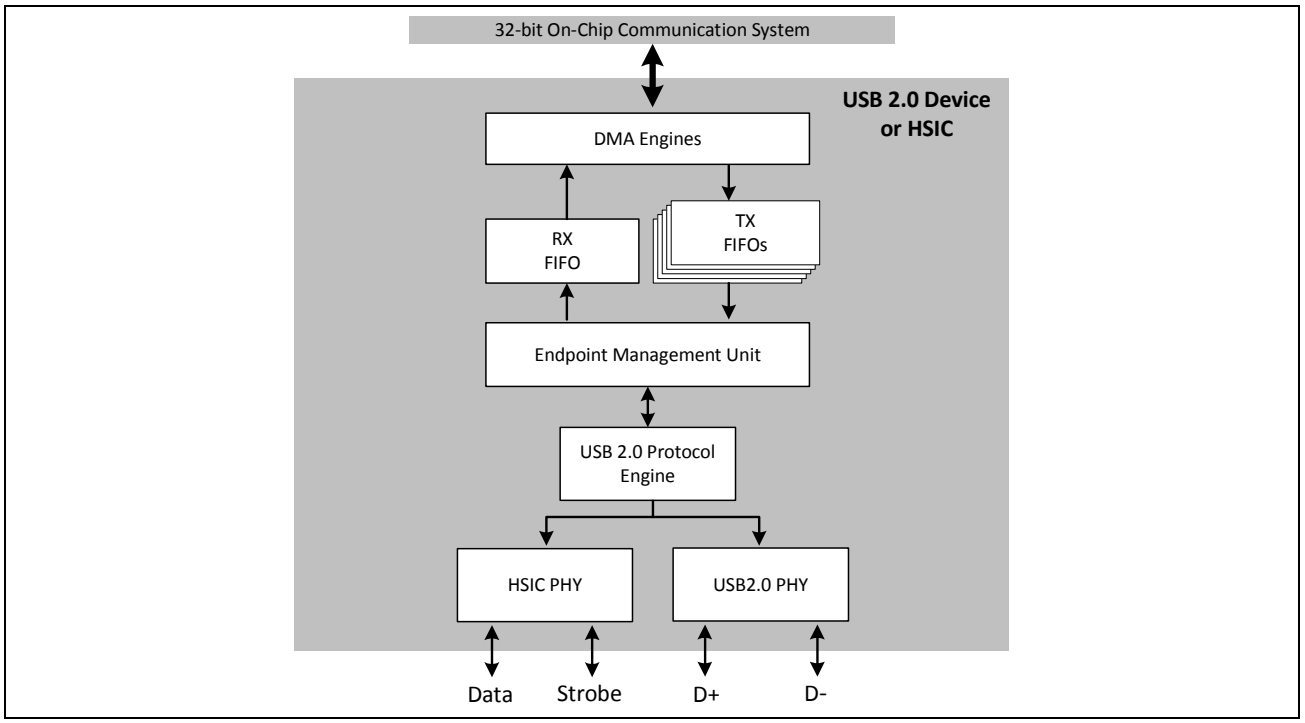


Figure 3: USB 2.0 Device/HSIC Core Block Diagram

The USB 2.0 PHY handles the USB protocol and the serial signaling interface between the host and device. It is primarily responsible for data transmission and recovery. On the transmit side, data is encoded, along with a clock, using the NRZI scheme with bit stuffing to ensure that the receiver detects a transition in the data stream. A SYNC field that precedes each packet enables the receiver to synchronize the data and clock recovery circuits. On the receive side, the serial data is deserialized, unstuffed, and checked for errors. The recovered data and clock are then shifted to the clock domain that is compatible with the internal bus logic.

The endpoint management unit contains the PIE control logic and the endpoint logic. The PIE interfaces between the packet buffers and the USB transceiver. It handles packet identification (PID), USB packets, and transactions.

The endpoint logic contains nine uniquely-addressable endpoints. These endpoints are the source or sink of communication flow between the host and the device. Endpoint zero is used as a default control port for both the input and output directions. The USB system software uses this default control method to initialize and configure the device information and allows USB status and control access. Endpoint zero is always accessible after a device is attached, powered, and reset.

Endpoints are supported by 512-byte FIFO buffers, one for each IN endpoint and one shared by all OUT endpoints. Both TX and RX data transfers support a DMA burst of 4, which guarantees low latency and maximum throughput performance. The RX FIFO can never overflow by design. The maximum USB packet size cannot be more than 512 bytes.

Finally, the BCM43235 is either configured as a USB 2.0 device or as a PHY-less HSIC by selecting the appropriate strapping option. See Table 4 on page 23 for information on how to select the strapping options.

Crystal Oscillator

Table 1 lists the requirements for the crystal oscillator.

Table 1: Crystal Oscillator Requirements

Parameter	*Value*
Frequency	20 MHz
Mode	AT cut, fundamental
Load capacitance	16 pF
ESR	50Ω maximum
Frequency stability	±10 ppm at 25°C
	±10 ppm at 0°C to +85°C
Aging	±3 ppm/year max first year, ±1 ppm thereafter
Drive level	300 µW maximum
Q-factor	40,000 minimum
Shunt capacitance	< 5 pF

Figure 4 shows the recommended oscillator configuration.

Note: Refer to reference schematics for design-specific details.

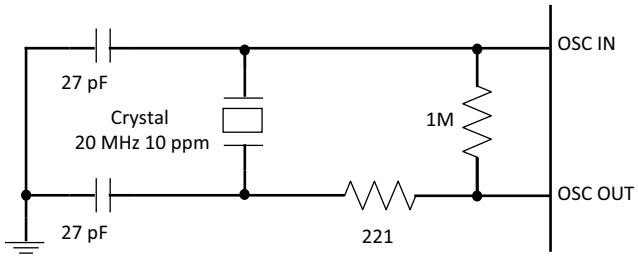


Figure 4: Recommended Oscillator Configuration

IEEE 802.11n MAC Description

The IEEE 802.11n MAC features include:

- Enhanced MAC for supporting 802.11n features
- Programmable Access Point (AP) or Station (STA) functionality
- Programmable Independent Basic Service Set (IBSS) or infrastructure mode
- Aggregated MPDU (MAC Protocol Data Unit) support for High-throughput (HT)
- Passive scanning
- Network Allocation Vector (NAV), Interframe Space (IFS), and Timing Synchronization Function (TSF) functionality
- RTS/CTS procedure
- Transmission of response frames (ACK/CTS)
- Address filtering of receive frames as specified by IBSS rules
- Multirate support
- Programmable Target Beacon Transmission Time (TBTT), beacon transmission/cancellation and programmable Announcement Traffic Indication Message (ATIM) window
- CF conformance: Setting NAV for neighborhood Point Coordination Function (PCF) operation
- Security through a variety of encryption schemes including WEP, TKIP, AES, WPA, WAP2, and IEEE 802.1X
- Power management
- Statistics counters for MIB support

The MAC core supports the transmission and reception of sequences of packets, together with related timing, without any packet-by-packet driver interaction. Time-critical tasks requiring response times of only a few milliseconds are handled in the MAC core. This achieves the required timing on the medium while keeping the host driver easier to write and maintain. Also, incoming packets are buffered in the MAC core, which allows the MAC driver to process them in bursts, enabling high bandwidth performance.

The MAC driver interacts with the MAC core to prepare queues of packets to transmit and to analyze and forward received packets to upper software layers. The internal blocks of the MAC core are connected to a Programmable State Machine (PSM) through the host interface that connects to the internal bus (see Figure 5).

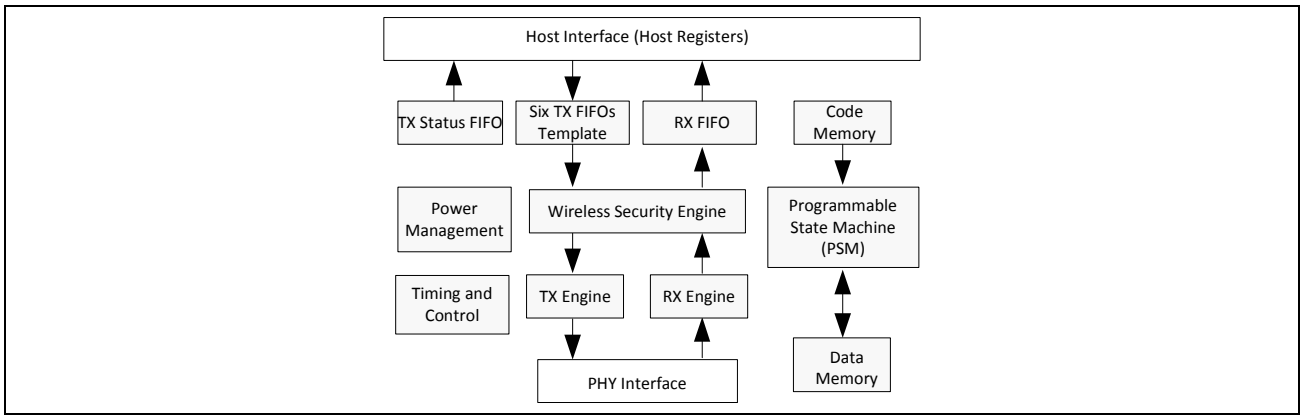


Figure 5: Enhanced MAC Block Diagram

The host interface consists of registers for controlling and monitoring the status of the MAC core and interfacing with the TX/RX FIFOs. For transmit, a total of 128 KB FIFO buffering is available that can be dynamically allocated to six transmit queues plus template space for beacons, ACKs, and probe responses. Whenever the host has a frame to transmit, the host queues the frame into one of the transmit FIFOs with a TX descriptor containing TX control information. The PSM schedules the transmission on the medium depending on the frame type, transmission rules in IEEE 802.11 protocol, and the current medium occupancy scenario. After the transmission is completed, a TX status is returned to the host, informing the host of the result that got transmitted.

The MAC contains a single 10 KB RX FIFO. Whenever a frame is received, the frame is sent to the host along with an RX descriptor that contains additional information about the frame reception conditions.

The power management block maintains the information regarding the power management state of the core (and the associated STAs in case of an AP) to help in dynamic decisions by the core regarding frame transmission.

The wireless security engine performs the required encryption/decryption on the TX/RX frames. This block supports separate transmit and receive keys with four shared keys and 50 link-specific keys. The link-specific keys are used to establish a secure link between any two STAs, with the required key being shared between only those two STAs, hence excluding all of the other STAs in the same network from deciphering the communication between those two STAs. The wireless security engine supports the following encryption schemes that can be selected on a per-destination basis:

- None: The wireless security engine acts as a pass-through
- WEP: 40-bit secure key and 24-bit IV as defined in IEEE Std. 802.11-2007
- WEP128: 104-bit secure key and 24-bit IV
- TKIP: IEEE Std. 802.11-2007
- AES: IEEE Std. 802.11-2007

The transmit engine is responsible for the byte flow from the TX FIFO to the PHY interface through the encryption engine and the addition of an FCS (CRC-32) as required by IEEE 802.11-2007. Similarly, the receive engine is responsible for byte flow from the PHY interface to the RX FIFO through the decryption engine and for detection of errors in the RX frame.

The timing block performs the TSF, NAV, and IFS functionality as described in IEEE Std. 802.11-2007.

The Programmable State Machine (PSM) coordinates the operation of different hardware blocks required for both transmission and reception. The PSM also maintains the statistics counters required for MIB support.

IEEE 802.11n PHY Description

The PHY features include:

- Programmable data rates from MCS 0–15 in 20 MHz and 40 MHz channels, as specified in 802.11n.
- Support for Short Guard Interval (SGI) and Space-Time Block Coding (STBC).
- All scrambling, encoding, forward error correction, and modulation in the transmit direction, and inverse operations in the receive direction.
- Advanced digital signal processing technology for best-in-class receive sensitivity.
- Both mixed-mode and optional greenfield preamble of 802.11n.
- Both long and optional short preambles of IEEE 802.11b.
- Resistance to multipath (>250 nanoseconds RMS delay spread) with maximal ratio combining for high throughput and range performance, including improved performance in legacy mode over existing IEEE 802.11b/g solutions.
- Automatic Gain Control (AGC).
- Available per-packet channel quality and signal strength measurements.

The PHYs integrated in the BCM43235 provide baseband processing at all mandatory data rates specified in 802.11n up to 300 Mbps, and the legacy rates specified in IEEE 802.11b/g including 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54 Mbps. This core acts as an intermediary between the MAC and the 2.4 GHz radio, converting back and forth between packets and baseband waveforms.

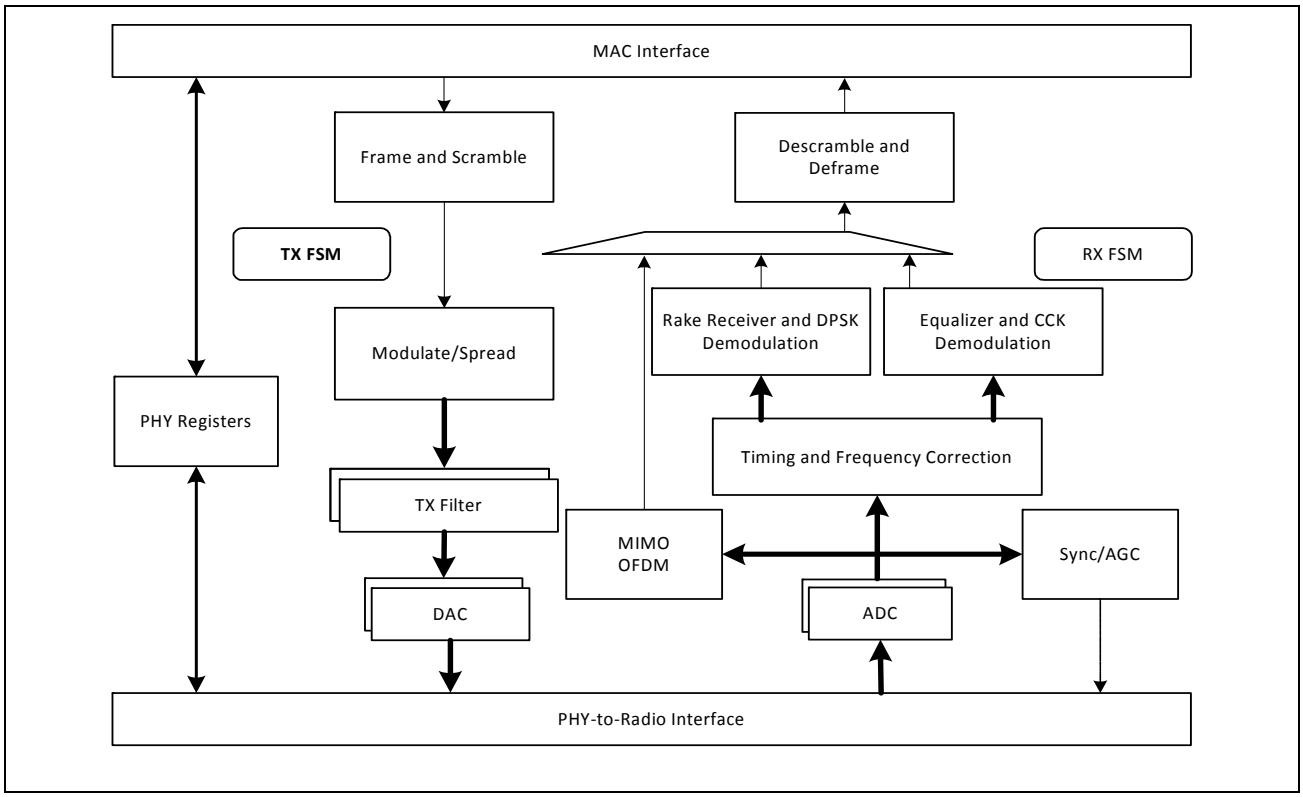


Figure 6: PHY Block Diagram

Radio Transceiver

Integrated into the BCM43235 is Broadcom's world-class 2.4 GHz radio transceiver that ensures low power consumption and robust communications for low-cost applications operating in the 2.4 GHz band. Channel bandwidths of 20 MHz and 40 MHz are supported as specified in 802.11n.

Receiver Path

The BCM43235 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The excellent noise figure of the receiver makes an external LNA unnecessary.

Transmitter Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band. Linear on-chip Power Amplifiers are included, which are capable of delivering a nominal output power exceeding +15 dBm while meeting the IEEE 802.11g specifications. The TX gain has a 78 dB range with a resolution of 0.25 dB.

Calibration

The BCM43235 features dynamic on-chip calibration, eliminating process variation across components. This enables the device to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation.

Section 3: Pin Assignments

This sections contains pin assignments and ballout information for the BCM43235 (88-pin) packages.

BCM43235 88-Pin QFN Assignments

		88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67		
		VDD	mimophy_core0_ant1_rx	mimophy_core0_ant1_tx	gpio_6	gpio_5	VDDIO	gpio_4	gpio_3	gpio_2	gpio_1	gpio_0	VDD	VDDIO/OTP_VDD	USB_RREF	HSIC_STRB	HSIC_DATA	USB AVDD 1p2	USB_DMNS	USB_DPLS	USB_AVDD3p3	USB_MONCDR	USBAVDD2p5		
1	VDDIO																							VDD	66
2	sflash_cs_l																							mimophy_core1_ant1_rx	65
3	sflash_q																							mimophy_core1_ant1_tx	64
4	sflash_c																							VDDIO	63
5	sflash_d																							UART_RX	62
6	mimophy_core0_ant0_tx																							UART_TX	61
7	mimophy_core0_ant0_rx																							VDD	60
8	VDD																							VDDPLL/RF_AVDD_1p2	59
9	mimophy_core1_ant0_tx																							USBLDO_2p5_out	58
10	mimophy_core1_ant0_rx																							LDO_3p3_in	57
11	VDDIO																							VREF	56
12	VDD																							PAREF	55
13	gpio_7																							PAREF_CTL1	54
14	jtag_trst_l																							PAREF_CTL2	53
15	jtag_tdi																							Ext_por	52
16	jtag_tck																							xtal_buf_out	51
17	analog_wlan_iqtest_VDD 1p2																							i_xtal_VDD2p5/ o_xtal_VDD2p5	50
18	jtag_tms																							xtal_in	49
19	jtag_tdo																							xtal_out	48
20	analog_wlan_iqtest_qp																							synth_VDD1p2	47
21	analog_wlan_iqtest_qn																							synth_vco_VDD1p2	46
22	analog_wlan_iqtest_in																							vreg3p3_VDD3p3	45
		23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44		
		analog_wlan_iqtest_ip	No connect/Unused GND	PAD_2G_CORE1_VDD3P3	No connect GND	TX_2G_CORE1_VDD1P2	No connect GND	core1_VDD1p2	rf_2g_antenna_core1	rx_2g_core1_VDD1p2	pa_2g_core1_VDD3p3	PA_2g_core1	PAD_2G_CORE0_VDD3P3	No connect GND	TX_2G_CORE0_VDD1P2	No connect GND	core0_VDD1p2	rf_2g_antenna_core0	rx_2g_core0_VDD1p2	pa_2g_core0_VDD3p3	PA_2g_core0	gpiao_GPIO_PAD	rcal_res_ext_core		

BCM43235 10 x 10 QFN

Figure 7: BCM43235 88-Pin QFN Package

Signals by Pin Number

Table 2: Pin Assignments

Pin	Signal Name
1	VDDIO
2	sflash_cs_l
3	sflash_q
4	sflash_c
5	sflash_d
6	mimophy_core0_ant0_tx
7	mimophy_core0_ant0_rx
8	VDD
9	mimophy_core1_ant0_tx
10	mimophy_core1_ant0_rx
11	VDDIO
12	VDD
13	gpio_7
14	jtag_trst_l
15	jtag_tdi
16	jtag_tck
17	analog_wlan_iqtest_VDD 1p2
18	jtag_tms
19	jtag_tdo
20	analog_wlan_iqtest_qp
21	analog_wlan_iqtest_qn
22	analog_wlan_iqtest_in

Pin	Signal Name
23	analog_wlan_iqtest_ip
24	No connect/Unused GND
25	PAD_2G_CORE1_VDD3P3
26	No connect GND
27	TX_2G_CORE1_VDD1P2
28	No connect GND
29	core1_VDD1p2
30	rf_2g_antenna_core1
31	tx_2g_core1_VDD1p2
32	pa_2g_core1_VDD3p3
33	PA_2g_core1
34	PAD_2G_CORE0_VDD3P3
35	No connect GND
36	TX_2G_CORE0_VDD1P2
37	No connect GND
38	core0_VDD1p2
39	rf_2g_antenna_core0
40	tx_2g_core0_VDD1p2
41	pa_2g_core0_VDD3p3
42	PA_2g_core0
43	gpiao_GPIO_PAD
44	rcal_res_ext_core
45	vreg3p3_VDD3p3

Pin	Signal Name
46	synth_vco_VDD1p2
47	synth_VDD1p2
48	xtal_out
49	xtal_in
50	i_xtal_VDD2p5/ o_xtal_VDD2p5
51	xtal_buf_out
52	Ext_por
53	PAREF_CTL2
54	PAREF_CTL1
55	PAREF
56	VREF
57	LDO_3p3_in
58	USBLDO_2p5_out
59	VDDPLL/RF_AVDD_1p2
60	VDD
61	UART_TX
62	UART_RX
63	VDDIO
64	mimophy_core1_ant1_tx
65	mimophy_core1_ant1_rx
66	VDD
67	USBAVDD2p5

Pin	Signal Name
68	USB_MONCDR
69	USB_AVDD3p3
70	USB_DPLS
71	USB_DMNS
72	USB AVDD 1p2
73	HSIC_DATA
74	HSIC_STRB
75	USB_RREF
76	VDDIO/OTP_VDD
77	VDD
78	gpio_0
79	gpio_1
80	gpio_2
81	gpio_3
82	gpio_4
83	VDDIO
84	gpio_5
85	gpio_6
86	mimophy_core0_ant1_tx
87	mimophy_core0_ant1_rx
88	VDD

Section 4: Signal and Pin Descriptions

Package Signal Descriptions

The signal name, type, and description of each pin in the BCM43235 88-pin QFN package is listed in Table 3. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any. See also Table 4 on page 23 for resistor strapping options.

Table 3: Signal Descriptions

Signal	*BCM43235*	*Type*	*Description*
Crystal Oscillator			
xtal_in	49	I	XTAL oscillator input. Connect a 20 MHz, 10 ppm crystal between the xtal_in and xtal_out pins.
xtal_out	48	O	XTAL oscillator output
xtal_buf_out	51	O	Buffered XTAL output
Serial Flash Interface			
sflash_cs_l	2	O (8 mA-PU)	Serial flash chip select
sflash_q	3	I (8 mA-PU)	Serial flash data input
sflash_c	4	O (8 mA-PD)	Serial flash clock
sflash_d	5	O (8 mA)	Serial flash data output
USB Interface			
usb_dmns	71	I/O	USB interface port D–
usb_dpls	70	I/O	USB interface port D+
usb_rref	75	O	During USB mode, this pin should be tied in parallel through a cap (100 pF) and resistor (4k) to ground. During HSIC mode, this pin should be tied to a resistor (5Ω) to ground.
hsic_strb	74	O	USB HSIC strobe
hsic_data	73	I/O	USB HSIC data
usb_moncdr	68	–	Test/diagnostic purposes only.
Miscellaneous Signals			
rcal_res_ext_core	44	O	Reference output, connect to ground via 15k 1% resistor.
ext_por_l	52	O	External power-on reset (POR) input. Active low. Allows an optional external power-on reset circuit to be connected. If installed, the external POR will override the internal POR.

Table 3: Signal Descriptions (Cont.)

Signal	BCM43235	Type	Description
analog_wlan_iqtest_qp	20	–	IQ test pin
analog_wlan_iqtest_qn	21	–	IQ test pin
analog_wlan_iqtest_in	22	–	IQ test pin
RF Control Interface			
mimophy_core0_ant0_tx	6	O	Antenna0 TR Switch controls for core 0. These pins are also used as strapping options, see Table 4 on page 23.
mimophy_core0_ant0_rx	7		
mimophy_core0_ant1_tx	86	O	Antenna1 TR Switch controls for core 0. These pins are also used as strapping options, see Table 4.
mimophy_core0_ant1_rx	87		
mimophy_core1_ant0_tx	9	O	Antenna0 TR Switch controls for core 1. These pins are also used as strapping options, see Table 4.
mimophy_core1_ant0_rx	10		
mimophy_core1_ant1_tx	64	O	Antenna1 TR Switch controls for core 1. These pins are also used as strapping options, see Table 4.
mimophy_core1_ant1_rx	65		
RF Signal Interface			
rf_2g_antenna_core0	39	I	Chain 0 RF receive input, 2.4 GHz band
rf_2g_antenna_core1	30	I	Chain 1 RF receive input, 2.4 GHz band
pa_2g_core0	42	O	Chain 0 RF transmit output, 2.4 GHz band
pa_2g_core1	33	O	Chain 1 RF transmit output, 2.4 GHz band
JTAG Interface			
jtag_trst_l	14	I/O	JTAG Reset Input. Resets the JTAG Controller. If not used, this pin should be pulled low by a 1 kΩ resistor. This pin is muxed with gpio0.
jtag_tck	16	I/O	JTAG Test Clock Input. Used to synchronize JTAG control and data transfers. If not used, this pin should be pulled low by a 1 kΩ resistor. This pin is muxed with btcx_rf_active (Bluetooth coexistence output, RF active).
jtag_tdi	15	I/O	JTAG Test Data Input. Serial data input to the JTAG TAP controller. Sampled on the rising edge of TCK. If not used, it may be left unconnected. This pin is muxed with btcx_tx_conf (Bluetooth coexistence output, WLAN transmit).
jtag_tdo	19	I/O	JTAG Test Data Output. Serial data output from the JTAG TAP controller. Sampled on the rising edge of TCK. If not used, it may be left unconnected. This pin is muxed with btcx_prisel (Bluetooth coexistence output, antenna select).

Table 3: Signal Descriptions (Cont.)

Signal	*BCM43235*	*Type*	*Description*
jtag_tms	18	I/O	JTAG Mode Select Input. Single control input to the JTAG TAP controller used to traverse the test logic state machine. Sampled on the rising edge of TCK. If not used, it may be left unconnected. This pin is muxed with btcx_status (Bluetooth coexistence output, status).
GPIO Interface			
gpio_0	78	I/O (8 mA)	General Purpose I/O pin. This pin is tristated on power-up and reset. Subsequently, it becomes an input or an output through software control. A programmable PU or PD resistor is available for each GPIO pin. This pin is muxed with wlan_led (WLAN LED output).
gpio_1	79	I/O	General Purpose I/O pin. This pin is muxed with mimophy_core0_ant_shd (antenna switch control for the shared [middle] antenna of a 2 of 3 design [core 0]).
gpio_2	80	I/O	General Purpose I/O pin. This pin is muxed with: • mimophy_core1_ant_shd: antenna switch control for the shared (middle) antenna of a 2 of 3 design (core 1). • btcx_freq: Bluetooth coexistence RF frequency
gpio_3	81	I/O	General Purpose I/O pin.
gpio_4	82	I/O	General Purpose I/O pin. This pin is muxed with: • ext_lna_2g_pu_0: 2.4 GHz band core 0 power amplifier control • ext_pa_2g_0: 2.4 GHz band core 0 power amplifier control • CS: SPI select
gpio_5	84	I/O	General Purpose I/O pin. This pin is muxed with: • ext_lna_2g_pu_1: 2.4 GHz band core 1 power amplifier control • ext_pa_2g_1: 2.4 GHz band core 1 power amplifier control • SCLK: SPI clock • I2C_SCL: I^2C clock
gpio_6	85	I/O	General Purpose I/O pin. This pin is muxed with: • SDI: SPI data input
gpio_7	13	I/O	General Purpose I/O pin. This pin is muxed with: • SDO: SPI data output • I2C_SDA: I^2C data
gpaio_gpio_pad	43	–	No connect; test only

Table 3: Signal Descriptions (Cont.)

Signal	BCM43235	Type	Description
UART Interface			
UART_RX	62	I (4 mA PU)	UART receive data
UART_TX	61	O (4 mA)	UART transmit data
Power and Ground			
vdd	8, 12, 60, 66, 77, 88	PWR	1.2V supply input for the core logic.
vddio	1, 11, 63, 83	PWR	3.3V supply input for I/O logic
vddio_otp_vdd	76	PWR	3.3V supply input for I/O logic
usb_avdd2p5	67	PWR	USB analog power supply
usbldo_2p5_out	58	PWR	USB LDO output; decouple to ground.
usb_avdd3p3	69	PWR	3.3V supply input to USB interface
usbavdd_1p2	72	PWR	1.2V supply input to USB interface
synth_vdd1p2	45	PWR	Analog 1.2V supply input
synth_vco_vdd1p2	46	PWR	Analog 1.2V supply input
vdd_cp_1p2	46	PWR	Analog 1.2V supply input
core0_vdd1p2	38	PWR	Analog 1.2V supply input
core1_vdd1p2	29	PWR	Analog 1.2V supply input
tx_2g_core0_vdd1p2	40	PWR	Analog 1.2V supply input
tx_2g_core1_vdd1p2	31	PWR	Analog 1.2V supply input
pa_2g_core0_vdd3p3	41	PWR	Filtered 3.3V input to internal PA
pa_2g_core1_vdd3p3	32	PWR	Filtered 3.3V input to internal PA
analog_wlan_iqtest_vdd_1p2	17	PWR	1.2V power supply for IQ test.
ldo_3p3_in	57	PWR	3.3V input to RF LDO
vddpll_rf_avdd1p2	59	O	XTAL power reference; decouple to ground.
vreg3p3_vdd3p3	45	PWR	Analog 3.3V supply
i_xtal_vdd2p5/o_xtal_vdd2p5	50	PWR	3.3V supply input for I/O logic
o_vref_ldo	58	O	LDO reference; decouple to ground.
vref	56	–	VREF; decouple to ground.
paref	55	–	PA reference; decouple to ground.
paref_ctl1	54	–	PA reference control 1
paref_ctl2	53	–	PA reference control 2
gnd_slug	H	GND	Ground
No connect/Unused GND	24	GND	Ground

Strapping Options

The pins listed in Table 4 are sampled at Power-on Reset (POR) to determine the various operating modes. Sampling occurs within a few milliseconds following internal POR or deassertion of external POR. After POR, each pin assumes the function specified in the signal descriptions table. Each pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND; use 10 kΩ or less (refer to the reference board schematics for further details).

Table 4: Strapping Options

Signal Name	*Mode*	*Default*	*Description*
mimophy_core0_ant0_tx	OTP select	PU	0: No OTP 1: OTP present
mimophy_core1_ant0_tx	SFLASH not present	PD	0: SFLASH not present 1: SFLASH present
mimophy_core0_ant0_rx	ST SFLASH	PD	0: SFLASH type is STMicroelectronics 1: SFLASH type is Atmel®
mimophy_core0_ant1_tx	USB PHY	PU	0: HSIC mode 1: USB PHY mode
mimophy_core0_ant1_rx	120 MHz	PU	0: Backplane at 96 (98.4) MHz 1: Backplane at 120 (123) MHz
gpio[7:6]	Boot from ROM	No pull	00: Remap to RAM; ARM processor to be held at reset. 01: Boot from ROM unless the ARM needs to be held at reset.

Section 5: Electrical Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 5: Absolute Maximum Ratings

Rating	*Symbol*	*Minimum*	*Maximum*	*Unit*
DC supply voltage for core	VDDC	–0.5	+1.4	V
DC supply voltage for I/O	VDDO	–0.5	+3.8	V
Voltage on any input or output pin	V_{IMAX}, V_{IMIN}	–0.5	+3.8[a]	V
Ambient Temp (Operating)	T_A	0	+65[b]	°C
Operating Junction Temperature 125°C	T_J	–	125	°C
Operating Humidity	–	–	85	%
Storage Temperature	T_{STG}	–40	+125	°C
Storage Humidity	–	–	60	%
ESD Protection (HBM)	V_{ESD}	–	2000	V

a. The max voltage requirement is to not exceed VDDO + 0.5V when VDDO < 3.3V.
b. The temperature above the shield is 65°C for the T_J to be less than 125°C with a P_{out} of 15 dBm.

Recommended Operating Conditions and DC Characteristics

Table 6: Recommended Operating Conditions and DC Characteristics

		Value			
Element	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
DC supply voltage for I/O	VDDO	2.97	3.3	3.63	V
DC supply voltage for core and 1.2V analog	VDD12	1.16	1.2	1.24	V
Input low voltage (VDDO = 3.3V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3.3V)	V_{IH}	2.0	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	VDDO – 0.4V	–	–	V

Current Consumption From the 3.3V Supply

Table 7: Current Consumption from 3.3V Supply

Item	***Typical***	***Maximum***	***Units***
Radio disabled state	TBD	TBD	mA
Idle and associated state, PM2 mode	TBD	TBD	mA
Active state, TX or RX, 40 MHz channel, maximum throughput, PM2 mode	TBD	800	mA

Current Consumption From the 1.2V Supply

Table 8: Current Consumption from 1.2V Supply

Item	Typical	Maximum	Units
Radio disabled state	TBD	TBD	mA
Idle and associated state, PM2 mode	TBD	TBD	mA
Active state, TX or RX, 40 MHz channel, maximum throughput, PM2 mode	TBD	1050	mA

Table 9: HSIC Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Comments
HSIC signaling voltage	V_{DD}	1.1	1.2	1.3	V	–
I/O voltage input low	V_{IL}	-0.3	–	$0.35*V_{DD}$	V	–
I/O voltage input high	V_{IH}	$0.65*V_{DD}$	–	$V_{DD} + 0.3$	V	–
I/O voltage output low	V_{OL}		–	$0.25*V_{DD}$	V	–
I/O voltage output high	V_{OH}	$0.75*V_{DD}$	–		V	–
I/O pad drive strength	O_D	40	–	60	Ω	Controlled output impedance driver
I/O weak keepers	I_L	20	–	70	µA	–
I/O Input Impedance	Z_I	100	–		kΩ	–
Total capacitive load	C_L	3	–	14	pF	Note[a]
Characteristic trace impedance	T_I	45	50	55	Ω	–
Circuit board trace length	T_L		–	10	cm	–
Circuit board trace propagation skew	T_S		–	15	ps	Note[b]
STROBE frequency	F_{STROBE}	239.988	240	240.012	MHz	±500 ppm[c]
Slew rate (rise and fail) STROBE & DATA	T_{slew}	$0.60*V_{DD}$	1.0	1.2	V/ns	Averaged from 30% ~ 70% points[c]
Receiver DATA setup time (with respect to STORBE)	T^s	300	–	–	ps	Measured at the 50% point[c]
Reciver DATA old time (with respect to STROBE	T_b	300	–	–	ps	Measured at the 50% point[c]

a. Includes device input/output capacitance , and the capacitance of a 50 ohm PCB trace with a length of 10 cm.
b. Maximum propagation delay skew in STROBE or DATA, with respect to each other. The trace delay should be matched between STROBE and DATA to ensure that the signal timing is within specification limits at the receiver.
c. Jitter and duty cycle are not separately specified parameters: they are incorporated into the values in the table.

Section 6: RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

2.4 GHz Band General RF Specifications

Table 10: 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
aRxTxTurnaroundTime	Including switch time	–	–	2	µs

2.4 GHz Band Receiver RF Specifications

Table 11: 2.4 GHz Band Receiver RF Specifications

Characteristic	Condition	Minimum	Typical	Maximum	Unit
Cascaded Noise Figure	–	–	4.5	–	dB
Maximum Receive Level[a]	@ 1, 2 Mbps	–4	–	–	dBm
	@ 5.5, 11 Mbps	–10	–	–	dBm
	@ 54 Mbps	–10	–	–	dBm
Input IP3	Maximum gain	–	–16	–	dBm
	Minimum gain	–	–2	–	dBm
LPF 3 dB Bandwidth	–	8	8.5	9	MHz
PGA DC Rejection Servo Loop Bandwidth	WB mode	–	1	–	MHz
	NB mode	120 Hz	–	230 kHz	–
LPF DC Rejection Servo Loop Bandwidth	WB mode	–	500	–	kHz
	NB mode	120 Hz	–	230 kHz	–
Maximum Receiver Gain	–	–	88	–	dB
Gain Control Step	–	–	3	–	dB/step

Table 11: 2.4 GHz Band Receiver RF Specifications (Cont.)

Characteristic	Condition	Minimum	Typical	Maximum	Unit
Rx Sensitivity	20 MHz channel spacing for all MCS rates				
(10% PER for 4096 octet PSDU) at WLAN RF port. Defined for default parameters: GF, 800 ns GI, and non-STBC.	MCS0 OFDM	–	–91	–	dBm
	MCS7 OFDM	–	–74	–	dBm
	MCS8 OFDM	–	–88.5	–	dBm
	MCS15 OFDM	–	–69	–	dBm
	40 MHz channel spacing for all MCS rates				
	MCS0 OFDM	–	–88	–	dBm
	MCS7 OFDM	–	–71	–	dBm
	MCS8 OFDM	–	–85.5	–	dBm
	MCS15 OFDM	–	–66	–	dBm

a. When using a suitable external switch.

2.4 GHz Band Transmitter RF Specifications

Table 12: 2.4 GHz Band Transmitter RF Specifications

Characteristic	Condition	Minimum	Typical	Maximum	Unit
RF Output Frequency Range	–	2400	–	2500	MHz
G band	20 MHz BW	–	–	16	dBm
	40 MHz BW	–	–	14.5	dBm
Carrier Suppression	–	15	–	–	dBr
TX Spectrum mask @ maximum gain	fc – 22 MHz < f < fc – 11 MHz	–	–	–30	dBr
	fc + 11 MHz < f < fc + 22 MHz	–	–	–30	dBr
	f < fc – 22 MHz; and f > fc + 22 MHz	–	–	–50	dBr
TX Modulation Accuracy (EVM) at maximum gain	IEEE 802.11b mode	–	–	35%	–
	IEEE 802.11g mode	–	–	5%	–
Gain Control Step Size	–	–	0.25	–	dB/step
I/Q Baseband Bandwidth	IEEE 802.11b mode	–	12	–	MHz
	IEEE 802.11g mode	–	12	–	MHz
Amplitude Balance[a]	DC input	–1	–	1	dB
Phase Balance[a]	DC input	–1.5	–	1.5	°C
Baseband Differential Input Voltage	Shaped pulse	–	0.6	–	Vpp

a. At a 3 MHz offset from the carrier frequency.

2.4 GHz Band Local Oscillator Specifications

Table 13: 2.4 GHz Band Local Oscillator Specifications

Characteristic	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
VCO Frequency Range	–	2412	–	2484	MHz
Reference Input Frequency Range	–	–	20	–	MHz
Clock Frequency Tolerance	–	–	–	±20	ppm
Reference Spurs	–	–	–	–34	dBc
Local Oscillator Phase Noise, single-sided from 1 kHz–300 kHz offset	–	–	–	–86.5	dBc/Hz

On-Chip Regulator Power Supply Characteristics

Table 14: On-Chip Regulator Power Supply Characteristics

Element	Value			Unit
	Minimum	Typical	Maximum	
2.5V–3.1V PA Reference LDO (default: off) Vout: 2.5V to 3.1V when output A, B, C and/or D is enabled. Control Step: 50 mV/step				
Input Power Supply	2.97	3.3	3.63	V
Vout (Note 1) Programmable, 50 mV/step	2.5	2.85	3.1	V
Absolute Accuracy	–4	–	+4	%
Maximum Output Current: A, B, C and D all enabled	–	–	40	mA
Maximum Output Current: any output A, B, C, or D	–	–	10	mA
Dropout Voltage	150	–	–	mV
Startup Time	–	–	100	µs
Switching ON Time (either A or G) Note: LDO is already powered.	20	30	100	ns
Switching OFF Time (either A or G) Note: LDO is already powered.	1	1.3	2	ns
3.3V–1.2V RF LDO				
Input power supply, Vbat	2.97	3.30	3.63	V
Vout (Note 1) Programmable, 50 mV/step	1.2	–	3.0	V
Absolute Accuracy	–4	–	+4	%
Dropout Voltage	150	–	–	mV
Maximum Output Current	–	–	120	mA
Startup time with 100 µs VDD Ramp	–	–	50	µs
3.3V–2.5V USB LDO				
Input power supply	2.97	3.30	3.63	V
Vout	2.3	2.5	2.65	V
Absolute accuracy	–4	–	+4	%
Dropout voltage	150	–	–	mV
Maximum output current	–	–	30	mA
Start-up time	–	–	50	µs
Note: It is required that the input supply be at least 200 mV higher than the output. More headroom is better for PSRR performance.				

Section 7: Timing Characteristics

Reset and Clock Timing Diagram

Resets are generated internally by the BCM43235. An optional external Power-On Reset (POR) circuit can be connected to the active-low Ext_por input pin. The BCM43235 is reset automatically as long as the power supplies are turned on in the following sequence. 3.3V first, 2.5V second, and 1.2V last.

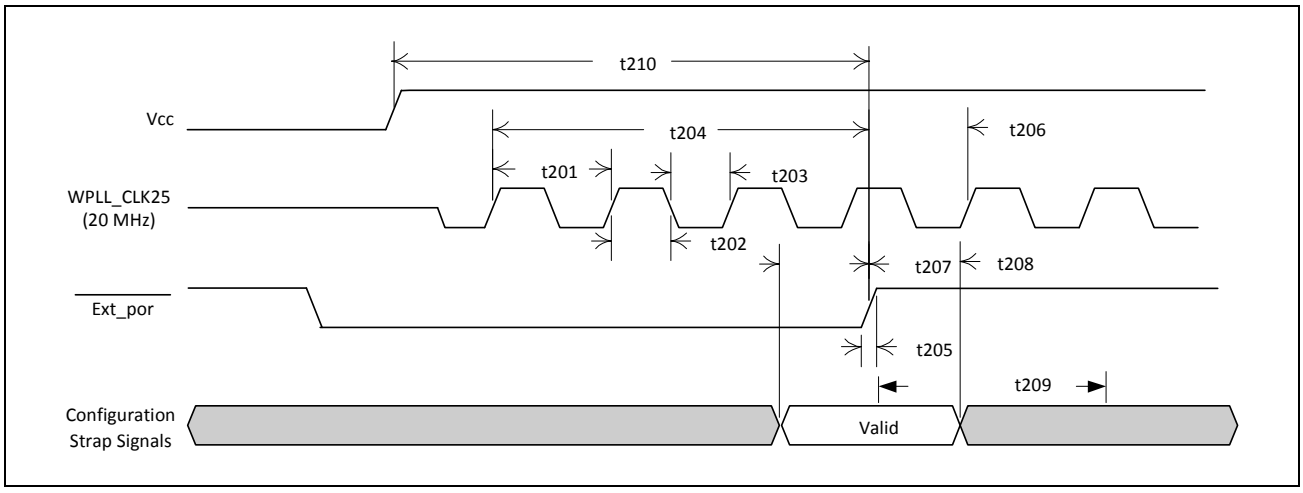


Figure 8: Timing for the Optional External Power-On Reset

Table 15: Ext_por and Clock Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*	*Units*
t201	OSCIN frequency	19.9995	20.0000	20.0005	MHz
t202	OSCIN high time	–	20	–	ns
t203	OSCIN low time	–	20	–	ns
t204	EXT_POR_L low pulse duration	50	–	–	ms
t207	Configuration valid setup to EXT_POR_L rising	50	–	–	µs
t208	Configuration valid hold from EXT_POR_L rising	1.7	–	2.8	ms
t209	EXT_POR_L deassertion to normal switch operation	–	3	–	ms
t210	Reset low hold time after power supplies stabilize	50	–	–	ms

Serial Flash Timing Diagram

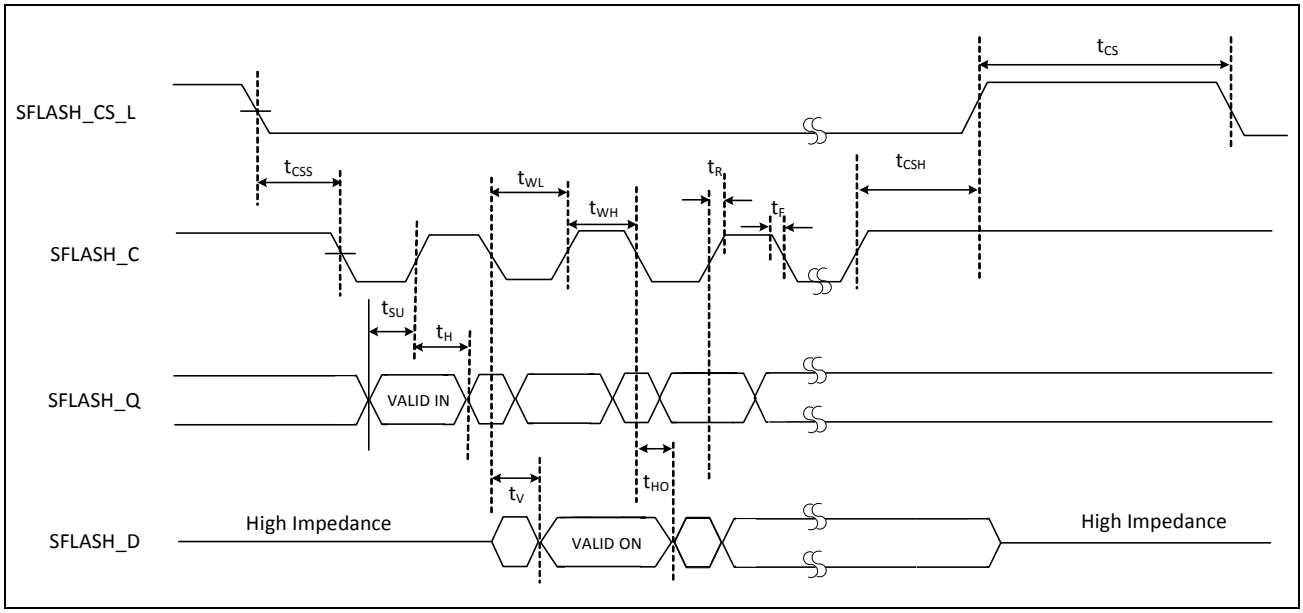


Figure 9: Serial Flash Timing Diagram (STMicroelectronics-Compatible)

Table 16: Serial Flash Timing

Parameter	*Descriptions*	*Minimum*	*Typical*	*Maximum*	*Units*
f_{SCK}	Serial flash clock frequency	–	12.5	66	MHz
t_{WH}	Serial flash clock high time	9	–	–	ns
t_{WL}	Serial flash clock low time	9	–	–	ns
t_R, t_F[a]	Clock rise and fall times[b]	TBD	–	–	V/ns
t_{CSS}	Chip select active setup time	5	–	–	ns
t_{CS}	Chip select deselect time	100	–	–	ns
t_{CSH}	Chip select hold time	5	–	–	ns
t_{SU}	Data input setup time	2	–	–	ns
t_H	Data input hold time	5	–	–	ns
t_{HO}	Data output hold time	0	–	–	ns
t_V	Clock low to output valid	–	–	8	ns

a. t_R and t_F are expressed as a slew-rate.
b. Peak-to-peak

Section 8: Thermal Information

Table 17: 88-Pin QFN Thermal Characteristics

Airflow	*0 fpm, 0 mps*	*100 fpm, 0.508 mps*	*200 fpm, 1.016 mps*	*400 fpm, 2.032 mps*	*600 fpm, 3.048 mps*
θ_{JA} (°C/W)	20.79	17.55	16.24	15.00	14.34
θ_{JB} (°C/W)	3.95	–	–	–	–
θ_{JC} (°C/W)	12.44	–	–	–	–
Ψ_{JT} (°C/W)	3.51	3.50	3.55	3.59	3.61

Note:

- In the thermal characterizations that were done on the BCM43235 using a 4-layer board, the temperature at 1 mm above the shield must be no higher than 65°C in order to keep the junction temperature (T_J) from exceeding 125°C.
- The BCM43235 is designed and rated for operation at a maximum junction temperature not to exceed 125°C.

Junction Temperature Estimation and PSI_{JT} Versus $Theta_{JC}$

Package thermal characterization parameter Psi-J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

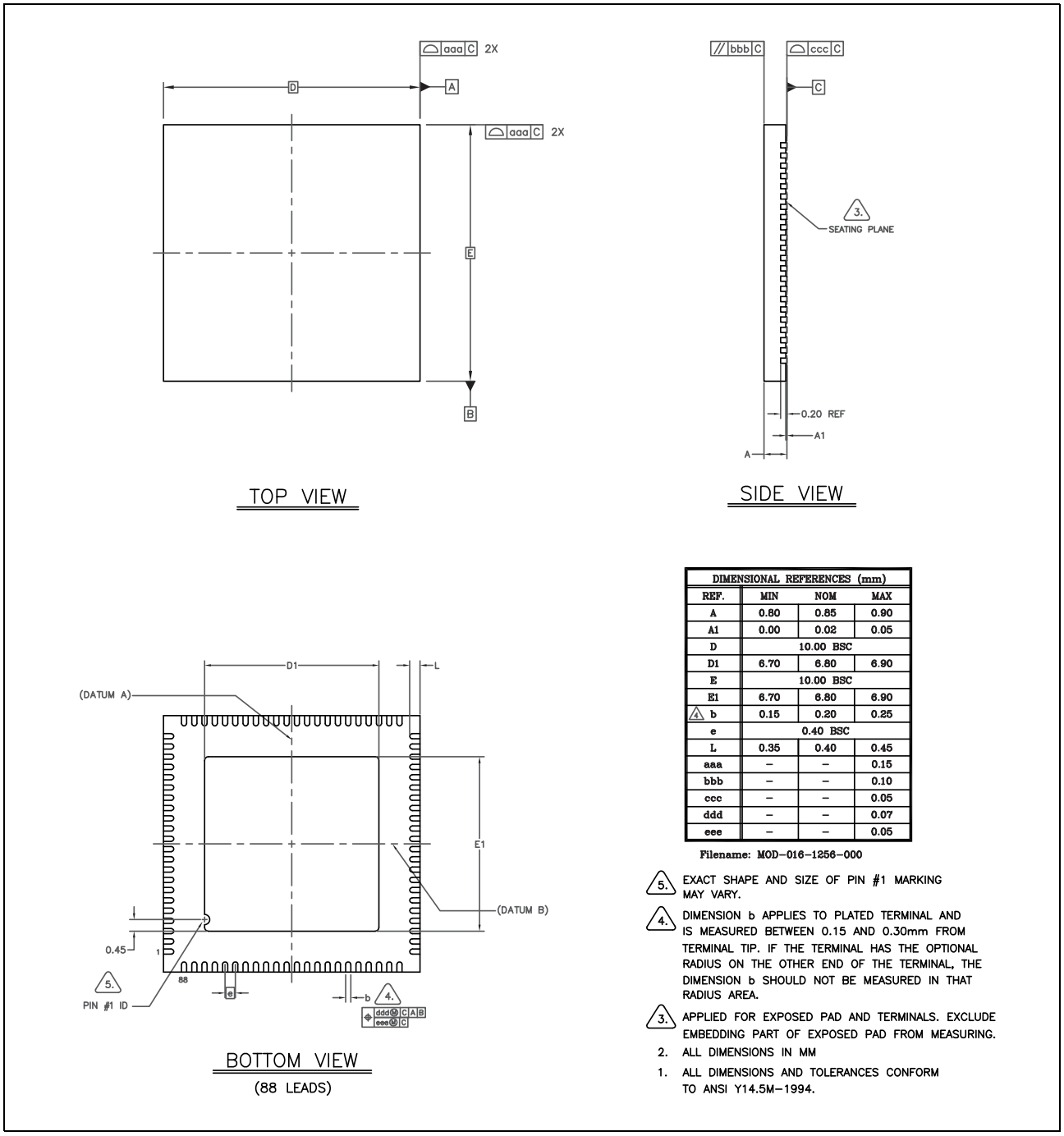
$$T_J = T_T + P \times \Psi_{JT}$$

Where:

- T_J = junction temperature at steady-state condition, °C
- T_T = package case top center temperature at steady-state condition, °C
- P = device power dissipation, Watts
- Ψ_{JT} = package thermal characteristics (no airflow), °C/W

Package thermal characterization measurements: the temperature above the shield is 65°C for T_J to be less than 125°C with a P_{out} of 15 dBm.

Section 9: Package Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
D		10.00 BSC	
D1	6.70	6.80	6.90
E		10.00 BSC	
E1	6.70	6.80	6.90
4. b	0.15	0.20	0.25
e		0.40 BSC	
L	0.35	0.40	0.45
aaa	–	–	0.15
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.07
eee	–	–	0.05

Filename: MOD–016–1256–000

5. EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
2. ALL DIMENSIONS IN MM
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.

Figure 10: BCM43235 Mechanical Drawing

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Section 10: Ordering Information

Table 18: Ordering Information

Part Number	*Package*	*Temperature 1 mm Above the Shield*
BCM43235KMLG	10 × 10, 88-pin QFN (RoHs compliant)	0°C to 65°C (32°F to 149°F)

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