

YC1089-M

High Performance Low Power BR/BLE 5.2 SoC

Preliminary Datasheet

General Descriptions

The YC1089-M is a high performance, low power System-on-Chip (SoC) integrating a Bluetooth® 5.2 compliant 2.4-GHz transceiver, 24 MHz proprietary 32 bit MCU with a RAM of 16 KB and a One-Time Programmable (OTP) memory of 8KB .

The YC1089-M supports Bluetooth Basic Rate, Bluetooth Low Energy and Bluetooth 5.2 features including high-throughput 2 Mbps, Long Range and the Direction Finding. It can be paired through HCI interface with a more powerful MCU for applications requiring advanced wireless connectivity.

The fully-featured multiprotocol radio, +10 dBm output power, -99 dBm sensitivity and extended temperature range of -40 to 110°C makes it suitable for lighting applications.

The YC1089-M features built-in USB, proprietary 32-bit MCU clocked at 24 MHz, integrated capless LDOs supporting 2.1-5.5V supply range, making it a perfect microcontroller for cost-sensitive applications such as mouse devices, toys and disposables.

Key Features

- MCU subsystems
 - 24 MHz 32-bit proprietary MCU for system control and PHY/link layer management
 - AES128 HW encryption
 - Serial wire debug
- Memories
 - 8 KB OTP with internal 6.5V charge pump
 - 16 KB data RAM
 - 8 KB RAM supporting retention mode
- Radio transceiver
 - BR/Bluetooth 5.2/Long Range
 - +10 dBm TX power in 1dB/steps
 - -99 dBm RX sensitivity @ BLE 1 Mbps
 - -96 dBm RX sensitivity @ BLE 2 Mbps
 - Integrated balun with single-ended output and direct connection to antenna
 - 6.3 mA RX system current @ BLE 1 Mbps -99 dBm sensitivity (3V ideal DC-DC converter)
 - 5.9 mA RX system current @ BLE 1 Mbps -97 dBm sensitivity (3V ideal DC-DC conveter)
 - 9.5 mA TX system current (3V ideal DC-DC converter, 0 dBm)
- Power management
 - Always-On (AON) supply: 2.1~ 5.5V
 - Main supply: 1.5 ~ 5.5V supporting external DCDC through a dedicated wakeup pin
 - Integrated LDOs requiring no external decoupling capacitors
 - 3.3V capless LDO
- 1.3 μ A in sleep mode (wake on RTC, no RAM retention)
- 2 μ A in sleep mode (wake on RTC, 4 KB RAM retention)
- Clock generation
 - Dedicated PLL to support 16M/24Mcrystals
 - Crystal trimming
 - 28 MHz RC oscillator for fast wakeup
 - Low jitter low power 32 KHz RC oscillator
- 10-channel 10-bit ADC
- Digital peripherals
 - Up to 23 GPIOs w/ functions fully multiplexed
 - 8 x PWMs up to 48 Mbps
 - Two-wire master (I²C compatible) up to 600 kbps
 - 2 x UART(RTS/CTS) with HCI-H5 protocol up to 3.25 Mbps
 - 2 x SPI Master/Slave up to 24 Mbps
 - 1-axis Quadrature Decoder
 - 12 Mbps Full Speed USB 2.0
- Temperature range: -40°C to +110°C

Applications

- Mouse devices
- Toys
- Lightning applications
- Disposables
- Commercial and industrial applications requiring advanced connectivity

Key Benefits

- Best-in-class sensitivity and output power for RF-demanding applications
- BR for enhanced interoperability
- Lowest system cost for cost-oriented designs

Revision History

Version	Date	Owner	Note
0.1	21/10/2022		Initial version
0.2			
0.3			

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1 Block Diagram

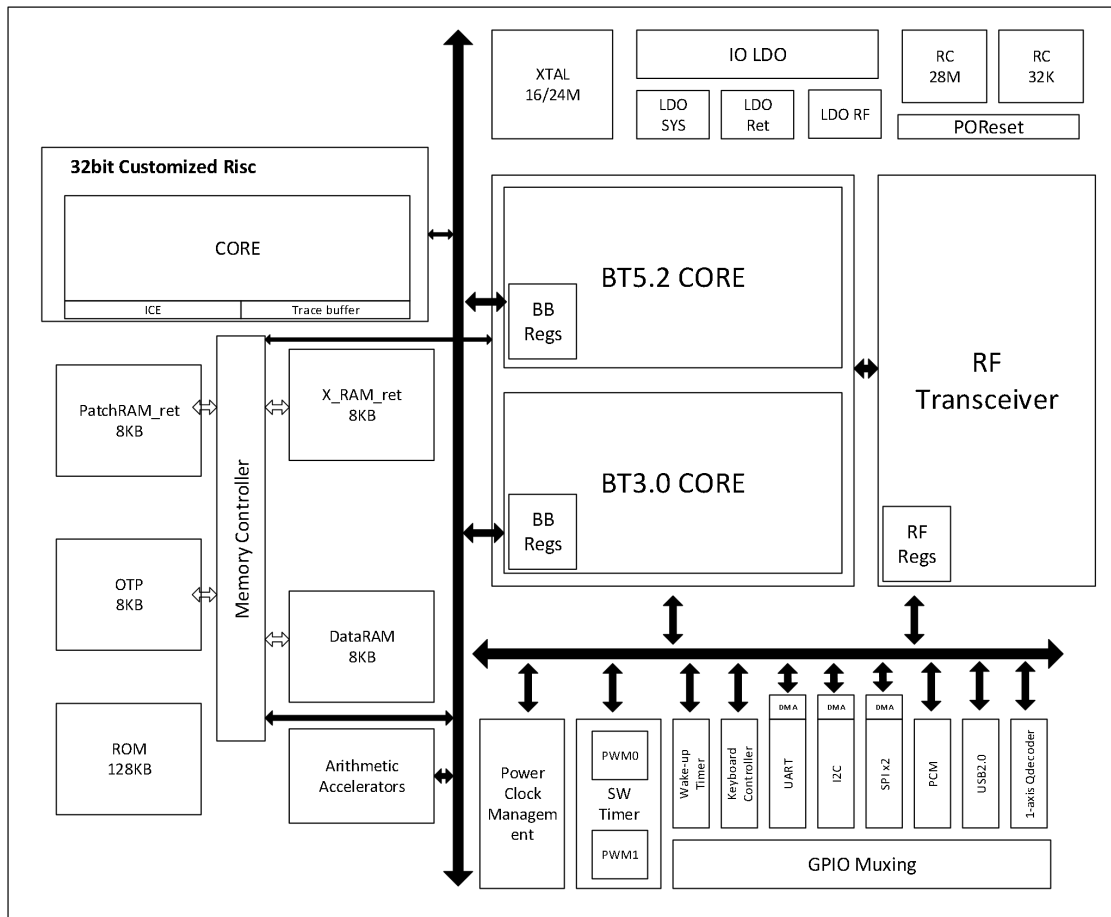


Figure 1- 1 Block diagram

2 Pinout Information

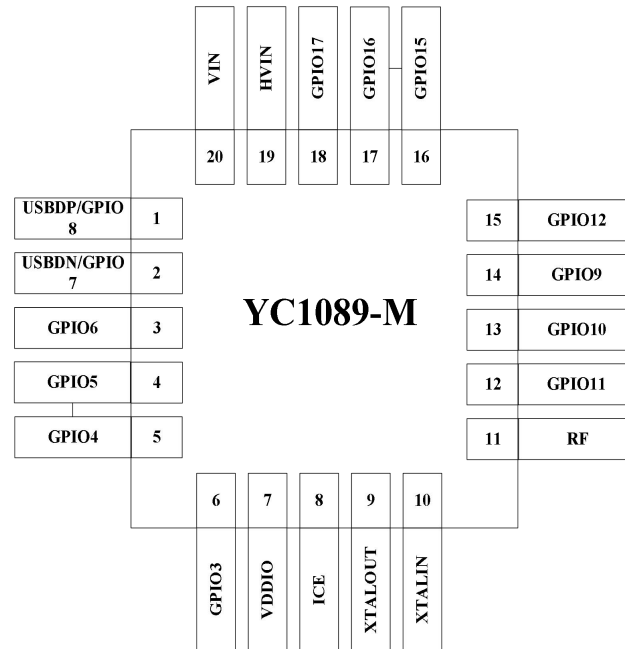


Figure 2- 1 Pinout top view (QFN20 package)

Abbreviations:

PWR: Power pin

AIO: Analog IO pin

DIO: Digital IO pin

RF: RF IO pin

Table 2- 1 Pinout Information

Pin Number	Type	Name	Description
1	DIO	GPIO8/USBDP	Refer to Table 2- 2/USB port.

2	DIO	GPIO7/USBDN	Refer to Table 2- 2/USB port.
3	DIO	GPIO6/ADC	Refer to Table 2- 2
4	DIO	GPIO5/ADC	
5	DIO	GPIO4/ADC	
6	DIO	GPIO3/ADC	
7	DIO	VDDIO	I/O power, 1.8~3.6V, no external capacitor needed
8	DIO	ICE	debug port, Tx & Rx
9	AIO	XTALOUT	XTAL port, or external reference clock input
10	AIO	XTALIN	XTAL port
11	RF	RF	ANT port
12	DIO	GPIO11/ADC	Refer to Table 2- 2
13	DIO	GPIO10/ADC	
14	DIO	GPIO9/ADC	
15	DIO	GPIO12/ADC	
16	DIO	GPIO15	
17	DIO	GPIO16	
18	DIO	GPIO17	
19	PWR	HVIN	Always-on power input, 2.1~5.5V, 1μF bypass cap
20	PWR	VIN	Main power input, 1.5~5.5V, 1μF bypass cap

Note 1 : Drive capability of GPIO[22:2] is up to 15mA, GPIO[1:0] internal pullup & pulldown resistance is 30K~50Kohm, Drive capability of VIO is up to 150mA.

Note 2 : GPIO[22] is by default not gpio function, and is in output high level status after por, which is used as external BUCK enable signal. GPIO[22] will restore gpio function by setting lpm_ctrl[52] to 0.

Note 3 : GPIO[22] can not used as lpm wakeup source.

Note 4 : GPIO[19] is by default in pullup status as ice function after por. GPIO[19] will restore gpio function by setting ice_mode to 0.

Table 2- 2 GPIO Multiplexing

Pin Name	boot function	function-analog
GPIO[0]		
GPIO[1]		
GPIO[2]		
GPIO[3]		
GPIO[4]		saradc [0]
GPIO[5]		saradc [1]
GPIO[6]		saradc [2]
GPIO[7]		saradc [3]
GPIO[8]		
GPIO[9]		saradc [4]
GPIO[10]		saradc [5]
GPIO[11]		saradc [6]
GPIO[12]		saradc [7]

GPIO[13]		
GPIO[14]		
GPIO[15]		
GPIO[16]		
GPIO[17]		
GPIO[18]		
GPIO[19]	ICE	
GPIO[20]		
GPIO[21]		
GPIO[22]	EXEN	

3 Specifications

3.1 Recommended Operating Conditions

Table 3- 1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage for pin VBAT	V_{BAT}		2.1		5.5	V
Supply voltage for pin VDCDC	V_{DCDC}		1.5		5.5	V
Supply voltage for pin VIO	V_{IO}	VIO supplied by a host chip not VDD33	1.8		3.6	V
Ambient temperature	T_A		-40		110	°C

3.2 Power Consumption

Table 3- 2 Power Consumption Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep						
Current through pin VIN	I_{VIN_SLEEP}	$V_{VIN} = 3.3V$		1.3		μA
	$I_{VIN_SLEEP_4KB_RET}$			2		μA
Current of pin VIN with ideal DC-DC converter	I_{VDCDC_SLEEP}	$V_{DCDC} = 1.2V$		20.0		nA
RX mode 1 Mbps BLE @ -99 dBm sensitivity						
Current through pin VIN	I_{VIN_RX}	$V_{VIN} = 3.3V$	10	11.0	13	mA
Current of pin VIN with ideal DC-DC converter	I_{VDCDC_RX}	$V_{VDCDC} = 1.2V$	5.8	6.3	7.2	mA
RX mode 1 Mbps BLE @ -97 dBm sensitivity						
Current through pin VIN	I_{VIN_RX}	$V_{VIN} = 3.3V$	9.5	10.2	12.5	mA
Current through pin VDCDC	I_{VDCDC_RX}	$V_{VDCDC} = 1.2V$	5.6	5.9	7	mA
TX mode 0 dBm						

Current through pin VIN	I_{VIN_TX}	$V_{VIN} = 3.3V$	17.5	18.0	19.5	mA
Current of pin VIN with ideal DC-DC converter	I_{VDDC_TX}	$V_{VDDC} = 1.2V$	9.2	9.5	10.2	mA

3.3 Radio

All parameters are referred to chip port and measured on the condition of $V_{IN} = 3.3V$ if not stated otherwise.

Table 3- 3 Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	f_{TX}		2402		2480	MHz
Output power	P_{out}		-20.0		10	dBm
Power control step	P_{step}	For part-to-part power calibrations		1		dB
Spurious emissions (@ 4 dBm)	P_{spur}	30 MHz to 1000 MHz		-43.7		dBm
		1 GHz to 12.75 GHz		-31.0		dBm
		47 MHz to 74 MHz		-75		dBm
		87.5 MHz to 108 MHz		-75		dBm
		174 MHz to 230 MHz		-75		dBm
		470 MHz to 862 MHz		-44.0		dBm

Table 3- 4 Receiver Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	f _{RX}		2402		2480	MHz
Out-of-band blocking	OOB	30 MHz – 2000 MHz	-30			dBm
		2003 – 2399 MHz	-35			dBm
		2484 – 2997 MHz	-35			dBm
		3000 MHz – 12.75 GHz	-30			dBm
Basic Rate						
RX sensitivity	P _{SENS_BR}	0.1 % BER		-95		dBm
C/I co-channel	C/I _{CO_BR}	0.1 % BER		7		dB
C/I 1 MHz adjacent channel	C/I _{1_1M}	0.1 % BER		-9		dB
C/I 2 MHz adjacent channel	C/I _{2_1M}	0.1 % BER		-38		dB
C/I ≥3 MHz adjacent channel	C/I _{3_1M}	0.1 % BER		-44		dB
C/I image channel	C/I _{im_1M}	0.1 % BER		-26		dB
C/I image channel + 1MHz	C/I _{im+1_1M}	0.1 % BER		-39		dB
Maximum input signal level	P _{IN_MAX_1M}	0.1 % BER		0.0		dBm
1 Mbps BLE						
RX sensitivity	P _{SENS_1M}	30.8% PER		-99		dBm
C/I co-channel	C/I _{CO_1M}	30.8% PER		3		dB
C/I 1 MHz adjacent channel	C/I _{1_1M}	30.8% PER		-23		dB
C/I 2 MHz adjacent channel	C/I _{2_1M}	30.8% PER		-26		dB

C/I ≥ 3 MHz adjacent channel	C/I_{3_1M}	30.8% PER		-37		dB
C/I image channel	C/I_{im_1M}	30.8% PER		-16		dB
C/I image channel + 1MHz	C/I_{im+1_1M}	30.8% PER		-19		dB
Maximum input signal level	$P_{IN_MAX_1M}$	30.8% PER		0.0		dBm
2 Mbps BLE						
RX sensitivity	P_{SENS_1M}	30.8% PER		-95		dBm
C/I co-channel	C/I_{CO_2M}	30.8% PER		4		dB
C/I 2 MHz adjacent channel	C/I_{2_2M}	30.8% PER		-40		dB
C/I 4 MHz adjacent channel	C/I_{4_2M}	30.8% PER		-47		dB
C/I ≥ 6 MHz adjacent channel	C/I_{6_2M}	30.8% PER		-49		dB
C/I image channel	C/I_{im_2M}	30.8% PER		-17		dB
C/I image channel + 2MHz	C/I_{im+2_2M}	30.8% PER		-20		dB
Maximum input signal level	$P_{IN_MAX_2M}$	30.8% PER		0		dBm

3.4 24 MHz Crystal Oscillator

Table 3- 5 24 MHz Crystal Oscillator Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	f_{XTAL}		16	24		MHz
Crystal frequency tolerance	Δf_{XTAL}		-20		20	ppm
Load capacitance	C_{L_INN}	Programmable via registers		9	12	pF

3.5 LDO Characteristics

Table 3- 6 LDO Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}				5.5	MHz
Output voltage	V_{OUT_SLEEP}	$I_{LOAD}=20$ mA, when input voltage below 3.3V, output equals input		3.35		V
	V_{OUT_ACTIVE}	$I_{LOAD}=100$ μ A, when input voltage below 3.3V, output equals input		3.35		V
Maximum load current	I_{LOAD}	Active mode			100	mA
Output load capacitance	C_L		0		1	μ F
Quiescent current	I_{Q_SLEEP}	doze mode		50		nA
	I_{Q_ACTIVE}	active mode		150		μ A

3.6 Reset Characteristics

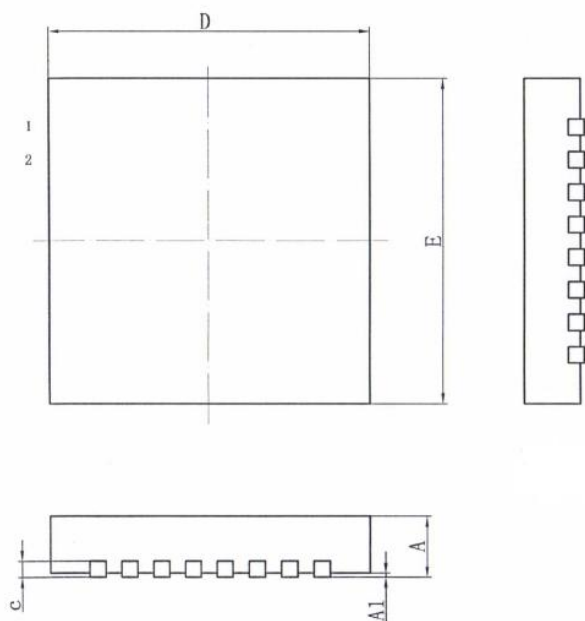
Reset voltage is monitored on pin VBAT_HIGH.

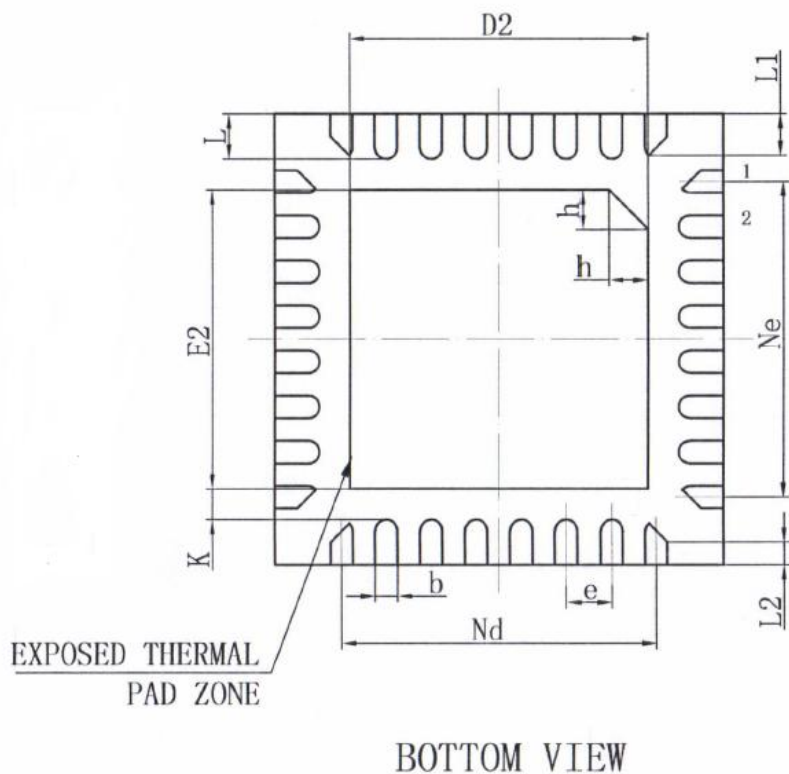
Table 3- 7 Reset Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset voltage threshold	V_{POR}	rising edge	1.55	1.70	2.2	V
	V_{PDR}	falling edge	1.50	1.65	2.15	V
POR stretch time	T_{POR}			20.00		mS
PDR stretch time	T_{PDR}			20		μ S

4 Application Schematic

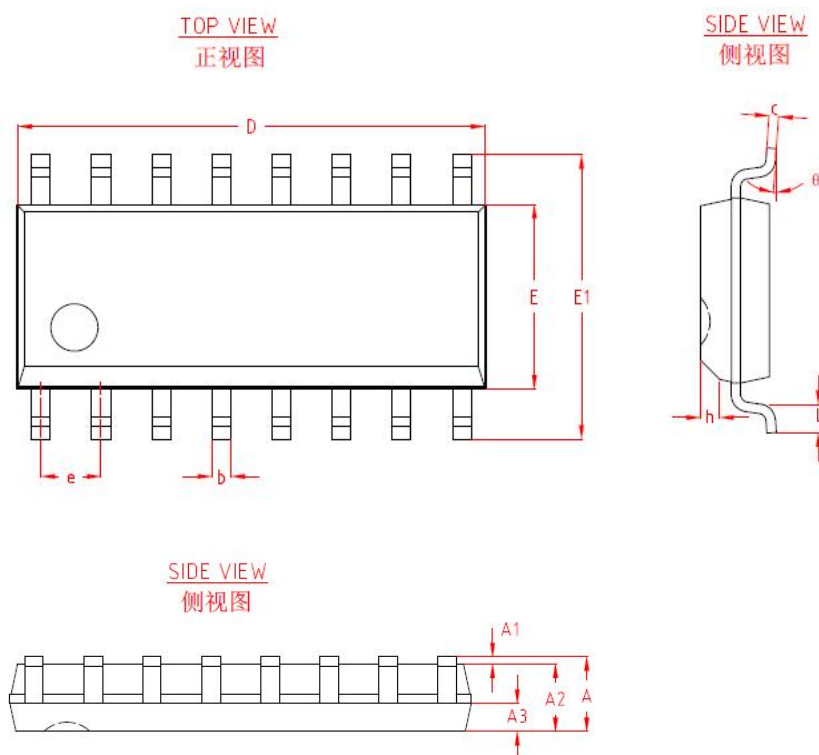
5 Package Information





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	—	—
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/P载体尺寸 (mm)	112*112		

Figure 5- 1 QFN32 package dimensions



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.35	—	0.50
c	0.19	—	0.25
D	9.80	10.00	10.20
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	—	0.50
L	0.40	—	0.80
θ	0°	—	8°

Figure 5- 2 SOP16 package dimensions

FCC Warning:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Caution: Any changes or modifications to this device not explicitly approved by manufacturer could void your authority to operate this equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 0cm between the radiator and your body.