NILE Series - NILE

Bluetooth 5.0/Bluetooth Mesh/Thread/802.15.4 + NFC-A Standalone Module

NILE module Datasheet

Version 1.0

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1 Overview

NILE is an ultra-low power certified full featured Bluetooth 5.0 standalone module. This small form-factor module reduces design cost and time to market by integrating a powerful ARM Cortex-M4 with 1MB FLASH and 256KB RAM, high performance antenna, all the needed components and crystals. NILE with fine-tuned RF provides exceptional performance, long range and very low power. NILE can support 802.15.4 Thread/Zigbee concurrently with Bluetooth. By supporting Bluetooth Mesh, this module reduces the deployment cost and provides flexibility. NILE enables touch-to-pair feature by supporting NFC-A.

NILE reduces user's development cost and time to market with integrated Bluetooth stack, application APIs and all the advanced security features (ARM Trust Zone Cryptocell-310). NILE module is based on Nordic nRF52840 SoC and comes with a highly efficient development environment for ease of application development in various IoT verticals like Wearables, Home automation, Industrial IoT and smart medical.

Module specifications

- Wireless Protocols: Bluetooth 5.0, Thread, Zigbee, NFC
- Frequency: 2.402 – 2.480 GHz
- On-air Data rates:
    - Bluetooth 5 - 2Mbps, 1Mbps, 500kbps, 125kbps
    - 802.15.4 - 250kbps
    - NFC - 106kbps
- Security Features: ARM CryptoCell 310, 128-bit AES HW accelerator, Secure boot and all security features of BLE specification
- Antenna options: PCB antenna or MHF4 connector
- Operating modes: BLE, BLE Mesh (Adopted profiles), 802.15.4 - Zigbee, Thread, BLE + Zigbee, BLE + Thread
- Programmable output power: -40dBm to +8dBm
- Application Peak Throughput: 1317.47Kbps
- Receive Sensitivity: Bluetooth 5.0
    - -103dBm at 125kbps
    - -99dBm at 500kbps
    - -95dBm at 1Mbps
    - -92dBm at 2Mbps
- Receive Sensitivity: 802.15.4
    - -100dBm at 250kbps
- Current consumption:
    - 450nA – Deep sleep mode
    - 1.5µA – System standby mode, no RAM retention
    - Peak current: 4.8mA – TX at 0dBm output power, 4.6mA in RX mode
- Range: > 1400 meters (Line of Sight)
- Power supply and voltage range: 1.7v to 5.5v with integrated DCDC and LDO

- Temperature: -40°C to 85°C
- Humidity: 5-90% non-condensing
- Package: 10 mm x 15 mm x 1.6 mm (including shield), 0.5mm pitch

2 Features

2.1 NILE Features

- Full featured Bluetooth 5.0 - Long Range, 2Mbps, improved co-existence and advertising extensions.
- GPIO: 45 configurable general purpose I/O pins
- Supports advanced mesh networking protocols - Certified software stacks for Bluetooth Mesh, Thread and Zigbee
- Powerful Open CPU: 32bit, 64MHz ARM Cortex-M4 CPU with Floating Point Unit (FPU) and has 1MB flash with cache and 256kB RAM that stands enough for customer's high-end applications
- Support for secure boot, secure erase, BLE secure connections and privacy
- ARM® CryptoCell 310 cryptographic accelerator and AES 128-bit encryption
- Over the air device firmware upgrade (OTA DFU)
- Generic GATT client and server APIs
- Nordic SDK with examples and comprehensive documentation covers all the features supported by the module. SDKs are available for BLE, Bluetooth Mesh, Thread, Zigbee, and HomeKit
- NFC: NFC-A (Type 2) Tag with wake-on field, "Touch to pair" support, OOB pairing
- 1.8V – 3.3V regulated supply output for external peripherals with on/off control

Interfaces

- 2 x UART
- Up-to 4 x SPI master/ 3x SPI slave
- 2 x I2C master, 1 x I2C slave
- 1 x Quad SPI (32Mhz)
- Audio: 1 x I2S, 1 x PDM
- 4 x PWM, 4 channel with easy DMA
- 1 x Quadrature decoder
- 12bit, 8 x ADC channels with programmable gain, 200 ksps
- 64 level comparator, 15 level low power comparator with wake up from system OFF
- 5 x 32-bit timers, 3 x RTC
- 20 channel programmable peripheral interface (PPI)
- 1x USB 2.0 FS (12 mbps)

Certifications

- Regulatory certifications - FCC/IC, ETSI
- BT SIG 5 product level (module) certification

Full Featured Bluetooth 5

It supports all Bluetooth 5 features including long range (125kbps and 500kbps), 2Mbps, advertising extensions and improved co-existence

Bluetooth mesh and Thread support

The NILE is ideal for building products and infrastructure employing mesh networking. It has hardware and software support for Bluetooth mesh with https://www.nordicsemi.com/eng/Products/Bluetooth-low-energy/nRF5-SDK-for-MeshnRF5 SDK for Mesh. It is a Zigbee/Thread certified component and is supported by the https://www.nordicsemi.com/eng/Products/nRF5-SDK-for-ThreadnRF5 SDK for Thread and Zigbee for those building Thread compatible products

Processing power and flash flexibility

The NILE incorporates the powerful ARM Cortex-M4 CPU with Floating Point Unit (FPU) running at 64 MHz enabling the most demanding applications with complex arithmetic requirements to be realized in a single chip solution.

It has got a flash-based SoC and offers all the flexibility associated with using flash memory. It supports Over-The-Air Device Firmware Updates (OTA-DFU) when it is in the field.

On-chip NFC tag support

This module includes a passive NFC tag functionality. It works at 13.56MHz with a data rate of 106kbps. An external NFC reader can read and write data to the module through this interface. Module can't initiate NFC communications or read other NFC tags. This interface can be used to wake-on-field to wake up the module from deep sleep enabling low power applications. Can be used OOB (out of band) pairing with Bluetooth applications to simplify the authentication by carrying authentication information on NFC link.

NFC Applications:

- Advanced high-performance wearable's
- Wearables for secure payments
- Virtual Reality/Augmented Reality systems
- Smart Home sensor networks
- Smart city sensor networks
- High performance HID controllers
- Internet of Things (IoT) sensor networks
- Smart door locks
- Connected white goods

3 Module block Diagram

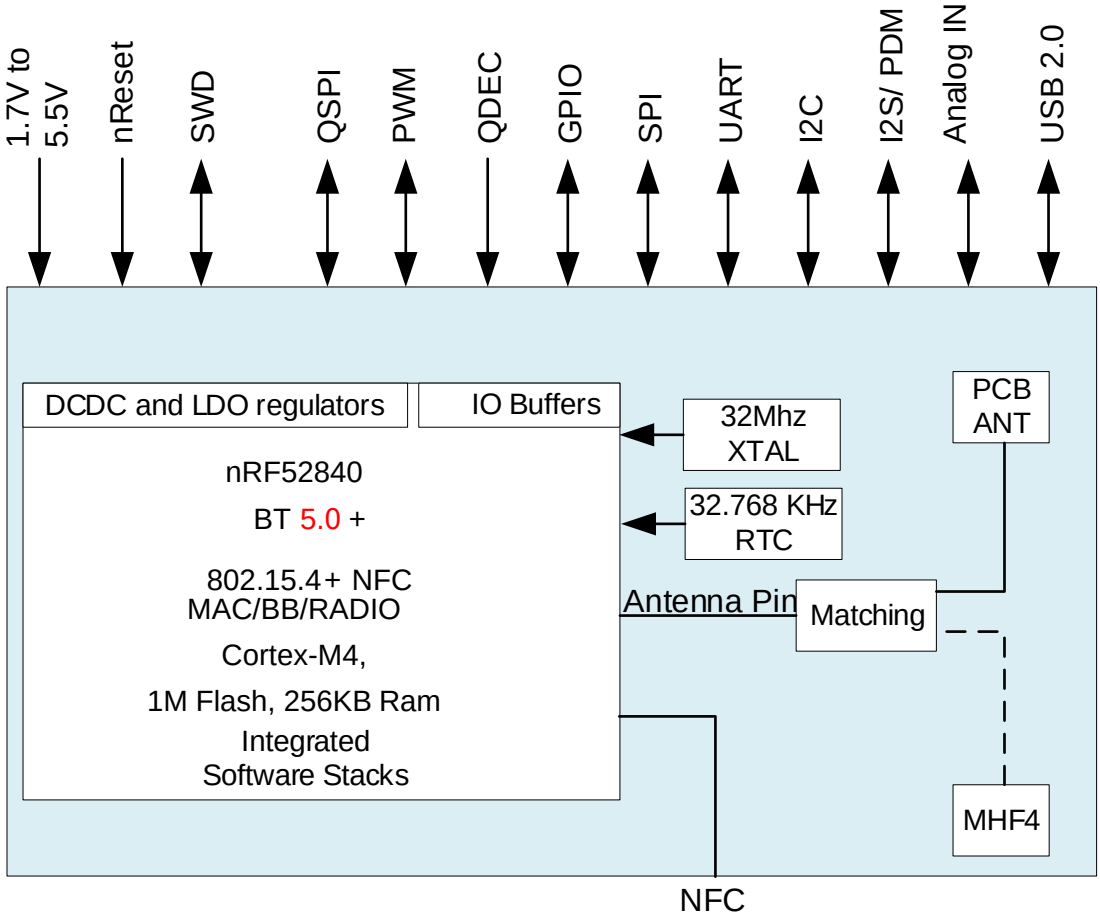

Figure 1 : Block diagram

4 Pin Definition

4.1 Pin-out with description

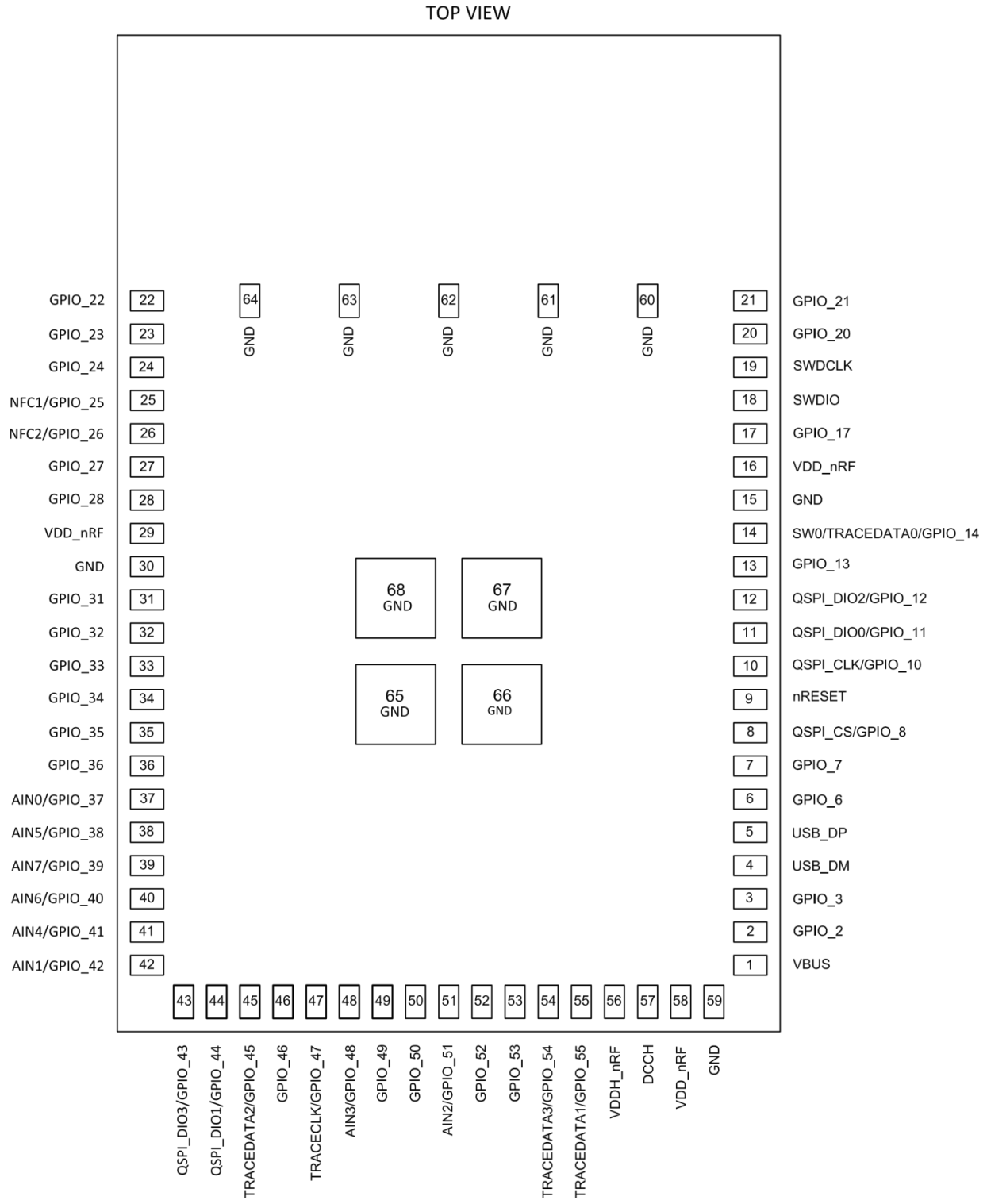

Figure 2 : Showing pin out

4.2 Pin Table

Note: Unless mentioned specifically, any GPIO can be configured to required digital or analog interface.

Pin Number	Pin Name	Pin Type	Description	nRF52 Pin
1	VBUS	Power	5V input from USB	
2	GPIO_2	I/O	General purpose IO	P0.13
3	GPIO_3	I/O	General purpose IO	P0.15
4	USB_DM	AI/AO	Digital I/O USB D+	
5	USB_DP	AI/AO	Digital I/O USB D-	
6	GPIO_6	I/O	General purpose IO	P0.14
7	GPIO_7	I/O	General purpose IO	P0.16
8	QSPI_CS/GPIO_8	I/O	General purpose IO Recommended pin for QSPI_CS	P0.17
9	nRESET	I/O	Active low reset	P0.18
10	QSPI_CLK/GPIO_10	I/O	General purpose IO Recommended pin for QSPI_CLK	P0.19
11	QSPI_DIO0/GPIO_11	I/O	General purpose IO Recommended pin for QSPI_DIO0	P0.20
12	QSPI_DIO2/GPIO_12	I/O	General purpose IO Recommended pin for QSPI_DIO2	P0.22
13	GPIO_13	I/O	General purpose IO	P0.24
14	SWO/TRACEDATA0/GPIO_14	I/O	General purpose IO May be used for parallel/serial trace debug	P1.00
15	GND	Ground	Ground pad	
16	VDD_nRF	Power	3.3V DCDC output Power supply. When 5V input is used, this pin can supply 3.3V accessories (max 20mA drive). 1.7V – 3.6V	
17	GPIO_17	I/O	General purpose IO	P0.25
18	SWDIO	I/O	Serial wire debug I/O for debug and programming	
19	SWDCLK	I	Serial wire debug clock input for debug and programming	
20	GPIO_20	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.01
21	GPIO_21	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.02
22	GPIO_22	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.03
23	GPIO_23	I/O	General purpose IO	P1.04
24	GPIO_24	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.06
25	NFC1/GPIO_25	I/O	May be configured as General-purpose IO if NFC is not used Recommended for Standard drive, low frequency I/O	P0.09
26	NFC2/GPIO_26	I/O	May be configured as General-purpose IO if NFC is not used Recommended for Standard drive, low frequency I/O	P0.10
27	GPIO_27	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.07
28	GPIO_28	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.05
29	VDD_nRF	Power	3.3V DCDC output Power supply. When 5V input is used, this pin can supply 3.3V accessories (max 20mA drive). 1.7V – 3.6V	
30	GND	Ground	Ground pad	
31	GPIO_31	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.14
32	GPIO_32	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.10
33	GPIO_33	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.11

34	GPIO_34	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.12
35	GPIO_35	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.13
36	GPIO_36	I/O	General purpose IO Recommended for Standard drive, low frequency I/O	P1.15
37	AIN0/GPIO_37	AI/IO	General purpose IO / Analog input 0 Recommended for Standard drive, low frequency I/O	P0.02
38	AIN5/GPIO_38	AI/IO	General purpose IO / Analog input 5 Recommended for Standard drive, low frequency I/O	P0.29
39	AIN7/GPIO_39	AI/IO	General purpose IO / Analog input 7 Recommended for Standard drive, low frequency I/O	P0.31
40	AIN6/GPIO_40	AI/IO	General purpose IO / Analog input 6 Recommended for Standard drive, low frequency I/O	P0.30
41	AIN4/GPIO_41	AI/IO	General purpose IO / Analog input 4 Recommended for Standard drive, low frequency I/O	P0.28
42	AIN1/GPIO_42	AI/IO	General purpose IO / Analog input 1 Recommended for Standard drive, low frequency I/O	P0.03
43	QSPI_DIO3/GPIO_43	I/O	General purpose IO Recommended pin for QSPI_DIO3	P0.23
44	QSPI_DIO1/GPIO_44	I/O	General purpose IO Recommended pin for QSPI_DIO1	P0.21
45	TRACEDATA2/GPIO_45	I/O	General purpose IO	P0.11
46	GPIO_46	I/O	General purpose IO	P1.08
47	TRACECLK/GPIO_47	I/O	General purpose IO	P0.07
48	AIN3/GPIO_48	AI/IO	General purpose IO / Analog input 3	P0.05
49	GPIO_49	I/O	General purpose IO	P0.27
50	GPIO_50	I/O	General purpose IO	P0.26
51	AIN2/GPIO_51	AI/IO	General purpose IO / Analog input 2	P0.04
52	GPIO_52	I/O	General purpose IO	P0.06
53	GPIO_53	I/O	General purpose IO	P0.08
54	TRACEDATA3/GPIO_54	I/O	General purpose IO	P1.09
55	TRACEDATA1/GPIO_55	I/O	General purpose IO	P0.12
56	VDDH_nRF	Power	5V external supply (2.5V – 5.5V)	
57	DCCH	Power	First stage DCDC output. Add a 10uH between this pin and pin 16 when 5V DCDC is enabled	
58	VDD_nRF	Power	3.3V DCDC output Power supply. When 5V input is used, this pin can supply 3.3V accessories (max 20mA drive). 1.7V – 3.6V	
59	GND	Ground	Ground pad	
60	GND	Ground	Ground pad	
61	GND	Ground	Ground pad	
62	GND	Ground	Ground pad	
63	GND	Ground	Ground pad	
64	GND	Ground	Ground pad	
65	GND	Ground	Ground paddle	
66	GND	Ground	Ground paddle	
67	GND	Ground	Ground paddle	
68	GND	Ground	Ground paddle	

Table 1: NILE Pin Table

5 Electrical Specifications

5.1 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Parameter	Min.	Max.	Units
Supply voltages			
VDD	-0.3	+3.9	V
VDDH	-0.3	+5.8	V
VBUS	-0.3	+5.8	V
VSS		0	V
I/O pin voltage			
$V_{I/O}$, VDD <=3.6V	-0.3	VDD + 0.3	V
$V_{I/O}$, VDD >3.6V	-0.3	3.9	V
NFC antenna pin current			
$I_{NFC1/2}$		80	mA
Radio			
RF input level		10	dBm
Environmental aQFN™ 73 package			
Storage temperature	-40	+125	^{0}C
Moisture Sensitivity Level		2	
ESD Human Body Model		2	kV
ESD Human Body Model Class		2	
ESD Charged Device Model		750	V
Flash memory			

Endurance		10000	Write/erase cycles
Retention		10 years at 85^{0}C	

Table 2: Absolute maximum ratings

5.2 Recommended operating conditions

The operating conditions are the physical parameters that the module can operate within.

Symbol	Parameter	Min.	Nom.	Max.	Units
VDD	VDD supply voltage, independent of DCDC enable	1.7	3.0	3.6	V
VDD_{POR}	VDD supply voltage needed during power-on reset	1.75			V
VDDH	VDDH supply voltage, independent of DCDC enable	2.5	3.7	5.5	V
VBUS	VBUS USB supply voltage	4.35	5	5.5	V
t_{R_VDD}	Supply rise time (0 V to 1.7 V)			60	ms
t_{R_VDDH}	Supply rise time (0 V to 3.7 V)			100	ms
TA	Operating temperature	-40	25	85	^{0}C
T_J	Junction temperature			90	^{0}C

Table 3: Recommended operating conditions

Important: The module power-on reset circuitry may not function properly for rise times longer than the specified maximum.

5.3 Performance specifications

5.3.1 Radio performance specifications

5.3.1.1 General radio characteristics

Symbol	Description	Min.	Typ.	Max.	Units
f_{op}	Operating frequencies	2360		2500	MHz

$f_{PLL,CH,SP}$	PLL channel spacing		1		MHz
$f_{DELTA,1M}$	Frequency deviation @1 Mbps		±170		kHz
$f_{DELTA,BLE,1M}$	Frequency deviation @BLE 1 Mbps		±250		kHz
$f_{DELTA,2M}$	Frequency deviation @2 Mbps		±320		kHz
$f_{DELTA,BLE,2M}$	Frequency deviation @BLE 2 Mbps		±500		kHz
fsk_{BPS}	On-the-air data rate	125		2000	kbps
$f_{Chip,\ IEEE\ 802.15.4}$	Chip rate in IEEE 802.15.4 mode		2000		kchips

Table 4: General radio characteristics

5.3.1.2 Receiver characteristics

Symbol	Description	Min.	Typ.	Max.	Units
$P_{RX,MAX}$	Maximum received signal strength at < 0.1% PER		0		dBm
$P_{SENS,IT,1M}$	Sensitivity, 1 Mbps nRFmode ideal transmitter[18]		-93		dBm
$P_{SENS,IT,2M}$	Sensitivity, 2 Mbps nRF mode ideal transmitter[19]		-89		dBm
$P_{SENS,IT,SP,1M,BLE}$	Sensitivity, 1 Mbps BLE ideal transmitter, packet length ≤ 37 bytes BER=1E-3[21]		-95		dBm
$P_{SENS,IT,LP,1M,BLE}$	Sensitivity, 1 Mbps BLE ideal transmitter, packet length ≥ 128 bytes BER=1E-4[22]		-94		dBm
$P_{SENS,IT,SP,2M,BLE}$	Sensitivity, 2 Mbps BLE ideal transmitter, packet length ≤ 37 bytes		-92		dBm
$P_{SENS,IT,BLE\ LE125k}$	Sensitivity, 125 Kbps BLE mode		-103		dBm
$P_{SENS,IT,BLE\ LE500K}$	Sensitivity, 500 Kbps BLE mode		-99		dBm
$P_{SENS,IEEE\ 802.15.4}$	Sensitivity in IEEE 802.15.4		-100		dBm

Table 5: Receiver characteristics

[19] Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR [1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3 dB
[20] Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR [1...7] are Used for receiver address correlation, the typical sensitivity for this mode is degraded by 3 dB

[21] As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

[22] Equivalent BER limit < 10E-04

5.3.1.3 Transmitter characteristics

Symbol	Description	Min.	Typ.	Max.	Units
P_{RF}	Maximum output power		8.0		dBm
P_{RFC}	RF power control range		28.0		dB
P_{RFCR}	RF power accuracy			±4	dB
$P_{RF1,1}$	1st Adjacent Channel Transmit Power 1 MHz (1 Mbps)		-24.8		dBc
$P_{RF2,1}$	2nd Adjacent Channel Transmit Power 2 MHz (1 Mbps)		-54.0		dBc
$P_{RF1,2}$	1st Adjacent channel Transmit Power 2 MHz (2 Mbps)		-25		dBc
$P_{RF2,2}$	2nd Adjacent Channel Transmit Power 4 MHz (2 Mbps)		-54.0		dBc
E_{VM}	Error vector magnitude IEEE 802.15.4		8		%rms
$P_{harm2nd, IEEE 802.15.4}$	2nd harmonics in IEEE 802.15.4 mode		-51.0		dBm
$P_{harm3rd, IEEE 802.15.4}$	3rd harmonics in IEEE 802.15.4		-48.0		dBm

Table 6: Transmit characteristics

5.3.1.4 RSSI Specifications

Symbol	Description	Min.	Typ.	Max.	Units
$RSSI_{ACC}$	RSSI accuracy valid range -90 to -20 dBm		±2		dB
$RSSI_{RESOLUTION}$	RSSI resolution		1		dB
$RSSI_{PERIOD}$	RSSI sampling time from RSSI_START task		0.25		µs
$RSSI_{SETTLE}$	RSSI settling time after signal level change		15		µs

Table 7: RSSI

5.3.2 NFC Power and Performance

5.3.2.1 NFCT (Near Field Communication Tag)

Symbol	Description	Min.	Typ.	Max.	Units
I_{sense}	Current in SENSE STATE		100		nA
$I_{activated}$	Current in ACTIVATED STATE		400		µA

Table 8: NFCT power

5.3.2.2 NFCT Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
f_c	Frequency of operation		13.56		MHz
C_{MI}	Carrier modulation index	95			%
DR	Data Rate		106		kbps
V_{sense}	Peak differential Field detect threshold level on NFC1 NFC2		1.2		Vp
I_{max}	Maximum input current on NFCT pins			80	mA

Table 9: NFCT electrical specification

6 Functional description

This section briefly explains the major functional blocks of this module. For extensive details on these functions please refer to the most recent data sheet of the nRF52840 SoC from Nordic Semiconductor.

6.1 Clocks

NILE series module integrates 32MHz and 32KHz crystals for hi-frequency clock (HFCLK, 64MHz) and low-frequency clock (LFCLK, 32KHz).

An integrated RC based low-frequency clock (LFRC) is also available with a reduced accuracy. LFRC needs calibration.

6.2 RESET pin

Module reset can be triggered by following methods

- Power on reset generator
- Pin reset
- Wake up from system off mode
- Soft reset
- Brownout reset

6.3 Real-Time-Counter (RTC)

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). It can generate TICK, OVERFLOW and COMPARE events.

If enabled, a TICK event is generated on each increment of this counter. Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

6.4 CPU and Memory

NILE series modules include a powerful Arm Cortex M4 processor. The processor works with a superset of 16 and 32-bit instructions (Thumb-2) at 64 MHz clock speed. It can use up to 37 interrupt vectors and 3 priority bits. The nRF52840 chip has 1 MB of flash and 256 KB of RAM for code and data storage. Additionally, up to 4 GB of external memory can be added with Execute in Place (XIP) support via the QSPI interface.

RAM can be retained in system OFF/ ON modes. A retained register is a register that will retain its value in System OFF mode and through a reset, depending on reset source.

6.5 DMA

DMA is a module implemented by some peripherals to gain direct access to Data RAM. DMA cannot access the flash. A peripheral can implement multiple DMA instances to provide dedicated channels.

6.6 Security

NILE series module integrates Nordic Semi's nRF52840 SoC. It supports the following security functions

6.6.1 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the Resolvable Private Address Resolution procedure described in *Bluetooth Core Specification* v4.0. Resolvable Private Address generation should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

6.6.2 ACL — Access control lists

The Access control lists (ACL) peripheral is designed to assign and enforce access permissions to different regions of the on-chip flash memory map. The size of the region in bytes is restricted to a multiple of the flash page size, and the maximum region size is limited to half the flash size.

Access control to a configured region is enforced by the hardware two CPU clock cycles after the ADDR, SIZE, and PERM registers for an ACL instance have been successfully written. The protection is only enforced if a valid start address of the flash page boundary is written into the ADDR register, and the values of the SIZE and PERM registers are not zero.

The ADDR, SIZE, and PERM registers can only be written once. All ACL configuration registers are cleared on reset (by resetting the device from any reset source), which is also the only way of clearing the configuration registers. To ensure that the desired permission schemes are always enforced by the ACL peripheral, the device boot sequence must perform the necessary configuration.

Debugger read access to a read-protected region will be Read-As-Zero (RAZ), while debugger write access to a write-protected region will be Write-Ignored (WI).

6.6.3 CCM — AES CCM mode encryption

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in *Bluetooth* terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the four-byte MIC field in one operation. CCM and RADIO can be configured to work synchronously. CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF RFC3610, and depends on the AES-128 block cipher.

The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for Bluetooth Low Energy.

The CCM block uses EasyDMA to load key counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM peripheral supports three operations: keystream generation, packet encryption, and packet decryption. These operations are performed in compliance with the *Bluetooth* AES CCM 128-bit block encryption, see *Bluetooth Core specification Version 4.0*.

6.6.4 CRYPTOCELL

ARM® TrustZone® CryptoCell 310 (CRYPTOCELL) is a security subsystem which provides root of trust (RoT) and cryptographic services for a device.

The following cryptographic features are provided:

- True random number generator (TRNG) compliant with NIST 800-90B, AIS-31, and FIPS 140-2
- Pseudorandom number generator (PRNG) using underlying AES engine compliant with NIST 800-90A
- RSA public key cryptography
    - Up to 2048-bit key size
    - PKCS#1 v2.1/v1.5
    - Optional CRT support
- Elliptic curve cryptography (ECC)
    - NIST FIPS 186-4 recommended curves using pseudorandom parameters, up to 521 bits:
        - Prime field: P-192, P-224, P-256, P-384, P-521
    - SEC 2 recommended curves using pseudorandom parameters, up to 521 bits:
        - Prime field: secp160r1, secp192r1, secp224r1, secp256r1, secp384r1, secp521r1
    - Koblitz curves using fixed parameters, up to 256 bits:
        - Prime field: secp160k1, secp192k1, secp224k1, secp256k1
    - Edwards/Montgomery curves:
        - Ed25519, Curve25519
    - ECDH/ECDSA support
- Secure remote password protocol (SRP)
    - Up to 3072-bit operations
- Hashing functions
    - SHA-1, SHA-2 up to 256 bits
    - Keyed-hash message authentication code (HMAC)
- AES symmetric encryption
    - General purpose AES engine (encrypt/decrypt, sign/verify)
    - 128-bit key size
    - Supported encryption modes: ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM* (CCM* is a minor variation of CCM)
- ChaCha20/Poly1305 symmetric encryption
    - Supported key size: 128 and 256 bits
    - Authenticated encryption with associated data (AEAD) mode
- The CRYPTOCELL subsystem has an internal always-on (AO) power domain for retaining device secrets when CRYPTOCELL is disabled

6.6.5 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128-bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks, and is an asynchronous operation which may not complete if the AES core is busy.

6.6.6 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

6.7 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees

6.8 TIMER — Timer/counter

This peripheral is a general-purpose timer designed to keep track of time in user-selective time intervals. TIMER can operate in two modes: Timer mode and Counter mode.

6.9 Digital Interfaces

6.9.1 UART

UART is a 4-wire serial interface which supports hardware flow control and baud rate up to 1Mbps.

The following UART signals are mapped to physical pins using configuration registers PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD when UART is disabled and used when UART is enabled.

TXD	-	Module output, should be connected to RXD of other device
RXD	-	Module input, should be connected to TXD of other device
RTS	-	Module output, active low flow control signal, set when module can receive data, connected to CTS of other device
CTS	-	Module input, active low flow control signal, module sends data if CTS is set, connected to RTS of other device

Features:

- Full-duplex operation. LSB transmitted first while frame transmission.
- Automatic hardware flow control
- Parity checking and generation for the 9th data bit
- UART uses one or two stop bits.
- UART can be used with EasyDMA for direct data transfer from/to RAM.
- Disable all peripherals that have the same ID as UART. It is important to configure all relevant UART registers explicitly before using UART to ensure proper operation.

Note: Level conversion must be added to use with RS232 level compliant interface.

6.9.2 USB

The USB device (USBD) controller implements a full speed USB 2.0 device function

Features:

- Full speed 12Mbps USB 2.0 controller including on-chip PHY USB transceiver which is powered separately from rest of device.
- Provides CDC driver/Virtual UART as well as usb_audio, usb_hid, usb_generic, usb_msc (mass storage device) classes via Nordic SDK

Pin description:

The signal pins consist of the D+ and D- pins (Pins 5 and 4 of module), which are to be connected to the USB host and will operate only while VBUS is in its valid voltage range (4.35V to 5.5V)

6.9.3 SPI

Supports both Mater and Slave modes. The SPI master can communicate with multiple SPI slaves using individual chip select signals for each slave.

Listed here are the main features for the SPI master:

- EasyDMA direct transfer to/from RAM
- SPI mode 0-3
- Individual selection of I/O pins
- Optional D/CX output line for distinguishing between command and data bytes

Listed here are the main features for the SPI slave:

- EasyDMA
- The SPIS supports SPI modes 0 through 3. The CONFIG register allows configuring these modes.
- Individual selection of I/O pins

Pin description:

- SCLK - Serial clock output from Master and Input to slave
- MOSI - Master Output Slave Input data line
- MISO - Master Input Slave Output data line
- CS - Chip Select output from Master and input to slave. Active low. Selects which slave on the bus is selected.
- The serial clock supports both normal and inverted clock polarity (CPOL) and data should be captured on rising or falling clock edge (CPHA).

6.9.4 I2C interface

Main Features of I2C Interface:

- NILE module can work as either master or slave on I2C bus
- The master is compatible with I2C operating at 100 kHz and 400 kHz.
- Master supports clock stretching performed by the slaves (non-I2C compliant)
- I2C master with EasyDMA is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus. Multi-master not supported
- Supports data rates: 100 kbps, 250 kbps, or 400 kbps
- This I2C interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). SCL is driven by master and SDA can be driven by either master or slave.
- The protocol makes it possible to interconnect up to 127 individually addressable devices.
- Not compatible with CBUS
- The I2C slave operates in a low power mode while waiting for a I2C master to initiate a transfer. As long as the I2C slave is not addressed, it will remain in this low power mode.

Note: Appropriate external pull-up resistors are needed on both these pins for proper operation.

6.9.5 I2S interface

Main Features of I2S Interface:

The I2S (Inter-IC Sound) module, supports the original two-channel I2S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention. The most significant bit (MSB) is always transmitted first.

The I2S peripheral has the following main features:

- Master and Slave mode
- Simultaneous bidirectional (TX and RX) audio streaming
- Original I2S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

Pin description:

- MCK - The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode. The MCK is generated by an internal MCK generator. NILE series modules always provide this clock, LRCK and SCK when in master mode or in slave mode if external master is not able to generate MCK.
- SCK - The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT
- LRCK - The Left Right Clock (LRCK) is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN
- SDIN and SDOUT: Serial data-in and data-out

6.9.6 QSPI interface

The QSPI peripheral provides support for communicating with an external flash memory device using SPI to increase the application space.

Listed here are the main features for the QSPI peripheral:

- Single/dual/quad SPI Input/Output
- 2–32 MHz configurable clock frequency
- Single-word read/write access from/to external flash
- EasyDMA for block read and write transfers
- Up to 16 MB/sec EasyDMA read rate
- Execute in place (XIP) for executing program directly from external flash

6.9.7 PWM interface

The pulse width modulation (PWM) module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

The following are the main features of a PWM module:

- Programmable PWM frequency
- Up to four PWM channels with individual polarity and duty cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty cycle arrays (sequences) defined in RAM
- Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA (no CPU involvement). RAM sequences can be repeated or connected into loops
- Change of polarity, duty cycle, and base frequency possibly on every PWM period. Frequency is adjustable (up to 1 MHz) and the duty cycle can be set over a range from 0% to 100%.

6.9.8 PDM interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (left and right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- Up to two PDM microphones configured as a left/right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- HW decimation filters
- Selectable ratio of 64 or 80 between PDM_CLK and output sample rate

The PDM module illustrated below is interfacing up to two digital microphones with the PDM interface. EasyDMA is implemented to relieve the real-time requirements associated with controlling of the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce pulse code modulation (PCM) samples. The PDM module allows continuous audio streaming.

6.9.9 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors. The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Digital waveform decoding from off-chip quadrature encoder
- Sample accumulation eliminating hard real-time requirements to be enforced on application
- Optional input de-bounce filters.
- Optional LED output signal for optical encoders

6.10 Analog Interfaces

6.10.1 SAADC

Features:

- The SAADC is a differential successive approximation register (SAR) analog-to-digital converter.
- Comprises 8 channels for single ended or 4 channels for differential input
- Each channel can use pins AIN0 through AIN7, the VDD pin, or the VDDH pin as input.
- 8/10/12 bit resolution, 14-bit resolution with oversampling.
- Continuous sampling supported
- Output samples are automatically written to RAM as 16bit 2's compliment values using EasyDMA.
- Individual reference selection for each channel VDD or internal reference.

6.10.2 COMP

Features:

The comparator (COMP) compares an input voltage (VIN+) against a second input voltage (VIN-). VIN+ can be derived from an analog input pin (AIN0-AIN7). VIN- can be derived from multiple sources depending on the operation mode of the comparator differential mode and single ended mode.

The main features of COMP are the following:

- Input ranges from 0 V to VDD
- Single-ended mode: Fully flexible hysteresis using a 64-level reference ladder
- Differential mode: Configurable hysteresis
- Reference inputs (VREF):
    - VDD
    - External reference from AIN0 to AIN7 (between 0 V and VDD)
    - Internal references 1.2 V, 1.8 V, and 2.4 V
- Three speed/power consumption modes: Low-power, Normal and High-speed
- Event generation on output changes
    - UP event on VIN- > VIN+
    - DOWN event on VIN- < VIN+
    - CROSS event on VIN+ and VIN- crossing
    - READY event on core and internal reference (if used) ready

6.10.3 LPCOMP

Low-power comparator (LPCOMP) compares an input voltage against a reference voltage. It can only be used when COMP block is not active.

Listed here are the main features of LPCOMP:

- 0 - VDD input range
- Ultra-low power
- Eight input options (AIN0 to AIN7)
- Reference voltage options:
  - Two external analog reference inputs, or
  - 15-level internal reference ladder (VDD/16)
- Optional hysteresis enable on input
- Can be used as a wakeup source from System OFF mode

In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low-power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

6.11 GPIO

- The NILE series modules support flexible pin configuration. In non-configured state, there will be 46 GPIO pins.
- All interfaces or functions must then be allocated to a GPIO pin before use. 8 out of the 46 GPIO pins are analog enabled, meaning that they can have an analog function allocated to them.
- 2 of the GPIOs are optional NFC pins.

6.12 Debug and Trace interfaces

The module can be programmed and debugged using the two-pin serial wire debug interface SWD on the module. Debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

The main features of the debug and trace system are the following:

- Two-pin serial wire debug (SWD) interface
- Flash patch and breakpoint (FPB) unit that supports:
  - Two literal comparators
  - Six instruction comparators
- Data watchpoint and trace (DWT) unit with four comparators
- Instrumentation trace macrocell (ITM)
- Embedded trace macrocell (ETM)
- Trace port interface unit (TPIU)
  - 4-bit parallel trace of ITM and ETM trace data
  - Serial wire output (SWO) trace of ITM data

6.13 NFCT — Near field communication tag

The NFCT peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

Listed here are the main features for the NFCT peripheral:

- NFC-A listen mode operation
  - 13.56 MHz input frequency
  - Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- Programmable frame timing controller
- Integrated automatic collision resolution, cyclic redundancy check (CRC), and parity functions

To use NFC in NILE, configure pins GPIO25 and GPIO 26 as NFC1 and NFC 2. It will damage the device if you connect the NFC antenna without configuring the pins.
Connect the NFC antenna differentially between the 2 terminals and use external tuning capacitors for best performance.

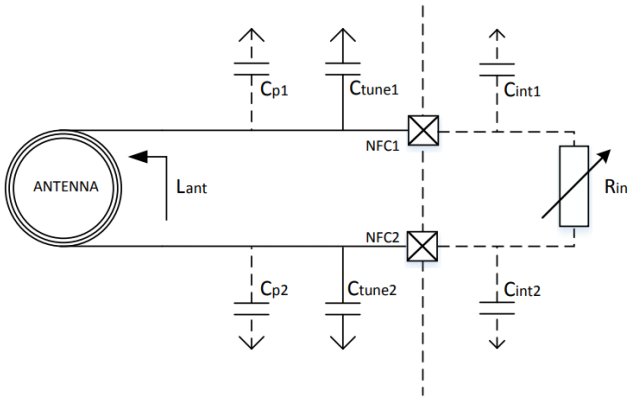

Figure 3: NFCT Antenna tuning

The required tuning capacitor value is given by the below equations:

$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} \quad where\ C'_{tune} = \frac{1}{2} \cdot (C_p + C_{\text{int}} + C_{tune})$$

$$and\ C_{tune1} = C_{tune2} = C_{tune} \qquad C_{p1} = C_{p2} = C_p \qquad C_{\text{int1}} = C_{\text{int2}} = C_{\text{int}}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} - C_p - C_{\text{int}}$$

C_{int} is approximately 4pf. An antenna inductance of Lant = 2 µH will give tuning capacitors in the range of 130 pF on each pin. The total capacitance on NFC1 and NFC2 must be matched. Please check the APP note 'NFC antenna tuning' by Nordic Semiconductor for more information on how to tune antenna.

6.13.1 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures. If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.

6.14 Antenna Interface

NILE module comes with PCB antenna or MHF4 connector. Check with 'NILE series Module Integration Guide (MIG)' for design guide lines to integrate NILE series modules for better performance

6.15 Programmable Peripheral Interconnect

The programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using events and tasks independent of the CPU and reduces the delays and power consumption of the device.

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel.

7 Power management

NILE series modules employ power and resource management to maximize application energy efficiency and battery life. The supply range between 1.7V and 5.5V, supports primary and secondary cell battery technologies and direct USB supply without the need for external regulators. All peripherals have independent and automated clock and power management to ensure they are powered down when not required for task operation to keep power consumption to a minimum without the application having to implement and test complex power management schemes.

7.1 Power Supply options

NILE series modules support multiple power supply options with a built-in DCDC and/or LDO (selected by software configuration).

Normal voltage option: (1.7V to 3.6V)
NILE will be in this mode when power is connected to both VDDH_nRF and VDD_nRF at the same time.

High voltage option: (2.5V to 5.5V)
NILE will be in this mode when power is connected to VDDH_nRF only. In this mode VDD_nRF can be used to supply power to attached peripherals (max 30 amp when module is ON).

Note: When using USB interface, a 5V supply (4.35V to 5.5V) should be connected to the VBUS pin irrespective of Normal voltage or High voltage option. This same supply can be connected to VDDH_nRF in case of High voltage option.

7.2 Power modes

7.2.1 System OFF mode

System OFF is the deepest power saving mode the module can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.
When in System OFF mode, the device can be woken up through one of the following wakeup sources:

1. A reset
2. GPIO interrupt
3. NFC Field (adds 100nA)
4. External analog signal generated by the LPCOMP module
5. Detecting a valid USB voltage on the VBUS pin

The system is reset when it wakes up from the System OFF mode. One or more RAM sections can be retained in System OFF mode. Before entering the System OFF mode, the user must make sure that all on-going EasyDMA transactions have been completed.

7.2.2 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing. The system can switch the appropriate internal power sources on and off, depending on the amount of power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral fluctuates when specific tasks are triggered or events are generated.

7.3 Current consumption numbers

S.No	Case	Min.	Typ.	Max.	Units
1	System OFF, no RAM retention, wake on reset	-	0.4	-	µA
2	System ON, no RAM retention, wake on RTC (running from LFRC clock)	-	1.5	-	µA
3	System ON Idle mode with full RAM retention	-	3	-	µA
4	TX only run current (DC/DC, 3V) PRF = 0 dBm	-	4.9	-	mA
5	RX only run current (DC/DC, 3V) 1 Mbps/1 Mbps BLE	-	4.7	-	mA

Table 10: Current consumption numbers

8 Software architecture

8.1 SoftDevice

NILE series modules support s140 soft device from Nordic Semiconductor.

8.1.1 Overview

The S140 SoftDevice is a Bluetooth Low Energy Central and Peripheral protocol stack solution. The S140 SoftDevice supports running up to twenty connections concurrently, with an additional observer role and broadcaster role. The S140 SoftDevice integrates a Bluetooth Low Energy Controller and Host, and provides a full and flexible API for building Bluetooth Low Energy solutions.

The SoftDevice enables the application developer to develop their code as a standard ARM Cortex -M4 project without having the need to integrate with proprietary IC vendor software frameworks. This means that any ARM Cortex -M4-compatible toolchain can be used to develop Bluetooth Low Energy applications with the SoftDevice. The SoftDevice can be programmed onto compatible nRF52 Series ICs during both development and production

8.1.2 Features

- Bluetooth 5.1 compliant single-mode Bluetooth Low Energy protocol stack
    - Concurrent central, observer, peripheral, and broadcaster roles with up to 20 concurrent connections along with one Observer and one Broadcaster
    - Extended Advertising support
        - Advertising and scanning up to 255 bytes of advertising data in an advertising event
        - Advertising, scanning, and connecting on all supported PHYs
        - Anonymous advertising
    - Configurable number of connections and connection properties
    - Configurable attribute table size
    - Custom UUID support
    - Link layer supporting LE 1M PHY, LE 2M PHY, and LE Coded PHY
    - LL Privacy, including for the Extended Advertising modes
    - LE Data Packet Length Extension
    - ATT and SM protocols
    - L2CAP with LE Credit-based Flow Control
    - LE Secure Connections pairing model
    - GATT and GAP APIs
    - GATT Client and Server
    - Configurable ATT MTU
- Complementary nRF5 SDK including Bluetooth profiles and example applications
- Master Boot Record for over-the-air device firmware update
    - SoftDevice, application, and bootloader can be updated separately
- Memory isolation between the application and the protocol stack for robustness and security
- Thread-safe supervisor-call based API

- Asynchronous, event-driven behavior
- No RTOS dependency
  - Any RTOS can be used
- No link-time dependencies
  - Standard ARM® Cortex® -M4 project configuration for application development
- Support for concurrent and non-concurrent multiprotocol operation
  - Concurrent with the Bluetooth stack using Radio Timeslot API
  - Alternate protocol stack in application space
- Support for control of external power amplifiers and low noise amplifiers
- Quality of service feature for channel monitoring

8.1.3 Software Block diagram

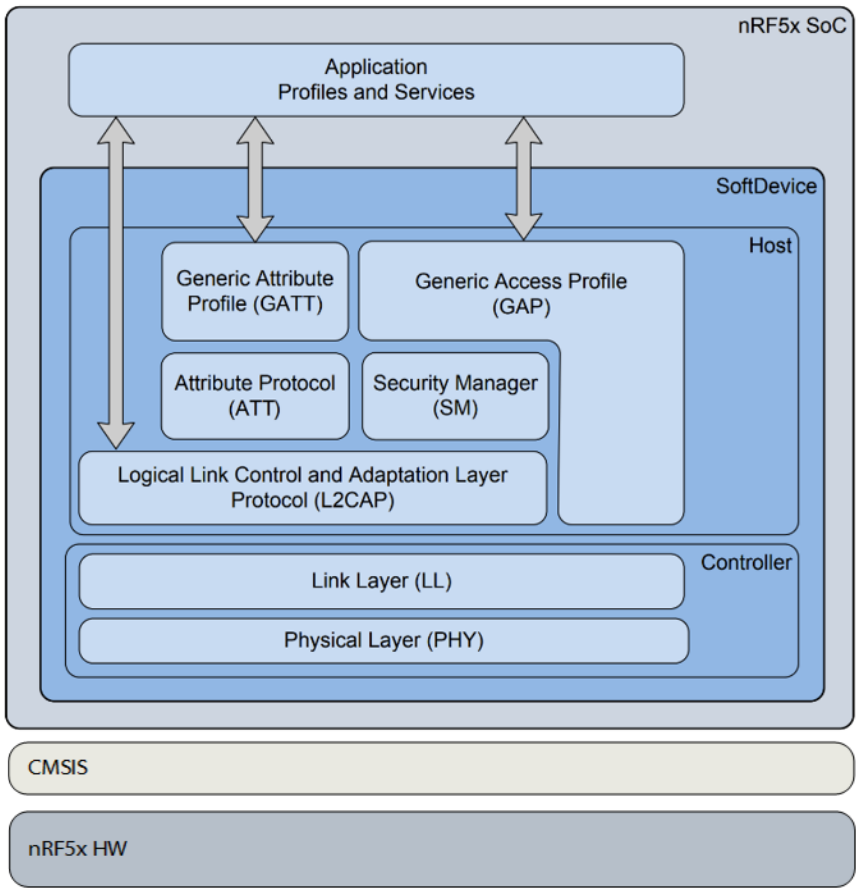

Figure 4: NILE Software Block Diagram

8.1.4 Applications

Few applications supported by this SoftDevice are

- Sports and fitness devices
  - Sports watches
  - Bike computers
  - Fitness machines
- Personal area networks
  - Health and fitness sensor and monitoring devices
  - Medical devices
  - Key fobs and wrist watches
- Home automation
- AirFuel wireless charging
- Remote control toys
- Computer peripherals and I/O devices
  - Mice
  - Keyboards
  - Multi-touch trackpads
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers
- Sensors in remote location

8.2 Software development

Please refer to the NILE EVK User guide for information on how to get started with existing examples testing or developing new applications in standalone and embedded modes.

9 Package Description

9.1 Mechanical characteristics

Parameter	Value (L X W X H)	Units
Module Dimensions	10 X 15 X 1.6	mm
Tolerance	+/- 0.15	mm

Table 11: Mechanical characteristics

9.2 Landing pattern

Please see 'NILE series Module Integration guide (MIG)'

9.3 Physical Dimensions and pad Location

Please see 'NILE series Module Integration Guide (MIG)'

10 Regulatory qualifications and approvals

NILE series modules are certified for FCC, IC and CE/ETSI. Host product manufacturer can leverage the certification of the modular transmitter to reduce their end product certification requirements and complexity as long as they are responsible to follow the integration guidance from Ivativ mentioned in 'NILE series Regulatory Compliance App Note' for any modifications and types of antennas to use. Not following the guidelines from Ivativ will result in the device to be certified afresh. They should perform a limited set of transmitter module verification testing, to ensure the end product is in compliance with the FCC Subpart C, IC and CE/ETSI rules. Also host product manufacturers are responsible for all additional equipment authorization and testing for technical requirements not covered by the module grant (e.g., unintentional radiator FCC Part Subpart B requirements, or transmitters used in the host that are not certified modules).

For detailed information on how to integrate NILE series modules for leveraging the module certification, please see 'NILE series Regulatory Compliance App Note'.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Warning: changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This Module complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator and your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC/RSS rules:
47 CFR Part 15, Subpart C 15.203
47 CFR Part 15, Subpart C 15.205
47 CFR Part 15, Subpart C 15.207
47 CFR Part 15, Subpart C 15.209
47 CFR Part 15, Subpart C 15.247
47 CFR Part 2.1091
RSS-247

11 Product Shipping, Storage and Handling

11.1 Package Information

The NILE series modules are delivered as hermetically sealed trays and reels. For more information, please refer to 'Ivativ Package Shipping, Storage and Handling Guide'.

11.2 Storage and Baking Instructions

NILE series modules are moisture sensitive devices and are rated at MSL 3. The new packages contain desiccate to absorb moisture and humidity indicator card to display the moisture level maintained during storage and shipment. If the card recommends baking, bake the parts in accordance with JEDEC standard J-STD-033. Floor life for these modules is 168 hours of factory conditions (≤ 30°C, 60% RH). For more information, please refer to 'Ivativ Package Shipping, Storage and Handling Guide'.

11.3 Mounting process and soldering recommendations

Please see 'NILE series Module Integration Guide (MIG)'.

12 Product label and ordering information

The figure below illustrates the marking on the modules which indicates Ivativ logo, model number, date code and lot number. Due to small size of the module label certification IDs are shown only in the user manual and not on the label.

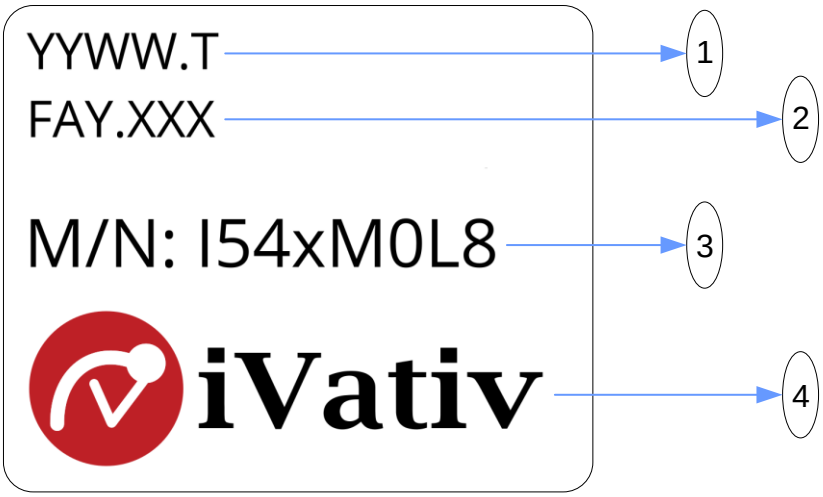

Figure 5: Module Label

The table below describes the markings on the label.

Reference	Description
1	Date Code. YYWW.T: Year/Week/Temp Grade
2	Lot Number. FAY.XXX FAY: Fab, assembly and single digit year of make XXX: Lot number
3	Model number. Where 'x' indicates host interface * 0- PCB antenna(0.5dBi) 1- MHF4 Antenna(Dipole Antenna, 50Ω, 3dBi)
4	Ivativ Logo. Round logo symbol indicates the pin 1, unless marked specifically

Table 12: Module Label Description

*: If you desire to increase antenna gain and either change antenna type or use same antenna type certified, a Class II permissive change application is required to be filed by us, or you (host manufacturer) can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

12.1 Part Ordering

NILE module

I540M0L8-I2LT	NILE multi-protocol module with PCB Antenna, Tray packing
I540M0L8-I2LR	NILE multi-protocol module with PCB Antenna, Tape and Reel packing
I541M0L8-I3LT	NILE multi-protocol module with MHF4 Antenna connector, Tray packing
I541M0L8-I3LR	NILE multi-protocol module with MHF4 Antenna connector, Tape and Reel packing

Table 13: Part Ordering for NILE module

NILE EVK/DVK

I540M0L8-2L-DVK	NILE DVK kit with PCB Antenna
I541M0L8-3L-DVK	NILE DVK kit with MHF4 Antenna connector

Table 14: Part Ordering for NILE EVK/DVK

12.2 Label and compliance information

Please notice that if the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains FCC ID: 2AYLDI54" any similar wording that expresses the same meaning may be used.

§ 15.19 Labelling requirements shall be complied on end user device.
Labelling rules for special device, please refer to §2.925, § 15.19 (a)(5) and relevant KDB publications. For E-label, please refer to §2.935.

12.3 Information on test modes and additional testing requirements

The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.

Note: Control the test sample into engineering mode with the NILE EVK, which could be transmitted continued at the highest, middle & lowest frequency.

12.4 FCC other Parts, Part 15B Compliance Requirements for Host product manufacturer

This modular transmitter is only FCC authorized for the specific rule parts listed on our grant, host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

Host manufacturer in any case shall ensure host product which is installed and operating with the module is in compliant with Part 15B requirements.

Please note that For a Class B or Class A digital device or peripheral, the instructions furnished the user manual of the end-user product shall include statement set out in §15.105 Information to the user or such similar statement and place it in a prominent location in the text of host product manual. Original texts as following:

For Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

For Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

12.5 ISED compliance statement

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

(1) This device may not cause interference.

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) L'appareil ne doit pas produire de brouillage;

(2) L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

12.6 ISED Radiation Exposure statement

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body.

Cet équipement est conforme aux limites d'exposition aux radiations IC CNR-102 établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec une distance minimale de 20 cm entre le radiateur et votre corps. Cet émetteur ne doit pas être colocalisé ou fonctionner en conjonction avec une autre antenne ou un autre émetteur.

Please notice that if the IC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains IC: XXXX" any similar wording that expresses the same meaning may be used.

L'étiquette d'homologation d'un module d'Innovation, Sciences et Développement économique Canada devra être posée sur le produit hôte à un endroit bien en vue, en tout temps. En l'absence d'étiquette, le produit hôte doit porter une étiquette sur laquelle figure le numéro d'homologation du module d'Innovation, Sciences et Développement économique Canada, précédé du mot « contient », ou d'une formulation similaire allant dans le même sens et qui va comme suit :
Contient IC : XXXX est le numéro d'homologation du module

This radio transmitter [IC: XXXX] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Contact Information

Please contact www.ivativ.com