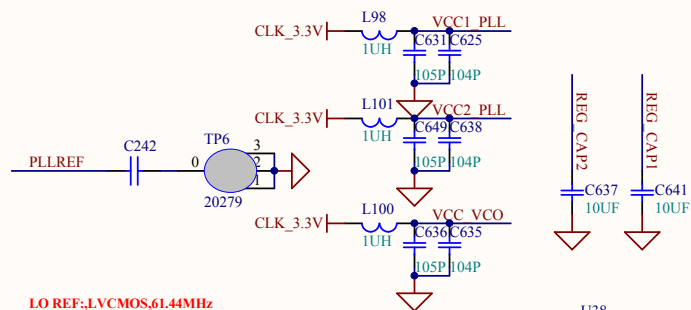
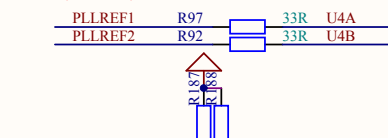


Title			TD_PICO_v2.1		
Size	Number			Revision	
A4				v2.1	
Date:	3/6/2015			Sheet of	
File:	D:_v5_ADC_SchDoc			Drawn By:	Timbo.Ye



LO REF: LVCMOS, 61.44MHz



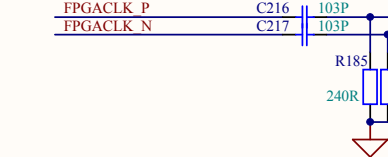
ADC: 122.88MHz: LVDS



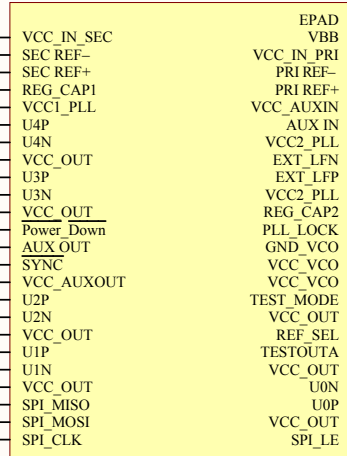
DAC: 122.88MHz: LVPECL



FPGA: 122.88MHz: LVPECL



U38



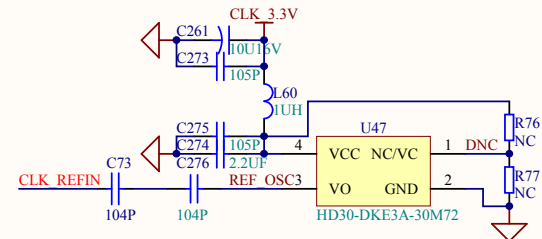
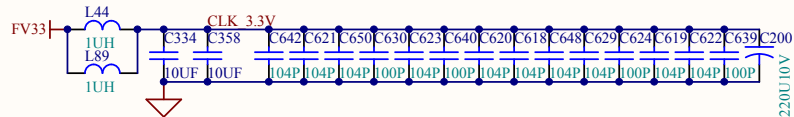
CDCE62005RGZ

CLK LE1

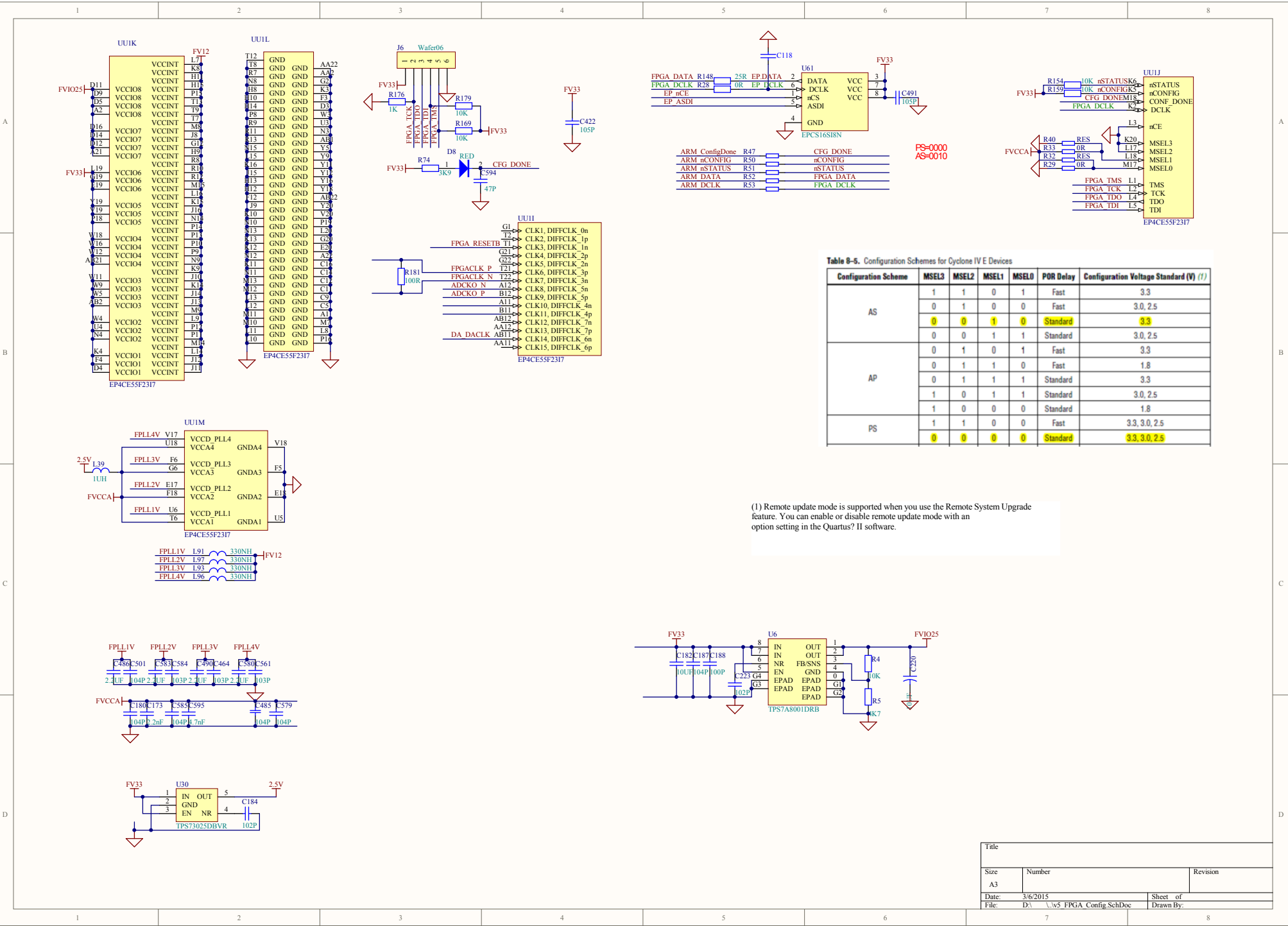
CLK CLK1

CLK MOSI1

CLK MISO1

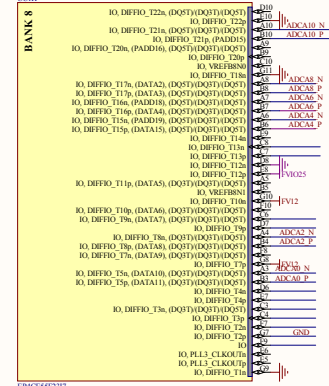
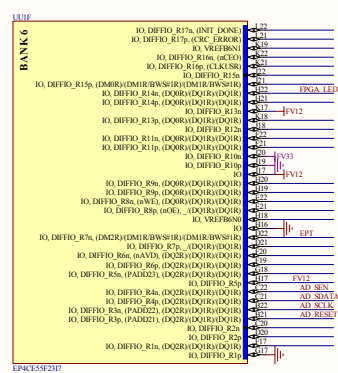
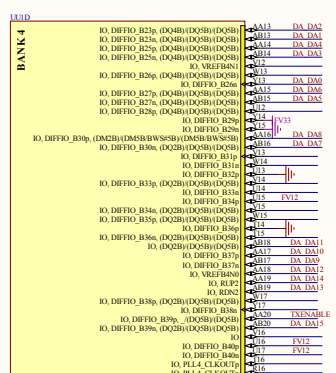
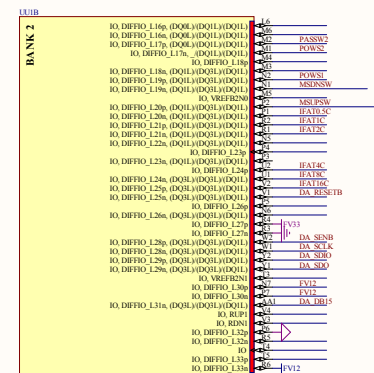
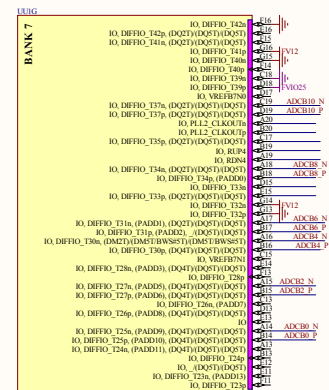
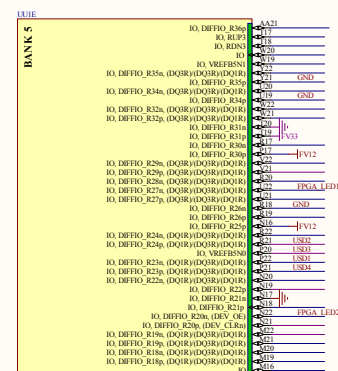
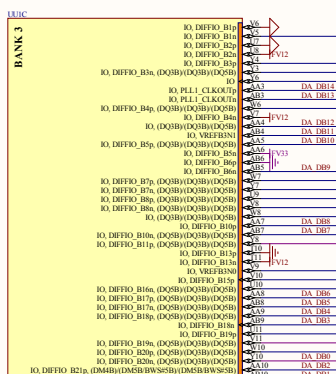
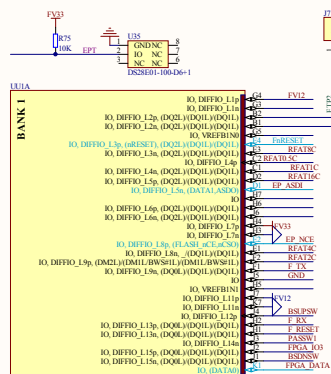


Title			DigPico v1.0_CLK	
Size	Number		Revision	
A4			v1.0	
Date:	3/6/2015		Sheet of	Timbo.Ye
File:	D:\...v5_CLK.SchDoc		Drawn By:	

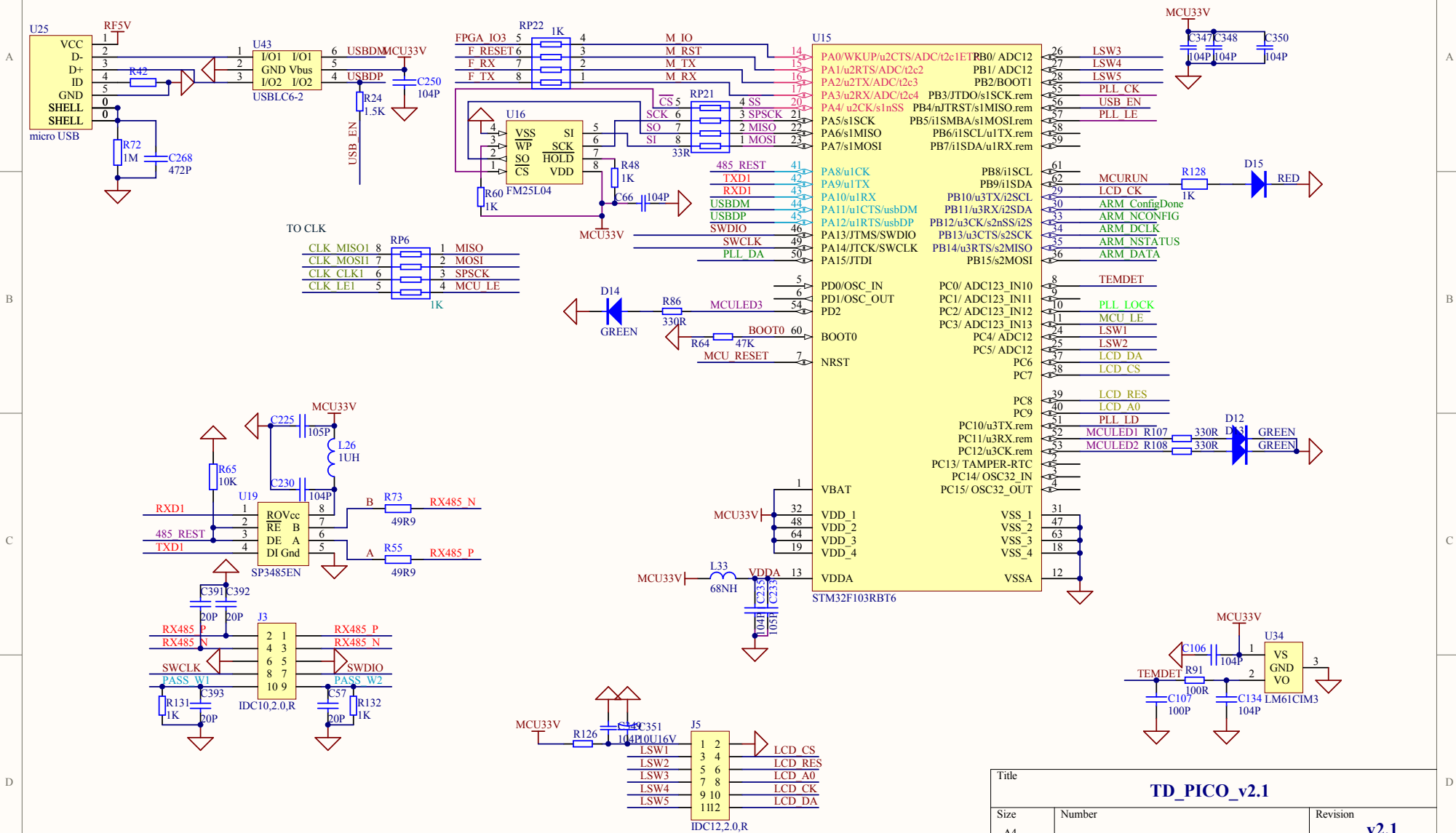


(1) Remote update mode is supported when you use the Remote System Upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus II software.

Title		
Size	Number	Revision
A3		
Date:	3/6/2015	Sheet of
File:	D:\...v5 FPGA Config SchDoc	Drawn By:



Title		
Size A2	Number	Revision
Date 3/6/2015	Sheet of	
File D:\3\5\ FPGAAssn SchDoc	Drawn by	



Title		
TD_PICO_v2.1		
Size	Number	Revision
A4		v2.1
Date:	3/6/2015	Sheet of
File:	D:\v5 MCU.SchDoc	Drawn By: Timbo.Ye

1.RLM6302_P MOS
BSS138_N MOS

Defaut 1: SW2=1, SW1=0, DN ON

TD_P co v2.1

Defaut 1: SW2=1, SW1=0, BS To M6 ON

Title		Revision	
Size	Number	Revision	
A3		Tl rito. Ye	
Date:	3/6/2015	Sheet of	
File:	D:\A\c\5 RF&PLL SchDoc	Drawn By:	