Product Specification

Model Name(HVIN): BTA65AI, BTA65BI, BTA65CI, BTA65DI, BTA65TI
BTA65AE, BTA65BE, BTA65CE, BTA65DE, BTA65TE

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BTA65 Specification

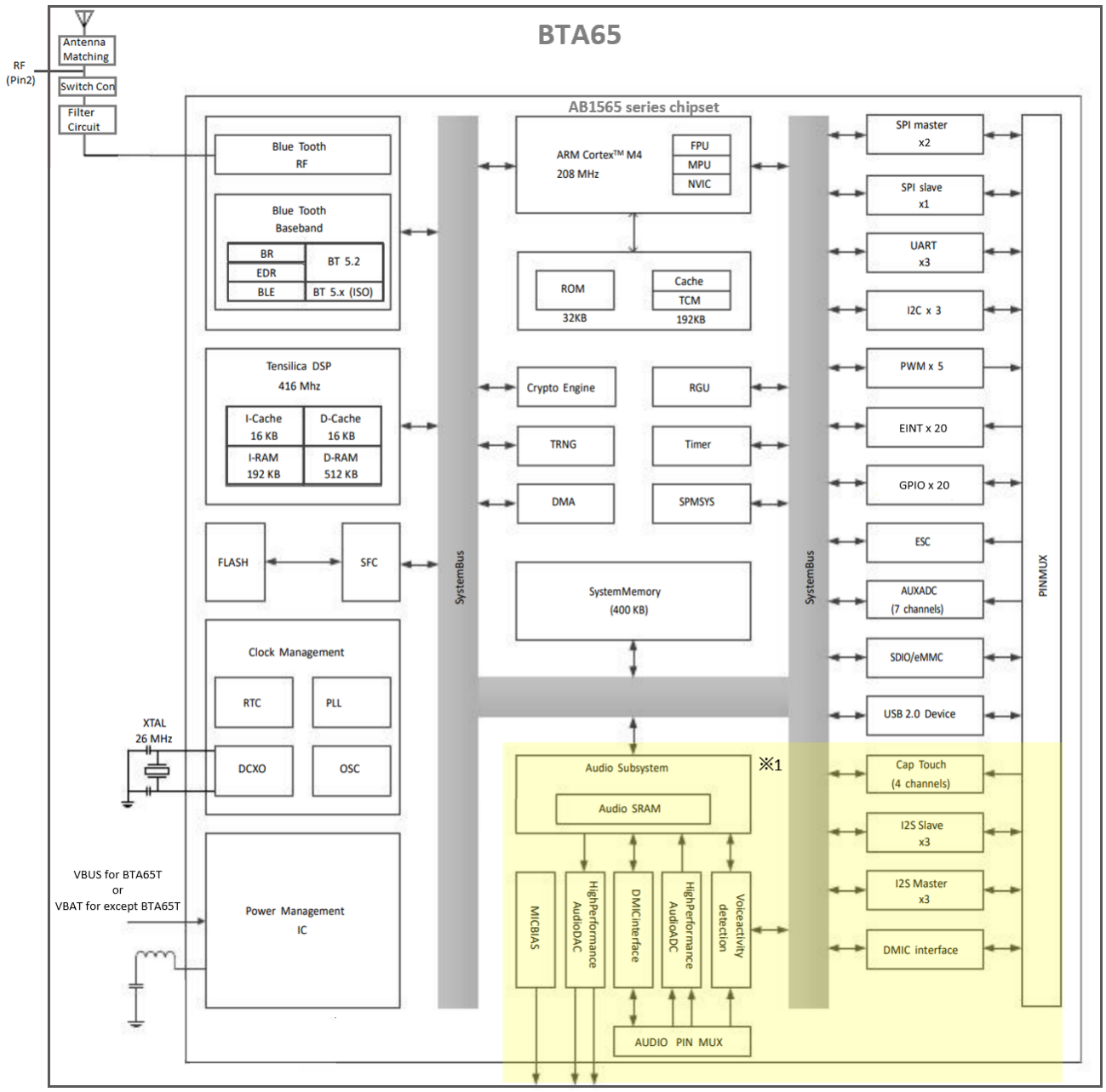
Change History

Version	Date	Change Descriptions
0.1	2022-06-01	First version
0.2	2022-09-08	Updated [5 Module size]
0.3	2022-11-02	Modified part number description mistakes in [1.1 Features] Modified pitch size information in [5 Module size] Updated [3.2 Functional specification] Updated [10 Module label specification]
0.4	2022-12-13	Updated [2.3.1 Audio downlink (Analog part)] Updated [3.2 Functional specification] Updated the photo in [4 Pin description]
0.5	2023-11-20	Updated module block diagram in [1 Product description] Updated module size information in [1.1 Features] Updated [1.2 Product family] Updated [4 Pin description] Updated [5 Module size] Updated [6 Electrical specification] Updated [7.1 Internal antenna performance] Updated [7.2 Antenna application note] Updated [10 Module label specification] Updated [11 Package]
0.6	2024-03-25	Updated [3.2 Functional specification] Updated [1.2.1 BTA65 series part number]
0.7	2024-07-20	Modified Bluetooth core version in [1.1 Features] Updated [9.1 Bluetooth BQB certification] Added [9.2 Radio Certification] Updated [10. Module label specification]
1.0	2024-08-12	Updated [7 Antenna type, performance and application note] Updated [9.2 Radio Certification]

Contents

1 Product description

The BTA65 series module, intended for Bluetooth audio applications, integrates the ARM® Cortex™ - M4F, PMU, DSP, BT and audio functions into a single chip. The Tensilica HiFi Mini DSP is a general processor and used for audio data processing. The Bluetooth RF, integrating the balun and the band pass filter, provides good Tx/Rx performance. High performance audio drivers and hardware active noise cancellation circuits are also included for better audio quality.



※1: BTA65T module doesn't include the yellow part block.

1.1 Features

Host processor

- ARM® Cortex®-M4 with Floating Point Unit (FPU) and Memory Protection Unit (MPU)
- Maximum speed: 208MHz
- 192KB memory with zero wait state. It can be programmed as L1 cache or Tightly Couple Memory(TCM)
- Configurable L1 cache size: 32KB, 16KB, 8KB or 0KB
- Execute In Place (XIP) on flash memory

DSP processor

- Cadence® HiFi Mini Audio Engine DSP coprocessor with HiFi EP® extension
- Maximum speed: 416MHz
- 16KB instruction cache and 16KB data cache with high hit rate and zero wait state
- 192KB instruction RAM with zero wait state
- 512KB data RAM with zero wait state

Memory

- Low latency 400KB system RAM (SYSRAM) with maximum speed 208MHz
- On-die memories (SRAMs) with up to 192KB at CPU clock speed with zero wait state
- SiP low-power flash with maximum speed 104MHz
- BTA65A, BTA65B, BTA65T: 32Mbit
- BTA65C, BTA65D: 64Mbit

Peripheral

- USB2.0 device
- MSDC (eMMC4.41 / SDIO v2.0) up to 48MHz
- I2C interfaces up to 3.4MHz
- UART interfaces up to 3Mbps
- SPI master interface up to 52MHz
- 12-bit AUXADC channels
- PWM channels
- Capacitive Touch

Bluetooth

- Fully compliant with Bluetooth core specification 5.3
- Low-IF architecture with high degree of linearity and high order channel filter
- Integrated T/R switch and balun
- Fully integrated PA provides 10dBm output power
- -96dBm sensitivity with interference rejection performance
- Baseband support for dual mode (Bluetooth and LE) and isochronous channel
- Support for BLE 1M/2M

Audio

- Three uplink paths with analog/digital microphone input mode. The maximum sample rate is 192KHz
- One downlink path with maximum 192KHz sample rate
- Class AB amplifier
- Side-tone filter
- Two channel memory-based asynchronous sampling rate converter
- Hardware Active Noise Cancellation (ANC)
  - Feedforward ANC
  - Hybrid ANC (only BTA65B and BTA65D support)
- Hardware gain control
- I2S master or slave modes
- Voice detection

Power management

- Wide Li+ battery voltage from 3V to 4.8V
- Linear Battery Charger
  - Power Path Management
- Support for power key and reset function
- Support for hardware long press shutdown
- Over-current and thermal overload protection
- Under voltage lockout protection
- Support VBUS UART communication

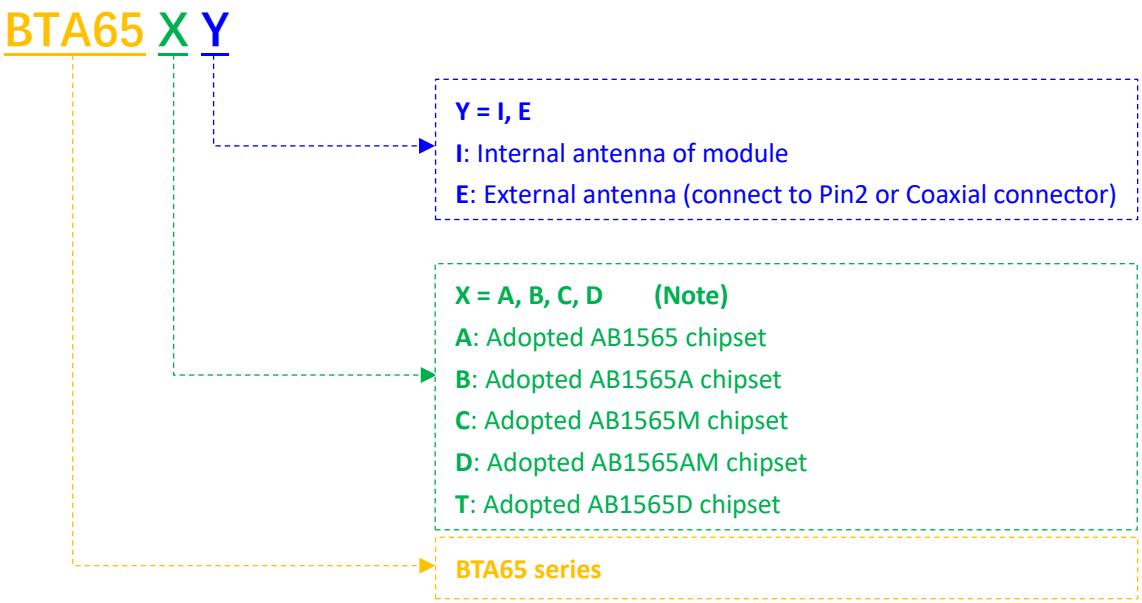
Package

- Stamp hole package, 23.5 x 12.6 x 2.2mm, 54pins

1.2 Product family

The BTA65 series provides several modules for different product requirement. Following table shows the differences and comparison of BTA65 series modules.

1.2.1 BTA65 series part number



Note: These chips(AB1565, AB1565A, AB1565M, AB1565AM, AB1565D) has the same package, belong to pin to pin compatible.

1.2.2 Product family comparison

Model Name (HVIN)	BTA65AI BTA65AE	BTA65BI BTA65BE	BTA65CI BTA65CE	BTA65DI BTA65DE	BTA65TI BTA65TE
Internal Flash Size	32Mbit	32Mbit	64Mbit	64Mbit	32Mbit
SRC/SINK Mode	SINK	SINK	SRC,SINK	SRC,SINK	SRC
LE Audio	No	No	Yes	Yes	Yes
Hybrid ANC	-	Yes	-	Yes	-

1.3 Target application

■ Bluetooth speakers ■ Bluetooth headphones ■ Bluetooth Transmitter

■ Soundbar/AV Receiver ■ Musical Instrument Amplifier

2 Functional description

2.1 Platform description

2.1.1 ARM® Cortex®-M4 with FPU

The Cortex-M4 with FPU is a low-power processor with 3-stage pipeline Harvard architecture. It has a reduced pin count with low power consumption and efficiently delivers high-performance and with low interrupt latency, making it ideal for embedded microcontroller products.

The processor incorporates:

- IEEE754-compliant single-precision floating-point computation unit (FPU).
- A Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing.
- Enhanced system debugging with extensive breakpoint.
- An optional Memory Protection Unit (MPU) to ensure platform security robustness.

The Cortex-M4 executes the Thumb®-2 instruction set with 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers. The instruction set is fully backward compatible with Cortex-M3/M0+.
BTA65 has further enhanced the Cortex-M4 with FPU to reduce the power by another 11% compared to the original Cortex-M4. Low power consumption is a significant feature for IoT and wearables application development.

2.1.2 DSP host processor subsystem

The DSP host processor uses Cadence Hifi Mini DSP audio processor as the CPU core.

The Cadence HiFi Mini DSP is a highly optimized audio processor geared for efficient execution of audio, voice codecs, as well as pre- & post-processing modules. The HiFi Mini DSP is part of the Xtensa LX processor family.

HiFi Mini is an enhanced version of the HiFi 2 architecture, and is especially suited for extremely low

power voice recognition as well as voice processing.

DSP host processor includes the HiFi EP Audio Engine DSP extension configuration option extending the HiFi 2 Audio Engine ISA with 32x24-bit multiply/accumulate operations, circular buffer loads and stores, a slot 0 select unit and bidirectional shifts.

2.2 Peripheral description

The following interfaces are multiplexed with GPIO.

Peripheral	Counts	Description
GPIO	20	Can be used as other functions
UART	3	Up to 3Mbps, Only UART0 and UART1 can support the flow control feature (RTS/CTS)
I2C	3	Master mode, 400kbps, up to 3.4Mbps
SPI Master	2	Clock up to 52MHz
SPI Slave	1	Clock up to 52MHz
USB	1	USB 2.0 device
eMMC/SDIO	1 master	MSDC: SDIO card v2.0, up to 48MHz, 1-bit/4-bit mode eMMC4.41, no booting and no support for DDR mode
AUXADC	7-channel	12-bit ADC, pin mux by AGPIO
PWM	5	Maximum toggle rate 24MHz

2.2.1 General purpose input/output (GPIO)

The pin multiplexing and general purpose input/output:GPIO controls connections and function. Each pin can function as GPIO to implement a variety of external function. Each pin can also work as an external interrupt (EINT) source to trigger interrupt when a transition is detected on the input. In addition, each pin is connected to up to six additional functions, with the selection controlled by the pin multiplexing module.

There are several modes for each I/O pad, including one GPIO mode and one EINT mode.
In GPIO mode, the Cortex-M4 can control the direction and output value of each pin, as well as read the input value. In EINT mode, an interrupt can be triggered when a transition is detected on the input.

The characteristics of I/O pin are configurable, including driving strength, pull-up/down resistance.

2.2.2 Universal asynchronous receiver/transmitter (UART)

The universal asynchronous receiver transmitter (UART) provides full duplex serial communication channels between the baseband chipset and external devices.

The UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bit, and is fully programmable by an 8-bit CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included with separate transmit and receive FIFOs. Two modern control lines and diagnostic loop-back mode are provided.
The UART also includes two DMA handshake lines, indicating when the FIFOs are ready to transfer data to the CPU.

・There are three UART channels, UART0, UART1, and UART2, supporting software flow control. All UART channels can support hardware flow control. Each UART has an individual interrupt source.

・For transmission, the UART supports word lengths from 5 to 8 bits with and optional parity bit and 1 to 2 stop bits.

・The UART supports standard baud rates of 110bps, 300bps, 1200bps, 2400bps, 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps, and non-standard baud rates from 110bps to 3Mbps.

・There are dedicated DMA channels for both transmit (TX) and receive (RX) for each UART.

・The UART supports automatic baud rate detection in RX mode. The recommended bard rate range is between 110bps and 115200bps.

2.2.3 Inter-integrated circuit controller (I2C)

Inter-Integrated Circuit (I2C) is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports mster role and conforms to the I2C specifiction.

・I2C compliant master mode operation

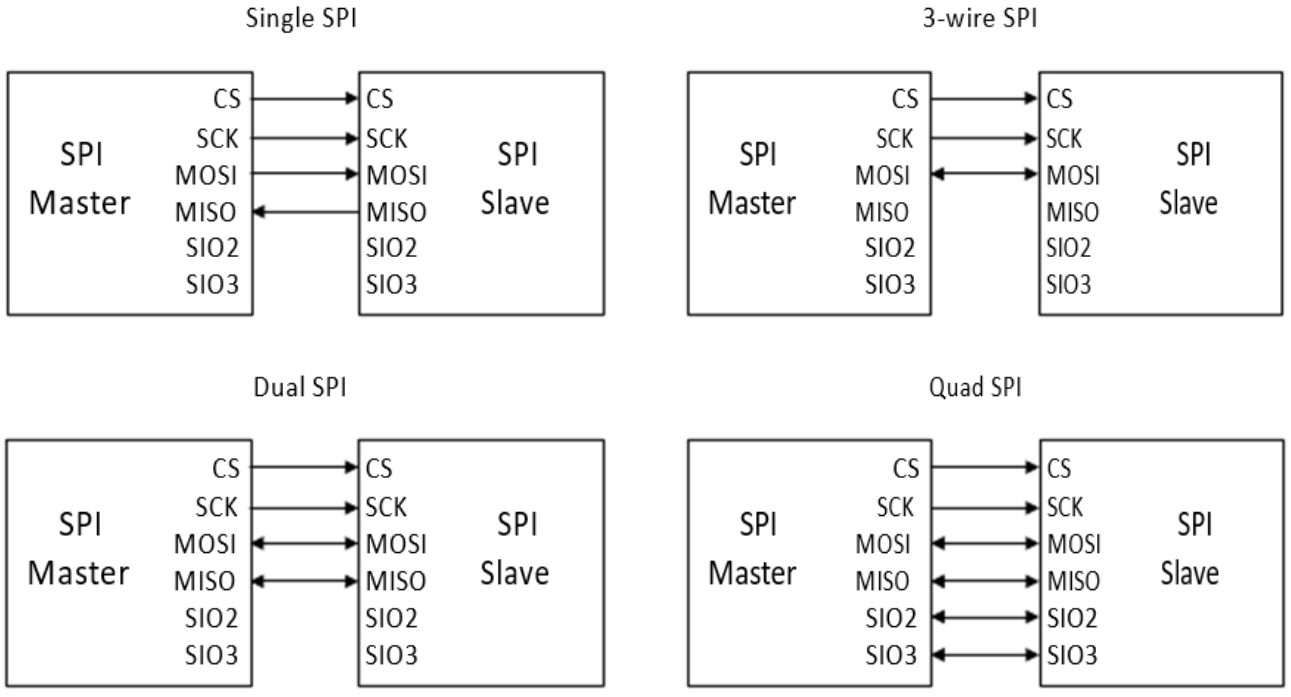
・Adjustable clock speed for Low-Speed and Fast-Speed mode operations

・Support for 7-bit/10-bit addressing

- Support for high-speed mode
- Support for slave clock extension under open-drain mode
- START/STOP/REPEATED START condition
- Multi-write per transfer (up to 65535 data bytes)
- Multi-read per transfer (up to 65535 data bytes)
- Multi-transfer per transaction (up to 65535 data bytes)
- Combined format transfer with length change capability

2.2.4 Serial peripheral interface (SPI)

The Serial Peripheral Interface (SPI) is a serial transmission protocol which supports single mode (fo ur-pin), 3-wire mode (three-pin), dual mode (four-pin) and quad mode (six-pin) for increased data throughput. The maximum serial clock (SCK) frequency is 52MHz. Note that single mode can support full duplex, but 3-wire, dual and quad mode only support half duplex. Following figure is an example of the connection between the SPI master and SPI slave. Following table shows the characteristic of each pin.



Signal Name	Type	Default value	Description
CS	O	1 (output)	Active low chip selection signal
SCK	O	0 (output)	Serial clock
MOSI	I/O	1 (output)	Data signal 0
MISO	I/O	Pull down (input)	Data signal 1
SIO2	I/O	1 (output)	Data signal 2
SIO3	I/O	1 (output)	Data signal 3

2.2.5 USB 2.0 high-speed device controller

USB2.0 controller support HS (480M)/FS(12M), The USB controller is configured for supporting 2 end points to receive packets and 4 endpoints to send packets except for endpoint 0. These endpoints can be individually configured in the software to manage either Bulk transfers, Interrupt transfers or Isochronous transfers. There are four DMA channels and the embedded RAM size is configurable size up to 3264 bytes. The embedded RAM can be dynamically configured to each endpoint.

Feature list	Description
Speed	High speed(480Mbps) / Full speed(12Mbps)
Enhanced feature	Generic Device
Endpoint	4 Tx 2 Rx
DAM channel	4
Embedded RAM	3264

2.2.6 eMMC/SD/SDIO card controller (MSDC)

The eMMC/SD/SDIO card host controller (MSDC) supports:

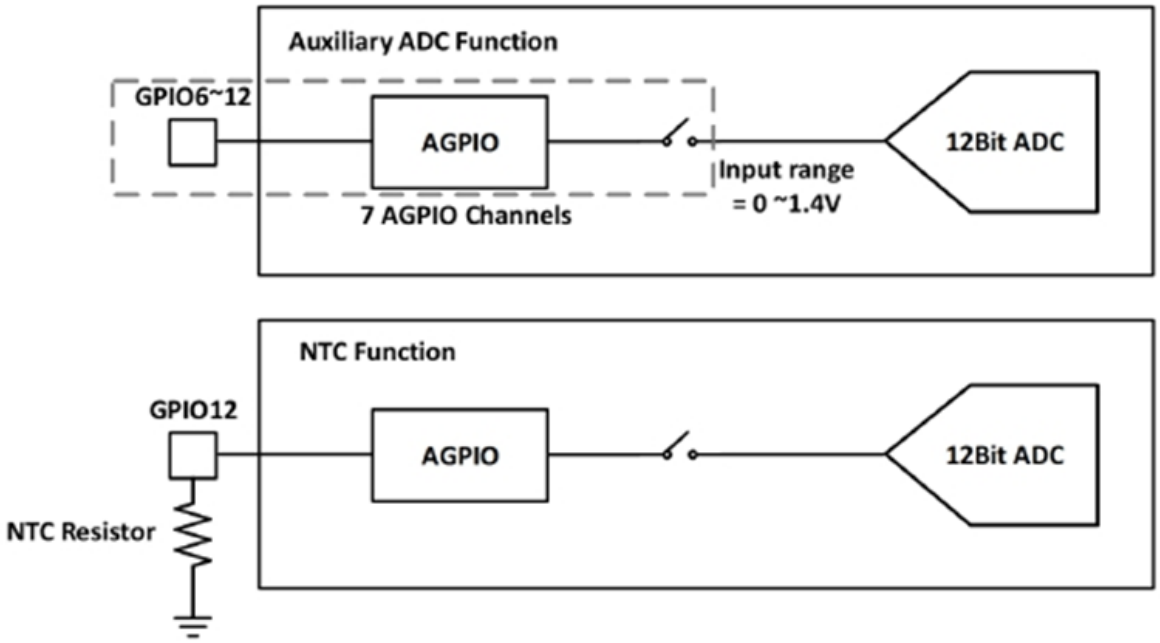
1) eMMC card specification version 4.41
2) SD memory card specification version 2.0
3) SDIO card specification version 2.0

The controller can be configured as a host for the eMMC/SD/SDIO card. There is one MSDC IP in this SOC. The main features of the controller are:

- 32-bit access for control registers
- Built-in CRC circuit
- Support for PIO mode, basic DMA mode, descriptor DMA mode
- Interrupt capabilities

- Support for SD/SDIO speed mode:
  - Default Speed mode (DS)
  - High Speed mode (HS)
- Support for eMMC speed mode:
  - Backwards Compatibility with legacy MMC card (DS)
  - High Speed SDR mode (HS)
- Support for 1-bit/4-bit SD/SDIO/eMMC bus widths. The module is targeted at a 48MHz operating clock at 0.8C and 0.9V. Date rates up to 48Mbps in 1-bit mode, 48 x 4 Mbps in 4-bit mode.
- Programmable serial clock rate on SD/SDIO/eMMC bus (256 gears)
- Card detection capabilities; This SOC uses the EINT controller for card detection
- No support for SPI mode for SD memory card
- No support for suspend/resume for SDIO card

2.2.7 Auxiliary ADC (AUXADC)



Block description

The auxiliary ADC includes the following functional blocks:

1) Analog multiplexer: Selects signal from one of the seven auxiliary input pins. Real-world messages, such as temperature, are monitored and translated to the voltage domain.
2) 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.
3) NTC function: With external mounted NTC resistor, NTC-resistor-sensed-temperature can be monitored and translated to the voltage domain.

Symbol	Parameter	Min	Type	Max	Unit
N	Resolution (Auxiliary ADC/NTC)	-	12	-	bit
VIN	Input swing	0.00	-	1.40	V
OE	Offset error @ Vin=0.07V～1.33V	-	±10	-	mV
FSE	Full swing error @Vin=0.07 V～1.33V	-	±10	-	mV
AVDD	Analog power supply	1.68	1.80	1.98	V

Auxiliary ADC specifications

Note-1: To guarantee the accuracy, ADC's output value is calculated by the following equation: Output value = ((code/4096 – OE) * 1.4/(1+GE)), where GE and OE are gain-error and offset-error preset in e-Fuse.

Note-2: The input voltage of AGPIO6～12 must be under 1.8V, when GPIO pins are configured as analog IO. Please note that the auxiliary ADC value is saturated when input voltage is higher than 1.4V.

2.3 Audio system

The features of the audio system are listed as below sections.

The audio codec part includes the downlink path, the uplink path, digital controller for Class AB amplifier. The other audio functions include the asynchronous sample rate converter, I2S bus, voice detection.

2.3.1 Audio downlink (Analog part)

BTA65 audio downlink includes stereo DACs and audio Class-AB amplifiers for audio playback is. The amplifier is implemented with Class-AB mode. The gain range of Class-AB amplifier is -22dB to +8dB, 1dB/step.

Audio downlink specifications of Class-AB are shown below.

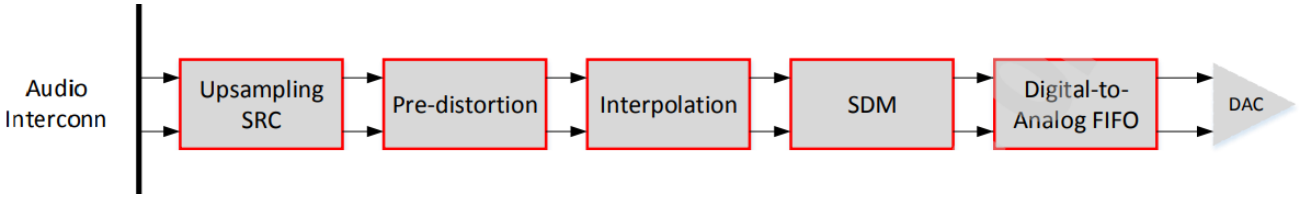
Audio Downlink Specifications (Class-AB)

Symbol	Parameter	Min	Type	Max	Unit
DAC to Class-AB Audio Buffer Output (Differential Output, AU_HPLP/N, AU_HPRP/N; without loading) Temp = 25deg, 1KHz sine wave signal, $F_{S,DL}$ = 48KHz, Digital Output Gain = 0dB, PGA_{DL} gain = -2dB, 24bit audio data, 20-20KHz(A-weighted), AVDD=1.8V					
P_{OUT}, MAX	Maximum output power @ <0.1% THD	-	0.66	-	Vrms
SNR (Note-1)	Signal to Noise Ratio (A-weighted) @0.66Vrms, BW = [20, 20KHz]	-	94	-	dB
Frequency Response	Frequency Response @0.66Vrms BW = [20, 20KHz]	-	±0.5	-	dB
THD+N	THD Plus Noise (THD+N) @0.66Vrms BW = [20, 20KHz]	< 0.1%			-
X_{TALK}	L/R Channel Crosstalk	-	-	-95	dB
R_{LOAD}	Output Resistor Load (Headphone)	8	32	-	Ω
$APGR_{DL}$	Downlink analog Programmable Gain Range	-22	-	8	dB
$APGS_{DL}$	Downlink analog Programmable Gain Step	-	1	-	dB

Note-1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20KHz bandwidth using an audio analyzer.

2.3.2 Audio downlink digital filter

Following figure shows the diagram of audio downlink paths. The audio downlink paths include the following blocks: up-sampling SRC, pre-distortion, interpolation, SDM and digital-to-analog FIFO. The downlink input source is from the audio interconnection. The output of digital-to-analog FIFO is sent to the analog DAC.



The proposed downlink path supports the following features:

- Support for one downlink path
- The data precisions in the downlink path are 24-bit data width
- the supported input sample rates for downlink:

  8K/11.025K/12K/16K/22.05K/24K/32K/44.1K/48K/96K/192K

2.3.3 Audio uplink (Analog part)

Audio uplink path is composed of PGA and audio ADC. The uplink front-end to PGA can be configured as ACC or DCC type. Besides the ACC type has 10KΩ and 20KΩ input impedance for selection. The PGA gain range is the 0~30dB per 6dB step and the ACC type of PGA can provide 3dB and 9dB gain option additionally. There are six input pairs of the uplink path that can be configured as DMIC or AMIC. Besides, the necessary MIC bias voltages (MICBIAS 0/1/2) are provided by this completed audio codec. Relative specification is shown below.

- Four channel PGA and ADC analog MIC input
- VIN0P/N ～ VIN3P/N can be configured as DMIC output/input
- Analog Gain Range is 0dB to 30dB
- ACC mode input impedance of PGA: 10KΩ or 20KΩ

Audio uplink specifications are shown below.

Audio Uplink Specifications (DCC)

Symbol	Parameter	Min	Type	Max	Unit
Analog input path to ADC (differential) DCC mode. Temp = 25deg, 1KHz sine wave signal, $F_{S,UL}$ = 48KHz, PGA_{UL} gain = 0dB, 24bit audio data, 20-20KHz(A-weighted) for Normal/High mode, 20-8KHz for Ultra-low power mode					
SNR (Note-1)	Signal to Noise Ratio @Ultra-low power mode @Normal operation mode @High-performance mode	-	 90 95 100	-	dB
THD	Total Harmonic Distortion (THD) @0dBV input @Ultra-low power mode @Normal operation mode @High-performance mode	-	 -75 -85 -90	-	dB
THD+N	THD Plus Noise (THD+N) @0dBV input @Ultra-low power mode @Normal operation mode @High-performance mode	-	 -75 -85 -90	-	dB
C_{IN}	Input impedance (single-ended)	-	24	-	pF
$APGR_{UL}$	Uplink analog Programmable Gain Range	0	-	30	dB
$APGS_{UL}$	Uplink analog Programmable Gain Step	-	6	-	dB

Audio Uplink Specifications (ACC 10K mode)

Symbol	Parameter	Min	Type	Max	Unit
Analog input path to ADC (differential) ACC 10K mode. Temp = 25deg, 1KHz sine wave signal, $F_{S,UL}$ = 48KHz, PGA_{UL} gain = 0dB, 24bit audio data, 20-20KHz(A-weighted) for Normal/High mode, 20-8KHz for Ultra-low power mode					
SNR (Note-1)	Signal to Noise Ratio @Ultra-low power mode @Normal operation mode @High-performance mode	-	 90 95 100	-	dB
THD	Total Harmonic Distortion (THD) @0dBV input @Ultra-low power mode @Normal operation mode @High-performance mode	-	 -75 -85 -90	-	dB
THD+N	THD Plus Noise (THD+N) @0dBV input @Ultra-low power mode @Normal operation mode @High-performance mode	-	 -75 -85 -90	-	dB
R_{IN}	Input impedance (single-ended)	-	10	-	KΩ
$APGR_{UL}$	Uplink analog Programmable Gain Range	0/3/6/9/12/18/24/30			dB
$APGS_{UL}$	Uplink analog Programmable Gain Step	3	6	-	dB

Audio Uplink Specifications (ACC 20K mode)

Symbol	Parameter	Min	Type	Max	Unit
Analog input path to ADC (differential) ACC 20K mode. Temp = 25deg, 1KHz sine wave signal, $F_{S,UL}$ = 48KHz, PGA_{UL} gain = 0dB, 24bit audio data, 20-20KHz(A-weighted) for Normal/High mode, 20-8KHz for Ultra-low power mode					
SNR (Note-1)	Signal to Noise Ratio @Ultra-low power mode @Normal operation mode @High-performance mode	-	 89 94 99	-	dB
THD	Total Harmonic Distortion (THD) @0dBV input @Ultra-low power mode @Normal operation mode @High-performance mode	-	 -74 -84 -89	-	dB
THD+N	THD Plus Noise (THD+N) @0dBV input @Ultra-low power mode @Normal operation mode @High-performance mode	-	 -74 -84 -89	-	dB
R_{IN}	Input impedance (single-ended)	-	20	-	KΩ
$APGR_{UL}$	Uplink analog Programmable Gain Range	0/3/6/9/12/18/24/30			dB
$APGS_{UL}$	Uplink analog Programmable Gain Step	3	6	-	dB

Note-1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20KHz bandwidth for Normal/High-performance mode and 20 to 8KHz for Ultra-low power mode using an audio analyzer.

MICBIAS Specifications

Symbol	Parameter	Min	Type	Max	Unit
Microphone Bias (MICBIAS) Temp = 25deg, 1uF capacitor on MICBIAS					
V_{OUT}	Microphone bias voltage (LDO 3.3V)	1.8/1.85/1.9/2.0/2.1/2.2/2.3/2.4/2.5			V
I_{OUT}	Maximum output current	-	-	12	mA
C_{load}	Output capacitor load on MICBIAS	1	-	22	uF

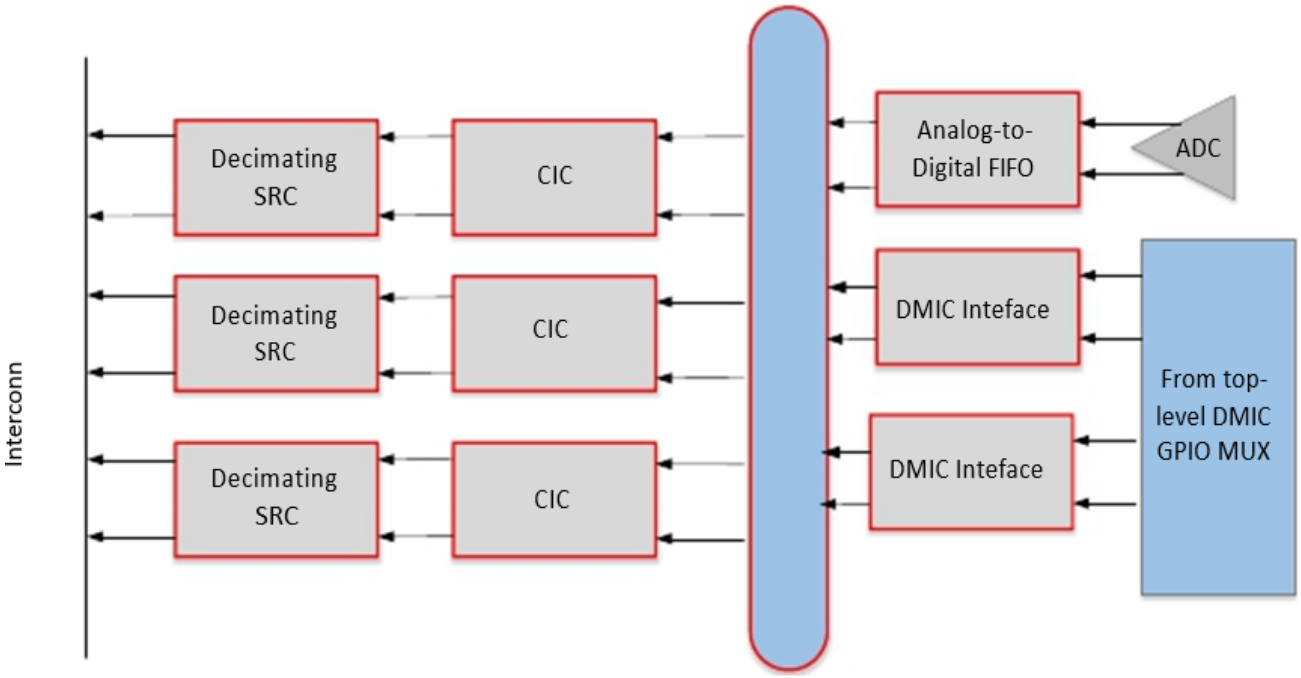
DMIC Specifications

Digital Mic					
Symbol	Parameter	Min	Type	Max	Unit
DCLK	DMIC clock frequency	3.25/1.625/0.8125/0.40625			MHz
DTY	DMIC clock duty cycle	40	-	60	%

2.3.4 Audio uplink digital filter

Following figure shows the complete block diagram of the audio uplink path. The digital uplink is composed of an analog/digital mic interface, CIC filter and decimating SRC. There are three uplink paths and all of them support DMIC input or AMIC input. One of these uplink paths can support audio

192KHz sampling rate, while the other two uplink paths can support up to 48KHz sampling rate. In the following description, the uplink with 192KHz sampling rate support is labeled as Uplink Path 1, and the other two paths are labeled as Uplink Path 2/3.



The proposed uplink path supports the following features:

- Analog/Digital MIC input mode
- DMIC has 8 modes (one-wire@3.25MHz/1.625MHz/812.5KHz/406.25KHz)
- Uplink Path 1 Support for sample rates: 8KHz/16KHz/32KHz/48KHz/96KHz/192KHz
- Uplink Path 2/3 Support for sample rates: 8KHz/16KHz/32KHz/48KHz
- All the uplink path are 24-bit width data precision

2.3.5 Asynchronous sample rate converter

Asynchronous Sample Rate Converter (ASRC) is a 2-channel asynchronous sample rate converter designed for high quality digital audio applications. The ASRC can be slaved to either input or output sample clocks that do not need to be synchronous with the chip clock. The input and output sample rates can be an arbitrary fraction of on another. The output is re-sampled to match the output sample

timing. The input and output ports are from/to memory space on sysytem bus. The ouput ports are to memory spaces or audio inter connnection.

- Support for 1 stereo channel-set or 1 mono channel per ASRC HW
- Each channel-set can configure its input frequency and output frequency
- Support for 1 stereo channel-set or 1 mono channel per ASRC HW
- Data format
  - 16/32 bit input
  - 16/32 bit output
- Support for frequency auto-tracking

  Should provide a signal related to the sampling rate, such as LRCK in I2S spec
- Versatile interrupt mechanism
- Provide 2 sample counters per ASRC HW for SE monitoring execution progress.

2.3.6 I2S

Inter-IC sound(I²S) is electrical serial bus interface standard connecting digital audio devices. Clock signal and serial data signal are separated in the I2S bus, resulting in a less jitter than average in communications systems that recover the clock from the data stream.

- The I²S master, I²S salve are supported.
- Support the I²S, EIAJ, Left-justified, Right-Justified formats
- Support 16-bit or 24-bit data width.
- Support mono or stereo transaction.
- Support sampling rates are 8KHz, 11.025KHz, 12KHz, 16KHz, 22.05KHz, 24KHz, 32KHz, 44.1KHz, 48KHz, 88.2KHz, 96KHz, 176.4KHz, 192KHz
- I2S_MCLK can support 49.152MHz/(n+1) or 45.1584MHz/(n+1), where n=0～127 (integer).

I²S Specifications

I²S Protocols	Bit Width (Bits)	Channel Width (Bits)	Input/output Sample Rates (KHz)
Master Mode	16, 24	16, 32	8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, 192
Slave Mode	16, 24	16, 32	8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, 192

I²S Bit Clock Jitter Percentage that generated from APLL

I²S Bit Clock Frequency (Hz)	Clock Jitter Percentage (%)
12288K	0.63000
11289.6K	0.59242
6144K	0.30778
5644.8K	0.38913

I²S Word Select Clock Jitter Percentage that generated from APLL

I²S Word Select Frequency (Hz)	Clock Jitter Percentage (%)
192K	0.01847
176.4K	0.01629

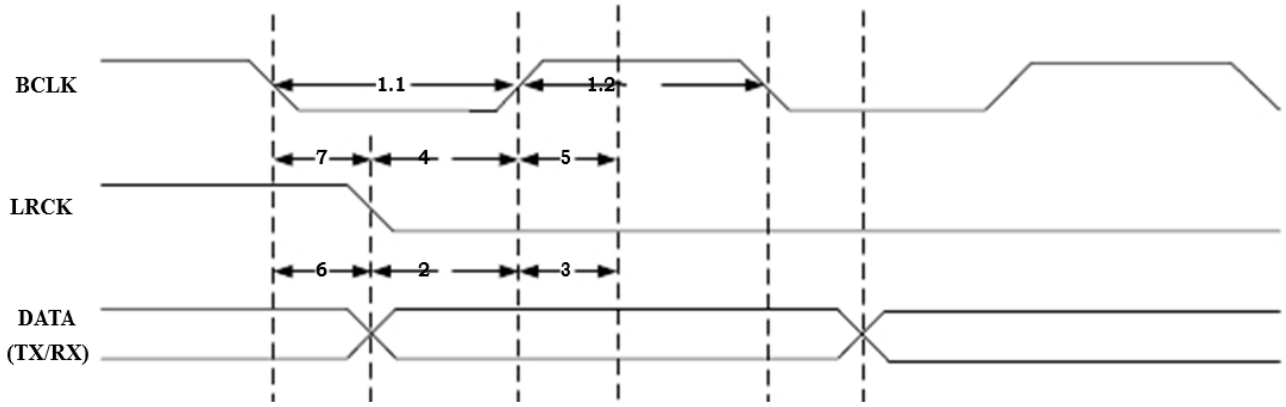
I²S Bit Clock Jitter Percentage that generated from XO

I²S Bit Clock Frequency (Hz)	Clock Jitter Percentage (%)
3072K	19.41845
2822.4K	14.18293
1536K	6.75211
1411.2K	9.09043

I²S Word Select Clock Jitter Percentage that generated from XO

I²S Word Select Frequency (Hz)	Clock Jitter Percentage (%)
48K	0.33700
44.1K	0.29277

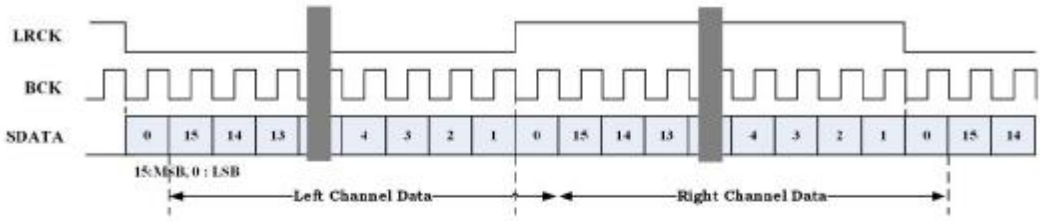
Following figure shows the timing requirement of I²S interface and corresponding timing requirements is listed.



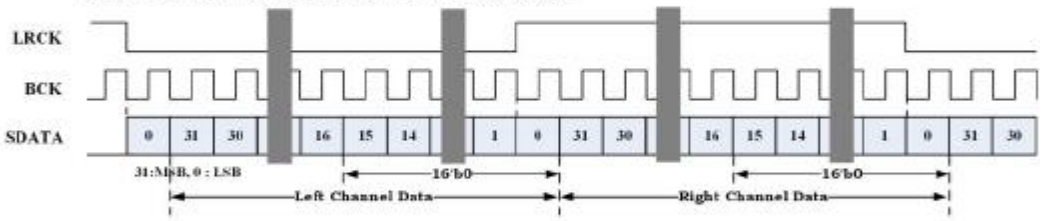
No.	Signal Type Description	Mater Min (ns)	Master Max (ns)	Slave Min (ns)	Slave Max (ns)	
1.1	Pulse duration, I2S_BCLK low	40%*T_{BCLK}	-	40%*T_{BCLK}	-	
1.2	Pulse duration, I2S_BCLK high	40%*T_{BCLK}	-	40%*T_{BCLK}	-	
2	Setup time, I2S_RX valid before I2S BCLK high	15	-	15	-	
3	Hold time, I2S_RX valid after I2S_BCLK high	3	-	3	-	
4	Setup time, I2S_LRCK valid before I2S BCLK high	-	-	15	-	
5	Hold time, I2S_LRCK valid after I2S_BCLK high	-	-	3	-	
6	Output Delay time, I2S_BCLK low to I2S_TX valid	0	15	0	15	
7	Delay time, I2S_BCLK low to I2S_LRCK valid	0	15	-	-	

The I²S bus protocol supports the I²S, EIAJ, Left-justified, Right-Justified formats. Following figures Show the details functional waveform of the four formats

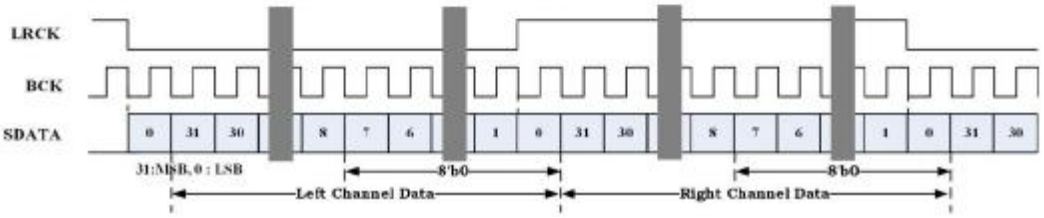
- (1-1) I2S format : 16-bits precision in 16-bits word length



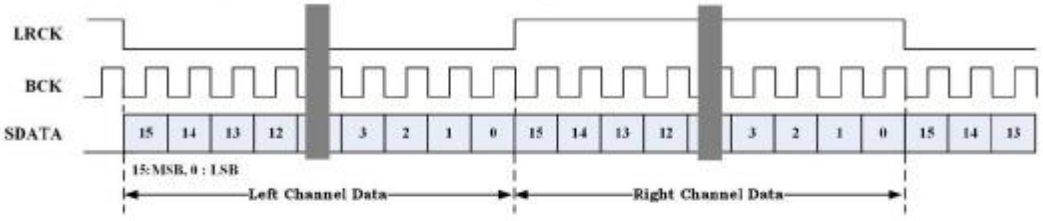
- (1-2) I2S format : 16-bits precision in 32-bits word length



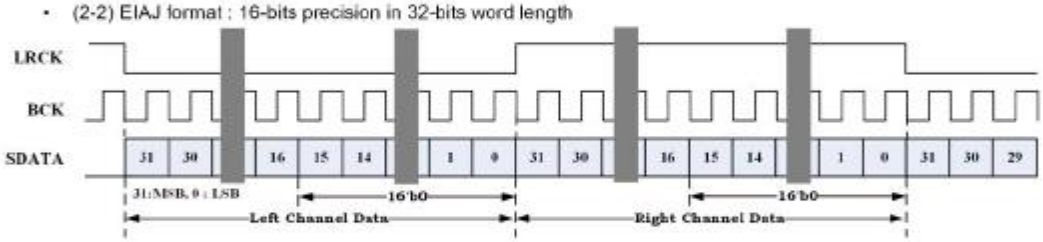
- (1-3) I2S format : 24-bits precision in 32-bits word length



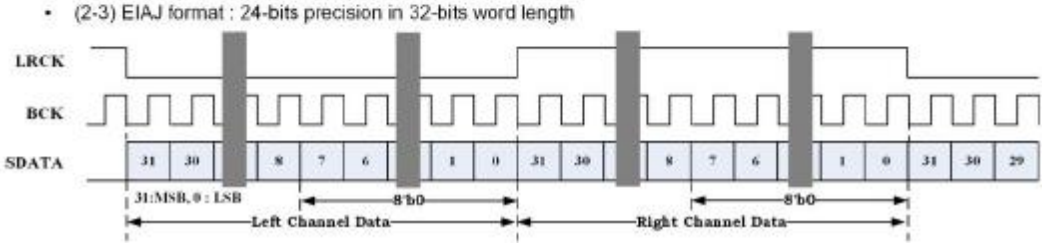
- (2-1) EIAJ format : 16-bits precision in 16-bits word length



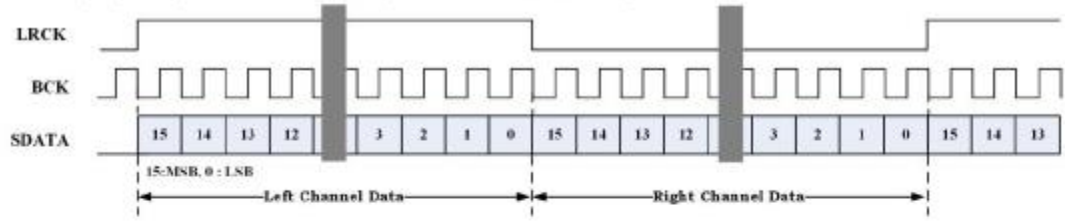
- (2-2) EIAJ format : 16-bits precision in 32-bits word length



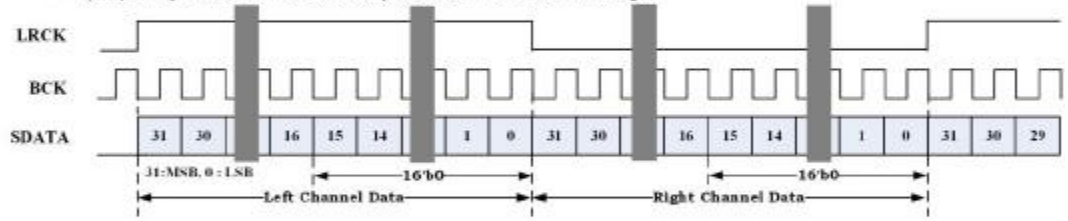
- (2-3) EIAJ format : 24-bits precision in 32-bits word length



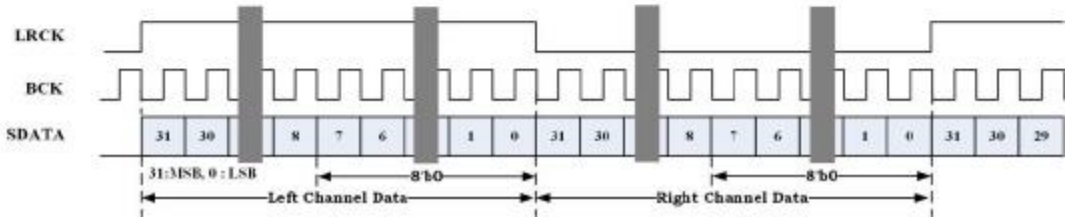
- (3-1) Left-justified format : 16-bits precision in 16-bits word length



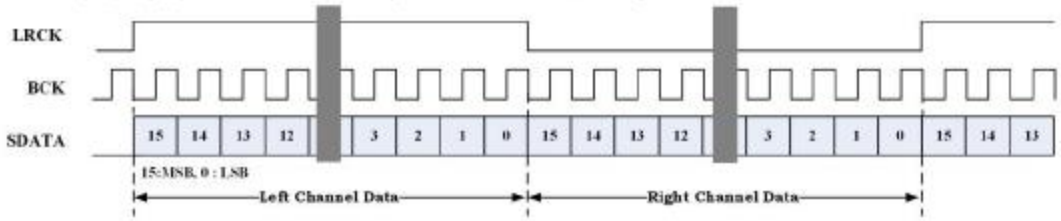
- (3-2) Left-justified format : 16-bits precision in 32-bits word length



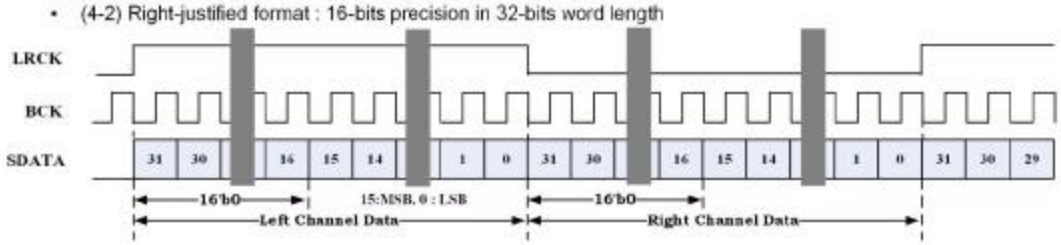
- (3-3) Left-justified format : 24-bits precision in 32-bits word length



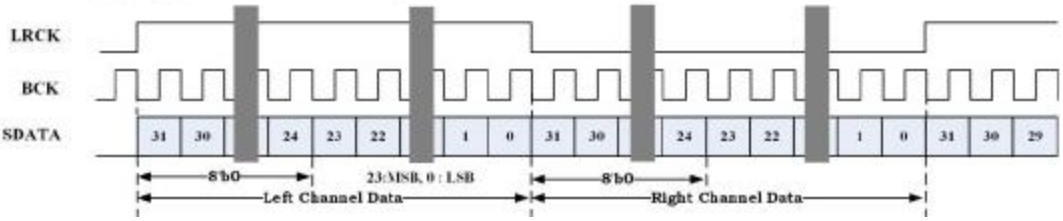
- (4-1) Right-justified format : 16-bits precision in 16-bits word length



- (4-2) Right-justified format : 16-bits precision in 32-bits word length

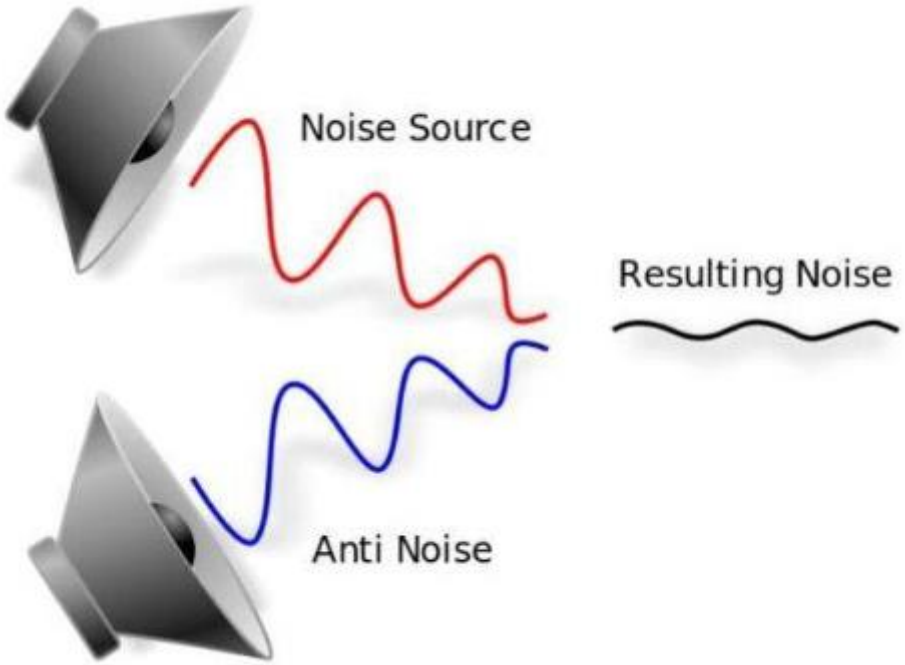


- (4-3) Right-justified format : 24-bits precision in 32-bits word length



2.3.7 Active noise cancellation (ANC)

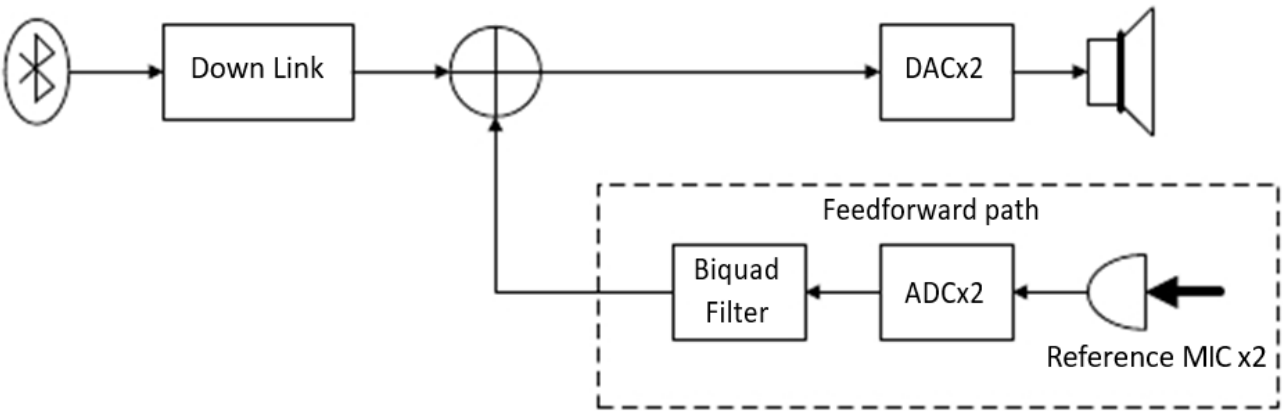
The generic active noise cancellation (ANC) is a method for reducing unwanted noise by the addition of a second sound that is designed to cancel the unwanted noise. The concept diagram of ANC is shown in following figure.



Feedforward ANC

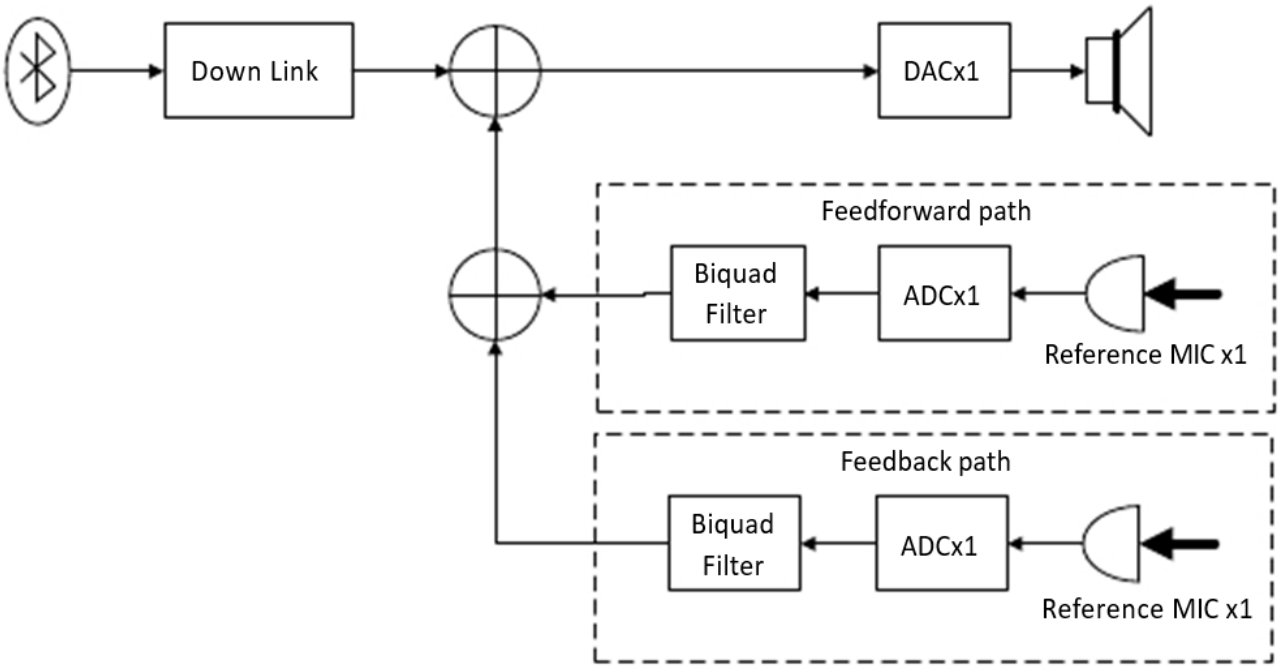
BTA65 Supports Feedforward mode that receive signals from reference microphone and generate anti-noise signals through biquad filter. The biquad filter is 9-cascade stage and each stage provides programmable coefficients that are used to modeling the various channel response digitally. The reference microphone can be selected as analog microphone or digital microphone respectively.

It supports gain ramp up and down with limiter function that smoothly adding anti-noise signal into down link path without suffering large pop-noise.



Hybrid ANC

BTA65 Supports Hybrid mode that receive signals from reference microphone for feedforward path and from another reference microphone for feedback path to generate anti-noise signals through biquad filter. In Hybrid ANC mode, selected as analog microphone or digital microphone respectively.



2.3.8 Voice detection

Voice Activity Detection

The voice activity detection (VAD), also known as speech activity detection or speech detection is provided. Once the voice activity is detected, an IRQ signal will be sent to wakeup DSP.

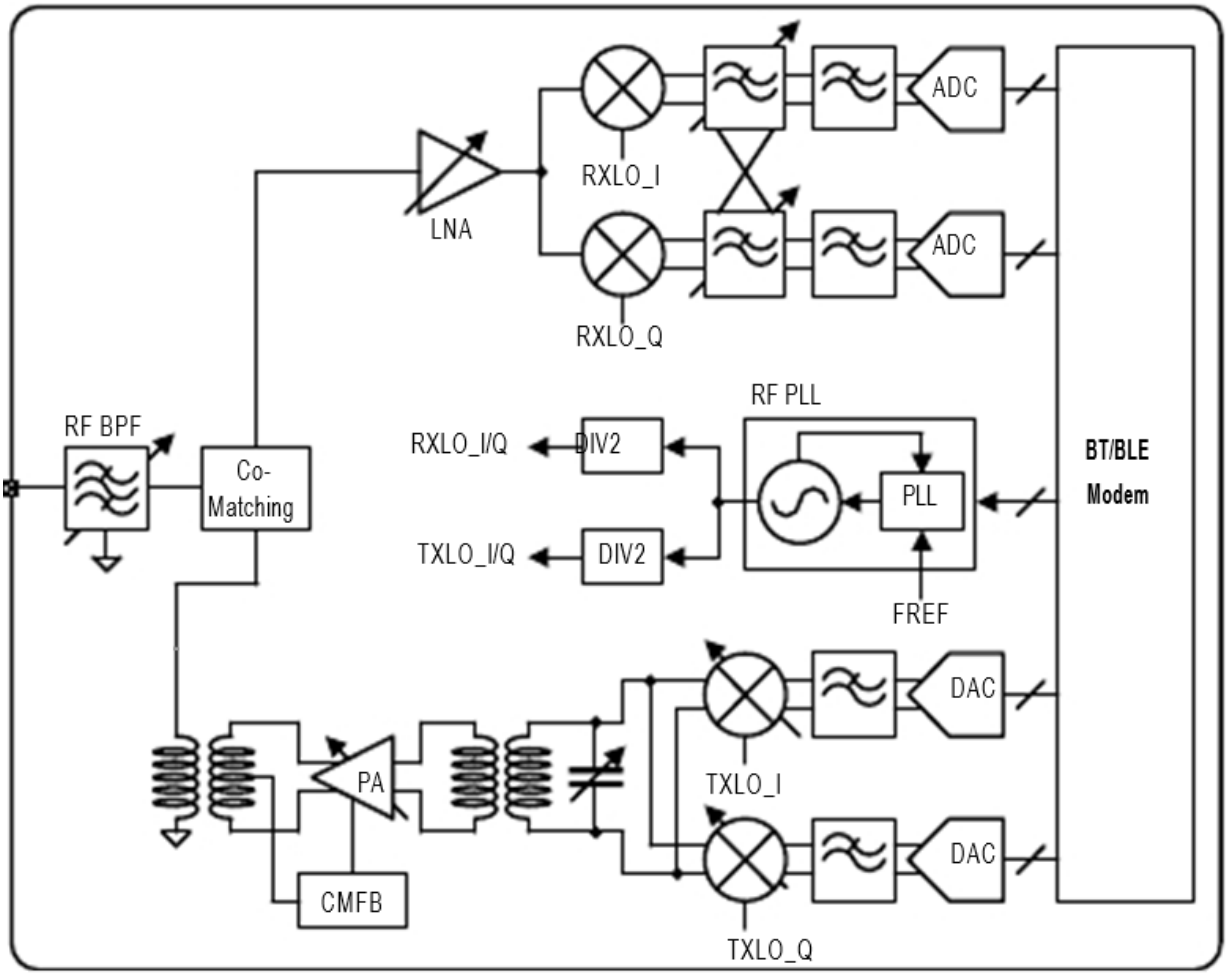
Voice Wake-up

The voice wake-up (VoW) is a dedicated HW to detect voice or speech, and can be compatible to both AMIC & DMIC component. After voice activity is detected, VoW can further receive and store the voice dat from AMIC or DMIC. VoW is a low power HW solution for key word detection process.

3 Bluetooth RF subsystem

3.1 Bluetooth description

BTA65 Bluetooth (BT) RF subsystem (as shown following Figure) consists of a highly integrated transceiver with tunable on-chip RF band pass filter (BPF) and BT TRX con-matching network.



BTA65 adopts a low intermediate frequency (LIF) receiver architecture. The receiver, including the on-chip RF BPF and TRX co-matching network, consists of a LNA and single balanced passive mixer, a complex BPF and a pair of 10-bit SAR ADCs. The BTA65 BT receiver has best-in-class out-of-band blocking performance without the need of any external RF BPF.

The direct conversion transmitter consists of a pair of 9-bit current DACs and passive LPFs, an active IQ modulator (IQM) and a Class AB push-pull PA. This PA is capable of transmitting +8dBm power for enhanced data rate (EDR) and +10dBm for basic data rate (BDR). This Class AB push-pull PA, together with on-chip RF BPF and TRX co-matching network, minimized TX harmonic distortion products significantly, eliminating the need for an external RF BPF.

The Δ-Σ fractional-N RF synthesizer is phase locked to 26MHz reference clock to generate the RF LO frequency. The BBPLL generates sampling clock for ADC and DAC as well as digital clock to BT modem.

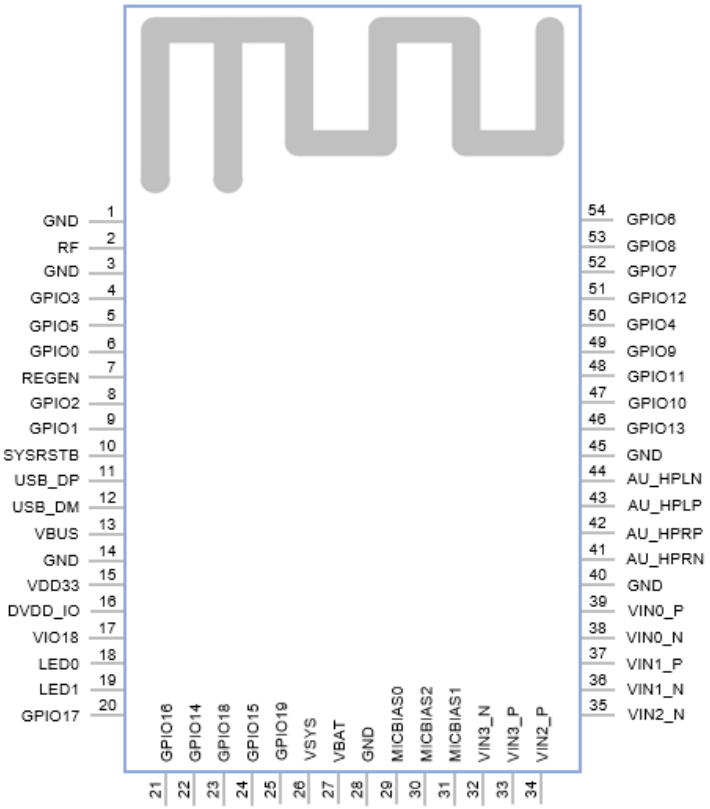
BTA65 implements various automatic calibration schemes to minimize changes in RF performance from chip-to-chip and temperature variations. No additional RF factory calibration is necessary.

3.2 Functional specification

Items	Units	Min.	Typ.	Max.
Frequency Range	MHz	2402	-	2480
RF Average Output Power - Basic Data Rate	dBm	5	7	8.5
RF Average Output Power - Enhanced Data Rate	dBm	3	5	6.5
RF Average Output Power - Low Energy	dBm	5	7	8.5
RF Power Control Gain Step Range	dBm	2	4	8
RF Receiver Sensitivity – Basic Data Rate [Condition: BER < 0.1% (DH5)]	dBm	-	-94	-70
RF Receiver Sensitivity - 2DH5 [Condition: π/4 DQPSK, BER < 0.01%]	dBm	-	-94	-70
RF Receiver Sensitivity - 3DH5 [Condition: 8DPSK, BER < 0.01%]	dBm	-	-87	-70
RF Receiver Sensitivity – Low Energy (1Mbps) [Condition: PER < 30.8%]	dBm	-	-98	-70
RF Receiver Sensitivity – Low Energy (2Mbps) [Condition: PER < 30.8%]	dBm	-	-95	-70
Crystal Frequency Calibration	Hz	-260	0	260
Carrier Frequency Drift	KHz	-75	-	75

4 Pin description

As the following figure shown, BTA65 has 54 stamp pins. Each pin number, pin type and supply is listed in the following table.



Name	Abbreviation	Description
Pin Type	AI	Analog input
	AO	Analog output
	AIO	Analog bi-direction
	DI	Digital input
	DO	Digital output
	DIO	Digital bi-direction
	P	Power
	G	Ground

#Pin	Pin Name	Pin Type	Supply Domain	Pin Functions	Alternate Pin Description
1	GND	G	Substrate Ground	GND	-
2	RF	AIO	-	RF port	-
3	GND	G	Substrate Ground	GND	-

4	GPIO3	DIO	DVDD_IO	General purpose input/output	UART0_CTS DMIC0_DAT UART2_RXD CTP1 EINT3
5	GPIO5	DIO	DVDD_IO	General purpose input/output	I2C1_SDA UART1_RXD DMIC1_DAT PWM4 CTP3 EINT5
6	GPIO0	DIO	DVDD_IO	General purpose input/output	UART0_TXD AUDIO_EXT_SYNC_EN EINT0
7	REGEN	AI	-	-	-
8	GPIO2	DIO	DVDD_IO	General purpose input/output	DMIC0_CLK EINT2
9	GPIO1	DIO	DVDD_IO	General purpose input/output	UART0_RXD EINT1
10	SYSRSTB	DI	Internal VDIG18	SYSRSTB button	-
11	USB_DP	AIO	VDD33	USB signal DP	-
12	USB_DM	AIO	VDD33	USB signal DM	-
13	VBUS	P	VBUS	Charge power input	-
14	GND	G	Substrate Ground	GND	-
15	VDD33	AO	VDD33	VLDO33 output voltage	Not used
16	DVDD_IO	P	-	Power input of GPIO	-
17	VIO18	AO	VSYS	SW node of VIO18	-
18	LED0	AO	VSYS	Current sink channel 0	-
19	LED1	AO	VSYS	Current sink channel 1	-
20	GPIO17	DIO	DVDD_IO	General purpose input/output	SPI_MST0_SIO2 MSDC0_DAT2 I2S_MST2_CK I2S_SLV2_CK I2C0_SDA MSDC0_CLK1 UART1_RTS EINT17
21	GPIO16	DIO	DVDD_IO	General purpose input/output	SPI_MST0_MISO MSDC0_DAT1 I2S_MST2_WS I2S_SLV2_WS I2C0_SCL DMIC1_DAT UART1_CTS EINT16

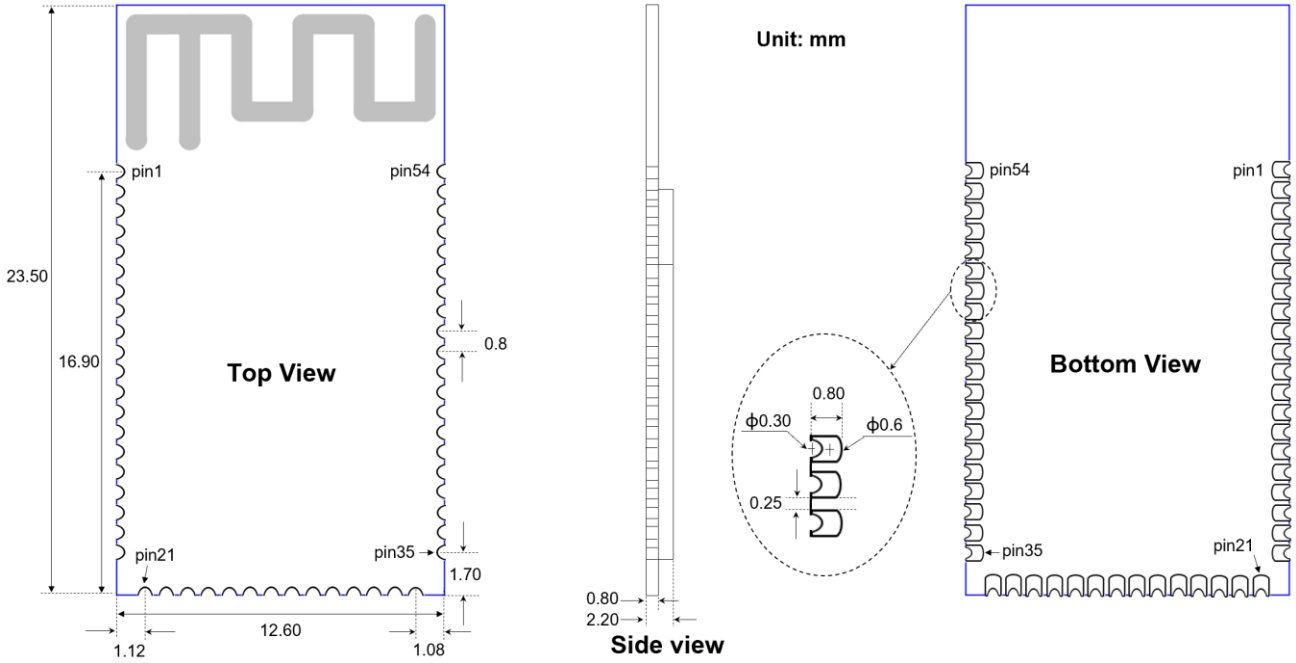
22	GPIO14	DIO	DVDD_IO	General purpose input/output	SPI_MST0_CS MSDC0_CMD I2S_MST1_RX I2S_SLV1_RX UART0_RTS DMIC0_DAT PWM1 EINT14
23	GPIO18	DIO	DVDD_IO	General purpose input/output	SPI_MST0_SIO3 MSDC0_DAT3 I2S_MST2_RX I2S_SLV2_RX I2S_MST1_MCLK MSDC0_CLK2 UART2_TXD EINT18
24	GPIO15	DIO	DVDD_IO	General purpose input/output	SPI_MST0_MOSI MSDC0_DAT0 I2S_MST1_WS I2S_SLV1_WS I2S_MST2_MCLK DMIC1_CLK UART2_TXD EINT15
25	GPIO19	DIO	DVDD_IO	General purpose input/output	SPI_MST0_SCK MSDC0_CLK0 I2S_MST2_TX I2S_SLV2_TX I2S_MST0_MCLK UART2_RXD EINT19
26	VSYS	P	VSYS	System load connection. Connect VSYS to system load	-
27	VBAT	P	VBAT	Battery connection. Connect VBAT to the positive terminal of battery	This pin of BTA65T is NC
28	GND	G	Substrate Ground	GND	-
29	MICBIAS0	AO	VDD33	Analog mic phone bias0	This pin of BTA65T is NC
30	MICBIAS2	AO	VDD33	Analog mic phone bias2	This pin of BTA65T is NC
31	MICBIAS1	AO	VDD33	Analog mic phone bias1	This pin of BTA65T is NC
32	VIN3_N	AI	-	Audio input CH3 N-side	This pin of BTA65T is GND
33	VIN3_P	AI	-	Audio input CH3 P-side	This pin of BTA65T is GND
34	VIN2_P	AI	-	Audio input CH2 P-side	This pin of BTA65T is GND
35	VIN2_N	AI	-	Audio input CH2 N-side	This pin of BTA65T is GND
36	VIN1_N	AI	-	Audio input CH1 N-side	This pin of BTA65T is GND

37	VIN1_P	AI	-	Audio input CH1 P-side	This pin of BTA65T is GND
38	VIN0_N	AI	-	Audio input CH0 N-side	This pin of BTA65T is GND
39	VIN0_P	AI	-	Audio input CH0 P-side	This pin of BTA65T is GND
40	GND	G	Substrate Ground	GND	-
41	AU_HPRN	AO	VIO18	Headphone R-ch N-side	This pin of BTA65T is NC
42	AU_HPRP	AO	VIO18	Headphone R-ch P-side	This pin of BTA65T is NC
43	AU_HPLP	AO	VIO18	Headphone L-ch P-side	This pin of BTA65T is NC
44	AU_HPLN	AO	VIO18	Headphone L-ch N-side	This pin of BTA65T is NC
45	GND	G	Substrate Ground	GND	-
46	GPIO13	DIO	DVDD_IO	General purpose input/output	PWM2 MSDC0_RST I2S_MST1_TX I2S_SLV1_TX DMIC0_CLK EINT13
47	GPIO10	DIO	DVDD_IO	General purpose input/output	SPI_MST1_SIO3 SPI_SLV0_SIO3 UART0_RTS I2S_MST0_WS I2S_SLV0_WS I2C1_SCL AUXADC2 EINT10
48	GPIO11	DIO	DVDD_IO	General purpose input/output	SPI_MST1_SCK SPI_SLV0_SCK UART1_TXD I2S_MST0_RX I2S_SLV0_RX I2C1_SDA AUXADC1 EINT11
49	GPIO9	DIO	DVDD_IO	General purpose input/output	SPI_MST1_SIO2 SPI_SLV0_SIO2 UART0_CTS I2S_MST0_CK I2S_SLV0_CK I2C0_SDA AUXADC3 EINT9
50	GPIO4	DIO	DVDD_IO	General purpose input/output	I2C1_SCL UART1_TXD DMIC1_CLK PWM3 CTP2 EINT4

51	GPIO12	DIO	DVDD_IO	General purpose input/output	AUDIO_EXT_SYNC_EN UART1_RXD I2S_MST1_CK I2S_SLV1_CK UART2_RXD AUXADC0 (NTC) EINT12
52	GPIO7	DIO	DVDD_IO	General purpose input/output	SPI_MST1_MOSI SPI_SLV0_MOSI UART1_RTS I2S_MST1_MCLK UART2_TXD I2C2_SDA AUXADC5 EINT7
53	GPIO8	DIO	DVDD_IO	General purpose input/output	SPI_MST1_MISO SPI_SLV0_MISO I2S_MST0_TX I2S_SLV0_TX I2C0_SCL AUXADC4 EINT8
54	GPIO6	DIO	DVDD_IO	General purpose input/output	SPI_MST1_CS SPI_SLV0_CS UART1_CTS I2S_MST0_MCLK PWM0 I2C2_SCL AUXADC6 EINT6

5 Module size

For BTA65, a 23.5 x 12.6 x 2.2 mm, 0.80 mm pitch, stamp pin package is offered. The weight of BTA65 module is about 1.2 g. The package view and size information are shown in following figure.



6 Electrical specification

6.1 Absolute maximum ratings

Description	Min.	Max.	Unit
VBAT: System power/Connect VBAT to the positive terminal of battery.	-0.50	4.80	V
VBUS: Charger power input	-0.50	6.00	V
DVDD_IO: I/O supply voltage	1.62	3.63	V
VSYS: System load connection. Connect VSYS to system load. (Key, LED etc.)	-0.50	5.00	V
REGEN: Regulator enable	-0.50	5.00	V
Operating temperature	-20	+70	℃
Storage temperature	-25	+85	℃

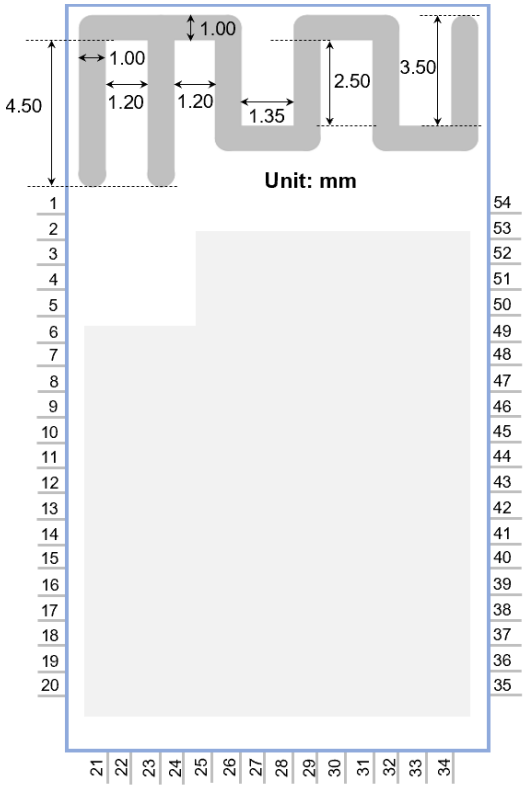
6.2 Operating conditions

Description	Min.	Typ.	Max.	Unit
VBAT: System power/Connect VBAT to the positive terminal of battery.	3.00	3.70	4.50	V
VBUS: Charger power input	4.50	-	5.50	V
DVDD_IO: I/O supply voltage	1.62	1.80 or 3.30	3.63	V
VSYS: System load connection. Connect VSYS to system load. (Key, LED etc.)	3.00	3.70	5.00	V
REGEN: Regulator enable	3.00	3.70	4.80	V
VDD33: VDD33 LDO output voltage (Rated Output Current: 110mA)	2.90	3.30	3.53	V
VIO18: VIO Buck Regulator (Rated Output Current: 350mA)	1.65	1.83	1.98	V
VIN0/VIN1/VIN2/VIN3	0	-	DVDD_IO	V
Operating temperature	-20	+25	+70	℃

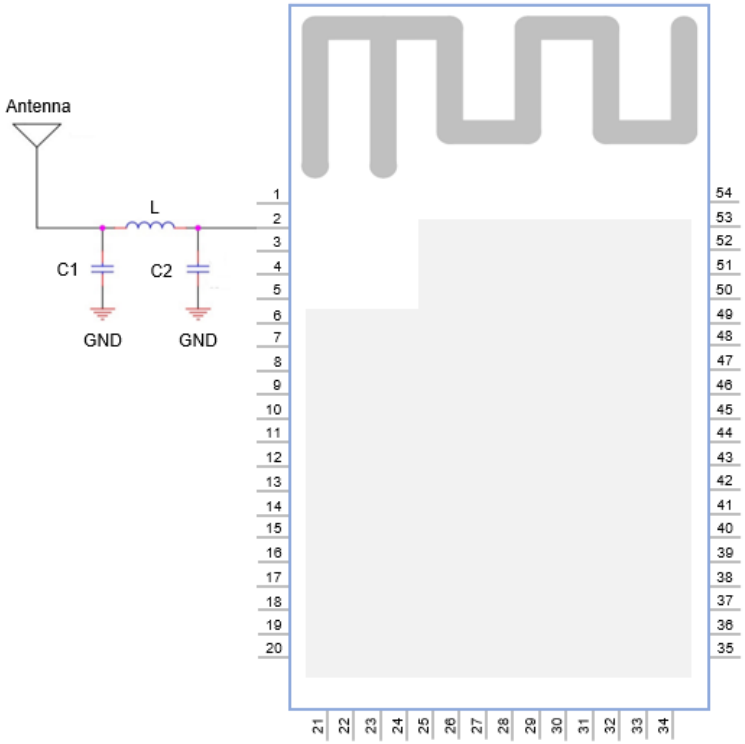
7 Antenna type, performance and application note

BTA65 provides two antenna types of internal antenna and external antenna.

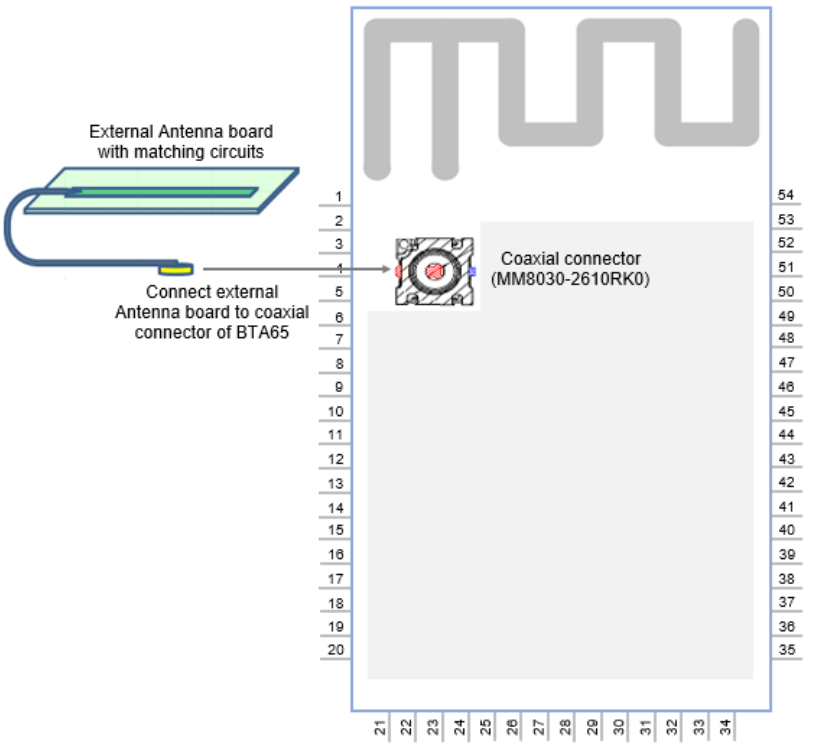
The internal antenna has good RF performance. The manufacturer of internal antenna is BOMIN, and its size information is as follows.



In addition, due to the limitation of some product structure, the performance of internal antenna may not meet the requirements. In order to obtain better RF performance, the pin 2 or the coaxial connector (MM8030-2610RK0) of BTA65 module can be connected to an external antenna as following figures.



Connect to external antenna via Pin 2 of BTA65

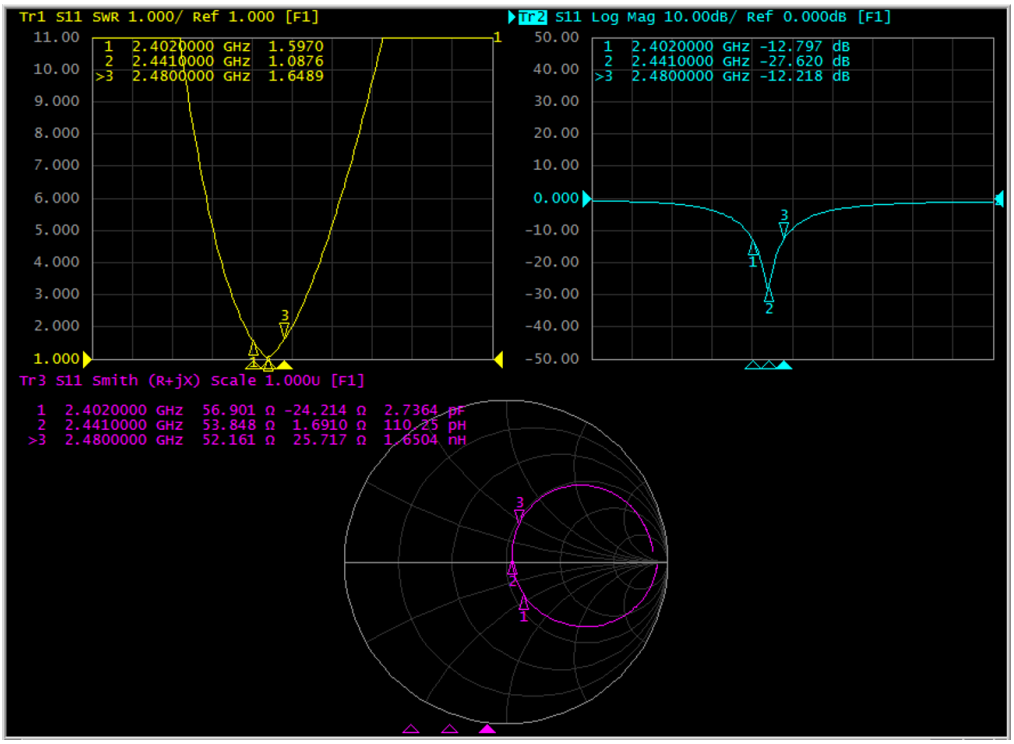


Connect to coaxial connector of BTA65

7.1 Internal antenna performance

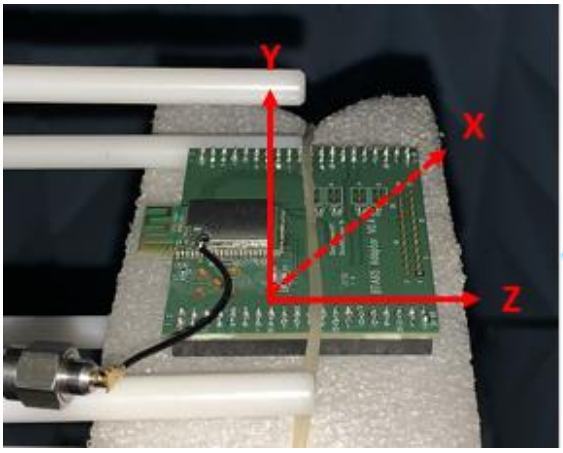
Max Gain	1.54 dBi @ 2443MHz
Max Effieiency	65.69% @2454MHz

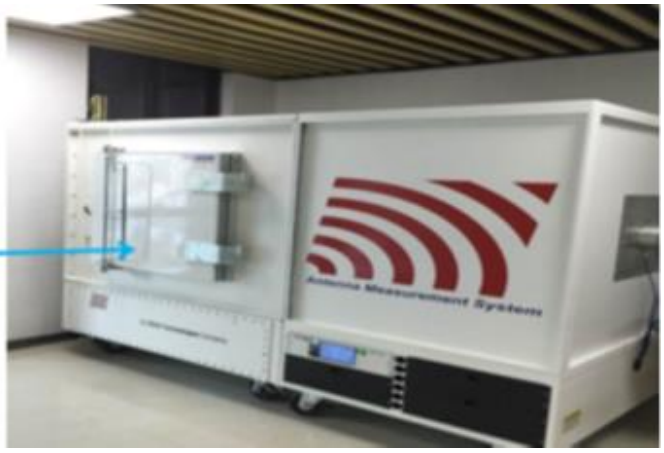
7.1.1 VSWR, Return Loss and Impedance



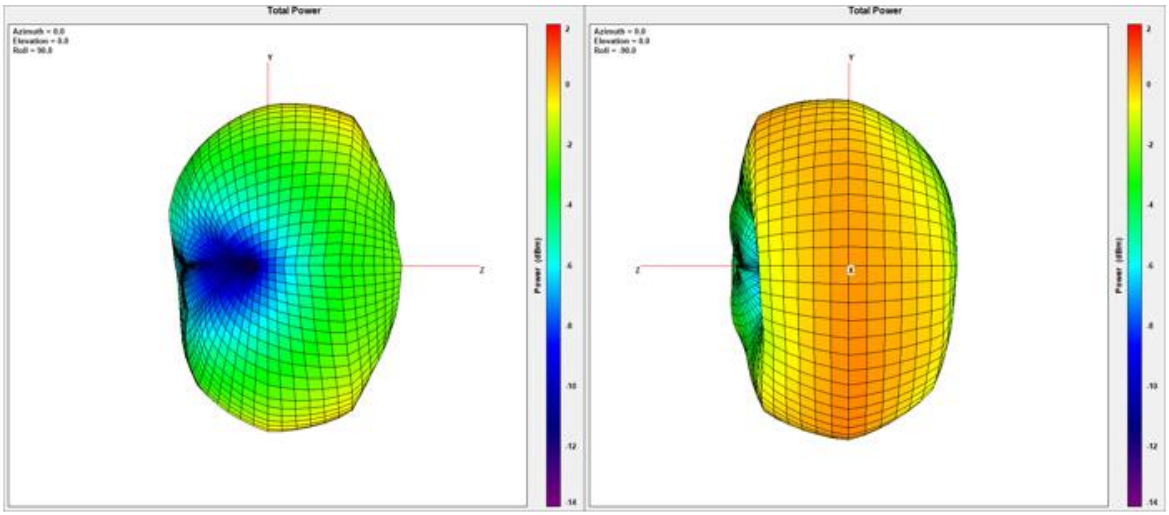
7.1.2 Antenna 3D Radiation, Efficiency and Gain

Test settings:

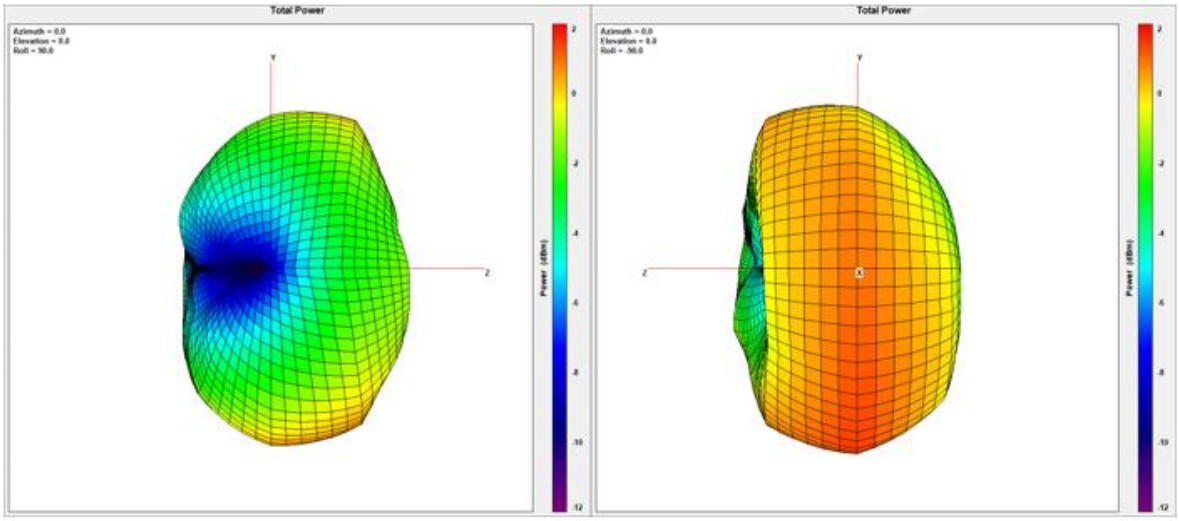




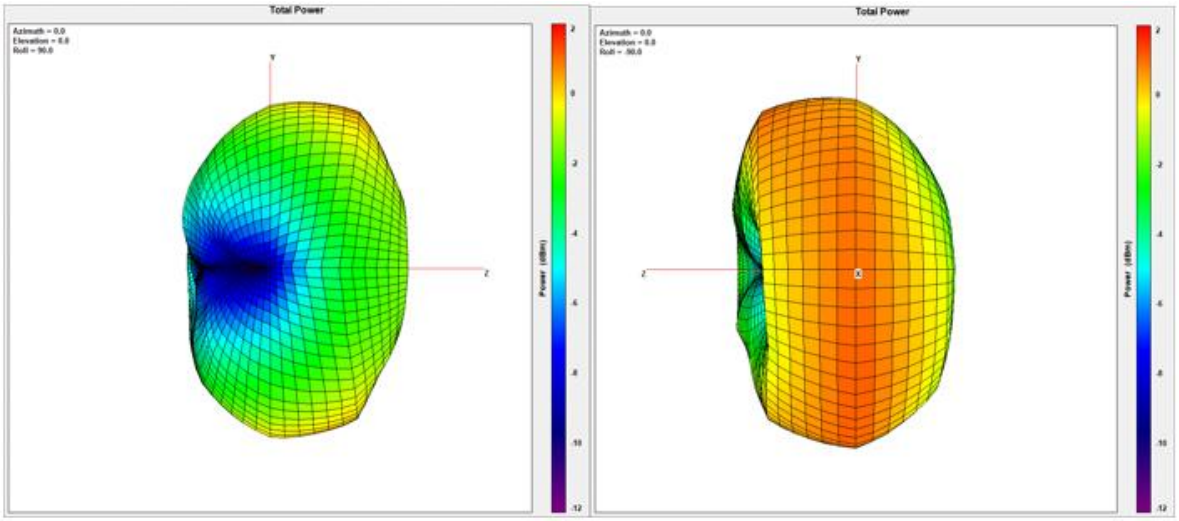
Antenna 3D Radiation Pattern (2402MHz):



Antenna 3D Radiation Pattern (2441MHz):



Antenna 3D Radiation Pattern (2480MHz):



Antenna Efficiency and Gain:

Point Values	Ant. Port Input Pwr. (dBm)	Tot. Rad. Pwr. (dBm)	Peak EIRP (dBm)	Directivity (dBi)	Efficiency (dB)	Efficiency (%)	Gain (dBi)
Frequency (MHz)							
2400	0	-2.39478	0.785812	3.18059	-2.39478	57.6132	0.785812
2401	0	-2.38062	0.771219	3.15184	-2.38062	57.8014	0.771219
2402	0	-2.36777	0.75755	3.12532	-2.36777	57.9726	0.75755
2403	0	-2.35655	0.749425	3.10597	-2.35655	58.1226	0.749425
2404	0	-2.34483	0.738148	3.08298	-2.34483	58.2796	0.738148
2405	0	-2.3289	0.732775	3.06168	-2.3289	58.4938	0.732775
2406	0	-2.3123	0.735283	3.04758	-2.3123	58.7178	0.735283
2407	0	-2.29512	0.743207	3.03833	-2.29512	58.9506	0.743207
2408	0	-2.28042	0.754919	3.03534	-2.28042	59.1504	0.754919
2409	0	-2.26409	0.765269	3.02936	-2.26409	59.3732	0.765269
2410	0	-2.24664	0.782129	3.02877	-2.24664	59.6123	0.782129
2411	0	-2.23182	0.795071	3.02689	-2.23182	59.8161	0.795071
2412	0	-2.21491	0.811126	3.02604	-2.21491	60.0495	0.811126
2413	0	-2.19778	0.825863	3.02364	-2.19778	60.2868	0.825863
2414	0	-2.18695	0.839941	3.02689	-2.18695	60.4372	0.839941
2415	0	-2.17353	0.857325	3.03086	-2.17353	60.6243	0.857325
2416	0	-2.16241	0.872764	3.03517	-2.16241	60.7798	0.872764
2417	0	-2.15052	0.885214	3.03573	-2.15052	60.9464	0.885214
2418	0	-2.13719	0.901648	3.03884	-2.13719	61.1338	0.901648
2419	0	-2.13008	0.918049	3.04813	-2.13008	61.234	0.918049
2420	0	-2.11753	0.932043	3.04958	-2.11753	61.4111	0.932043
2421	0	-2.10805	0.951199	3.05925	-2.10805	61.5454	0.951199
2422	0	-2.09662	0.974484	3.0711	-2.09662	61.7075	0.974484
2423	0	-2.08447	0.993918	3.07839	-2.08447	61.8803	0.993918
2424	0	-2.07214	1.02393	3.09607	-2.07214	62.0563	1.02393
2425	0	-2.06296	1.06305	3.12601	-2.06296	62.1877	1.06305

Point Values	Ant. Port Input Pwr. (dBm)	Tot. Rad. Pwr. (dBm)	Peak EIRP (dBm)	Directivity (dBi)	Efficiency (dB)	Efficiency (%)	Gain (dBi)
Frequency (MHz)							
2426	0	-2.04673	1.10268	3.14941	-2.04673	62.4204	1.10268
2427	0	-2.03027	1.1466	3.17687	-2.03027	62.6574	1.1466
2428	0	-2.01231	1.19047	3.20278	-2.01231	62.9171	1.19047
2429	0	-2.00164	1.22802	3.22966	-2.00164	63.0719	1.22802
2430	0	-1.98904	1.26963	3.25866	-1.98904	63.2552	1.26963
2431	0	-1.97821	1.30754	3.28575	-1.97821	63.4132	1.30754
2432	0	-1.96528	1.34426	3.30954	-1.96528	63.6022	1.34426
2433	0	-1.95338	1.37887	3.33225	-1.95338	63.7767	1.37887
2434	0	-1.9428	1.41248	3.35528	-1.9428	63.9322	1.41248
2435	0	-1.92929	1.44223	3.37152	-1.92929	64.1314	1.44223
2436	0	-1.92158	1.46601	3.3876	-1.92158	64.2453	1.46601
2437	0	-1.91225	1.49052	3.40277	-1.91225	64.3836	1.49052
2438	0	-1.90617	1.50568	3.41185	-1.90617	64.4738	1.50568
2439	0	-1.90008	1.52077	3.42085	-1.90008	64.5643	1.52077
2440	0	-1.89538	1.53222	3.4276	-1.89538	64.6342	1.53222
2441	0	-1.88756	1.53723	3.42479	-1.88756	64.7506	1.53723
2442	0	-1.88694	1.53875	3.42569	-1.88694	64.7599	1.53875
2443	0	-1.8821	1.5396	3.4217	-1.8821	64.8321	1.5396
2444	0	-1.88149	1.53619	3.41768	-1.88149	64.8412	1.53619
2445	0	-1.87549	1.53256	3.40805	-1.87549	64.9308	1.53256
2446	0	-1.86982	1.52873	3.39855	-1.86982	65.0157	1.52873
2447	0	-1.8625	1.52245	3.38494	-1.8625	65.1254	1.52245
2448	0	-1.85476	1.51553	3.37029	-1.85476	65.2415	1.51553
2449	0	-1.84488	1.50472	3.3496	-1.84488	65.3901	1.50472
2450	0	-1.83749	1.49117	3.32866	-1.83749	65.5015	1.49117
2451	0	-1.83335	1.47276	3.30611	-1.83335	65.5639	1.47276

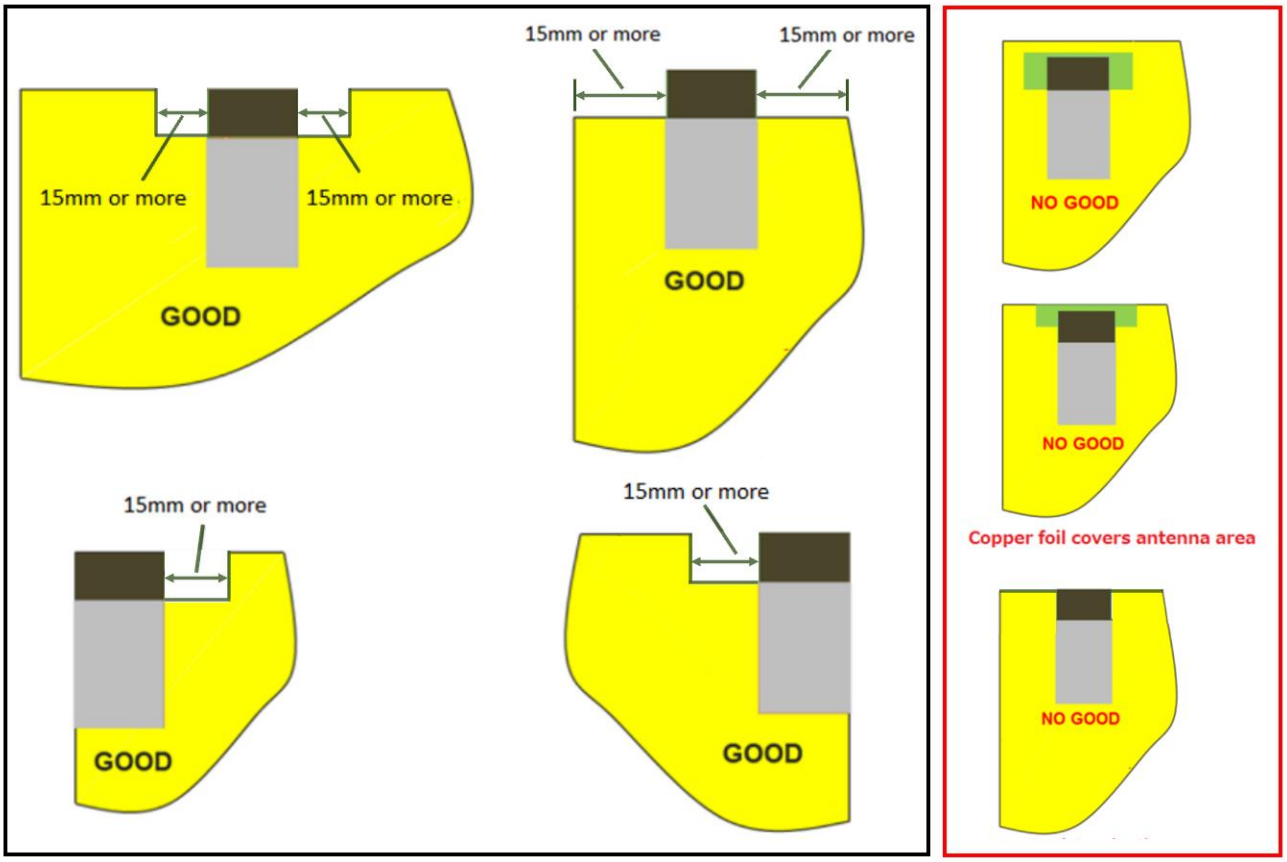
Point Values	Ant. Port Input Pwr. (dBm)	Tot. Rad. Pwr. (dBm)	Peak EIRP (dBm)	Directivity (dBi)	Efficiency (dB)	Efficiency (%)	Gain (dBi)
Frequency (MHz)							
2452	0	-1.82828	1.45414	3.28242	-1.82828	65.6406	1.45414
2453	0	-1.82716	1.43012	3.25728	-1.82716	65.6574	1.43012
2454	0	-1.82492	1.40921	3.23412	-1.82492	65.6914	1.40921
2455	0	-1.82773	1.37954	3.20727	-1.82773	65.6488	1.37954
2456	0	-1.82891	1.36349	3.1924	-1.82891	65.631	1.36349
2457	0	-1.83118	1.35633	3.1875	-1.83118	65.5967	1.35633
2458	0	-1.83146	1.34416	3.17562	-1.83146	65.5925	1.34416
2459	0	-1.83112	1.3376	3.16872	-1.83112	65.5975	1.3376
2460	0	-1.83485	1.328	3.16286	-1.83485	65.5412	1.328
2461	0	-1.83881	1.32318	3.16199	-1.83881	65.4816	1.32318
2462	0	-1.84122	1.31685	3.15807	-1.84122	65.4452	1.31685
2463	0	-1.8468	1.30574	3.15254	-1.8468	65.3612	1.30574
2464	0	-1.85103	1.30246	3.15349	-1.85103	65.2976	1.30246
2465	0	-1.85995	1.30033	3.16028	-1.85995	65.1636	1.30033
2466	0	-1.86424	1.29547	3.15971	-1.86424	65.0993	1.29547
2467	0	-1.86517	1.3008	3.16597	-1.86517	65.0852	1.3008
2468	0	-1.87086	1.2957	3.16657	-1.87086	65	1.2957
2469	0	-1.87635	1.29679	3.17314	-1.87635	64.918	1.29679
2470	0	-1.88173	1.29152	3.17325	-1.88173	64.8377	1.29152
2471	0	-1.88599	1.29049	3.17648	-1.88599	64.7741	1.29049
2472	0	-1.88947	1.29084	3.18031	-1.88947	64.7222	1.29084
2473	0	-1.89019	1.29049	3.18068	-1.89019	64.7114	1.29049
2474	0	-1.88951	1.29716	3.18667	-1.88951	64.7216	1.29716
2475	0	-1.89197	1.30143	3.1934	-1.89197	64.685	1.30143
2476	0	-1.89436	1.30209	3.19645	-1.89436	64.6493	1.30209
2477	0	-1.90168	1.30185	3.20352	-1.90168	64.5405	1.30185
2478	0	-1.90737	1.30324	3.21061	-1.90737	64.456	1.30324
2479	0	-1.91543	1.30546	3.22089	-1.91543	64.3365	1.30546
2480	0	-1.92365	1.30976	3.23341	-1.92365	64.2148	1.30976

7.2 Antenna application note

BTA65 has internal PCB pattern antenna, the antenna placement affects the overall performance of the system. The antenna requires free space to radiate RF signals and it must not be surrounded by the ground plane. Recommend that the areas underneath the antenna on the host PWB must not contain copper on top, inner, or bottom layers.

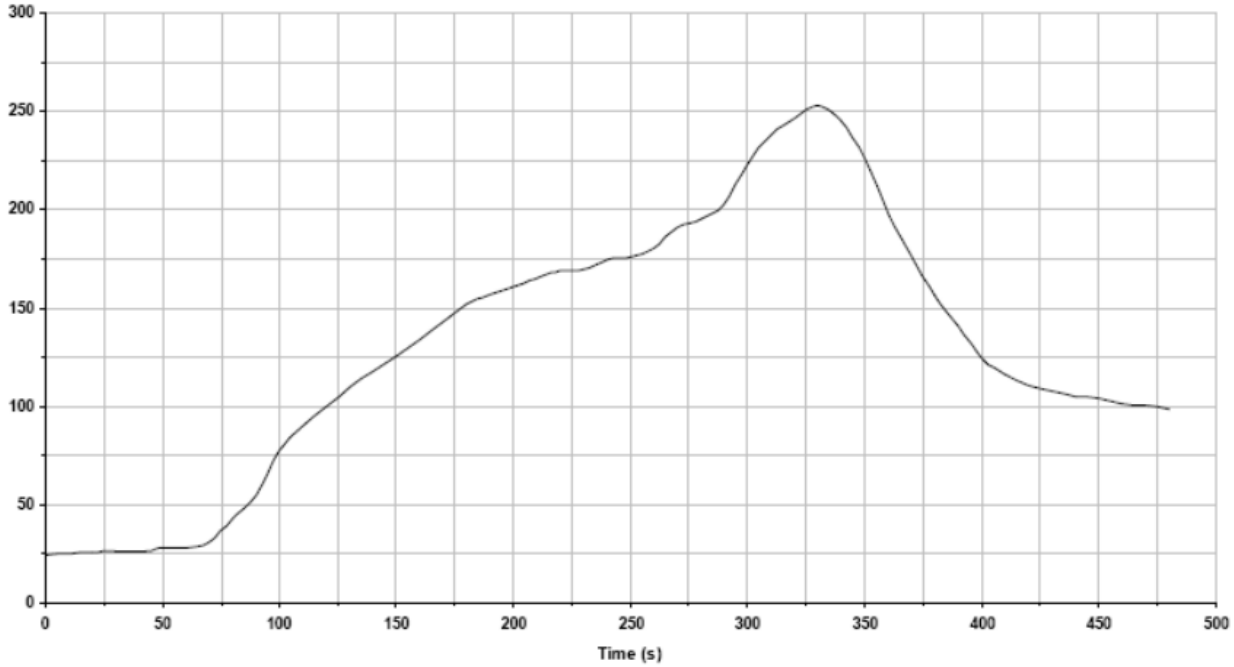
A low-impedance ground plane will ensure the best radio performance. The ground plane can be extended beyond the minimum recommendation, as required for the main PWB EMC noise reduction. For the best range performance, keep all external metal at least 15mm away from the on-board PWB trace antenna.

Following figure illustrates example of good and poor placement of BTA65 on a board with GND plane.



8 Handling precautions

8.1 Recommended reflow profile



Key features of the profile:

Initial Ramp = 1-3°C /sec to 175°C equilibrium

Equilibrium time = 60 to 90 seconds

Ramp to Maximum temperature (255°C) = 3°C /sec Max

Time above liquidus temperature (217°C): 60 – 90 seconds

Device absolute maximum reflow temperature: 255℃

Possible times of Reflow: ≤3 times

8.2 Storge and baking conditions

(1) If the moisture-proof package is not opened after shipment, please store in an environment of 25±3°C, 30%～60%RH.

(2) After open the moisture-proof packaging, please complete all mounting work within 168 hours.

(3) Baking Condition: if the criteria in (1), (2) are not met, please bake at 55°C, 24hours, in principle, baking should be done once.

9 Certification

9.1 Bluetooth BQB certification

The BTA65 series modules have completed the Bluetooth qualification process. Not only audio sink mode(Classic and LE Audio), but also audio source mode(Classic and LE Audio) has passed the certification test. The Bluetooth Qualification details are shown in following figure. You can also access following Bluetooth home page to confirm the qualification information.

https://launchstudio.bluetooth.com/ListingDetails/218613

Qualified Design:

QDID	244554
TCRL Version	TCRL 2023-1
Product Type	End Product
Combined Designs	182912,194027
Design Name	BTA65 series Bluetooth Module
Design Model Number	BTA65CI
Design Description	Bluetooth Module
Hardware Version Number	V0.7
Software Version Number	V100
Core Specification	5.3

Declaration Details

Listing Details

Declaration ID	D069014
Referenced Qualified Designs	
Company	USE Inc.
Listing Date	2024-06-26
Specification Name	5.3
Wi-Fi Certification ID	

Product List

Product Name	Product Website	Product Category	▼Publish Date	Archive Date	Model Number	Subset ID	Description
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65CI		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65AI		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65BI		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65DI		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65TI		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65AE		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65BE		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65CE		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65DE		Bluetooth Module
USE BTA65 series Bluetooth Module	https://www.use-inc.co.jp/	Unique Products	2024-06-26		BTA65TE		Bluetooth Module

9.2 Radio Certification

The internal antenna modules(BTA65AI, BTA65BI, BTA65CI, BTA65DI, BTA65TI) have completed radio certification of the following countries or regions.

No.	Country/Region	Certification	Standards	Certification No./ID
1	United States	FCC ID	Radio: FCC 47CFR §2.1091 FCC Part 15.247	2BHQU-BTA65
2	Canada	ISED	Radio: RSS-102 Issue 5, Amendment 1, February 2021 RSS-247 Issue 3, August 2023 RSS-Gen Issue 5, Amendment 2, February 2021	28613-BTA65
3	Japan	TELEC	Radio: Article 2 Paragraph 1 of Item 19, annex 43 and annex 1	220-JP8023
4	Europe	CE RED	Safety: EN IEC 62368-1:2020+A11:2020 EN IEC 62311: 2020 EMC: EN 55032:2015/A11:2020 EN 55035:2017/A11:2020 ETSI EN 301 489-1 V2.2.3 (2019-11) ETSI EN 301 489-17 V3.2.4 (2020-09) Radio: EN IEC 62311: 2020 ETSI EN 300 328 V2.2.2 (2019-07)	STS2406150RE

10 Module label specification

Label size: Length: 10mm*Width: 10mm

Label display:

“USE”: module maker.

“BTA65XX”: Module Part Number (XX is variable, please refer to “1.2.1 BTA65 series part number”).

“505E5CCB2620”: 12 letters Bluetooth MAC address/Serial number (it is variable).

“XXXXXXXX”: Customer Material Code (XXXXXXXX is variable, it is decided with customer).

“Vxxx”: the module firmware version (xxx is variable. V100 means the firmware is V1.0.0).

“FCC ID:2BHQU-BTA65”: USA FCC ID information.

“IC:28613-BTA65”: Canada IC ID information.

QR code area: QR code includes 12 letters Bluetooth MAC address information.

11 Package

Delivering Carton Box (Maximum 5040 pcs module per box if full pack)

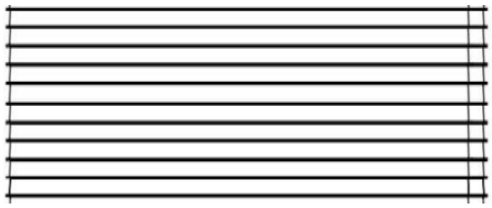
63 pcs per tray, 10 trays per ESD PE bag, sealed in ESD PE bag.

Maximum modules per ESD PE bag is 630 pcs.

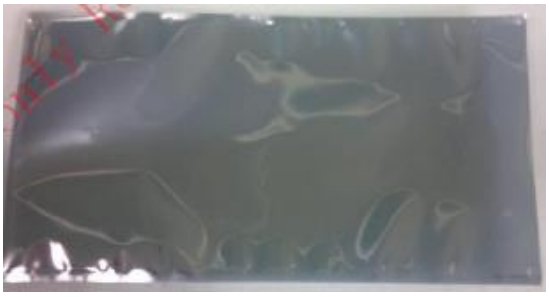
To hold of module carton box for shipment, Maximum 8 bags per box

Tray dimension 28mm x 15.1mm × 7mm (W x D x H)

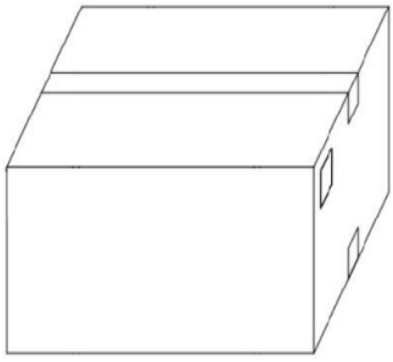
10 trays/per ESD PE bag



ESD PE bag dimension: 390mm x 220mm



Delivering carton box dimension: 34.5cm x 33.5cm x31.5cm (W x D x H)



Actual Photo

tray photo: 63 pcs/tray

10 trays packing per ESD PE bag (Maximum 630 pcs modules)

Carton box (Maximum 8 bags, 5040 pcs modules)

Contact Information

USE Inc.
9/F Technoport Taiju Life Building, 2-16-2
Minamikamata, Ota-ku, Tokyo, Japan
Postal Code: 144-0035
Tel: +81-3-5744-4532
Fax: +81-3-5744-4538

USE TECHNOLOGY (SHENZHEN) CO., LTD
Room 312, TianXin Automobile Life Venue,
No.46 Meilin Road, FuTian District, ShenZhen, China
Postal Code: 518049
Tel: +86-755-8202-0159
Fax: +86-755-2533-9389
E-mail: ken.ren@use-inc.co.jp

FCC Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

OEM INTEGRATION INSTRUCTIONS:

This device is intended only for OEM integrators under the following conditions:

The module must be installed in the host equipment such that 20 cm is maintained between the antenna and users, and the transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the internal on-board antenna that has been originally tested and certified with this module. External antennas are not supported. As long as these 3 conditions above are met, further transmitter test will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). The end-product may need Verification testing, Declaration of Conformity testing, a Permissive Class II Change or new Certification. Please involve a FCC certification specialist in order to determine what will be exactly applicable for the end-product.

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. In such cases, please involve a FCC certification specialist in order to determine if a Permissive Class II Change or new Certification is required.

Upgrade Firmware:

The software provided for firmware upgrade will not be capable to affect any RF parameters as certified for the FCC for this module, in order to prevent compliance issues.

End product labeling:

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID: 2BHQU-BTA65”.

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which

integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

2.2 List of applicable FCC rules

List the FCC rules that are applicable to the modular transmitter. These are the rules that specifically establish the bands of operation, the power, spurious emissions, and operating fundamental frequencies. DO NOT list compliance to unintentional-radiator rules (Part 15 Subpart B) since that is not a condition of a module grant that is extended to a host manufacturer. See also Section 2.10 below concerning the need to notify host manufacturers that further testing is required.

Explanation: This module meets the requirements of FCC part 15C(15.247).

2.3 Summarize the specific operational use conditions

Describe use conditions that are applicable to the modular transmitter, including for example any limits on antennas, etc. For example, if point-to-point antennas are used that require reduction in power or compensation for cable loss, then this information must be in the instructions. If the use condition limitations extend to professional users, then instructions must state that this information also extends to the host manufacturer's instruction manual. In addition, certain information may also be needed, such as peak gain per frequency band and minimum gain, specifically for master devices in 5 GHz DFS bands.

Explanation: The EUT has a PCB Antenna and the antenna use a permanently attached antenna which is not replaceable.

2.4 Limited module procedures

If a modular transmitter is approved as a "limited module," then the module manufacturer is responsible for approving the host environment that the limited module is used with. The manufacturer of a limited module must describe, both in the filing and in the installation instructions, the alternative means that the limited module manufacturer uses to verify that the host meets the necessary requirements to satisfy the module limiting conditions.

A limited module manufacturer has the flexibility to define its alternative method to address the conditions that limit the initial approval, such as: shielding, minimum signaling amplitude, buffered modulation/data inputs, or power supply regulation. The alternative method could include that the limited module manufacturer reviews detailed test data or host designs prior to giving the host manufacturer approval.

This limited module procedure is also applicable for RF exposure evaluation when it is necessary to demonstrate compliance in a specific host. The module manufacturer must state how control of the product into which the modular transmitter will be installed will be maintained such that full compliance of the product is always ensured. For additional hosts other than the specific host originally granted with a limited module, a Class II permissive change is required on the module grant to register the additional host as a specific host also approved with the module.

Explanation: The Module is not a limited module.

2.5 Trace antenna designs

For a modular transmitter with trace antenna designs, see the guidance in Question 11 of KDB Publication 996369 D02 FAQ – Modules for Micro-Strip Antennas and traces. The integration information shall include for the TCB review the integration instructions for the following aspects: layout of trace design, parts list (BOM), antenna, connectors, and isolation requirements.

a) Information that includes permitted variances (e.g., trace boundary limits, thickness, length, width, shape(s),dielectric constant, and impedance as applicable for each type of antenna);

b) Each design shall be considered a different type (e.g., antenna length in multiple(s) of frequency, the wavelength, and antenna shape (traces in phase) can affect antenna gain and must be considered); c) The parameters shall be provided in a manner permitting host manufacturers to design the printed circuit (PC) board layout;

d) Appropriate parts by manufacturer and specifications;

e) Test procedures for design verification; and

f) Production test procedures for ensuring compliance.

The module grantee shall provide a notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

Explanation: Yes, The module with PCB antenna designs, Please refer to the antenna specification book for antenna dimensions.

2.6 RF exposure considerations

It is essential for module grantees to clearly and explicitly state the RF exposure conditions that permit a host product manufacturer to use the module. Two types of instructions are required for RF exposure information: (1) to the host product manufacturer, to define the application conditions (mobile, portable – xx cm from a person’s body); and (2) additional text needed for the host product manufacturer to provide to end users in their end-product manuals. If RF exposure statements and use conditions are not provided, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID (new application).

Explanation: This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment, This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body." This module is designed to comply with the FCC statement, FCC ID is: 2BHQU-BTA65.

2.7 Antennas

A list of antennas included in the application for certification must be provided in the instructions. For modular transmitters approved as limited modules, all applicable professional installer instructions must be included as part of the information to the host product manufacturer. The antenna list shall also identify the antenna types (monopole, PIFA, dipole, etc. (note that for example an “omni-directional antenna” is not considered to be a specific “antenna type”)).

For situations where the host product manufacturer is responsible for an external connector, for example with an RF pin and antenna trace design, the integration instructions shall inform the installer that unique antenna connector must be used on the Part 15 authorized transmitters used in the host product. The module manufacturers shall provide a list of acceptable unique connectors.

Explanation: The EUT has a PCB Antenna, and the antenna use a permanently attached antenna which is unique.

2.8 Label and compliance information

Grantees are responsible for the continued compliance of their modules to the FCC rules. This includes advising host product manufacturers that they need to provide a physical or e-label stating “Contains FCC ID” with their finished product. See Guidelines for Labeling and User Information for RF Devices – KDB Publication 784748.

Explanation:The host system using this module, should have label in a visible area indicated the following texts: "Contains FCC ID: 2BHQU-BTA65."

2.9 Information on test modes and additional testing requirements[5]

Additional guidance for testing host products is given in KDB Publication 996369 D04 Module Integration Guide. Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.

The grantee should provide information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, versus with multiple, simultaneously transmitting modules or other transmitters in a host.

Grantees can increase the utility of their modular transmitters by providing special means, modes, or instructions that simulates or characterizes a connection by enabling a transmitter. This can greatly simplify a host manufacturer’s determination that a module as installed in a host complies with FCC requirements.

Explanation: Top band can increase the utility of our modular transmitters by providing instructions that simulates or characterizes a connection by enabling a transmitter.

2.10 Additional testing, Part 15 Subpart B disclaimer

The grantee should include a statement that the modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and

that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Explanation: The module without unintentional-radiator digital circuity, so the module does not require an evaluation by FCC Part 15 Subpart B. The host shoule be evaluated by the FCC Subpart B.

IC Warning

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:

(1) This device may not cause interference, and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

The modular can be installed or integrated in mobile or fix devices only. This modular cannot be installed in any portable device.

IC Radiation Exposure Statement

This modular complies with IC RF radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This modular must be installed and operated with a minimum distance of 20 cm between the radiator and user body.

For a host manufacture's using a certified modular, if (1) the module's IC number is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the IC number of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module IC: " 28613-BTA65" or "Contains IC: 28613-BTA65" must be used.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement

Le modular peut être installé ou intégré dans un mobile ou réparer une seule chose Installation dans n’importe quel appareil portable.

Déclaration de rayonnement IC

Ce modular complies avec des radiations émettrices de rayonnement Environnement. Ceci ne doit pas être co-localisé ou opérer avec des autres Ce modular doit être installé et obtenu avec une distance minimale de 20 cm entre les radiateurs et le corps de l’utilisateur.

Pour un hôte, on utilise un modular, si (1) le numéro de module est non visible Quand on est installé dans le serveur, or (2) si le propriétaire est commercialisé Straightforward commonly used for the access to remove travail so that the number IC en vue Le module est visible; Ensuite, le label permanent a été attribué au module: "Contient le Module IC:" 28613-BTA65" ou "contenu IC: 28613-BTA65" doit" be use