PSM803 Hardware Guide

V1.0

Disclaimer

Customers must design and develop their products referring to the information provided in the document. The Company shall not be liable for any damage caused by failure to comply with relevant operation or specifications or rules. Due to product version upgrade or other reasons, the Company reserves the right to modify any information in this document at any time without prior notice and any responsibility. Unless otherwise agreed, all statements, information and suggestions in this document do not constitute any express or implied guarantee.

The module will be installed on a fixed or mobile device.

Safety Instructions

Do not operate wireless communication products in areas where the use of radio is not recommended without proper equipment certification. These areas include environments that may generate radio interference, such as flammable and explosive environments, medical devices, aircraft or any other equipment that may be subject to any form of radio interference.

Wireless communication devices do not guarantee effective connection under any circumstances, such as when the (U) SIM card is invalid or the device is in arrears. In an emergency, please use the emergency call function when the device is turned on, and ensure that the device is located in an area with sufficient signal strength.

Directory

1. Introduction

1.1 Introduction

This document describes the hardware application interface of PSM803, including related application connection and RF interface, which can help users quickly understand detailed information such as module interface definition, electrical performance, and structural dimensions. And you can refer to its design scheme to optimize your own design.

Statement Acknowledging device restrictions:

Prohibited for control of or communications with unmanned aircraft systems, including drones.

1.2 FCC Statement

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is intended only for OEM integrators under the following conditions:

1. The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2. The transmitter module may not be co-located with any other transmitter or antenna,

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on

the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labelling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users.
The final end product must be labelled in a visible area with the following:
“Contains FCC ID:2BHQS-PSM803”.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

1.21 List of applicable FCC rules

FCC Part 15.247

1.22 Specific operational use conditions

This transmitter/module and its antenna(s) must not be co-located or operating in conjunction with any transmitter. This information also extends to the host manufacturer’s instruction manual.

1.23 Limited module procedures

Not applicable

1.24 Trace antenna designs

It is “not applicable” as trace antenna which is not used on the module.

1.25 Antennas

The module provides WiFi/BT antenna pins WIFI-ANT0 and WIFI-ANT1. The antenna on the user's motherboard should be connected to the module's antenna pins using a microstrip line or strip line with a characteristic impedance of 50 ohms.

Sub 6G antenna; 1.5dBi; 600MHz-5.0GMHZ 5Ghz-7.125Ghz

1.26 Label and compliance information

The end product must carry a physical label or shall use e-labeling followed KDB784748D01 and KDB 784748 stating “Contains Transmitter Module FCC ID: 2BHQS-PSM803”.

1.27 Information on test modes and additional testing requirements

For more information on testing, please contact the manufacturer.

1.28 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuity.

1.3 IC Statement

Industry Canada Statement

This device complies with industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:(1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exemptsde licence. L'exploitation est autorisée aux deux conditions suivantes:

(1)l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, méme si le brouillage estsusceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour unenvironnement non contrólé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm dedistance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the followingconditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans lesconditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne etles utilisateurs, et

2) Le module émetteur peut ne pas être coimplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur neseront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur sonproduit final pour toutes exigences de conformité supplémentaires requis pour ce module installé

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. in these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurationsd'ordinateur portable ou de certaines co-ocalisation avec un autre émetteur), l'autorisation duCanada n'est plus considéré comme valide et l'lD lC ne peut pas être utilisé sur le produit final. Dansces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur)et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: PSM803".

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antennepeut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et lesutilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:"Contient des IC: PSM803".

Manual information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'integrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant ala facon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final quiintègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réalementaires requises etavertissements comme indiqué dans ce manuel.

2. Module Overview

The PSM803 series module adopts the Qualcomm QCS8550 as main chip, paired with the WCN7851 wifi Bluetooth chip, and is equipped with 16GB LPDDR5X SDRAM (default) and 128GB UFS internal storage.

The PSM803 module can be used in multiple fields such as VR Camera, Smart Box, Intelligent Robot, Video Surveillance, and Vehicle.

The hardware interface of this module is as follows:

- 2 MIPI screen support
- 8 Camera interfaces (MIPI, one camera AON supported, up to 5 cameras can be opened simultaneously)
- 4 flash interfaces

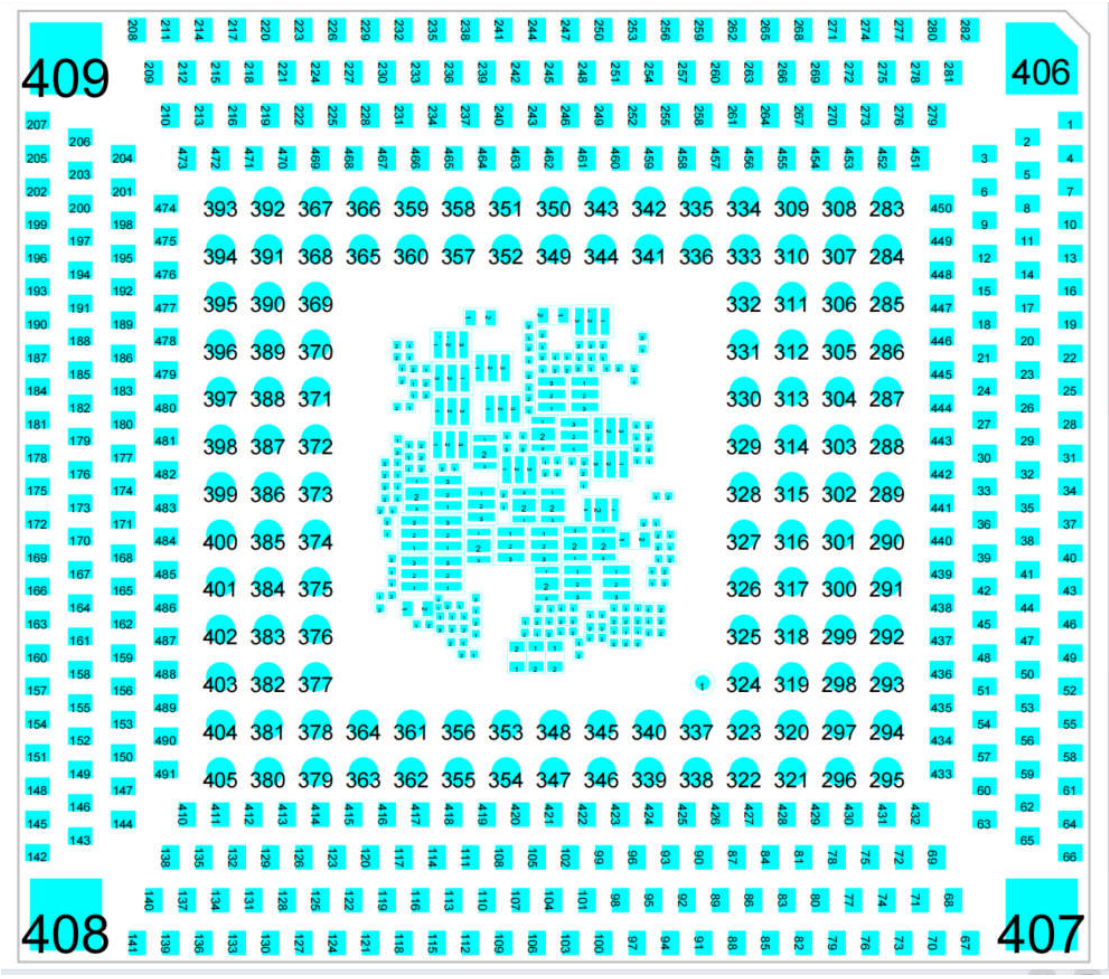
- 1 USB interface（USB2.0 and USB3.1 supported）
- 1 TF interface
- 3 RGB interface
- Multiple sets of SPI,UART,I2C interfaces (refer to the following GPIO multiplexing functions for details)
- 1 PCIE4.0 extension interface
- 6 I2S audio digital interfaces
- 5 ADC interface
- Supports WiFi 2.4/5/6/7 and Bluetooth 5.3 functions
- Multiple configurable GPIO groups

2.1 Module characteristic parameters

Characteristics	Illustration
Platform	Qualcomm QCS8550
CPU	Octa-core CPU
GPU	Adreno 740
Memory	128GB UFS+16GB LPDDR5X（Compatible with other memory configuration）
OS	Android 13
Scale	45.0x40.0x3.95mm
WI-FI	WCN7851:IEEE 802.11a/n/ac/ax/be 2.4G&5G&6G&7G
Bluetooth	BT5.3
Display	Max resolution：3480 × 2160 at 120 Hz, 3360 × 1600 at 144 Hz
	Interface: 2st LCM：MIPI DSI 4-lane;
Camera	Interface:8*CSI， 4-Lane (CSI4 is AON Camera)
	(36 M + 36 M + 36 M) @ 30 fps - triple camera (64 M + 36 M) @ 30 fps - dual camera 108 M @ 30 fps - single cameras
Video	Video decode 4K@240fps or 8K@60fps H.264/H.265/VP9 Video encode 4K@120fps or 8K@30fps H.264/H.265 Decode+Encode 4K60 Decode + 4K60 Encode
Input interface	Key（Power on/off，Volume+/-，reset）；TP，Hardware reset supported
Application interface	VBAT Input，3.5~4.2V
	SD3.0
	USB2.0(3.1), OTG supported, USB download supported
	Multiple BLSP interfaces
	5*ADC
	QC 5.0 supported
	Vibrator supported
	Wireless Charge supported
	RTC supported
	RF interface 2.4G WiFi/BT antenna ，5G/6G/7G WIFI-antenna
	5*I2S interface，4*DMIC interface

3. Module Package

3.1 Pin distribution diagram



3.2 Pin description

Pin Name	Pin No.	Power Domain	Description	Note
POWER				
VBATT	208,209,211, 212,214,215	3.5~4.2V	Module main power input	Additional voltage stabilizing capacitors and surge protection are required.
USB_VBUS	206,203,207,205	5~20V	USB input	Additional capacitance and surge protection are required
VCOIN	491	3V	Backup battery input	/
VREG_L9B_2P9	192	2.96V	SD/MMC Power voltage	1200mA
VREG_L8B_1P8	85	1.8V	SD CARD IO Power	150mA

			Domain	
VREG_L6B_1P8	324	1.8V	(NFC) - UICC0	300mA
VREG_L16B_2P8	484	2.8V	2P7V RF Switches	600mA
VREG_L3G_1P2	69	1.2V	PX 1P2 AON	1200mA
VREG_L11B_1P2	432	1.2V	Display DDIC Dig	600mA
VREG_L10B_1P8	309	1.8V	DMICs 1P8	300mA
VREG_L7B_1P8	371	1.8V	(NFC) - UICC1	300mA
VREG_L4B_1P8	372	1.8V	Reserved	300mA
VREG_L15B_1P8	299	1.8V	GPIO IO Voltage	2000mA
VREG_L1B_1P8	384	1.8V	Sensor Voltage	600 mA
VREG_L12B_1P8	472	1.8V	DISPLAY - TOUCH IO Voltage	1200mA
VREG_L14B_3P2	471	3.2V	TP Voltage	150mA
VREG_L13B_3P0	485	3V	Display Voltage	150mA
VREG_L2B_3P0	474	3V	Sensor Voltage	600 mA
VPH_PWR	113,115,116	3.5~4.2V	System Voltage	/
VREG_BOB1	191,189	3.3V	BOB Voltage，LV battery support	3000mA
VREG_BOB2	481,482	2.72V	BOB2 Voltage	3000mA
WPC_DIV2	210,473	5~20V	Wireless charger input	3A
KEY				
POWER_KEY	86	1.8/1.2V (Inner pull up）	Power on input	
PM_RESIN_N	89	1.8/1.2V (Inner pull up）	Reset Key（Volume+）	
KYPD_VOLP_N	296	MV power domain （VPH_PWR）	Volume-	
CSI				
CSI0_NC_CLK_P	462	CSI	CSI0 CLK and LANE	
CSI0_A0_CLK_M	463	CSI		
CSI0_B0_LN0_P	240	CSI		
CSI0_C0_LN0_M	243	CSI		
CSI0_A1_LN1_P	239	CSI		
CSI0_B1_LN1_M	242	CSI		
CSI0_C1_LN2_P	232	CSI		
CSI0_A2_LN2_M	235	CSI		
CSI0_B2_LN3_P	238	CSI		

CSI0_C2_LN3_M	241	CSI		
CSI1_NC_CLK_P	246	CSI	CSI1 CLK and LANE	
CSI1_A0_CLK_M	249	CSI		
CSI1_B0_LN0_P	459	CSI		
CSI1_C0_LN0_M	252	CSI		
CSI1_A1_LN1_P	458	CSI		
CSI1_B1_LN1_M	255	CSI		
CSI1_C1_LN2_P	247	CSI		
CSI1_A2_LN2_M	244	CSI		
CSI1_B2_LN3_P	245	CSI		
CSI1_C2_LN3_M	248	CSI		
CSI2_NC_CLK_P	256	CSI	CSI2 CLK and LANE	
CSI2_A0_CLK_M	259	CSI		
CSI2_B0_LN0_P	254	CSI		
CSI2_C0_LN0_M	253	CSI		
CSI2_A1_LN1_P	257	CSI		
CSI2_B1_LN1_M	260	CSI		
CSI2_C1_LN2_P	258	CSI		
CSI2_A2_LN2_M	457	CSI		
CSI2_B2_LN3_P	261	CSI		
CSI2_C2_LN3_M	456	CSI		
CSI3_NC_CLK_P	449	CSI	CSI3 CLK and LANE	
CSI3_A0_CLK_M	9	CSI		
CSI3_B0_LN0_P	450	CSI		
CSI3_C0_LN0_M	6	CSI		
CSI3_A1_LN1_P	2	CSI		
CSI3_B1_LN1_M	1	CSI		
CSI3_C1_LN2_P	5	CSI		
CSI3_A2_LN2_M	4	CSI		
CSI3_B2_LN3_P	8	CSI		
CSI3_C2_LN3_M	7	CSI		
CSI4_NC_CLK_P	270	CSI	CSI4 CLK and LANE	AON camera
CSI4_A0_CLK_M	454	CSI		
CSI4_B0_LN0_P	267	CSI		
CSI4_C0_LN0_M	455	CSI		
CSI4_A1_LN1_P	273	CSI		
CSI4_B1_LN1_M	453	CSI		
CSI4_C1_LN2_P	276	CSI		
CSI4_A2_LN2_M	452	CSI		
CSI4_B2_LN3_P	279	CSI		
CSI4_C2_LN3_M	451	CSI		
CSI5_NC_CLK_P	447	CSI	CSI5 CLK and LANE	
CSI5_A0_CLK_M	15	CSI		

CSI5_B0_LN0_P	448	CSI		
CSI5_C0_LN0_M	12	CSI		
CSI5_A1_LN1_P	14	CSI		
CSI5_B1_LN1_M	13	CSI		
CSI5_C1_LN2_P	17	CSI		
CSI5_A2_LN2_M	16	CSI		
CSI5_B2_LN3_P	20	CSI		
CSI5_C2_LN3_M	19	CSI		
CSI6_NC_CLK_P	226	CSI	CSI6 CLK and LANE	
CSI6_A0_CLK_M	227	CSI		
CSI6_B0_LN0_P	228	CSI		
CSI6_C0_LN0_M	229	CSI		
CSI6_A1_LN1_P	230	CSI		
CSI6_B1_LN1_M	231	CSI		
CSI6_C1_LN2_P	234	CSI		
CSI6_A2_LN2_M	237	CSI		
CSI6_B2_LN3_P	464	CSI		
CSI6_C2_LN3_M	465	CSI		
CSI7_NC_CLK_P	220	CSI	CSI7 CLK and LANE	
CSI7_A0_CLK_M	221	CSI		
CSI7_B0_LN0_P	222	CSI		
CSI7_C0_LN0_M	223	CSI		
CSI7_A1_LN1_P	224	CSI		
CSI7_B1_LN1_M	225	CSI		
CSI7_C1_LN2_P	466	CSI		
CSI7_A2_LN2_M	467	CSI		
CSI7_B2_LN3_P	468	CSI		
CSI7_C2_LN3_M	469	CSI		
DSI				
DSI0_A0_LN0_P	175	DSI	DSI0 CLK and LANE	
DSI0_B0_LN0_M	173	DSI		
DSI0_C0_LN1_P	160	DSI		
DSI0_A1_LN1_M	163	DSI		
DSI0_B1_CLK_P	172	DSI		
DSI0_C1_CLK_M	170	DSI		
DSI0_A2_LN2_P	169	DSI		
DSI0_B2_LN2_M	167	DSI		
DSI0_C2_LN3_P	161	DSI		
DSI0_NC_LN3_M	158	DSI		
DSI0_NC_CLK1_P	164	DSI	NC	
DSI0_NC_CLK1_M	166	DSI	NC	
DSI1_A0_LN0_P	182	DSI	DSI1 CLK and LANE	
DSI1_B0_LN0_M	184	DSI		

DSI1_C0_LN1_P	181	DSI		
DSI1_A1_LN1_M	179	DSI		
DSI1_B1_CLK_P	186	DSI		
DSI1_C1_CLK_M	183	DSI		
DSI1_A2_LN2_P	190	DSI		
DSI1_B2_LN2_M	188	DSI		
DSI1_C2_LN3_P	187	DSI		
DSI1_NC_LN3_M	185	DSI		
PCIE				
PCIE1_TX0_M	22	/	PCIE1 CLK and DATA	
PCIE1_TX0_P	25	/		
PCIE1_RX0_M	29	/		
PCIE1_RX0_P	27	/		
PCIE1_TX1_M	23	/		
PCIE1_TX1_P	24	/		
PCIE1_RX1_M	444	/		
PCIE1_RX1_P	443	/		
PCIE1_REFCLK_M	26	/		
PCIE1_REFCLK_P	28	/		
PCIE1_RESET_N/GPIO_97	49	1.8V	PCI Reset	If using the PCIE_ function, please use these three GPIOs by default and do not use other GPIOs
PCIE1_CLK_REQ_N/GPIO_98	50	1.8V	PCIE CLK Request	
PCIE1_WAKE_N/GPIO_99	52	1.8V	PCIE Wakeup Pin	
USB				
USB0_HS_DM	145	/	USB0	
USB0_HS_DP	142	/		
USB0_SS_TX0_P	149	/		
USB0_SS_TX0_M	152	/		
USB0_SS_TX1_M	146	/		
USB0_SS_TX1_P	143	/		
USB0_SS_RX0_M	153	/		
USB0_SS_RX0_P	150	/		
USB0_SS_RX1_P	144	/		
USB0_SS_RX1_M	147	/		
USB0_DP_AUX_N	151	/		If DP function is not used, this pin can be NC
USB0_DP_AUX_P	154	/		
USB_CC1	117	/		
USB_CC2	119	/		
SBU1	426	/		USB Audio Pin
SBU2	425	/		
SDIO				
SDC2_SDCARD_CMD	92	1.2V	SD Signal	Additional level shift required
SDC2_SDCARD_CLK	91	1.2V		

SDC2_SDCARD_DATA_0	94	1.2V		
SDC2_SDCARD_DATA_1	95	1.2V		
SDC2_SDCARD_DATA_2	97	1.2V		
SDC2_SDCARD_DATA_3	98	1.2V		
SDCARD_DETECT_N	101	1.8V	SD Detection	External reserved pull-up (input) required
GPIO				
* The following GPIO related configurations are recommended settings, and users can choose feasible solutions according to their actual needs.				
Function	Pin	Power Domain	Interrupt Wakeup	GPIO No.
GPIO0/CCI_I2C5_SDA	298	1.8V	Y	GPIO_0
GPIO1/CCI_I2C5_SCL	297	1.8V	N	GPIO_01
GPIO2/MULTI_EE_I2C_SDA/ NC	80	1.8V	Y	GPIO_02
GPIO3/MULTI_EE_I2C_SCL/ NC	87	1.8V	Y	GPIO_03
GPIO04	342	1.8V	N	GPIO_04
GPIO05	343	1.8V	N	GPIO_05
GPIO06	291	1.8V	N	GPIO_06
GPIO07	290	1.8V	N	GPIO_07
GPIO08	283	1.8V	Y	GPIO_08
GPIO09	308	1.8V	Y	GPIO_09
GPIO10	53	1.8V	N	GPIO_10
GPIO11/CC_DIR	402	1.8V	Y	GPIO_11
GPIO12	354	1.8V	N	GPIO_12
GPIO13	76	1.8V	N	GPIO_13
GPIO14	307	1.8V	Y	GPIO_14
GPIO15	367	1.8V	Y	GPIO_15
GPIO16/ALSP_INT_N	174	1.8V	Y	GPIO_16
GPIO17/HALL_INT_N	70	1.8V	Y	GPIO_17
GPIO18/PRESS_INT	320	1.8V	Y	GPIO_18
GPIO19/SAR_INT_N	288	1.8V	Y	GPIO_19
APPS_I2C_SDA/GPIO_20	105	1.8V	N	GPIO_20
APPS_I2C_SCL/GPIO_21	108	1.8V	N	GPIO_21
GPIO22	287	1.8V	N	GPIO_22
GPIO23	286	1.8V	N	GPIO_23
GPIO24/TS_RESET_N	341	1.8V	Y	GPIO_24
GPIO25*/TS_INT_N	349	1.8V	Y	GPIO_25
DEBUG_TX	358	1.8V	Y	GPIO_26
DEBUG_RX	359	1.8V	Y	GPIO_27
NFC_I2C_I3C_SDA/GPIO28	380	1.8V	Y	GPIO_28
NFC_I2C_I3C_SCL/GPIO29	381	1.8V	N	GPIO_29

NFC_RESET_N/GPIO30	382	1.8V	N	GPIO_30
NFC_CLK_REQ/GPIO31	383	1.8V	Y	GPIO_31
NFC_ESE_SPI_MISO/GPIO32	376	1.8V	Y	GPIO_32
NFC_ESE_SPI_MOSI/GPIO33	377	1.8V	N	GPIO_33
NFC_ESE_SPI_CLK/GPIO34	378	1.8V	N	GPIO_34
NFC_ESE_SPI_CS_N/GPIO35	379	1.8V	Y	GPIO_35
FP_SPI_MISO/GPIO36	475	1.8V	N	GPIO_36
FP_SPI_MOSI/GPIO37	194	1.8V	N	GPIO_37
FP_SPI_CLK/GPIO38	195	1.8V	N	GPIO_38
FP_SPI_CS_N/GPIO39	196	1.8V	N	GPIO_39
GPIO40*_CAM4_PWD_N	197	1.8V	Y	GPIO_40
FP_WUHB_INT_N/GPIO41	198	1.8V	Y	GPIO_41
GPIO42	199	1.8V	N	GPIO_42
FORCE_USB_BOOT	415	1.8V	Y	GPIO_43
GPIO44/TS_SPI_MISO_I2C_SDA	177	1.8V	Y	GPIO_44
GPIO45/TS_SPI_MOSI_I2C_SCL	180	1.8V	Y	GPIO_45
GPIO46/TS_SPI_CLK	159	1.8V	Y	GPIO_46
GPIO47*/TS_SPI_CS_N	162	1.8V	Y	GPIO_47
GPIO48	285	1.8V	Y	GPIO_48
GPIO49	350	1.8V	N	GPIO_49
GPIO50	334	1.8V	N	GPIO_50
GPIO51	335	1.8V	Y	GPIO_51
GPIO52	81	1.8V	N	GPIO_52
GPIO55/NFC_INT_RFQ	414	1.8V	Y	GPIO_55
GPIO56	43	1.8V	Y	GPIO_56
GPIO57	44	1.8V	N	GPIO_57
GPIO58	46	1.8V	N	GPIO_58
GPIO59	47	1.8V	Y	GPIO_59
CAM_I3C_SDA/GPIO_60	395	1.8V	Y	GPIO_60
CAM_I3C_SCL/GPIO_61	396	1.8V	N	GPIO_61
GPIO62	393	1.8V	Y	GPIO_62
GPIO63	394	1.8V	Y	GPIO_63
LRF_SPI_MISO/GPIO_64	37	1.8V	N	GPIO_64
LRF_SPI_MOSI/GPIO_65	38	1.8V	N	GPIO_65
LRF_SPI_CLK/GPIO_66	40	1.8V	N	GPIO_66
LRF_SPI_CS_N/GPIO_67	41	1.8V	Y	GPIO_67
GPIO_68/FD_SPI_MISO	388	1.8V	N	GPIO_68
GPIO69	389	1.8V	N	GPIO_69

GPIO_70/FD_SPI_CLK	390	1.8V	N	GPIO_70
GPIO71	391	1.8V	Y	GPIO_71
GPIO_74/CCI_I2C4_SDA	293	1.8V	N	GPIO_74
GPIO_75/CCI_I2C4_SCL	292	1.8V	Y	GPIO_75
GPIO84/IMU1_INT	171	1.8V	Y	GPIO_84
GPIO85/IMU2_INT	346	1.8V	Y	GPIO_85
GPIO86*_MDP_VSYNC_P	397	1.8V	Y	GPIO_86
GPIO87*_MDP1_VSYNC_S	398	1.8V	Y	GPIO_87
GPIO88*/TS_INT_N	399	1.8V	Y	GPIO_88
GPIO89*/WSA1_EN	400	1.8V	Y	GPIO_89
GPIO90_CAM1_PWD_N	301	1.8V	N	GPIO_90
GPIO91	77	1.8V	N	GPIO_91
GPIO93	428	1.8V	N	GPIO_93
CAM_MCLK0	310	1.8V	N	GPIO_100
CAM_MCLK1	311	1.8V	N	GPIO_101
CAM_MCLK2	312	1.8V	N	GPIO_102
CAM_MCLK3	313	1.8V	N	GPIO_103
CAM_MCLK4	315	1.8V	N	GPIO_104
CAM_MCLK5	314	1.8V	N	GPIO_105
CAM_MCLK6	316	1.8V	N	GPIO_106
CAM_MCLK7	317	1.8V	Y	GPIO_107
GPIO108	410	1.8V	N	GPIO_108
GPIO109/CCI_ASYNC_IN0	318	1.8V	N	GPIO_109
CCI_I2C0_SDA	39	1.8V	N	GPIO_110
CCI_I2C0_SCL	42	1.8V	N	GPIO_111
CCI_I2C1_SDA	45	1.8V	N	GPIO_112
CCI_I2C1_SCL	48	1.8V	N	GPIO_113
CCI_I2C2_SDA	51	1.8V	N	GPIO_114
CCI_I2C2_SCL	54	1.8V	N	GPIO_115
CAM0_RST_N	66	1.8V	N	GPIO_116
CAM1_RST_N	61	1.8V	N	GPIO_117
GPIO118_CAM2_RST_N	63	1.8V	N	GPIO_118
CAM3_RST_N	65	1.8V	Y	GPIO_119
AON_CAM_RESET_N	62	1.8V	Y	GPIO_120
GPIO121/I2S1_SCK	88	1.8V	N	GPIO_121
GPIO122/I2S1_DATA0	90	1.8V	N	GPIO_122
GPIO123/I2S1_WS	336	1.8V	N	GPIO_123
GPIO124/I2S1_DATA1	93	1.8V	N	GPIO_124
GPIO125_CAM2_PWD_N	385	1.8V	N	GPIO_125
PRI_I2S_MCLK	100	1.8V	N	GPIO_125
I2S0_SCK	103	1.8V	N	GPIO_126
I2S0_DATA0	106	1.8V	N	GPIO_127
I2S0_DATA1	107	1.8V	N	GPIO_128

I2S0_WS	104	1.8V	N	GPIO_129
GPIO130	431	1.2V	N	GPIO_130
GPIO131	430	1.2V	N	GPIO_131
GPIO132	429	1.2V	N	GPIO_132
GPIO133/DISP0_RESET_N	351	1.8V	Y	GPIO_133
GPIO134	72	1.2V	N	GPIO_134
GPIO135	75	1.2V	N	GPIO_135
GPIO136	78	1.2V	N	GPIO_136
GPIO137/DISP1_RESET_N	401	1.8V	Y	GPIO_137
GPIO138	357	1.8V	N	GPIO_138
GPIO139	360	1.8V	N	GPIO_139
GPIO140	365	1.8V	N	GPIO_140
GPIO141	344	1.8V	N	GPIO_141
GPIO142	386	1.8V	N	GPIO_142
GPIO143_CAM0_PWD_N	300	1.8V	N	GPIO_143
GPIO144_CAM5_RST_N	64	1.8V	N	GPIO_144
GPIO146	387	1.8V	N	GPIO_146
GPIO147	480	1.8V	N	GPIO_147
GPIO150	73	1.8V	Y	GPIO_150
GPIO151	74	1.8V	N	GPIO_151
GPIO152	483	1.8V	N	GPIO_152
GPIO153	403	1.8V	Y	GPIO_153
GPIO154	404	1.8V	Y	GPIO_154
GPIO155	355	1.8V	Y	GPIO_155
GPIO156	319	1.8V	Y	GPIO_156
GPIO159*_CAM3_PWD_N	339	1.8V	Y	GPIO_159
GPIO161	284	1.8V	N	GPIO_161
GPIO163	347	1.8V	N	GPIO_163
GPIO165_LPI_I2S0_SCK	487	1.8V	N	GPIO_165
GPIO166*_LPI_I2S0_WS	363	1.8V	Y	GPIO_166
GPIO167_LPI_I2S0_DATA0	489	1.8V	N	GPIO_167
GPIO168_LPI_I2S0_DATA1	486	1.8V	N	GPIO_168
GPIO169_LPI_I2S0_DATA2	411	1.8V	Y	GPIO_169
GPIO170_LPI_I2S0_DATA3	120	1.8V	N	GPIO_170
LPI_I2S1_CLK	121	1.8V	Y	GPIO_171
LPI_I2S1_WS	122	1.8V	Y	GPIO_172
LPI_I2S1_DATA0	123	1.8V	N	GPIO_173
LPI_I2S1_DATA1	124	1.8V	Y	GPIO_174
LPI_I2S2_CLK	125	1.8V	N	GPIO_175
LPI_I2S2_WS	126	1.8V	Y	GPIO_176
LPI_DMIC3_CLK/I2S3_CLK	132	1.8V	Y	GPIO_177
LPI_DMIC3_DATA/I2S3_WS	133	1.8V	N	GPIO_178
GPIO179	129	1.8V	N	GPIO_179

LPI_I2S2_DATA0	127	1.8V	N	GPIO_180
LPI_I2S2_DATA1	128	1.8V	Y	GPIO_181
LPI_DMIC4_CLK/I2S3_DATA0	130	1.8V	Y	GPIO_182
LPI_DMIC4_DATA/I2S3_DATA1	131	1.8V	N	GPIO_183
GPIO186	337	1.8V	N	GPIO_186
GPIO187	323	1.8V	Y	GPIO_187
GPIO188*/I2C_SDA	340	1.8V	Y	GPIO_188
GPIO189/I2C_SDL	345	1.8V	N	GPIO_189
MAG_ALPS_I2C_SDA	134	1.8V	Y	GPIO_190
MAG_ALPS_I2C_SCL	135	1.8V	Y	GPIO_191
GPIO192/IMU_SPI_MISO	136	1.8V	Y	GPIO_192
GPIO193/IMU_SPI_MOSI	137	1.8V	Y	GPIO_193
GPIO194/IMU_SPI_CLK	138	1.8V	N	GPIO_194
GPIO195/IMU_SPI_CS_N	139	1.8V	N	GPIO_195
SENSOR_I2C_SDA	140	1.8V	Y	GPIO_196
SENSOR_I2C_SCL	141	1.8V	Y	GPIO_197
GPIO198	289	1.8V	Y	GPIO_198
GPIO199	436	1.8V	Y	GPIO_199
GPIO200	362	1.8V	Y	GPIO_200
AON_CAM_STANDBY_0	412	1.8V	Y	GPIO_206
AON_CAM_STANDBY_1	413	1.8V	Y	GPIO_207
GPIO208/CCI_I2C3_SDA	57	1.8V	Y	GPIO_208
GPIO209/CCI_I2C3_SCL	60	1.8V	Y	GPIO_209

Special function pins		
Pin Definition	No.	Note
PMK_CLK7_NFC_IN	422	NFC CLK Output
USB_OVP_DRV	118	USB Overvoltage output enable
AOSS_SLEEP_INDICATOR	488	AOSS Sleep indication
PM8550_PWM_OUT_GPIO11	438	PWM（This pin shares one PWM circuit with BLUE. If BLUE light function is used, it is not recommended to use this pin for PWM function again）
PM8010_2_RESET_N	306	PM8010 Reset pin（This module does not support external PM8010 and it is not recommended to use this pin）
PM8010_1_RESET_N	366	PM8010 Reset pin（This module does not support external PM8010 and it is not recommended to use this pin）
USB_CC_OUT	21	USB_CC control pin，connect with GPIO_11
ANT0	268	WCN7851 antenna
ANT1	280	WCN7851 antenna
VBATT_PACK_SNS_M	441	Battery negative pole detection pin, directly connected to the battery negative pole
VBATT_CONN_VSENSE_M	440	Battery negative voltage detection

VBATT_CONN_VSENSE_P	439	Battery positive voltage detection
BATT_ID	33	Battery ID detection
BATT_THERM	30	Battery temperature detection
OVP_SNS	109	USB overvoltage detection
AMUX_2/SYS_THERM2_ADC	419	ADC
SYS_THERM4	420	ADC
AMUX_4/SYS_THERM3_ADC	322	ADC
AMUX_5/TOF_THERM	294	ADC
SYS_THERM5	338	USB_THERM
SYS_THERM7	295	ADC
SPMI_CLK	110	SPMI signal
SPMI_DATA	112	
PWM1	18	PWM，Shared PWM with RED, if using RED function, it is not recommended to reuse.
HAP_SWR_RX_CLK	67	Audio digital interface used to control linear motors, recommended for WSA_SWR connection with GPIO_175, GPIO_176 combination
HAP_SWR_RX_DATA0	68	
WLS_NEN	264	Wireless charge enable
VSW_HAP_M	424	Vibrator control
VSW_HAP_P	79	
PM8550_GPIO_9	437	PWM4, Independent PWM function pins that can be used to control screen backlight
RGB_RED	476	RGB
RGB_GREEN	477	
RGB_BLUE	478	
FLASH_LED1	201	Flash_LED
FLASH_LED2	202	
FLASH_LED3	200	
FLASH_LED4	204	
PM8550_CBL_PWR_N	321	NC
GND	3,10,11,31,32,34,35,36,55,56,58,59,82,83,84,96,99,102,111,114,148,155,156,157,165,168,176,178,71,193,213,233,236,250,251,262,263,265,266,269,271,272,274,275,277,278,281,282,302,303,304,305,325,326,327,328,329,330,331,332,333,348,352,353,356,361,364,368,369,370,373,374,375,392,405,406,407,408,409,417,418,421,423,427,433,434,435,442,445,446,460,461,470,479,216,217,218,219,490,416	

4. Module Function Description and Circuit Design Scheme

4.1 System power supply and power on/off

1）The internal power supply of the module and the system load are both powered by the output of the VPH.PWR, but it is not recommended to directly supply power to the VPH.PWR from an external power source. It is recommended to use DC-DC to reduce voltage to VBAT, and then convert from VBAT to VPH.PWR. The voltage range is recommended to be 3.6-4.4V, commonly 4V. The reference power supply design is shown in the following figure. At the input and output of the power supply, large capacitor voltage regulation and small capacitor filtering should be added according to the actual situation. At the same time, pay attention to leaving TVS tubes and surge tubes as protective devices, which should be placed before the voltage stabilizing capacitor

2） If the system is powered by the battery and the module comes with a charging IC, it can support a maximum of 20V.

3） Automatic Power on Circuit.

Note: PSM803 has a relatively high startup current, and the maximum recommended sustainable output current is 4.5A according to the reference design. An even larger instantaneous current is needed to ensure the normal startup of the system. If a user developed algorithm is added to the PSM803 module, it may require a larger sustainable output current. Please pay attention to the selected DC-DC, inductor design, and take good heat dissipation measures.

Power on and off: In addition to using an automatic power on solution, PSM803 can also be powered on using buttons or inserting USB_VBUS. The specific design scheme can be referred to in the following text. Shutdown supports button shutdown or software shutdown processes.

4.2 MIPI_CSI

4.2.1 GPIOs configuration suggestion

Function	Normal Mode	GPIO #	说明
CAM_0	CAM_MCLK0	GPIO_100	1. The Camera consists of 8 groups, each with a separate MCLK. The module already has an LC filtering circuit, which does not require added. The universal camera I2C has a total of 4 channels, namely CCI_I2C0,CCI_I2C1,CCI_I2C2,CCI_I2C4，These 4 sets of I2C can be cross reused within 7 camera groups, as long as the address of the camera sensor used is different, and the reset pin of the camera can be configured with any GPIO. However, as an AON camera, CSI4 must use its dedicated I2C and corresponding GPIO, and replacement is not recommended. 2. The module does not reserve the dedicated camera power supply, and customers need to build their own power circuit according to the actual situation.
	CAM0_RESET_N	GPIO_116	
	CCI_I2C0_SDA	GPIO_110	
	CCI_I2C0_SCL	GPIO_111	
CAM_1	CAM_MCLK1	GPIO_101	
	CAM1_RESET_N	GPIO_117	
	CCI_I2C1_SDA	GPIO_112	
	CCI_I2C1_SCL	GPIO_113	
CAM_2	CAM_MCLK2	GPIO_102	
	CAM2_RESET_N	GPIO_118	
	CCI_I2C2_SDA	GPIO_114	
	CCI_I2C2_SCL	GPIO_115	
CAM_3	CAM_MCLK3	GPIO_103	
	CAM3_RESET_N	GPIO_119	
	CCI_I2C4_SDA	GPIO_74	
	CCI_I2C4_SCL	GPIO_75	
CAM_4	CAM_AON_MCLK4	GPIO_104	
	CAM4_RESET_N	GPIO_120	
	AON_CAM_SDA	GPIO_208	

	AON_CAM_SCL	GPIO_209	
	AON_CAM_STANDBY_0	GPIO_206	
	AON_CAM_STANDBY_1	GPIO_207	
CAM_5	CAM_MCLK5	GPIO_105	
	CAM5_RESET_N	GPIO_144	
	CCI_I2C0_SDA	GPIO_110	
	CCI_I2C0_SCL	GPIO_111	
CAM_6	CAM_MCLK6	GPIO_106	
	CAM6_RESET_N	GPIO_161	
	CCI_I2C1_SDA	GPIO_112	
	CCI_I2C1_SCL	GPIO_113	
CAM_7	CAM_MCLK7	GPIO_107	
	CAM7_RESET_N	GPIO_109	
	CCI_I2C2_SDA	GPIO_114	
	CCI_I2C2_SCL	GPIO_115	

4.2.2 Reference Design

1）Customers should reserve common mode inductors on MIPI differential pairs based on their actual usage to prevent interference from common mode signals, and reserve appropriate TVS tubes on key signals such as RESET and I2C to prevent static electricity. When multiple cameras are used simultaneously, it is recommended that each camera's AVDD be used independently. DVDD, IOVDD, and AFVDD can be reused according to the actual situation, but it is necessary to ensure that the selected DC-DC current is sufficient to support the maximum current required for the camera to work simultaneously.

2）MIPI_CSI Layout design requirement

C-PHY：Single ended impedance of 45 Ω or 50 Ω; The isometric error of the intra group wiring should be within 0.7mm, and the isometric error between groups should be within 4.2mm; The wiring width within the group should be 1.5 times the line width spacing, and the wiring width between groups should be more than 1.5 times the line width; The distance between mipi and other signal lines should be at least 3 times the line width.

D-PHY: Differential impedance of 80 or 100 Ω; Within the group, the equal length error of the wiring is within 0.7mm, and between groups, the equal length error is within 1.4mm; The spacing between differential pairs is one time the line width, and the spacing between differential pairs is one or 1.5 times the line width. MIPI should maintain a line width of 2.5 times or more between other signals.

4.3 MIIPI_DSI

4.3.1 Recommended GPIO configuration

LCD	MDP_VSYNC_P	GPIO_86	synchronization signal
	DISP0_RESET_N	GPIO_133	Screen reset
	LCD_ID	GPIO_19	ID

	TS_RESET_N	GPIO_24	TP reset
	TS_INT_N	GPIO_25	TP interrupt
	TS_I2C_SDA	GPIO_44	TP I2C
	TS_I2C_SCL	GPIO_45	
	PM8550_PWM_OUT_GPIO09	PM8550_PWM_OUT_GPIO09	Backlight PWM control
	APPS_I2C_SCL	GPIO_21	I2C for Screen bias drive IC （AW37501CSR)
	APPS_I2C_SDA	GPIO_20	
	DISPLAY_BIAS_DRIVER_EN_1	GPIO_163	AVEE enable
	DISPLAY_BIAS_DRIVER_EN	GPIO_137	AVDD enable

4.3.2 Reference Design

The backlight voltage and bias of the LCD screen require an external circuit design. PWM control of the backlight is enabled in the backlight circuit by PM8550_GPIO.09. This GPIO function is not recommended for other functions, nor is it recommended to use other PWM (RGB light) as the backlight control pin, as this may cause conflicts between the RGB light state and the backlight.

OLED Screen：

The core power supply of DSI has been provided by the module internally, with VREG-L12 and VREG-L13 remaining externally for power supply. However, the power module of PM8350B has not been provided, and this part requires the customer to build their own peripheral circuit design.

MIPI_DSI LAYOUT design requirement：

C-PHY: Single ended impedance of 45 Ω or 50 Ω; The isometric error of the intra group wiring should be within 0.7mm, and the isometric error between groups should be within 4.2mm; The wiring width within the group should be 1.5 times the line width spacing, and the wiring width between groups should be more than 1.5 times the line width; The distance between mipi and other signal lines should be at least three times the line width.

D-PHY: Differential impedance of 80 or 100 Ω; Within the group, the equal length error of the wiring is within 0.7mm, and between groups, the equal length error is within 1.4mm; The spacing between differential pairs is one time the line width, and the spacing between differential pairs is one or 1.5 times the line width. MIPI should maintain a line width of at least twice that of other signals.

4.4 Audio design scheme

4.4.1 External WCD9385 codec design

Audio design description：

1）Audio input

WCD9385 has 7 group of AMIC inputs， AMIC1~AMIC5 do not have built-in MIC-BIAS and require external MIC-BIAS driver, supporting HDR design; AMIC6 and AMIC7 are equipped with built-in MIC-BIAS, capacitive coupling input supported.

Analog audio input supports three operating modes：

- Hi-Fi mode

Programmable gain range: -9dB~24dB, step size 1.5dB; Input reference noise 3.2uVrms, signal-to-noise ratio 109dB at 0dB gain.

- Standard mode

Programmable gain range：-9dB~30dB, step size 1.5dB; input reference noise 6.4uVrms, signal-to-noise ratio 104dB at 0dB gain.

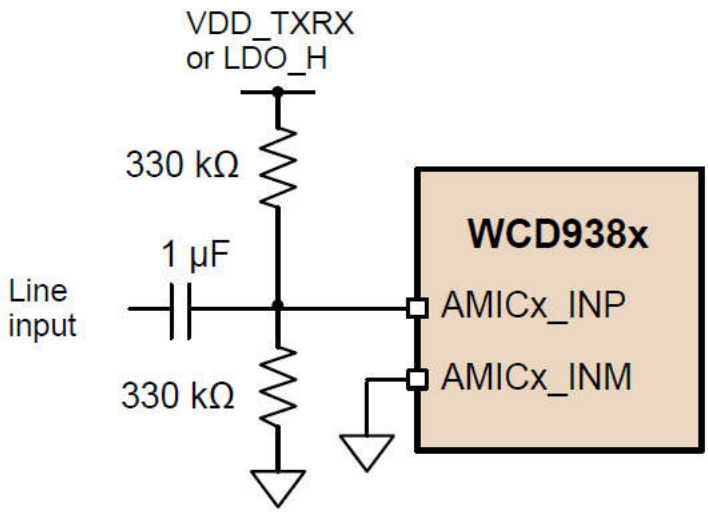
- Low power mode

Programmable gain range：0dB~30dB, step size 1.5dB; input reference noise 10uVrms, signal-to-noise ratio 100dB at 0dB gain。

Corner frequency under different gains：

Gain(dB)	0~4.5	6~10.5	12~16.5	18~22.5	24~28.5	30
Fc(Hz)	0.37	0.55	0.91	1.63	3.1	6

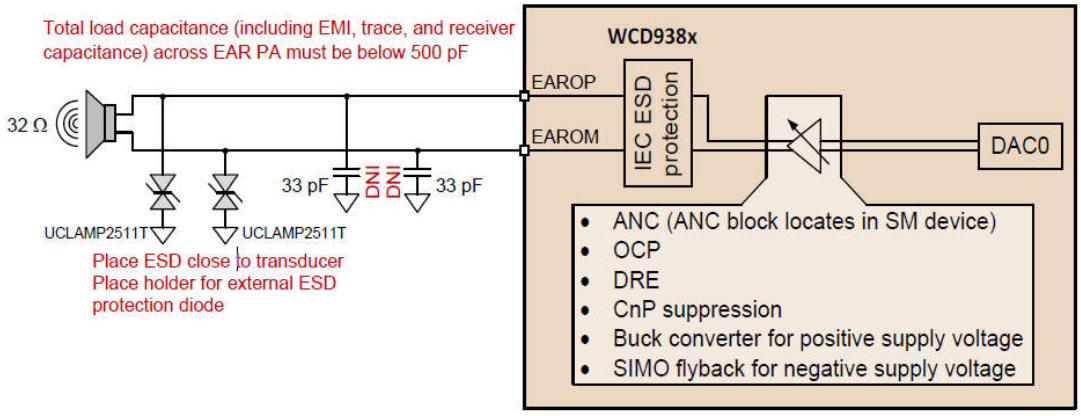
Line in input



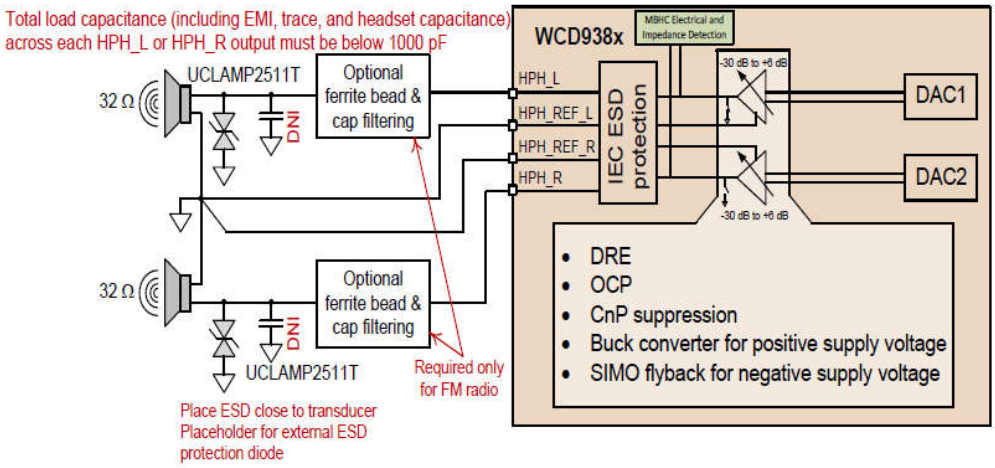
For Line in input design, AMIC6 and AMIC7 do not require external bias and come with built-in bias voltage. When using LDOH as an external bias, the maximum signal allowed by its power supply can reach 3V.

2）Audio output

- Receiver output design：

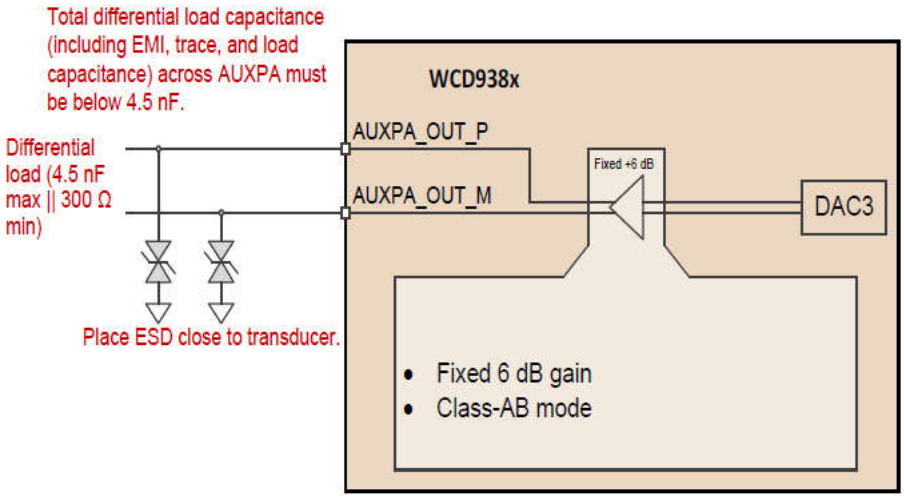


- Earphone output design



AUX differential assisted PA design (can be used as a tactile sensor)

Note: If AUX PA and HPH are used simultaneously, both channels need to use the same sampling rate, 44.1KH or 48KHz.



4.4.2 DMIC design scheme

The PSM803 module comes with 4 DMIC audio input channels, and can be equipped with up to 8 digital MICs externally, suitable for design schemes such as MIC arrays.

It is recommended that customers use a separate LDO for the 1.8V power supply of MIC, or use the built-in 1.8V power supply VREG-L10B_1P8 of PSM803.

4.4.3 PSM803 Audio Interface

Chip GPIO	Description	Primary function	Alt function 0	Alt function 1
GPIO_165	Codec (SoundWire, Tx)	SWR_TX_CLK	LPI_I2S0_SCK	
GPIO_166		SWR_TX_DATA0	LPI_I2S0_WS	
GPIO_167		SWR_TX_DATA1	LPI_I2S0_DATA0	
GPIO_179		SWR_TX_DATA2		EXT_MCLK1_D
GPIO_168	Codec (SoundWire, Rx)	SWR_RX_CLK	LPI_I2S0_DATA1	
GPIO_169		SWR_RX_DATA0	LPI_I2S0_DATA2	
GPIO_170		SWR_RX_DATA1	LPI_I2S0_DATA3	EXT_MCLK1_C
GPIO_171	Digital MICs	LPI_DMIC1_CLK	LPI_I2S1_CLK	
GPIO_172		LPI_DMIC1_DATA	LPI_I2S1_WS	
GPIO_173		LPI_DMIC2_CLK	LPI_I2S1_DATA0	
GPIO_174		LPI_DMIC2_DATA	LPI_I2S1_DATA1	EXT_MCLK1_B
GPIO_175	WSA (SoundWire)	WSA_SWR_CLK	LPI_I2S2_CLK	
GPIO_176		WSA_SWR_DATA	LPI_I2S2_WS	
GPIO_180	WSA2 (SoundWire)	WSA2_SWR_CLK	LPI_I2S2_DATA0	
GPIO_181		WSA2_SWR_DATA	LPI_I2S2_DATA1	
GPIO_177	Digital MICs	LPI_DMIC3_CLK	LPI_I2S3_CLK	
GPIO_178		LPI_DMIC3_DATA	LPI_I2S3_WS	EXT_MCLK1_A
GPIO_182		LPI_DMIC4_CLK	LPI_I2S3_DATA0	
GPIO_183		LPI_DMIC4_DATA	LPI_I2S3_DATA1	
GPIO_184	SLIMbus	SLIMBUS_CLK	LPI_I2S4_CLK	
GPIO_185		SLIMBUS_DATA	LPI_I2S4_WS	
GPIO_186			LPI_I2S4_DATA0	
GPIO_187			LPI_I2S4_DATA1	EXT_MCLK1_E

Chip GPIO	Description	Primary function [2]	Alt function 0
GPIO_121	I2S1	I2S1_SCK	
GPIO_122		I2S1_DATA0	
GPIO_123		I2S1_WS	
GPIO_124		I2S1_DATA1	AUDIO_EXT_MCLK1 AUDIO_REF_CLK [1]
GPIO_125	I2S0	AUDIO_EXT_MCLK0	
GPIO_126		I2S0_SCK	
GPIO_127		I2S0_DATA0	
GPIO_128		I2S0_DATA1	
GPIO_129		I2S0_WS	

Note: GPIO_124 is a bidirectional MCLK. It can provide an MCLK for external I2S devices or receive an external clock from external devices.

4.5 USB design

PSM803 Only one set of USB3.1 and one set of USB2.0 are supported for full functionality design.

1) It is recommended to use the above design to input the MOS transistor detected by the OVP sensor into the USBVBUS pin of PSM803, which is the USBVBUS-FET of the module.

2) Module GPIO_11 should be short circuited at CC-OUT as part of the default CC detection and is not

recommended to be changed.
3) If DP function is required to be supported, the AUX switch needs to be externally built.

USB3.1 Requirements for Layout：
Differential impedance 85+/-15 Ω; The difference in the length of the differential wiring within the group is within 0.7mm, the difference in the wiring between groups is within 10mm, and the error in the differential wiring between DP-AUX-P and DP-AUX-M is within 7mm. The spacing between TX and RX needs to be at least 4 times the line width for 10Gbps, and at least 3 times the line width for 5Gbps. Maintain a line spacing of at least 4 times the line width between the USB-SS and other signals. Reserve a capacitance range of 75~265nf on TX; The reserved capacitance range on RX is 297-363nf.

USB2.0 Requirements for Layout：
Differential impedance of 90+/-20 Ω, with an equal length error of 0.7mm or less for the internal routing of the differential line. The differential line maintains a line width of more than 3 times that of other routing lines.

4.6 PCIE design

The PSM803 module reserves a PCIE4.0 extension interface, which can be used to plug M.2, PCIE extension USB port, or other PCIE supported devices. The specific GPIO configuration can refer to the above GPIO configuration table. The maximum speed of PCIE4.0 can reach 16Gbps, and it is recommended that the total length of external wiring should not exceed 180mm.

1) The TX terminal capacitor module of PCIE1 is already internally connected with 220NF, so there is no need to add it again. Only a 220NF capacitor needs to be externally connected to the RX of the external device.
2) The impedance of the wiring should be controlled between 72.5~97.5 Ω, and the difference in length of the internal wiring should not exceed 0.7mm. The distance between TX and RX, as well as between PCIE and other wiring, should be maintained within a range of 4 times the line width.

4.7 T-flash card design

PSM803 Supports a set of expandable T-flash cards, with a maximum capacity of 1TB of expandable storage.

When routing the PCB, attention should be paid to the impedance requirement between the clock and signal lines, which should be between 36~50 Ω. The CLK module reserves 22 Ω for impedance matching at the internal output end, and no additional resistance is required for peripheral design. When the CLK clock frequency is 50MHz or 100MHz, it is recommended that the maximum total length of its peripheral clock and data line should not exceed 125mm; The maximum length difference between CLK and data lines is within 6mm; For the requirement of a clock frequency of 208MHz, the maximum total length of the clock and data line should not exceed 25mm. The maximum length difference between CLK and data lines is within 2mm. Keep the distance between lines at 1.5 times the line width or more.

4.8 Battery design

In addition to being compatible with DC-IN input for power on, the PSM803 module can also adopt a battery

input design scheme, supporting battery charging design. The VBAT pin on the battery connector should be reserved with TVS devices to prevent damage to the system from EOS and ESD events.

The reserved design scheme for BAT-ID and BAT-THERM is shown in the above figure. If there are corresponding NTC and ID resistors inside the battery, they can be omitted. Suggest the resistance value to be consistent with the reference design.

PSM803 charging performance parameters:

1) The maximum input voltage for USB/wireless charging is 20V;
2) Maximum input current USB 5A; Wireless input 3A
3) Maximum charging current 6A
4) OVP voltage (select the corresponding configuration according to the maximum input voltage required, with a software programmable range of 6.6~23.5V) (This option directly affects the protection voltage of the external OVP chip, please note)
5) Trickle current requirement: Battery voltage below 2.0-2.2V (default 2.1V), current 50mA;
Pre charging requirements: 2.1V~Vsys_min (default 3.0V, adjustable to 3.4V), current 600mA (maximum)
Constant current requirement: MAX 6A
Constant voltage requirement: cut-off current 200mA (adjustable from 50 to 750mA)
Recharge voltage: 3.6-4.8V programmable, SOC 0%~100% programmable
6) Support charging protocol: BC1.2; PD3.0; Hardware QC2.03.0; Software programmable QC4.0; QC5.0.

OTG output capability:

The USB channel supports a maximum output of 5V 3A; Wireless supports up to 12V 1A output.
Additionally, PSM803 can use Haptics boost to boost voltage and output 10V 1A or 5V 2A from USB. But its output cannot be used simultaneously with the OTG function.

4.9 RGB and FLASH Reference Design

PSM803 supports three RGB designs and four FLASH designs.

Both RGB and flash need to reserve TVS for ESD protection. At the same time, it should also be noted that the FLASH current is very high, and the wiring requirements should follow the reference design, with each FLASH being above 800mA.

4.10 ADC performance parameter

Description	Min	Typical	Max	Unit
Input voltage range	0		1.875	V
analog input bandwidth	-	500	-	KHz
sampling frequency	-	4.8	-	MHz

4.11 PSM803 Scalable GPIO Function List

4.11.1 GPIO configuration table supporting UART, I2C, SPI interfaces

	L0	L1	L2	L3	L4	L5	L6
QUP1_SE0	GPIO_28	GPIO_29	GPIO_30	GPIO_31	–	–	–
QUP1_SE1	GPIO_32	GPIO_33	GPIO_34	GPIO_35	–	–	–
QUP1_SE2	GPIO_36	GPIO_37	GPIO_38	GPIO_39	GPIO_40	GPIO_41	GPIO_42
QUP1_SE3	GPIO_40	GPIO_41	GPIO_42	GPIO_43	–	–	–
QUP1_SE4	GPIO_44	GPIO_45	GPIO_46	GPIO_47	–	–	–
QUP1_SE6	GPIO_48	GPIO_49	GPIO_50	GPIO_51	–	–	–
QUP1_SE7	GPIO_24	GPIO_25	GPIO_26	GPIO_27	–	–	–
QUP2_SE0	GPIO_0 GPIO_56	GPIO_1 GPIO_57	/ GPIO_58	/ GPIO_59	GPIO_63	GPIO_66	GPIO_67
QUP2_SE1	GPIO_60	GPIO_61	GPIO_62	GPIO_63	–	–	–
QUP2_SE2	GPIO_64	GPIO_65	GPIO_66	GPIO_67	–	–	–
QUP2_SE3	GPIO_68	GPIO_69	GPIO_70	GPIO_71	–	–	–
QUP2_SE4	GPIO_2	GPIO_3	/	/	–	–	–
QUP2_SE7	/	/	GPIO_74	GPIO_75	–	–	–

Note：

	L0	L1	L2	L3	L4	L5	L6
(HS)-UART	CTS	RFR	TX	RX	–	–	–
I2C/I3C	SDA	SCL	–	–	–	–	–
SPI	MISO	MOSI	SCLK	CS_0	CS_1	CS_2	CS_3

4.11.2 SENSOR dedicated interface

SSC_QUP_SE0	GPIO_188	SSC_0		SDA		Accelerometer/Gyroscope (DAE)
	GPIO_189	SSC_1		SCL		
SSC_QUP_SE1	GPIO_190	SSC_2	SDA			Magnetometer
	GPIO_191	SSC_3	SCL			ALS/Proximity
	GPIO_204	SSC_16				
	GPIO_205	SSC_17				
SSC_QUP_SE2	GPIO_192	SSC_4			MISO	Not used
	GPIO_193	SSC_5			MOSI	
	GPIO_194	SSC_6			SCLK	

	GPIO_195	SSC_7			CS_0	
	GPIO_196	SSC_8				
SSC_QUP_SE3	GPIO_196	SSC_8	SDA			Pressure SAR
	GPIO_197	SSC_9	SCL			Humidity

4.12 RF reference design

The module provides WiFi/BT antenna pins WIFI-ANT0 and WIFI-ANT1. The antenna on the user's motherboard should be connected to the module's antenna pins using a microstrip line or strip line with a characteristic impedance of 50 ohms.

For the convenience of antenna debugging and certification testing, an RF connector and antenna matching network should be added.

In the above figure, R9404, L9404, and L9436 are antenna matching components, and the specific component values can be determined after the antenna is debugged by the antenna factory. Among them, R9404 defaults to pasting 0R, while L9404 and L9436 default to not pasting.

5. Module parameters

5.1 Module power voltage

Parameter	Min	Typical	Max	Unit
VBAT	3.5	4.0	4.35	V
VBUS	3.7	-	21.5	V
Power off voltage		3.4		V

5.2 Digital interface characteristics

Parameter	Description	Min	Typical	Max	Unit
V_{IH}	Input high-level voltage	1.17	-	2.1	V
V_{IL}	Input low-level voltage	-0.3	-	0.63	V
V_{OH}	Ouput high-level voltage	1.35	-	1.8	V
V_{OL}	Ouput low-level voltage	0	-	0.45	V

Note：All of PSM803 GPIOs voltage are 1.8V.

5.3 WIFI RF performance

The following table lists the main RF performance under WIFI conduction.

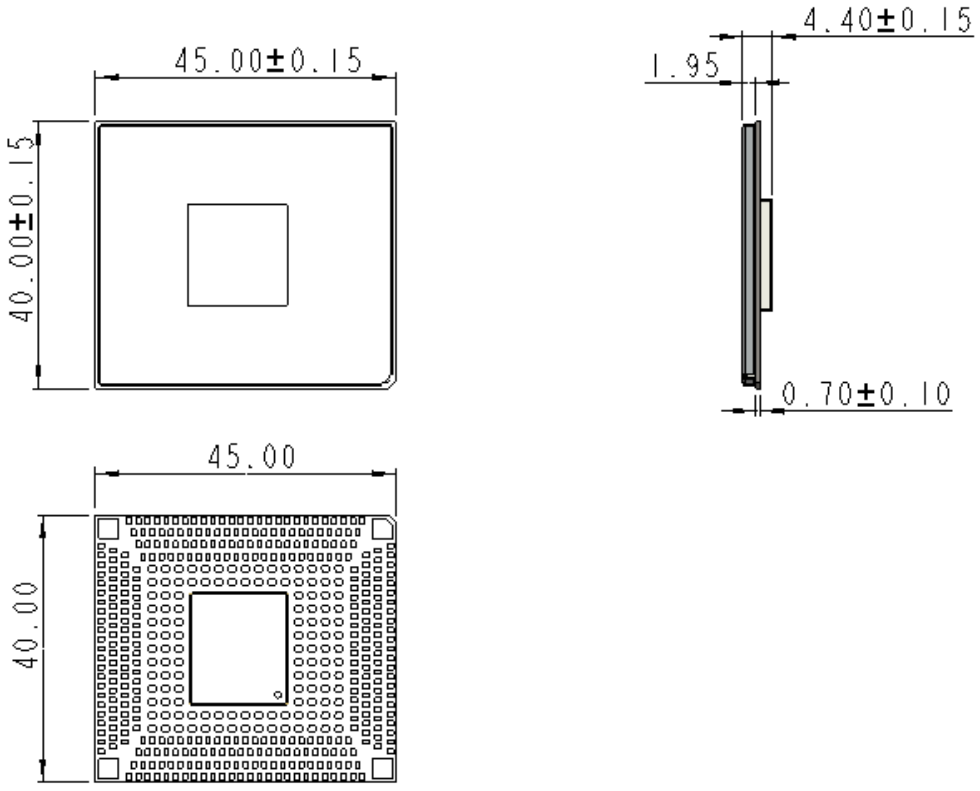
Emission performance									
	2.4G				5-7G				
	802.11B	802.11G	802.11N	802.11AX/BE	802.11A	802.11N	802.11AC	802.11AX/BE	
Emission power (Minimum rate)	18	16	15.5	14	15.5	14.5	13.5	12	dBm
Emission power (Maximum rate)	17	15	14	12	14	13	12	10	dBm
Receiving performance									
	2.4G				5-7G				
Receiving sensitivity	802.11B	802.11G	802.11N	802.11AX/BE	802.11A	802.11N	802.11AC	802.11AX/BE	
Minimum rate	-93	-90	-89	-87	-89	-88	-86	-85	dBm
Maximum rate	-86	-72	-69	-58	-70	-68	-64	-57	dBm

5.4 BT RF performance

The following table lists the main RF performance under BT conduction.

Emission performance				
Emission power	BR	EDR	BLE	
	10	10	10	dBm
Receiving performance				
Receiving sensitivity	BR	EDR	BLE	
	-94	-85	-93	dBm

6.0 Module packaging size


45.00±0.15
40.00±0.15
4.40±0.15
1.95
0.70±0.10
45.00
40.00