FN990 Family

HW Design Guide

1VV0301752 Rev. 3 – 2022-10-07

Telit Technical Documentation

APPLICABILITY TABLE

PRODUCTS	Description
FN990A28	3G / 4G (16 Layer) / Sub-6 (BW : 120MHz) cellular module
FN990A40	3G / 4G (20 Layer) / Sub-6 (BW : 200MHz) cellular module

CONTENTS

1. INTRODUCTION

1.1. Scope

This document introduces the Telit FN990 Family module and presents possible and recommended hardware solutions for the development of a product based on this module. All the features and solutions described in this document are applicable to all FN990 Family variants listed in the applicability table.

This document cannot include every hardware solution or every product that can be designed. Where the suggested hardware configurations are not to be considered mandatory, the information provided should be used as a guide and starting point for the proper development of the product with the Telit FN990 Family module.

1.2. Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using the Telit FN990 Family module.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report of documentation errors contact Telit Technical Support at:

- *TS-EMEA@telit.com*
- *TS-AMERICAS@telit.com*
- *TS-APAC@telit.com*
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Alternatively, use:

https://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

https://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates the user feedback on our information.

1.4. Symbol Conventions

	**Danger:** This information MUST be followed or catastrophic equipment failure or personal injury may occur.
	**Warning:** Alerts the user on important steps about the module integration.
	**Note/Tip:** Provides advice and suggestions that may be useful when integrating the module.
	**Electro-static Discharge:** Notifies the user to take proper grounding precautions before handling the product.

Table 1: Symbol Conventions

All dates are in ISO 8601 format, that is YYYY-MM-DD.

1.5. Related Documents

- FN990 SW User Guide, 1VV0301750
- FN990 AT Commands Reference Guide, 80691ST11097A
- Generic EVB HW User Guide, 1VV0301249
- Telit EVB 2.0 HW User Guide, 1VV0301732
- FN990 TLB HW User Guide, 1VV0301753
- FN990 Thermal Design Guide, 1VV0301804
- FN990 CA / EN-DC list, 30691NT12001A

2. GENERAL PRODUCT DESCRIPTION

2.1. Overview

The aim of this document is to present the possible and recommended hardware solutions useful for developing a product with the Telit FN990 Family M.2 module.

FN990 Family is Telit's platform for the M.2 module for applications, such as M2M applications and industrial IoT device platforms, based on the following technologies:

- 5G sub-6 / 4G / 3G networks for data communication
- Designed for industrial grade quality

Front-end for mobile products, offering mobile communication features to an external host CPU through its rich interfaces.

FN990 Family is available in hardware variants as listed in the APPLICABILITY TABLE.

The designated RF band set for each variant are detailed in Section 2.2. Frequency Bands and CA / EN-DC Combinations.

2.2. Frequency Bands and CA / EN-DC Combinations

2.2.1. Frequency Bands

Operating frequencies in 5G, LTE and WCDMA modes conform to 3GPP specifications.

The table below lists the FN990 operating frequencies on 5G, LTE and WCDMA mode.

5G NR Sub-6 Bands Supportive

NR BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels	SCS (kHz)
n1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 384000 - 396000 Rx: 422000 - 434000	15
n2 - 1900 PCS	FDD	1850 - 1910	1930 - 1990	Tx: 370000 - 382000 Rx: 386000 - 398000	15
n3 - 1800	FDD	1710 - 1785	1805 - 1880	Tx: 342000 - 357000 Rx: 361000 - 376000	15
n5 - 850	FDD	824 - 849	869 - 894	Tx: 164800 - 169800 Rx: 173800 - 178800	15
n7 - 2600	FDD	2500 - 2570	2620 - 2690	Tx: 500000 - 514000 Rx: 524000 - 538000	15
n8 - 900	FDD	880 - 915	925 - 960	Tx: 176000 - 183000 Rx: 185000 - 192000	15
n20 - 800	FDD	832 - 862	791 - 821	Tx: 166400 - 172400 Rx: 158200 - 164200	15
n25 -1900+	FDD	1850 - 1915	1930 - 1995	Tx: 370000 - 383000 Rx: 386000 - 399000	15

NR BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels	SCS (kHz)
n28 - 700 APT	FDD	703 - 748	758 - 803	Tx: 140600 - 149600 Rx: 151600 - 160600	15
n30 - WCS	FDD	2305 - 2315	2350 - 2360	Tx: 461000 - 463000 Rx: 470000 - 472000	15
n38 - 2600	TDD	2570 - 2620		T/Rx: 514000 - 524000	30
n40 - 2300	TDD	2300 - 2400		T/Rx: 460000 - 480000	30
n41 - 2600+	TDD	2496 - 2690		T/Rx: 499200 - 537996	30
n48 - 3600	TDD	3550 - 3700		T/Rx: 636668 - 646666	30
n66 - AWS-3	FDD	1710 - 1780	2110 - 2200	Tx: 342000 - 356000 Rx: 422000 - 440000	15
n71 - 600	FDD	663 - 698	617 - 652	Tx: 132600 - 139600 Rx: 123400 - 130400	15
n75 – DL 1500+	SDL	-	1432 – 1517	Rx: 286400 - 303400	30
n77 - 3700	TDD	3300 - 4200		T/Rx: 620000 - 680000	30
n78 - 3500	TDD	3300 - 3800		T/Rx: 620000 - 653332	30
n79 - 4700	TDD	4400 - 5000		T/Rx: 693334 - 733332	30

Table 2: 5G NR Sub-6 Bands supportive

LTE Bands supportive

E-UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 18000 - 18599 Rx: 0 - 599
B2 - 1900 PCS	FDD	1850 - 1910	1930 - 1990	Tx: 18600 - 19199 Rx: 600 - 1199
B3 - 1800+	FDD	1710 - 1785	1805 - 1880	Tx: 19200 - 19949 Rx: 1200 - 1949
B4 - AWS-1	FDD	1710 - 1755	2110 - 2155	Tx: 19950 - 20399 Rx: 1950 - 2399
B5 - 850	FDD	824 - 849	869 - 894	Tx: 20400 - 20649 Rx: 2400 - 2649
B7 - 2600	FDD	2500 - 2570	2620 - 2690	Tx: 20750 - 21449 Rx: 2750 - 3449
B8 - 900 GSM	FDD	880 - 915	925 - 960	Tx: 21450 - 21799 Rx: 3450 - 3799
B12 - 700 a	FDD	699 - 716	729 - 746	Tx : 23010 - 23179 Rx : 5010 - 5179
B13 - 700 c	FDD	777 - 787	746 - 756	Tx : 23180 - 23279 Rx : 5180 - 5279
B14 - 700 PS	FDD	788 - 798	758 - 768	Tx : 23280 - 23379 Rx : 5280 - 5379
B17 - 700 b	FDD	704 - 716	734 - 746	Tx: 23730 - 23849 Rx: 5730 - 5849
B18 - 800 Lower	FDD	815 - 830	860 - 875	Tx: 23850 - 23999 Rx: 5850 - 5999

E-UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B19 - 800 Upper	FDD	830 - 845	875 - 890	Tx: 24000 - 24149 Rx: 6000 - 6149
B20 - 800 DD	FDD	832 - 862	791 - 821	Tx: 24150 - 24449 Rx: 6150 - 6449
B25 - 1900+	FDD	1850 - 1915	1930 - 1995	Tx: 26040 - 26689 Rx: 8040 - 8689
B26 - 850+	FDD	814 - 849	859 - 894	Tx: 26690 – 27039 Rx: 8690 - 9039
B28 - 700 APT	FDD	703 - 748	758 - 803	Tx: 27210 - 27659 Rx: 9210 - 9659
B29 - 700 d	FDD	N/A	717 - 728	Rx: 9660 - 9769
B30 - 2300 WCS	FDD	2305 - 2315	2350 - 2360	Tx: 27660 - 27759 Rx: 9770 - 9869
B32 - 1500 L	FDD	N/A	1452 - 1496	Rx: 9920 - 10359
B34 - 2000	TDD	2010 – 2025		T/Rx: 36200 - 36349
B38 - 2600	TDD	2570 - 2620		T/Rx: 37750 - 38249
B39 - 1900+	TDD	1880 - 1920		T/Rx: 38250 - 38649
B40 - 2300	TDD	2300 - 2400		T/Rx: 38650 - 39649
B41 - 2600+	TDD	2496 - 2690		T/Rx: 39650 - 41589
B42 - 3500	TDD	3400 - 3600		T/Rx: 41590 - 43589
B43 - 3700	TDD	3600 – 3800		T/Rx: 43590 – 45589
B46 - 5200	TDD	5150 – 5925 (DL only)		Rx: 46790 - 54539
B48 - 3600	TDD	3550 - 3700		T/Rx: 55240 - 56739
B66 - AWS-3	FDD	1710 - 1780	2110 - 2200	Tx: 131972 - 132671 Rx: 66436 - 67335
B71 - 600	FDD	663 - 698	617 - 652	Tx: 133122 - 133471 Rx: 68586 - 68935

Table 3: LTE Bands supportive

WCDMA Bands supportive

UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B1 - 2100	FDD	1920 - 1980	2110 - 2170	Tx: 9612 - 9888 Rx: 10562 - 10838
B2 - 1900 PCS	FDD	1850 - 1910	1930 - 1990	Tx: 9262 - 9538 Rx: 9662 - 9938
B4 - AWS-1	FDD	1710 - 1755	2110 - 2155	Tx: 1312 - 1513 Rx: 1537 - 1738
B5 - 850	FDD	824 - 849	869 - 894	Tx: 4132 - 4233 Rx: 4357 - 4458
B6 - 850 Japan	FDD	830 - 840	875 - 885	Tx: 4162 - 4188 Rx: 4387 - 4413

UTRA BAND	Duplex Mode	Uplink Frequency (MHz)	Downlink Frequency (MHz)	Channels
B8 - 900 GSM	FDD	880 - 915	925 - 960	Tx: 2712 - 2863 Rx: 2937 - 3088
B19 - 800 Japan	FDD	830 - 845	875 - 890	Tx: 312 - 363 Rx: 712 - 763

Table 4: WCDMA Bands supportive

2.2.2. CA / MIMO / EN-DC

The FN990 Family supports 2CA, 3CA, 4CA, 5CA, 6CA and 7CA for LTE CA combinations and EN-DC for NR FR1 configuration.

Note: Refer to the FN990 Family CA / EN-DC list, 30691NT12001A for detailed combinations of CA and EN-DC.

2.3. Target Market

The FN990 Family can be used for telematics applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are required, for example:

- Industrial equipment
- Home network
- Internet connectivity

2.4. Main Features

The FN990 Family of industrial grade cellular modules features 5G Sub-6, LTE and multi-RAT module together with an on-chip powerful application processor and a rich set of interfaces.

Main functions and features are listed below:

Function	Features
Physical	M.2 Type 3052-S3-B
Cellular technology	• FN990A28 5G: FR1(Sub 6G), Rel 16 4G: CAT. 19 (1.6Gbps) on DL, CAT. 18 (211Mbps) on UL, Rel 16 3G: HSPA+ Rel9 up to 42/5.7Mbps in DL/UL • FN990A40 5G: FR1(Sub 6G), Rel 16 4G: CAT. 20 (2Gbps) on DL, CAT. 18 (211Mbps) on UL, Rel 16 3G: HSPA+ Rel9 up to 42/5.7Mbps in DL/UL
4x4 MIMO	5G: n1/n2/n3/n7/n25/n30/n38/n40/n41/n48/n66/n75/n77/n78/n79 4G: B1/B2/B3/B4/B7/B25/B30/B32/B34/B38/B39/B40/B41/B42/B43/B48/B66
Diversity/2nd Rx	4G: all operating bands 3G: all operating bands
GNSS	Upper L-band: GPS/Glonass/Beidou/Galileo
USIM port – Dual Voltage	Two SIM support (UIM2 can be assigned as optional eSIM) Class B and Class C support
Application processor	Application processor to run customer application code 32 bit ARM s-A7 up to 1.8 GHz running the Linux operating system 4Gbit NAND Flash + 4Gbit LPDDR4 2133 MHz MCP is supported
Main Interfaces	PCIe Gen3 x 1-lane USB 3.1 Gen 2 Peripheral Ports – GPIOs
Antenna connection	4 x MHF-4 type Cellular/GNSS antenna connectors 1 x MHF-4 type Dedicated GNSS antenna connector
From factor	M.2 Form factor (30 * 52 * 2.25 mm), accommodating the multiple RF bands
Environment and quality requirements	The device is designed and qualified by Telit to satisfy environmental and quality requirements.
Single supply module	The module internally generates all its required internal supply voltages.

Function	Features
RTC	Real time clock is supported.
Operating temperature	Range -40 degC to +85 degC (conditions as defined in Section 2.8.1, Temperature Range)

Table 5: Main Features

2.4.1. Configurations Pins

Telit M.2 module indicates the main serial interface applicable on the combination of 4 configuration pins. FN990 Family is configured as an USB 3.1 Gen 2.

Pin	Signal	State	Interface Type
21	CONFIG_0	GND	USB 3.1 Gen 2 Port Configuration 2 (Applicable to WWAN only)
69	CONFIG_1	GND	
75	CONFIG_2	NC	
1	CONFIG_3	NC	

Table 6: Configurations Pins

Note: On the platform side, each of the CONFIG_0 to CONFIG_3 signals must be equipped with a pull-up resistor. Based on the state of the configuration pins on the Add-in Card, being tied to GND or left No Connect (NC), the detected pins will create 4-bit logic state that required decoding.

For more details, please refer to the PCI Express M.2 Specification document.

2.5. Block Diagram

The figure below shows an overview of the internal architecture of the FN990 Family module.

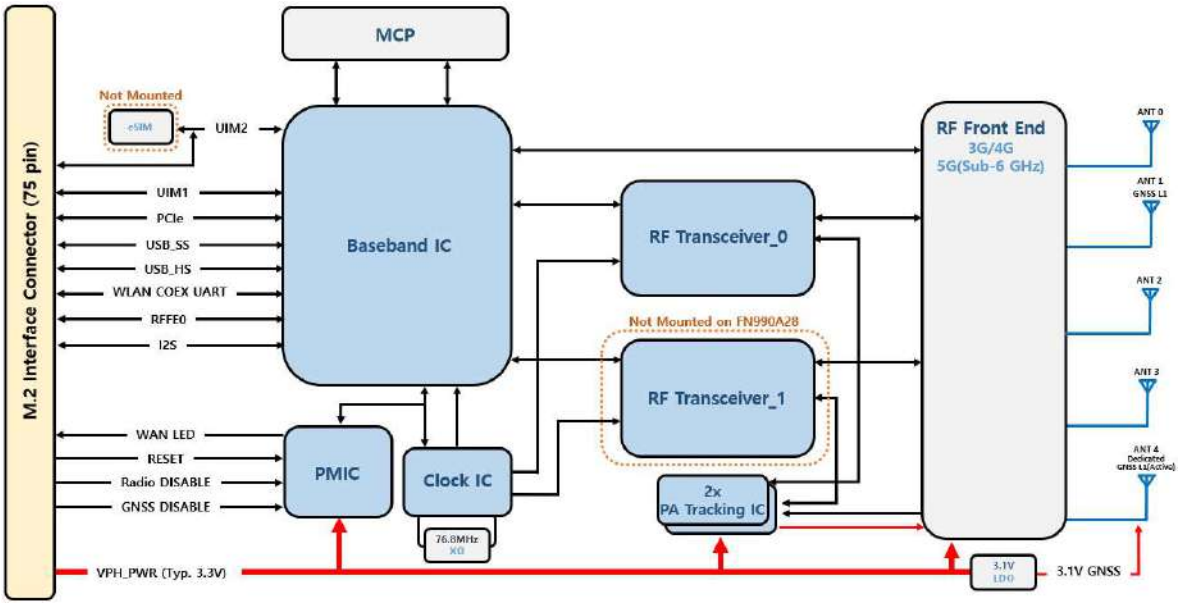

Figure 1: FN990 Family Block Diagram

2.6. RF Performance

The RF performance in 5G, LTE and WCDMA modes conforms to the 3GPP specifications.

2.6.1. Conducted Transmit Output Power

TX power follows the measurement conditions and specifications defined in 3GPP.

Band	Power class	RF Power (dBm)
5G NR Sub-6 n1, n2, n3, n5, n7, n8, n20, n25, n28, n30, n38, n40, n41, n48, n66, n71, n77, n78, n79	3 (0.2W)	23 (+2dB / -2dB)
5G NR Sub-6 n41, n77, n78, n79 Supports Power Class 2	2 (0.4W)	26 (+2dB / -2dB)
LTE All Bands B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B30, B34, B38, B39, B40, B41, B42, B43, B48, B66, B71	3 (0.2W)	23 (+2dB / -2dB)
LTE B41 Supports Power Class 2	2 (0.4W)	26 (+2dB / -2dB)

Band	Power class	RF Power (dBm)
3G WCDMA B1, B2, B4, B5, B6, B8, B19	3 (0.2W)	23 (+2dB / -2dB)

Table 7: Conducted Transmit Output Power

2.6.2. Conducted Receiver Sensitivity

The Sensitivity of the receiver follows the measurement conditions and specifications defined in 3GPP.

Technology	3GPP Compliance
5G NR Sub-6	Throughput >95%
4G LTE	Throughput >95%
3G WCDMA	BER <0.1% 12.2 Kbps

Table 8: 3GPP compliance for Conducted Receiver Sensitivity

NR Band	Typical Conducted Rx Sensitivity (dBm) *						
	SCS (kHz)	BW (MHz)	ANT0	ANT1	ANT2	ANT3	Combined
NR FDD n1	15	20	-95	-94	-96	-95	-100
NR FDD n2	15	20	-95	-94	-95	-95	-100
NR FDD n3	15	20	-94	-94	-96	-95	-100
NR FDD n5	15	20	-96	NA	-98	NA	-99
NR FDD n7	15	20	-93	-94	-94	-95	-99
NR FDD n8	15	20	-96	NA	-98	NA	-99
NR FDD n20	15	20	-96	NA	-98	NA	-100
NR FDD n25	15	20	-94	-94	-95	-95	-100
NR FDD n28	15	20	-96	NA	-98	NA	-100
NR FDD n30	15	10	-96	-96	-98	-98	-102
NR TDD n38	30	20	-95	-94	-94	-94	-99
NR TDD n40	30	80	-88	-88	-88	-89	-93
NR TDD n41	30	100	-88	-86	-87	-87	-92
NR TDD n48	30	40	-91	-91	-93	-92	-97
NR FDD n66	15	20	-94	-94	-95	-97	-99

NR Band	Typical Conducted Rx Sensitivity (dBm) *						
NR FDD n71	15	20	-97	NA	-98	NA	-100
NR TDD n75 (DL only)	30	30	-92	-93	-92	-92	-97
NR TDD n77	30	100	-88	-89	-87	-87	-93
NR TDD n78	30	100	-88	-88	-87	-87	-93
NR TDD n79	30	100	-85	-90	-89	-88	-93

Table 9: Typical Conducted Receiver Sensitivity - NR Bands
**3.3 Voltage / Room temperature*

E-UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
	ANT0	ANT1	ANT2	ANT3	Combined
LTE FDD B1	-97	-96.5	-96.5	-96.5	-103
LTE FDD B2	-97	-96	-96	-96	-103
LTE FDD B3	-97	-96	-96	-96	-103
LTE FDD B4	-97	-96	-96	-96	-103
LTE FDD B5	-99	NA	-99	NA	-102
LTE FDD B7	-97	-96	-96	-96	-103
LTE FDD B8	-99	NA	-99	NA	-102
LTE FDD B12	-99	NA	-99	NA	-102
LTE FDD B13	-99	NA	-99	NA	-102
LTE FDD B14	-99	NA	-99	NA	-102
LTE FDD B17	-99	NA	-99	NA	-102
LTE FDD B18	-99	NA	-99	NA	-102
LTE FDD B19	-99	NA	-99	NA	-102
LTE FDD B20	-99	NA	-99	NA	-102
LTE FDD B25	-97	-96	-96	-96	-103
LTE FDD B26	-99	NA	-99	NA	-102
LTE FDD B28	-99	NA	-99	NA	-102
LTE FDD B29 (DL only)	-99	NA	-99	NA	-101
LTE FDD B30	-96	-95	-95	-95	-102

E-UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
LTE FDD B32 (DL only)	-97	-97	-97	-97	-101
LTE TDD B34	-96.5	NA	-98	NA	-100
LTE TDD B38	-97	-96.5	-96.5	-96.5	-103
LTE TDD B39	-97	-97	-97	-97	-103
LTE TDD B40	-96.5	-96.5	-96.5	-96.5	-103
LTE TDD B41	-96	-96	-96	-96	-102
LTE TDD B42	-97	-96	-96	-96	-102
LTE TDD B43	-97	-96	-96	-96	-102
LTE TDD B46 (DL only)	-92	NA	-90	NA	-93
LTE TDD B48	-97	-96	-96	-96	-103
LTE FDD B66	-97	-96	-96	-96	-103
LTE FDD B71	-99	NA	-99	NA	-102

Table 10: Typical Conducted Receiver Sensitivity - LTE Bands
**3.3 Voltage / Room temperature*

UTRA Band	Typical Conducted Rx Sensitivity (dBm) *				
	ANT0	ANT1	ANT2	ANT3	Combined
WCDMA FDD B1	-110	NA	-109	NA	NA
WCDMA FDD B2	-110	NA	-110	NA	NA
WCDMA FDD B4	-110	NA	-109	NA	NA
WCDMA FDD B5	-110	NA	-110	NA	NA
WCDMA FDD B6	-110	NA	-110	NA	NA
WCDMA FDD B8	-110	NA	-110	NA	NA
WCDMA FDD B19	-110	NA	-110	NA	NA

Table 11: Typical Conducted Receiver Sensitivity - WCDMA Bands
**3.3 Voltage / Room temperature*

Note: The sensitivity level has deviation of approximately +/- <2dB, device and channel because the level shows a typical value.

The sensitivity level of the NR bands has a deviation of approximately +/- <3dB depending on the EN-DC combinations, but the combined sensitivity performance meets the 3GPP requirements.

LTE level is measured at BW 10 MHz except Band 46

B46 BW = 20 MHz

2.7. Mechanical Specifications

2.7.1. Dimensions

The overall dimensions of FN990 Family modems are:

- Length: 52 mm
- Width: 30 mm
- Thickness: 2.25 mm

2.7.2. Weight

The nominal weight of the FN990A40 is 8.2 grams.

The nominal weight of the FN990A28 is 8.0 grams.

2.8. Environmental Requirements

2.8.1. Temperature Range

Mode	Temperature	Note
Operating Temperature Range	–20°C ~ +55°C	This range is defined by 3GPP (the global standard for wireless mobile communication). Telit guarantees that its modules comply with all 3GPP requirements and that it has the full functionality of the module in this range.
	–40°C ~ +85°C	Telit guarantees full functionality within this range as well. However, there may possibly be some performance deviations in this extended range related to 3GPP requirements, which means that some RF parameters may deviate

Mode	Temperature	Note
		from the 3GPP specification on the receiver or the maximum output power may be slightly degraded. Even so, all functionalities, such as connection to calls, SMS, USB communication, UART activation and so on, will be maintained, and the effect of such degradations will not lead to malfunctions.
Storage and non-operating Temperature Range	–40°C ~ +85°C	

Table 12: Temperature Range

Warning: The application processor temperature which is in the FN990 Family must be kept below 95 degC for the best performance. Depending on the various application, a heat sink, thermal pad or other cooling system may be required to properly dissipate the heat.

A large solder resist opening area is located on the bottom side of the module. Adding a TIM on that area with a heatsink is one of the best way to dissipate the heat well. The temperature can be read via AT commands. For more details, please refer to SW user guide or thermal design guideline.

2.8.2. RoHS Compliance

As a part of the Telit corporate policy of environmental protection, the FN990 Family products comply with the RoHS (Restriction of Hazardous Substances) directive of the European Union (EU directive 2011/65/EU).

3. PINS ALLOCATION

3.1. Pin-out

Pin	Signal	I/O	Function	Type	Comment
USB Communication Port					
7	USB_HS_DP	I/O	USB 2.0 Data Plus	Analog	
9	USB_HS_DM	I/O	USB 2.0 Data Minus	Analog	
29	USB_SS_TX_M	O	USB 3.1 super-speed transmit – Minus	Analog	
31	USB_SS_TX_P	O	USB 3.1 super-speed transmit – Plus	Analog	
35	USB_SS_RX_M	I	USB 3.1 super-speed receive – Minus	Analog	
37	USB_SS_RX_P	I	USB 3.1 super-speed receive – Plus	Analog	
PCIe Communication Port					
41	PCIE_TX0_M	O	PCIe transmit 0 – Minus	Analog	
43	PCIE_TX0_P	O	PCIe transmit 0 – Plus	Analog	
47	PCIE_RX0_M	I	PCIe receive 0 – Minus	Analog	
49	PCIE_RX0_P	I	PCIe receive 0 – Plus	Analog	
53	PCIE_REFCLK_M	I	PCIe differential reference clock – Minus	Analog	
55	PCIE_REFCLK_P	I	PCIe differential reference clock – Plus	Analog	
50	PCIE_RESET_N	I	Functional reset to PCIe bus	VPH_PWR	Default PU
52	PCIE_CLKREQ_N	O	PCIe reference clock request signl	VPH_PWR	Internal 100k PU
54	PCIE_WAKE_N	O	PCIe wake-up	VPH_PWR	Internal 100k PU
SIM Card Interface 1					
36	UIM1_VCC	O	Supply output for an external UIM1 card	1.8V / 2.95V	Power

Pin	Signal	I/O	Function	Type	Comment
34	UIM1_DATA	I/O	Data connection with an external UIM1 card	1.8V / 2.95V	Internal 20k PU
32	UIM1_CLK	O	Clock output to an external UIM1 card	1.8V / 2.95V	
30	UIM1_RESET_N	O	Reset output to an external UIM1 card	1.8V / 2.95V	
66	UIM1_PRESENT	I	UIM1 Card Present Detect	1.8V	Internal 100k PU Active LOW
SIM Card Interface 2					
48	UIM2_VCC	O	Supply output for an external UIM2 card	1.8V / 2.95V	Power
42	UIM2_DATA	I/O	Data connection with an external UIM2 card	1.8V / 2.95V	Internal 20k PU
44	UIM2_CLK	O	Clock output to an external UIM2 card	1.8V / 2.95V	
46	UIM2_RESET_N	O	Reset output to an external UIM2 card	1.8V / 2.95V	
40	UIM2_PRESENT	I	UIM2 Card Present Detect	1.8V	Internal 100k PU Active LOW
Miscellaneous Functions					
6	FULL_CARD_POWER_OFF_N	I	Module On/Off	1.8V / VPH_PWR	Internal 47k PD
8	W_DISABLE_N	I	RF disable	VPH_PWR	Internal 100k PU
10	LED_N	O	LED control		Open Drain
23	WAKE_ON_WAN_N	O	Wake Host	1.8V	Default PU
65	VREG_L6B_1P8	O	Reference Voltage	1.8V	Power
67	SYS_RESIN_N	I	Reset Input	1.8V	Internal 100k PU
68	TGPIO_01	I/O	General Purpose I/O Can be I2S_CLK	1.8V	
25	TGPIO_02	I/O	General Purpose I/O Can be DPR	1.8V	
62	TGPIO_03	I/O	General Purpose I/O	1.8V	
64	TGPIO_04	I/O	General Purpose I/O	1.8V	
20	USB_PCIE_SWITCH	I	Swich Host Interface	1.8V	Internal 10k PU
22	TGPIO_06	I/O	General Purpose I/O Can be I2S_DIN	1.8V	

Pin	Signal	I/O	Function	Type	Comment
24	TGPIO_07	I/O	General Purpose I/O Can be I2S_DOUT	1.8V	
28	TGPIO_08	I/O	General Purpose I/O Can be I2S_WS	1.8V	
56	I2C_SDA	I/O	I2C Data Can be TGPIO_09	1.8V	Internal 2.2k PU
58	I2C_SCL	I/O	I2C Clock Can be TGPIO_10	1.8V	Internal 2.2k PU
38	1PPS	O	1PPS/TSN	1.8V	
26	W_DISABLE2_N	I	GNSS disable	VPH_PWR	Internal 100k PU
MIPI Control					
61	RFFE0_DATA	I/O	Data	1.8V	
63	RFFE0_CLK	O	Clock	1.8V	
Power Supply					
2	VPH_PWR	I	Power supply	Power	
4	VPH_PWR	I	Power supply	Power	
70	VPH_PWR	I	Power supply	Power	
72	VPH_PWR	I	Power supply	Power	
74	VPH_PWR	I	Power supply	Power	
GROUND					
3	GND	-	Ground	Ground	
5	GND	-	Ground	Ground	
11	GND	-	Ground	Ground	
27	GND	-	Ground	Ground	
33	GND	-	Ground	Ground	
39	GND	-	Ground	Ground	
45	GND	-	Ground	Ground	
51	GND	-	Ground	Ground	
57	GND	-	Ground	Ground	
71	GND	-	Ground	Ground	
73	GND	-	Ground	Ground	
Config					
21	CONFIG_0	-		Ground	
69	CONFIG_1	-		Ground	

Pin	Signal	I/O	Function	Type	Comment
75	CONFIG_2	-		Floating	
1	CONFIG_3	-		Floating	
Reserved for Future Use					
59	RFU				
60	RFU				

Table 13: FN990 Family Pin-out Information

Warning: Reserved pins must not be connected.

3.2. FN990 Family Signals That Must be Connected

Below table specifies the FN990 Family signals that must be connected for debugging purposes, even if not used by the end application:

Pin	Signal	Notes
2, 4, 70, 72, 74	VPH_PWR	
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND	
6	FULL_CARD_POWER_OFF_N	
7	USB_D+	If not used, connect to a test point or an USB connector
9	USB_D-	If not used, connect to a test point or an USB connector

Table 14: Mandatory Signals

3.3. Pin Layout

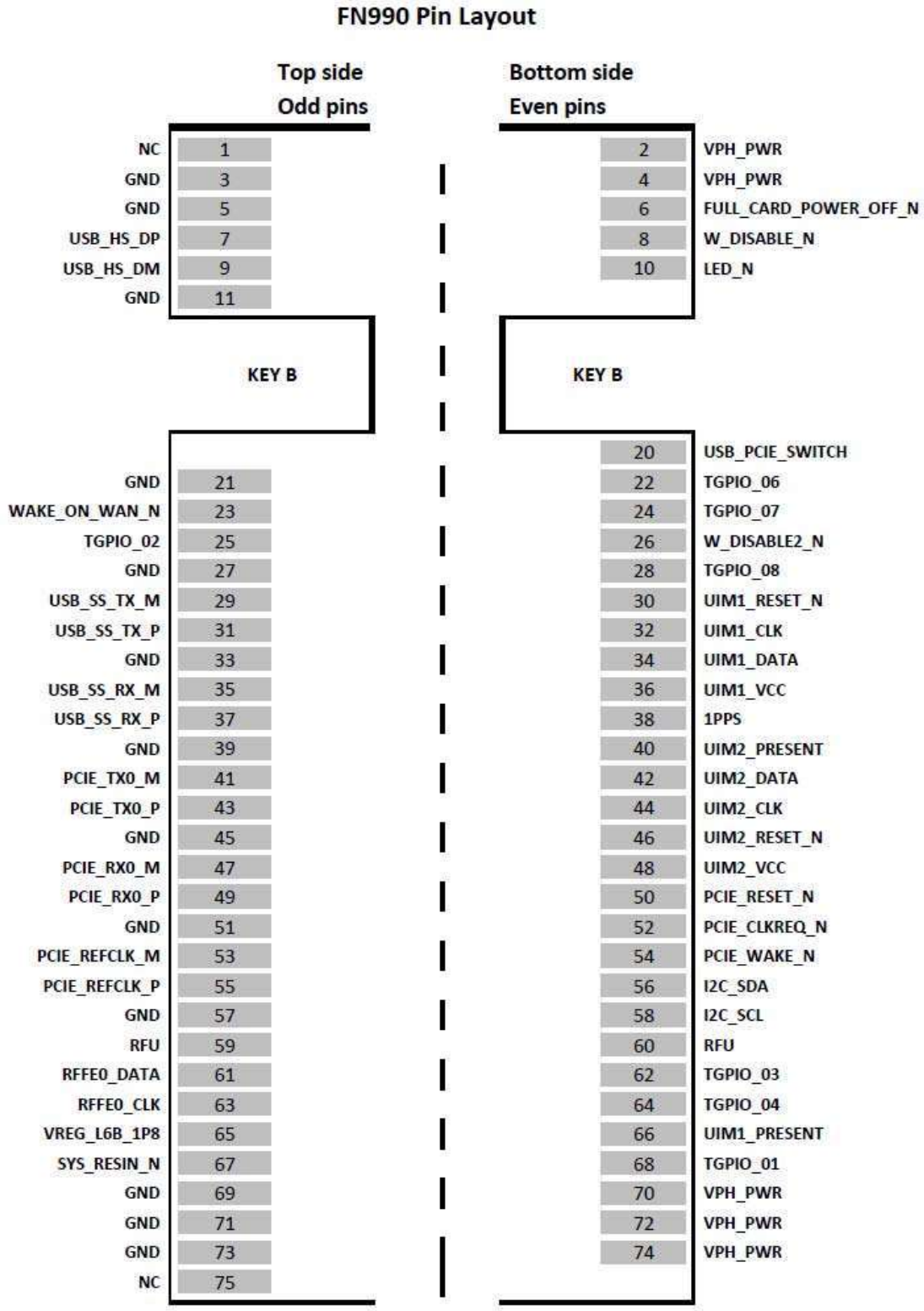

Figure 2: FN990 Family Pin out

4. POWER SUPPLY

The power supply circuitry and board layout are very important areas of the whole product design, with critical impact on the overall product performance. Please follow carefully the following requirements and guidelines to ensure reliable and stable design.

4.1. Power Supply Requirements

The FN990 Family power requirements are as follows:

Power Supply	Value
Nominal Supply Voltage	3.3V
Supply Voltage Range	3.135 V – 4.4 V
Maximum ripple on module input supply	30 mV
Peak current consumption	3.3 V @ 4 A

Table 15: Power Supply Requirements

4.2. Power Consumption

Mode	Average [Typ.]	Mode Description
IDLE Mode		
CFUN=1	35mA	No call connection USB is connected to a host
Airplane Mode (PSMWDISACFG=1, W_DISABLE_N: Low)		
CFUN=4	< 3mA	Tx and Rx are disabled; module is not registered on the network (Airplane mode) USB is disconnected
Standby Mode (PSMWDISACFG=1, W_DISABLE_N: Low)		
CFUN=1	< 5mA	Module cycles between wake and sleep USB is disconnected
Operative Mode (WCDMA)		
WCDMA Voice	850mA	WCDMA B1 voice call (Tx=23dBm)
WCDMA HSPA	650mA	WCDAM data call (DC-HSDPA up to 42Mbps, Max through-put)
Operative Mode (LTE)		
Single mode (1DL/1UL SISO)	800mA	Non-CA ,B2 BW 10MHz, 1 RB, 23dBm, QPSK DL / QPSK UL
2DLCA (4x4MIMO) with 2ULCA(SISO)	(TBD) mA	CA_2A-66A, BW 20MHz, Full RB, 256QAM DL / 256QAM UL(800Mbps DL / 170Mbps UL)

Mode	Average [Typ.]	Mode Description
7DLCA (4x4,2x2MIMO) with 1UL(SISO)	1450mA	CA_1A-3C-7C-20A-38A, Full RB, 256QAM DL/ 256QAM UL(1500Mbps DL / 103Mbps UL)
5DLCA (4x4MIMO) with 1UL(SISO)	1150mA	CA_1A-3C-7C, Full RB, 256QAM DL/ 256QAM UL(2Gbps DL / 103Mbps UL)
Operative Mode (NR-FR1)		
NSA mode 1CC+1FR1	900 mA	EN-DC_1A(1DL/UL SISO)-n78A(1DL/1UL SISO)
		LTE : BW 20MHz, 1 RB, QPSK DL / QPSK UL, 23dBm
		FR1 : BW 100MHz, Inner RB 137(Number)@64(Position), QPSK DL / QPSK UL, 23 dBm
NSA mode 6CC+1FR1	2000mA	EN-DC_1A(DL2x2/1UL SISO)-3C(DL4x4)-7C(DL4x4)_28A(DL2x2) -n78(1DL 4x4MIMO/1UL SISO/60M)
		LTE : BW 20MHz, Full RB, 256QAM DL / 256QAM UL(2Gbps DL / 103Mbps UL)
		FR1 : BW100MHz, Full RB, 256QAM DL / 256QAM UL(1.6Gbps DL/118Mbps)
SA mode 1FR1	380mA	FR1(n78A) : BW100MHz, Full RB, 256QAM DL / 256QAM UL(1.89Gbps DL/1.25Mbps)
SA mode 2FR1	730mA	FR1(CA_n78A_n78A) : BW200MHz, Full RB, 256QAM DL / 256QAM UL(3.8Gbps DL/1.25Mbps)

Table 16: FN990 Family Current Consumption

Note: Worst/best case current consumption values depend on mobile network configuration – not under module control.

* Loop-back mode in call equipment

* 3.3 voltage / room temperature

4.3. General Design Rule

The principal guidelines for the Power Supply Design include three different design steps:

- Electrical design
- Thermal design
- PCB layout

4.3.1. Electrical Design Guidelines

The electrical design of the power supply is highly dependent on the power source from which the power is drained.

4.3.1.1. +5V Source Power Supply Design Guidelines

- The desired power supply voltage output is 3.3V. Being the difference between the input source and the desired output moderate, a linear regulator can be used. A switching power supply is preferred to reduce power dissipation.
- When using a linear regulator, a proper heat sink must be provided to dissipate the power generated.
- A low ESR bypass capacitor of adequate capacity must be provided to cut the current absorption peaks close to the FN990 Family module. A 100 µF tantalum capacitor is usually suitable on VPH_PWR.
- Make sure that the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the modem power input to protect the FN990 Family module from power polarity inversion.

4.3.2. Thermal Design Guidelines

The aim of this paragraph is to provide thermal design guidelines useful for developing a product with a Telit FN990 modem.

Proper thermal protection design protects against human or component damage under worst-case conditions.

Furthermore, it reduces the probability of failure and does not adversely affect the use of the module, and greatly extents the operation time with maximum performance.

For more details, please refer to the thermal design guidelines.

Note: FN990 Family supports different RATs: 3G, 4G and 5G Sub-6.

Based on the Radio Access Technology, the FN990 modem might exhibithigh current consumption, thus proper thermal designs are essential to dissipate heat well.

Note: There is the large solder resist opening area on the bottom side of the module. Adding a TIM on that area with a heatsink is highly recommended to ensure proper heat dissipation.

The modem temperature vale can be read via AT command.

Note: For optimal RF performance, thermal dissipation and mecahnical stability, the FN990 must be connected to the ground and metal chassis of the host board.

The module shield and host device or metal chassis of the host device should be connected by means of conductive material.

4.3.3. Power Supply PCB Layout Guidelines

As described in the electrical design guidelines, a low ESR capacitor should be connected to the power supply output to reduce current peaks. A protection diode on the modem power supply input should be connecte to protect the FN990 from spikes and polarity inversion.

Placement of these components is crucial for correct operation: a misplaced component can badly affect power supply performance:

- The bypass low ESR capacitor must be placed close to the FN990 power input pins or - if the power supply is of a switching type - it can be placed close to the inductor to reduce ripple, as long as the PCB trace from the capacitor to FN990 is wide enough to avoid significant voltage drop even during the 4A current peaks.
- The protection diode must be placed close to the modem connector.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure that no voltage drops occur during the 4A current peaks.
- The PCB traces connecting the FN990 and bypass capacitor must be wide enough to avoid voltage drops even when 4A current absorbtion peaks occur. These traces should be kept as short as possible.
- The PCB traces connecting the switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode as closed as possible to the power switching IC (only for the switching power supplies). This is done to reduce the radiated field (noise) at the switching frequency (usually 100-500 kHz).

- Use a good common ground plane.
- Place the power supply on the board to ensure that the high current return paths in the ground plane do not overlap any noise sensitive circuitry, such as microphone amplifier/buffer or earphone amplifier.
- The power supply input cables must be kept separate from noise sensitive lines, such as microphone/earphone cables.

4.4. RTC

The RTC within the FN990 Family module does not have a dedicated RTC supply pin. The RTC block is supplied by the VPH_PWR supply.

If the VPH_PWR power is removed, RTC is not maintained so if it is necessary to maintain an internal RTC, VPH_PWR must be supplied continuously.

4.5. Reference Voltage

The 1.8V regulated power supply output is supplied as the reference voltage to a host board. This output is active when the module is turned ON and turns OFF when the module is shutdown.

This table lists the reference voltage of the FN990 Family modules.

Pin	Signal	I/O	Function	Type	Comment
65	VREG_L6B_1P8	O	Reference Voltage	Power	1.8V

Table 17: FN990 Family Reference Voltage

4.6. Internal LDO for GNSS Bias

The LDO for GNSS bias is applied inside the FN990 Family model.

The voltage supply is generated internally by the FN990 (LDO) and is fed to GNSS active antenna.

This table below lists the LDO for GNSS bias of FN990 Family modules.

Symbol	Parameter	Min	Typ	Max	Unit
$V_{GNSS\ DC\ bias}$	Voltage of internal LDO for GNSS bias	2.9	3.1	3.15	[V]
$I_{GNSS\ DC\ bias}$	Current of internal LDO for GNSS bias	-	-	100	[mA]

Table 18: LDO for GNSS bias of FN990 Family

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings – Not Optional

Warning: A deviation from the value ranges listed below could damage the FN990 module.

Symbol	Parameter	Min	Max	Unit
VPH_PWR	Battery supply voltage on pin VPH_PWR	-0.3	+4.7	[V]

Table 19: Absolute Maximum Ratings - Not optional

5.2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Ambient temperature	-40	+25	+85	[degC]
VPH_PWR	Battery supply voltage on pin VPH_PWR	3.135	3.3	4.4	[V]
I_{VPH_PWR}	Peak current on pin VPH_PWR	-	-	4	[A]

Table 20: Recommended Operating Conditions

6. DIGITAL SECTION

6.1. Logic Levels

Unless otherwise specified, all FN990 Family interface circuits are 1.8V CMOS logic.

Only USIM interfaces are capable of dual voltage I/O.

The following tables show the logic level specifications used in the FN990 interface circuits. The data specified in the tables below are valid throughout all drive strengths and the whole temperature range.

Warning: Do not connect FN990 digital logic signal directly to the application digital logic signals with a voltage higher than 2.134V for 1.8V CMOS signals.

6.1.1. 1.8V Pins – Absolute Maximum Ratings

Parameter	Min	Max
Input level on any digital pin when on	-	+2.134 V
Input voltage on analog pins when on	-	+2.134 V

Table 21: Absolute Maximum Ratings - Not Functional

6.1.2. 1.8V Standard GPIOs

Parameter		Min	Max	Unit	Comment
V_{IH}	Input high level	1.26	2.1	[V]	
V_{IL}	Input low level	-0.3	0.54	[V]	
V_{OH}	Output high level	1.35	1.8	[V]	
V_{OL}	Output low level	0	0.45	[V]	

Table 22: Operating Range - Interface Levels (1.8V CMOS)

6.1.3. 1.8V UIM1/UIM2 Pins

Parameter		Min	Max	Unit	Comment
V_{IH}	Input high level	1.17	2.1	[V]	
V_{IL}	Input low level	-0.3	0.63	[V]	

Parameter		Min	Max	Unit	Comment
V_{OH}	Output high level	1.35	1.8	[V]	
V_{OL}	Output low level	0	0.45	[V]	

Table 23: Operating Range - UIM Pins Working at 1.8V

6.1.4. 2.95V Pins – Absolute Maximum Ratings

Parameter	Min	Max
Input level on any digital pin when on	-	+3.344 V
Input voltage on analog pins when on	-	+3.344 V

Table 24: Absolute Maximum Ratings - Not Functional

6.1.5. 2.95V SIM Card Pins

Parameter		Min	Max	Unit	Comment
V_{IH}	Input high level	1.843	3.25	[V]	
V_{IL}	Input low level	-0.3	0.73	[V]	
V_{OH}	Output high level	2.21	2.95	[V]	
V_{OL}	Output low level	0	0.368	[V]	

Table 25: Operating Range - UIM Pins Working at 2.95V

6.1.6. VPH_PWR Level I/O Pins

Parameter		Min	Max	Unit
V_{IH}	Input high level	0.65 x VPH_PWR	-	[V]
V_{IL}	Input low level	-	0.35 x VPH_PWR	[V]
V_{OH}	Output high level	0.8 x VPH_PWR	VPH_PWR	[V]
V_{OL}	Output low level	0	0.2 x VPH_PWR	[V]

Table 26: Operating Range - I/O Pins Working at VPH_PWR

6.2. Power ON/OFF/RESET

The following tables show the description of power control pins.

Pin	Signal	I/O	Function	Type	Comment
6	FULL_CARD_POWER_OFF_N	I	Module On/Off	1.8V / VPH_PWR	Internal 47k PD
67	SYS_RESIN_N	I	Reset Input	1.8V	Internal 100k PU
65	VREG_L6B_1P8	O	Reference Voltage	1.8V	Power
*	BOOT_OK / Shutdown Indicator	O	Power ON/OFF Status Check	1.8V	* Can be assigned to GPIO

Table 27: Power Interface Signals

6.2.1. Power On

To turn on the FN990 data card, the FULL_CARD_POWER_OFF_N pin must be asserted high.

Note: To turn on the FN990 module, the SYS_RESIN_N pin must not be asserted low. If asserted low for more than one second, the FN990 modem will be reset. Power on can be triggered by SYS_RESIN_N pin (low level) as well. Even so, please control the FN990 ON/OFF status by FULL_CARD_POWER_OFF_N pin.

6.2.1.1. Initialization and Activation State

After turning on the FN990 module, the device is not yet fully functional because the software boot and initialization process takes some time to complete. For this reason, it is not recommended to start communicating with the FN990 module during the initialization phase.

The AT command interface is accessible via USB or PCIe port. In general, as shown in figure below, the FN990 modems become fully operational (in the Activation state) at least 50 seconds after the FULL_CARD_POWER_OFF_N is asserted.

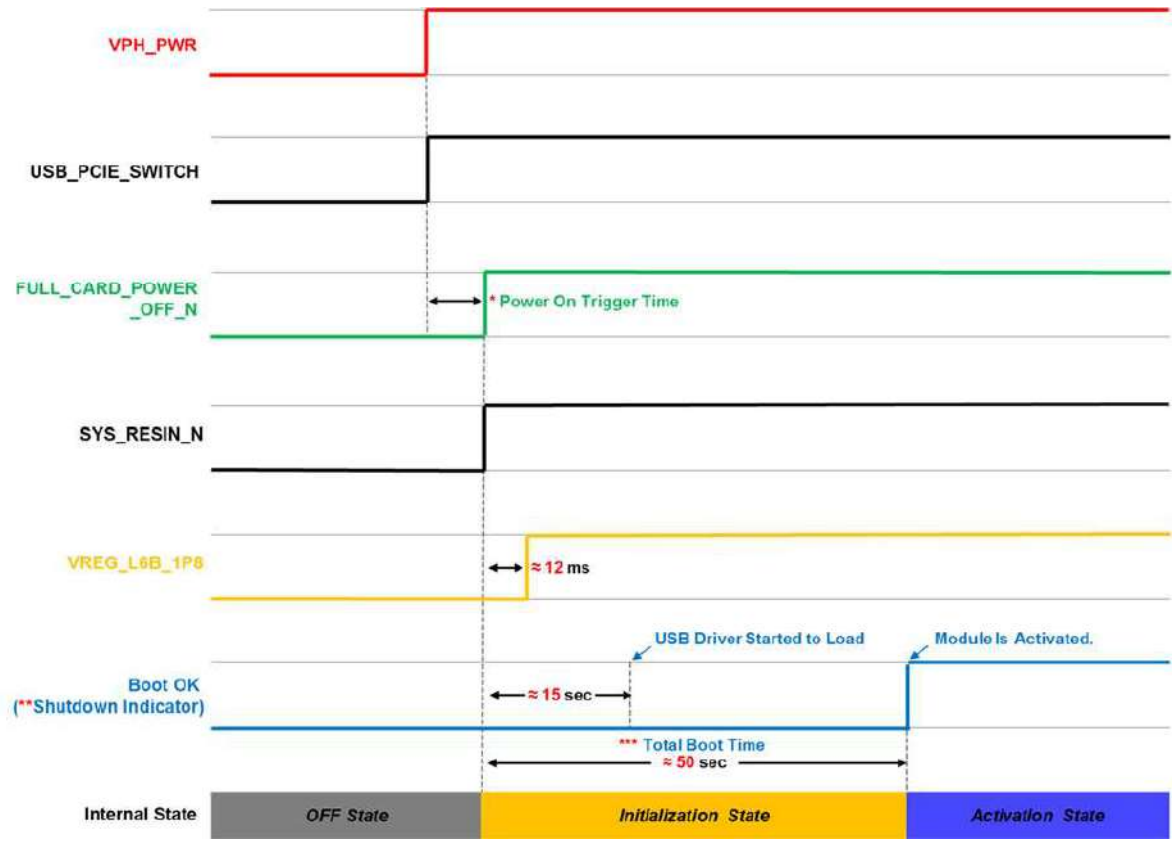

Figure 3: FN990 Family Power ON Sequence - USB mode (USB_PCIE_SWITCH: High, Default)

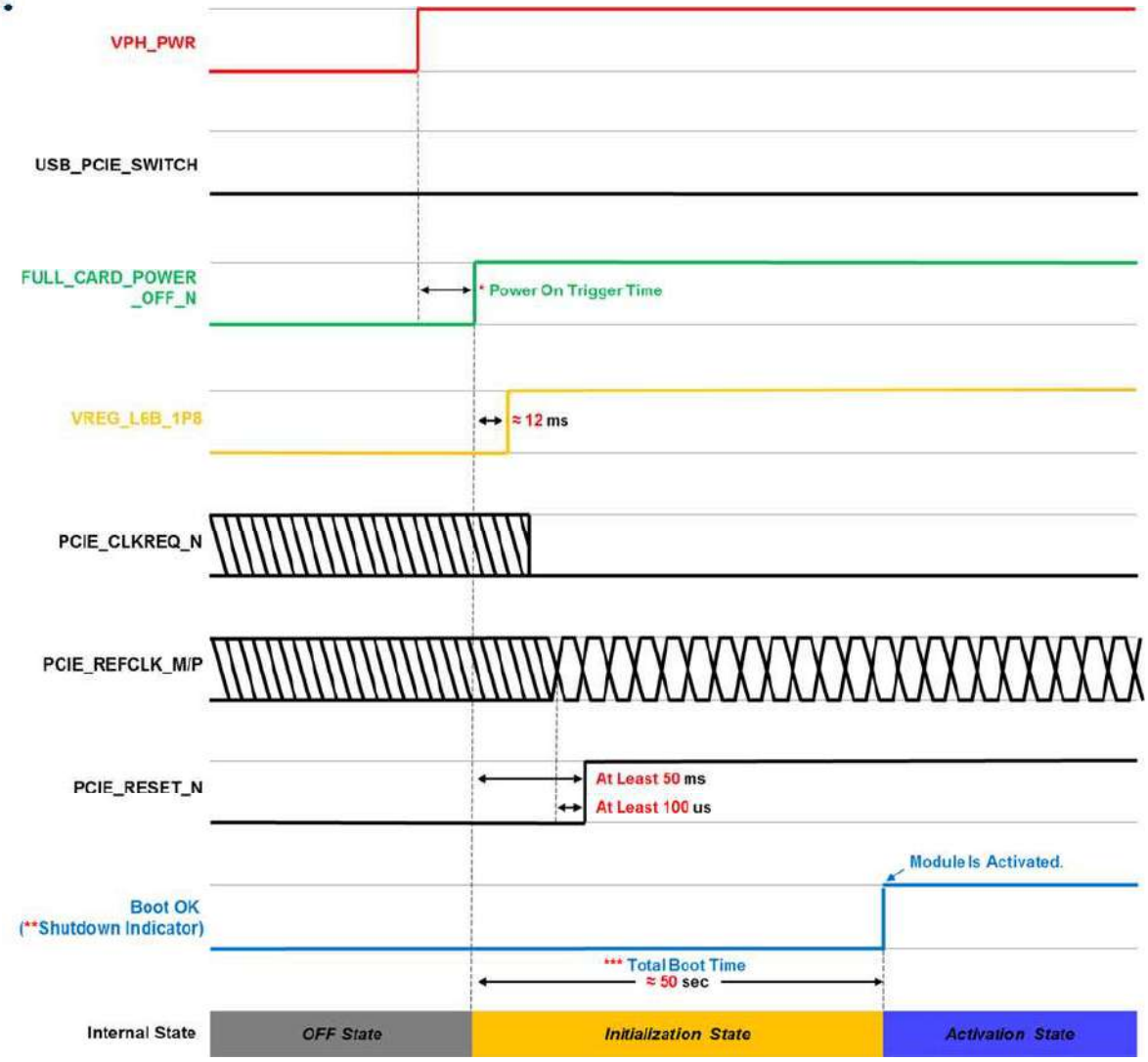

Figure 4: FN990 Family Power ON Sequence – PCIe EP mode (USB_PCIE_SWITCH: Low)

Note: To verify if the FN990 Family has powered up properly, please follow the indications below:

* Power on trigger time is the interval between VPH_PWR to FULL_CARD_POWER_OFF_N: this could be null (0 ms) if the customer application requires turning on the module automatically.

** Monitoring BOOT_OK (Shutdown indicator) pin. When the status translates to high, the moduleboot-up process is complete. To use BOOT_OK (Shutdown indicator), the shutdown indication function must be enabled through the AT#SHDNIND command. (please refer to the AT Reference Guide document)

*** The stated total boot time is an approximate measure of the latest SW and HW combination. The boot time may be lengthened or shortened depending on the module configuration, firmware or hardware version.

Note: Active low signals are labeled with a name ending with "_N"

Note: To avoid a back-powering effect, it is recommended to prevent any HIGH logic level signals from being applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

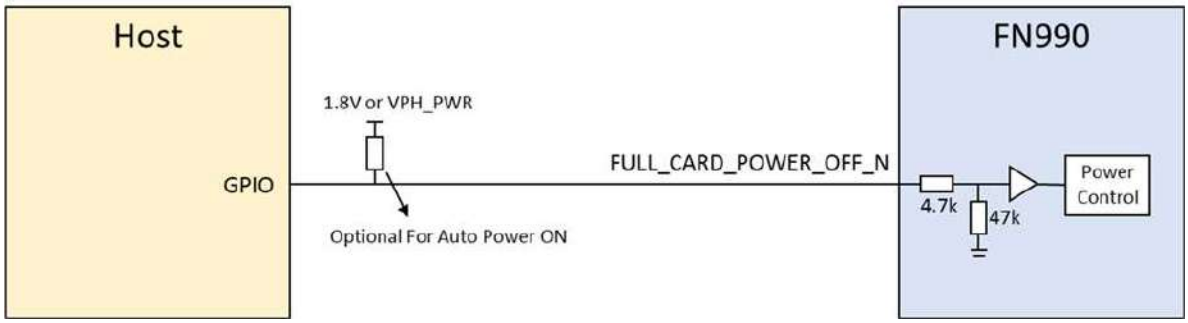

Figure 5: Example Circuit for ON/OFF by FULL_CARD_POWER_N

6.2.2. Power Off

Power off of the device can be done in two different ways:

- Graceful shutdown by FULL_CARD_POWER_OFF_N

Fast shutdown by GPIO triggered

6.2.2.1. Graceful Shutdown

To shutdown the FN990 Family module safely, host can use the graceful shutdown function.

The graceful shutdown can be triggered by:

- FULL_CARD_POWER_OFF_N

6.2.2.1.1. Graceful Shutdown by FULL_CARD_OFF_N

To gracefully shutdown the FN990 , FULL_CARD_POWER_OFF_N should be asserted to Low.

Once FULL_CARD_POWER_N is asserted to Low, the FN990 enters finalization state, terminates active processes and prepares to turn off safely.

As shown in the diagram below, VREG_L6B_1P8 will indicate when the module is ready to be turned off.

Figure 6: Graceful Shutdown by FULL_CARD_POWER_OFF_N

Note: Graceful Shutdown triggered by FULL_CARD_POWER_OFF_N is only effective after module boots up completely.

* The stated total shutdown time is an approximate measure of the latest SW and HW combination. The shutdown time may be lengthened or shortened depending on the SW configuration, SW or HW version.

6.2.2.2. Fast Shutdown

For quicker FN990 module shutdown, the host application can use the fast shutdown function, which can be triggered by:

- GPIO (+ optional shutdown indicator)

6.2.2.2.1. Fast Shutdown by GPIO

To leverage fast shutdown feature, one of the GPIO lines should be assigned as Fast Shutdown Trigger by means of the AT commands.

Once the fast shutdown trigger senses a High to Low transition, fast shutdown is started: the FN990 enters finalization state, terminates active processes and prepares to turn off safely. As shown in the figure below, when the module is ready to be turned off, it will be indicated via VREG_L6B_1P8.

Please refer to the AT User Guide for more details on how to enable the shutdown indicator and fast shutdown trigger.

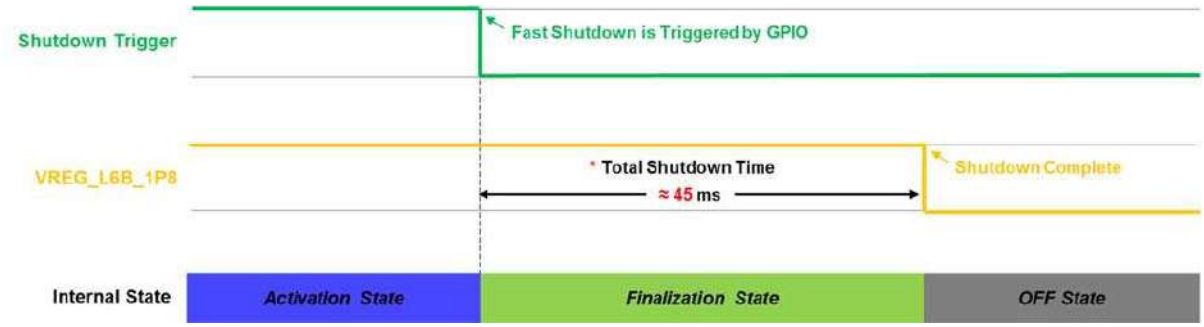

Figure 7: Fast Shutdown by GPIO

Note: Using a fast shutdown without shutdown indicator function, FULL_CARD_POWER_N pin should be controlled to prevent the FN990 from rebooting.

For more information, please refer to the AT commands reference guide and SW user guide document.

* The stated total shutdown time is an approximate measure of the latest SW and HW combination. The shutdown time may be lengthened or shortened depending on the SW configuration, SW or HW version.

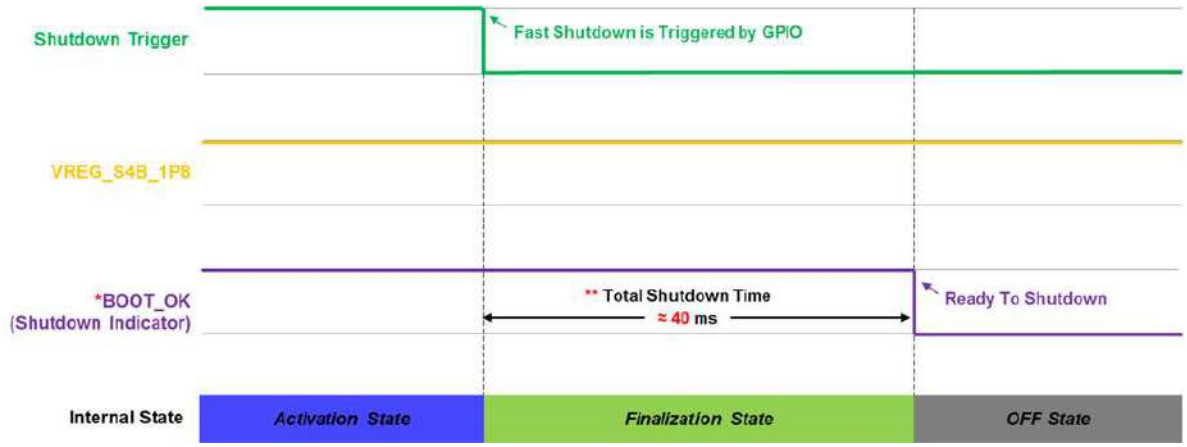

*Figure 8: Fast Shutdown by GPIO (*SHDNIND Enable, Optional)*

Note: *Shutdown Indicator is an optional function and is disabled by default. The host can verify the module entered OFF state by monitoring the shutdown indicator pin status. To turn on the module after using a fast shutdown with shutdown indicator function, it should be re-powered or reboot.

For more information, please refer to AT Commands Reference Guide and SW User Guide document.

Note: Fast shutdown function is disabled by default. To use fast shutdown function, please refer to the AT Commands Reference Guide and SW User Guide document.

Warning: If the VPH_PWR is to be kept at a high status, the module will re-boot. (Not applicable to Shutdown Indicator function)

Warning: Failure to follow recommended shut-down procedures might damage the device and consequently void the warranty.

6.2.3. Reset

Device reset can be achieved as follows:

- Unconditional reset using the SYS_RESIN_N

6.2.3.1. Unconditional Hardware Reset

To unconditionally restart the FN990 Family module, the SYS_RESIN_N pin must be asserted low more than 1 second and then released.

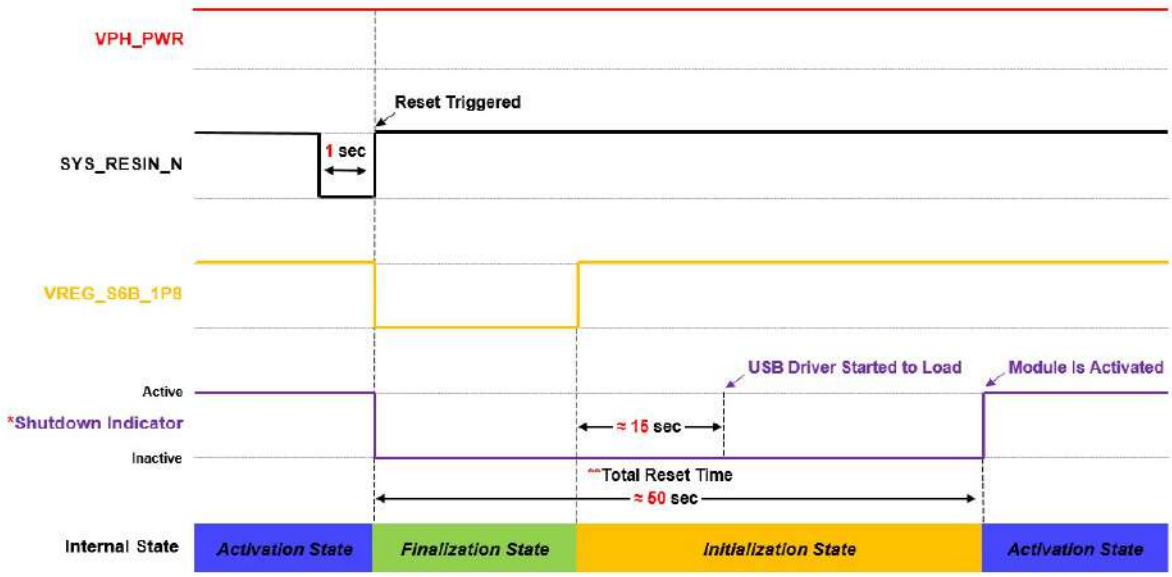

Figure 9: Unconditional Hardware Reset by SYS_RESIN_N

Note: *Shutdown Indicator is an optional function. If SHDIND is enabled, it can verify the status via SHDIND function.

Please refer to the AT commands user guide document.

** The stated total reset time is an approximate measure of the latest SW and HW combination. The shutdown time may be lengthened or shortened depending on the SW configuration, SW or HW version.

Note: Unconditional hardware reset must be used only as an emergency procedure, and not as a normal power-off operation.

Note: Do not use any pull-up resistor on the RESET_N line or any totem pole digital output. Using a pull-up resistor may cause latch-up problems on the FN990 Family power regulator and improper functioning on the module.

The RESET_N line must be connected only in an open-collector configuration.

Below figure shows a simple circuit for this action.

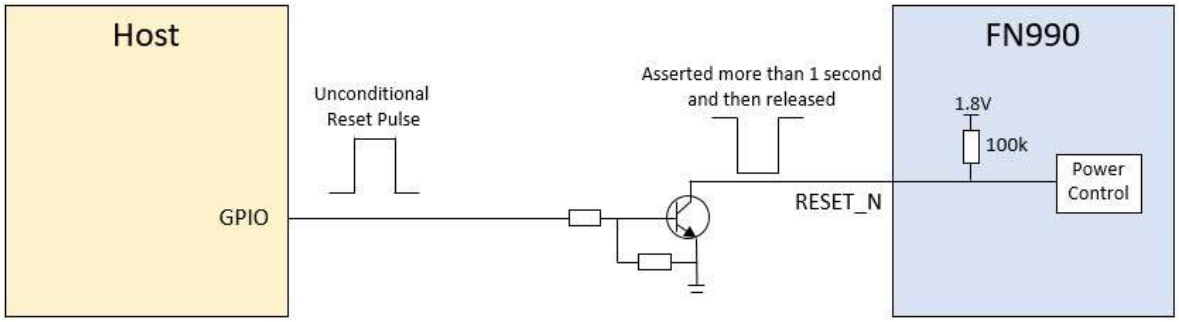

Figure 10: Example Circuit for RESET by SYSTEM_RESET_N

6.3. Communication Ports

The below table summarizes all the hardware interface of the FN990 Family module.

Interface	Description
PCIe	Peripheral Component Interconnect Express Gen 4.0
USB	USB 3.1 Gen 2 interface
USIM	x2 dual voltage each (1.8V / 2.95V)
eSIM	Embeded SIM (optional)
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
Control Interfaces	W_DISABLE_N, WAKE_ON_WAN_N, LED, DPR
Antenna ports	x4 Cellular, 1 for GNSS

Table 28: FN990 Family Hardware Interfaces

6.3.1. Host Interface

Note: FN990 M.2 data card supports USB 3.1 Gen 2 and PCIe Gen 4 respectively. This means USB 3.1 and PCIe 4.0 interface cannot be used at the same time.

Basically, the host interface operates as USB 3.1 Gen 2: if the application requires to use PCIe Gen 4.0 host interface switch must be used.

6.3.1.1. Host Interface Switch Function

This chapter describes the host interface switch functions.

Pin	Signal	I/O	Function	Type	Comment
20	USB_PCIE_SWITCH	I	Swich Host Interface	1.8V	Internal 10k PU

Table 29: Host Interface Switch Pin

FN990 Family M.2 Card determines the host interface by checking the status of USB_PCIE_SWITCH pin at the beginning of the power on sequences.

High(Default): USB 3.1 or USB 2.0

Low: PCIe 3.0 + (USB 3.1 or USB 2.0)*

*USB interface is only used as debugging purposes when USB/PCIe Switch pin is low.

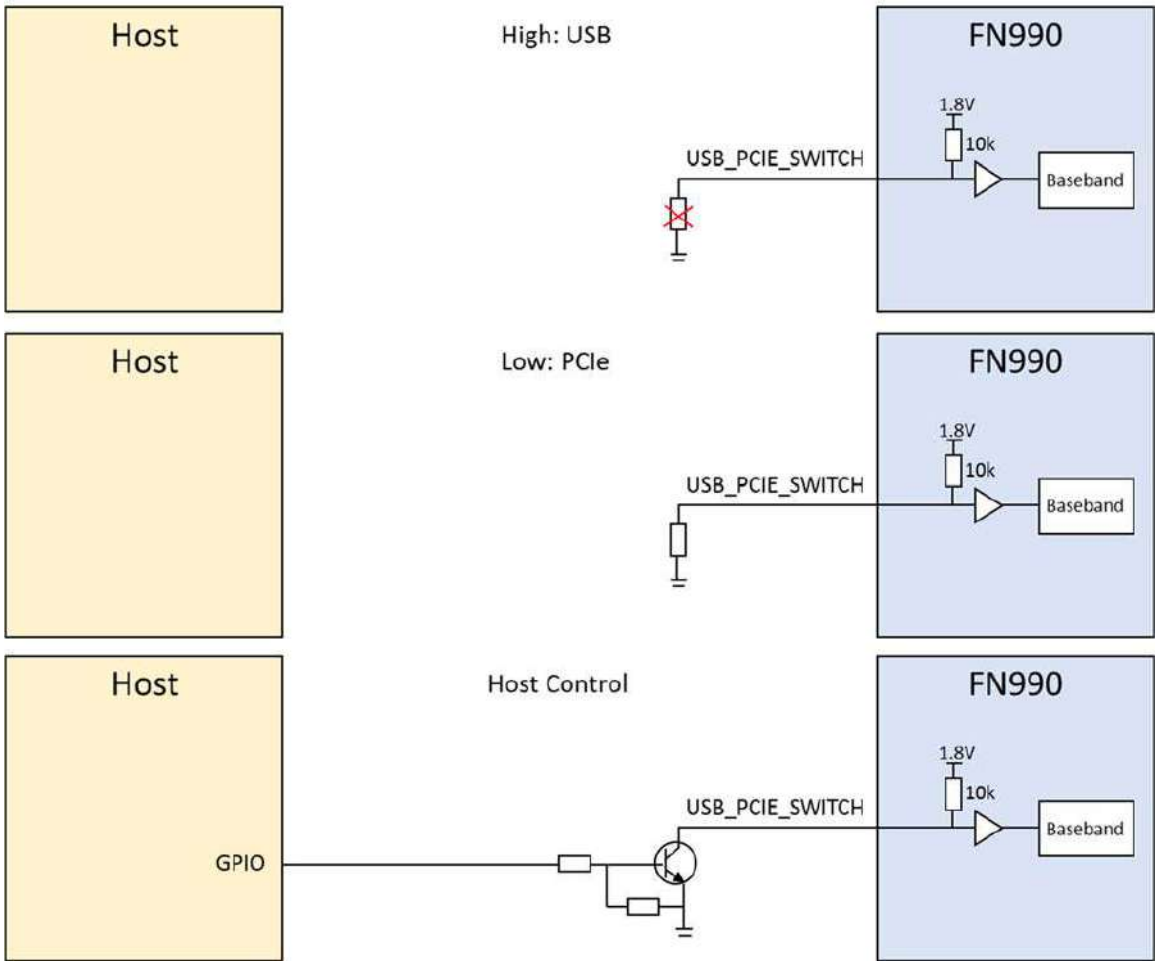

Figure 11: Example Circuit for HOST Interface Switch Function

6.3.1.2. PCIe Interface

The FN990 Family module includes PCIe interface. PCIe needs AC coupling series capacitors on the TX lines in both directions. In order to interface PCIe with the application board that controls the modem, 0.22 uF capacitors should be installed on PCIE_RX_P/M lines of the FN990. The series capacitors are already placed on PCIE_TX_P/M lines inside the FN990.

Internally, VPH_PWR level 100k pull-up resistor is already mounted on PCIE_WAKE_N and PCIE_CLKREQ_N.

The suggested PCIe interface connection is shown in the diagram below: