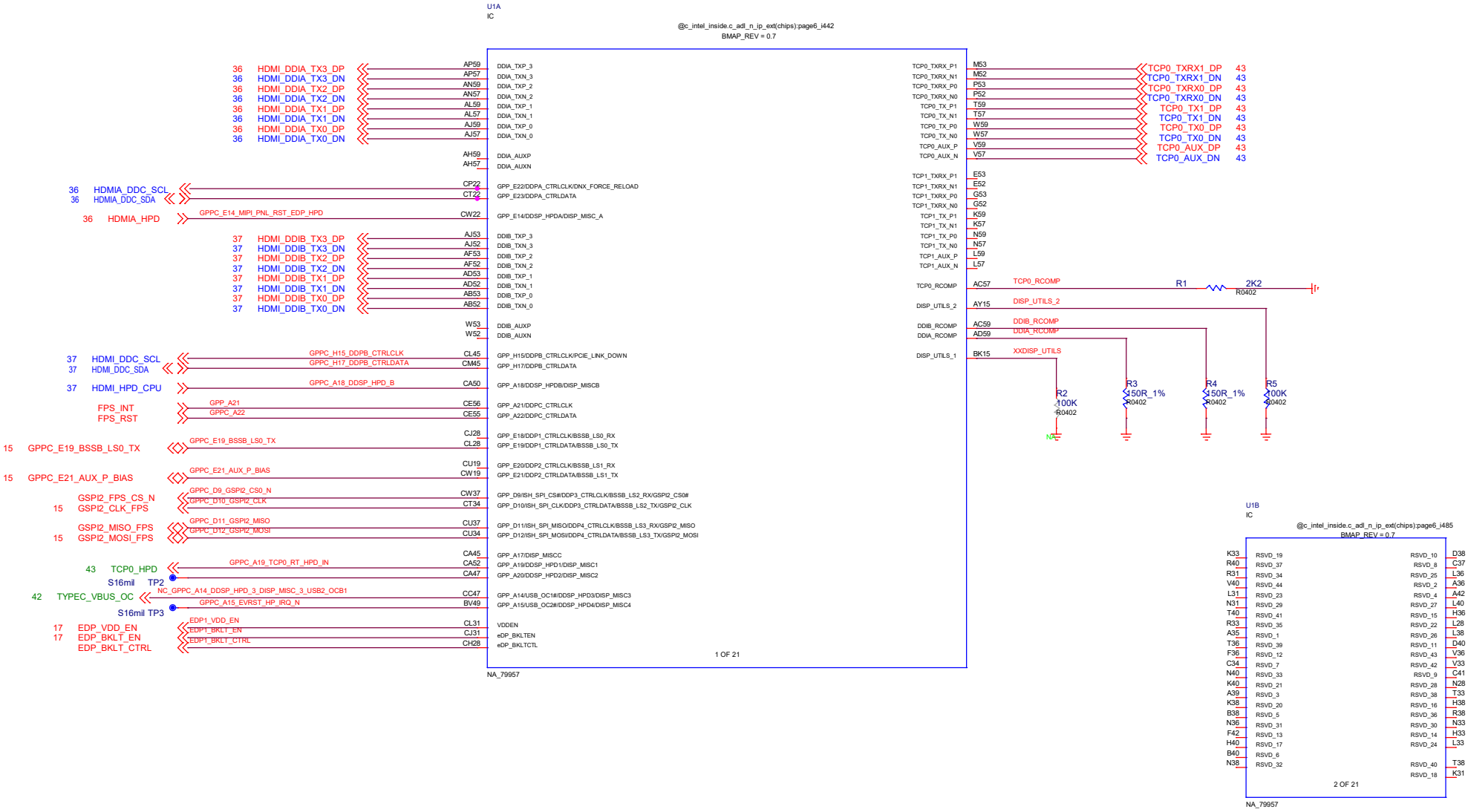
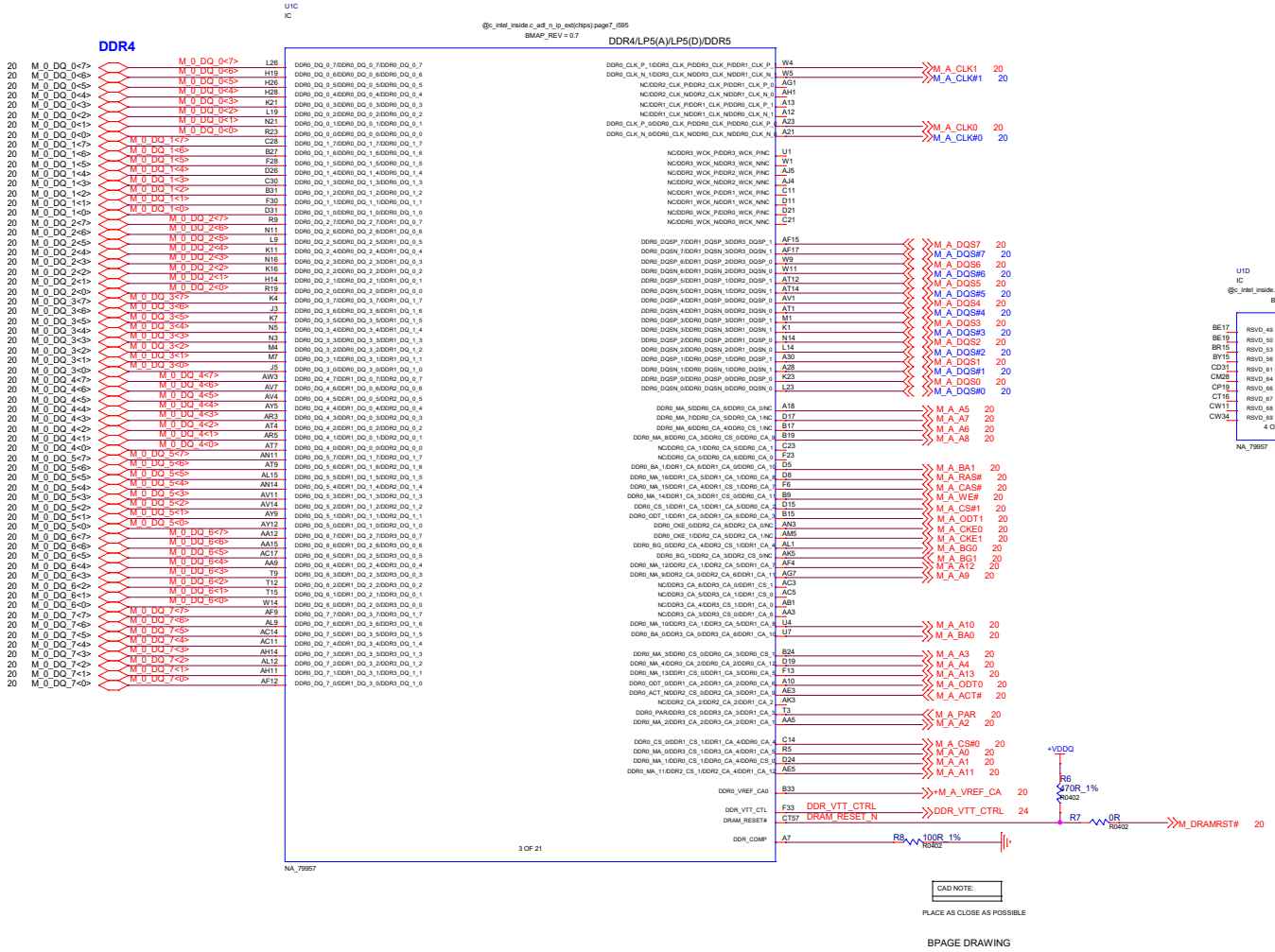
04_ADL-N MCP-DISP



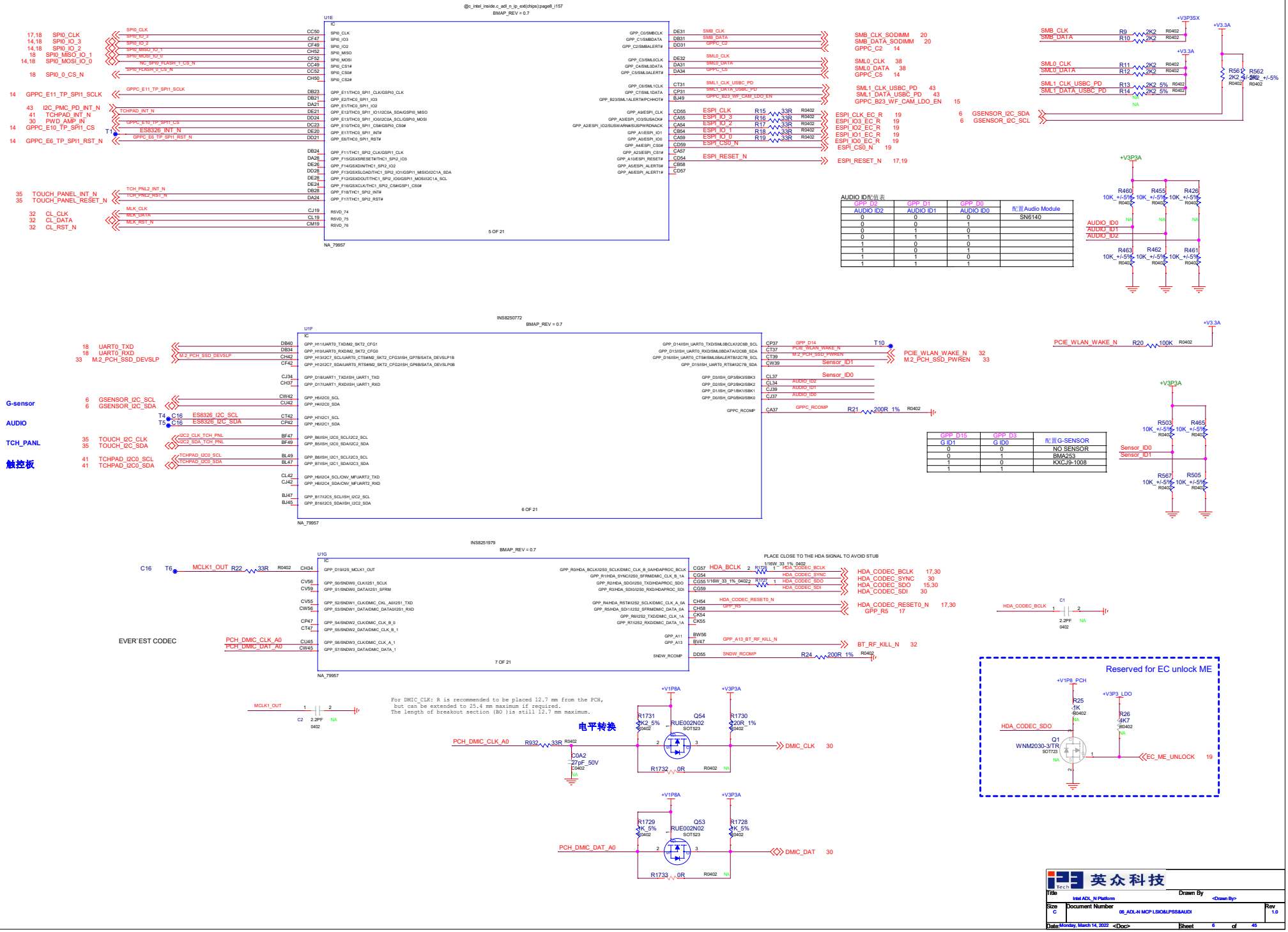
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size	Custom	Document Number	04_ADL-N MCP-DISP
Rev	1.0		
Date	Monday, March 14, 2022	<Doc>	Sheet 4 of 45

05_ADL-N MCP -MEMOR

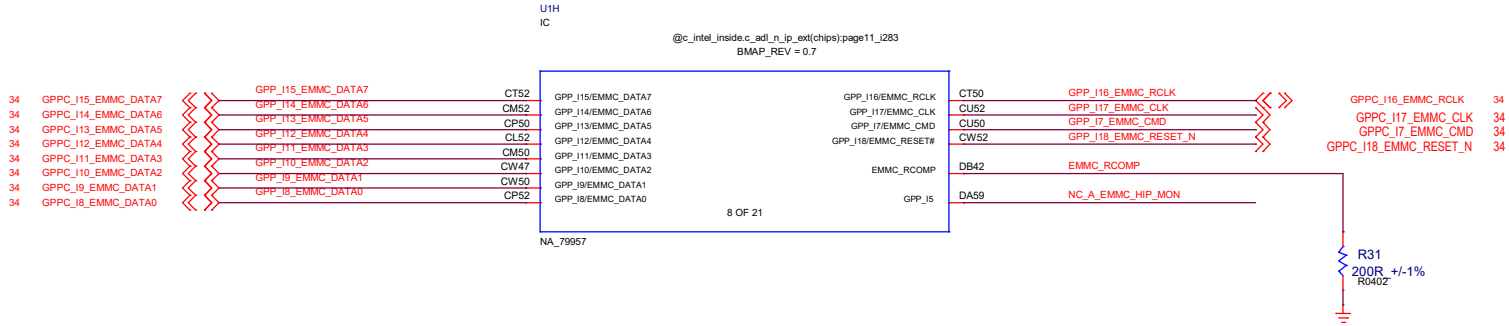


Title	Drawn By
Intel ADL_N Platform	<Drawn By>
Size: Custom	Document Number: 05_ADL-N MCP -MEMOR
Rev: 1.0	
Date: Monday, March 14, 2022 <Doc>	Sheet 5 of 45

06_ADL-N MCP LSIO&LPSS&AUDI



07_ADL-N MCP - EMMC

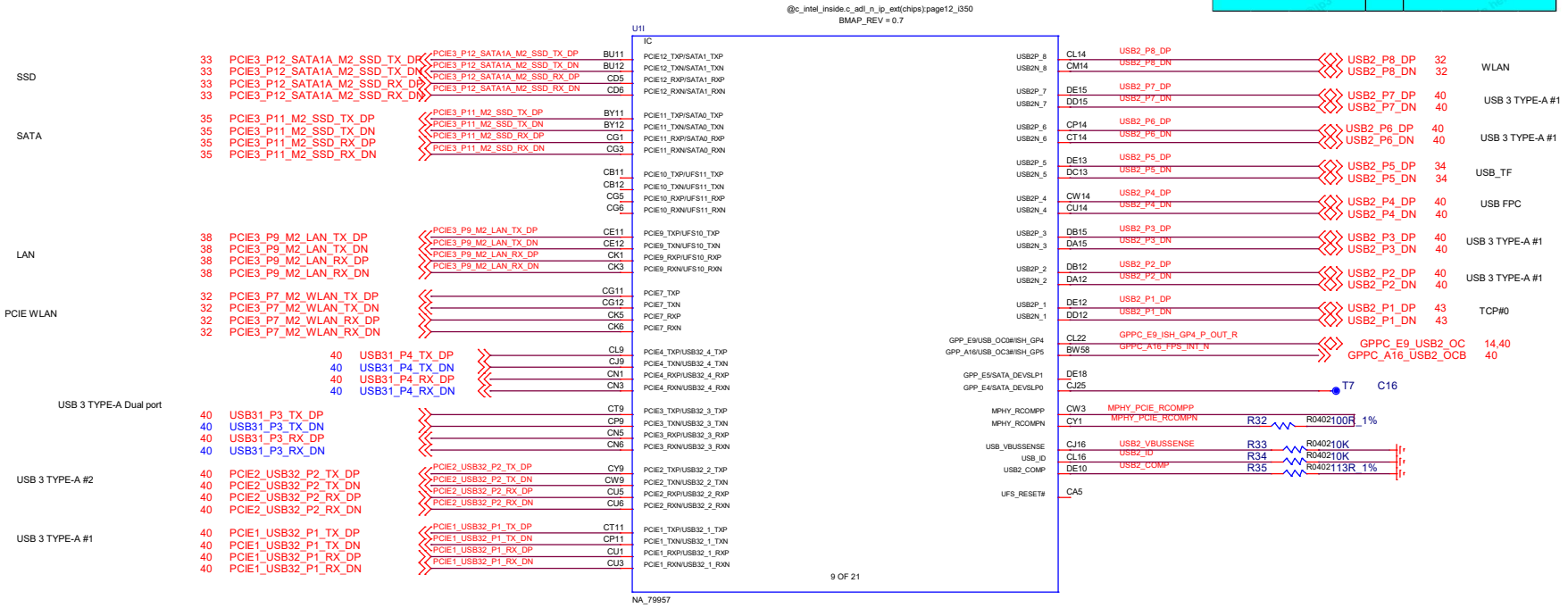


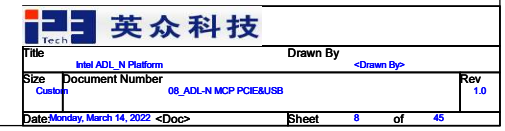
Title	Intel ADL_N Platform	Drawn By <Drawn By>
Size B	Document Number 07_ADL-N MCP - EMMC	Rev 1.0
Date Monday, March 14, 2022 <Doc>	Sheet 7 of 45	

08_ADL-N MCP PCIE&USB

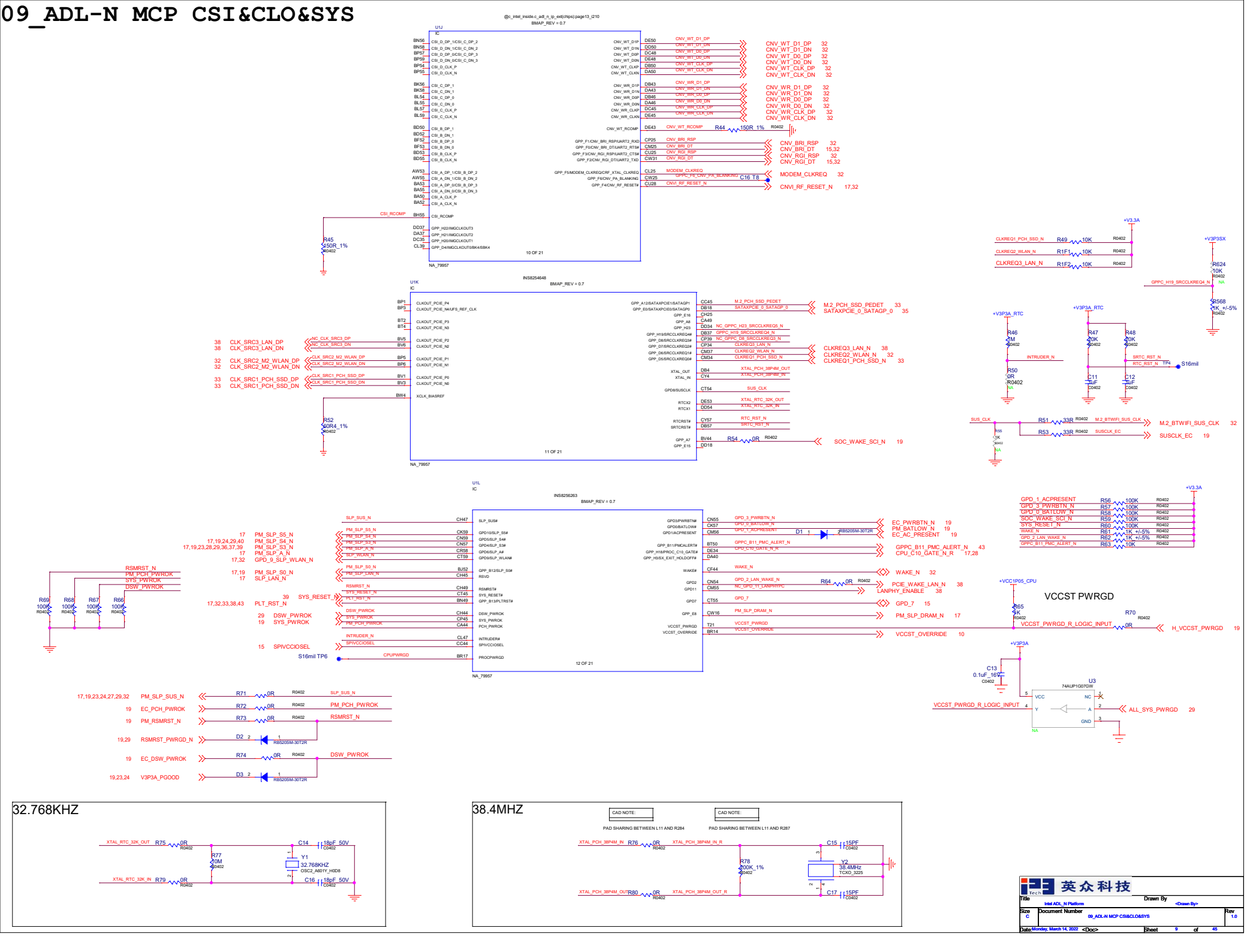
Alder Lake-N HSIO Lane Assignments

- Total 9 ModPHY Lanes
- Up to 9 PCIe* Gen 3 lanes with 5 PCIe* Clks
- Up to 4 USB3.2 Gen 2x1
- Up to 2 SATA3
- 4 USB3.2 Gen 1x1 + PCIe* muxed lanes
- 1 PCIe* only lanes
- 2 PCIe + UFS2.1 muxed lane
- 2 PCIe + SATA muxed lane

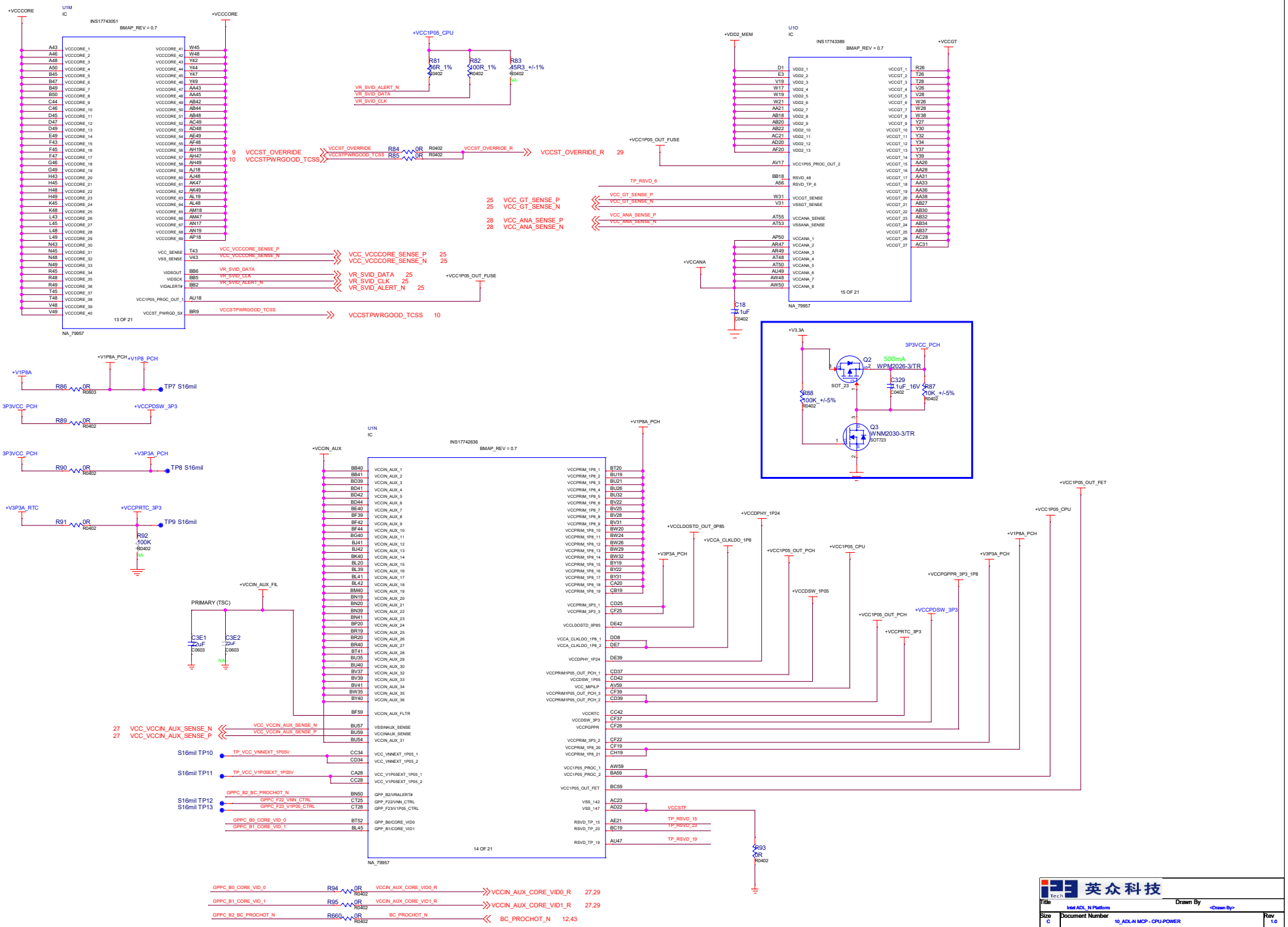




09_ADL-N MCP CSI&CLO&SYS

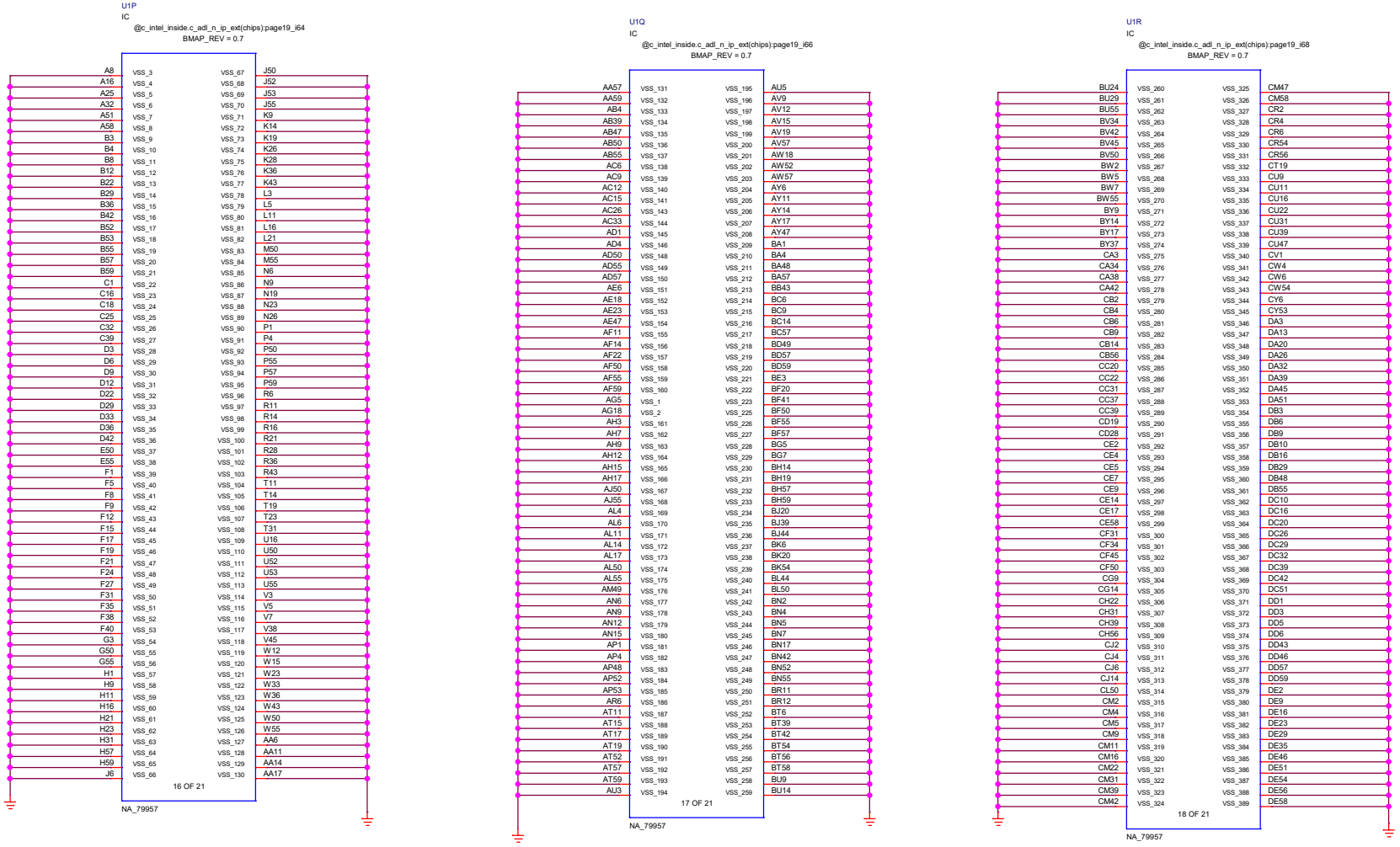


10_ADL-N MCP - CPU-POWER



Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 10_ADL-N MCP - CPU-POWER		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 10 of 45	

11_ADL-N MCP GND



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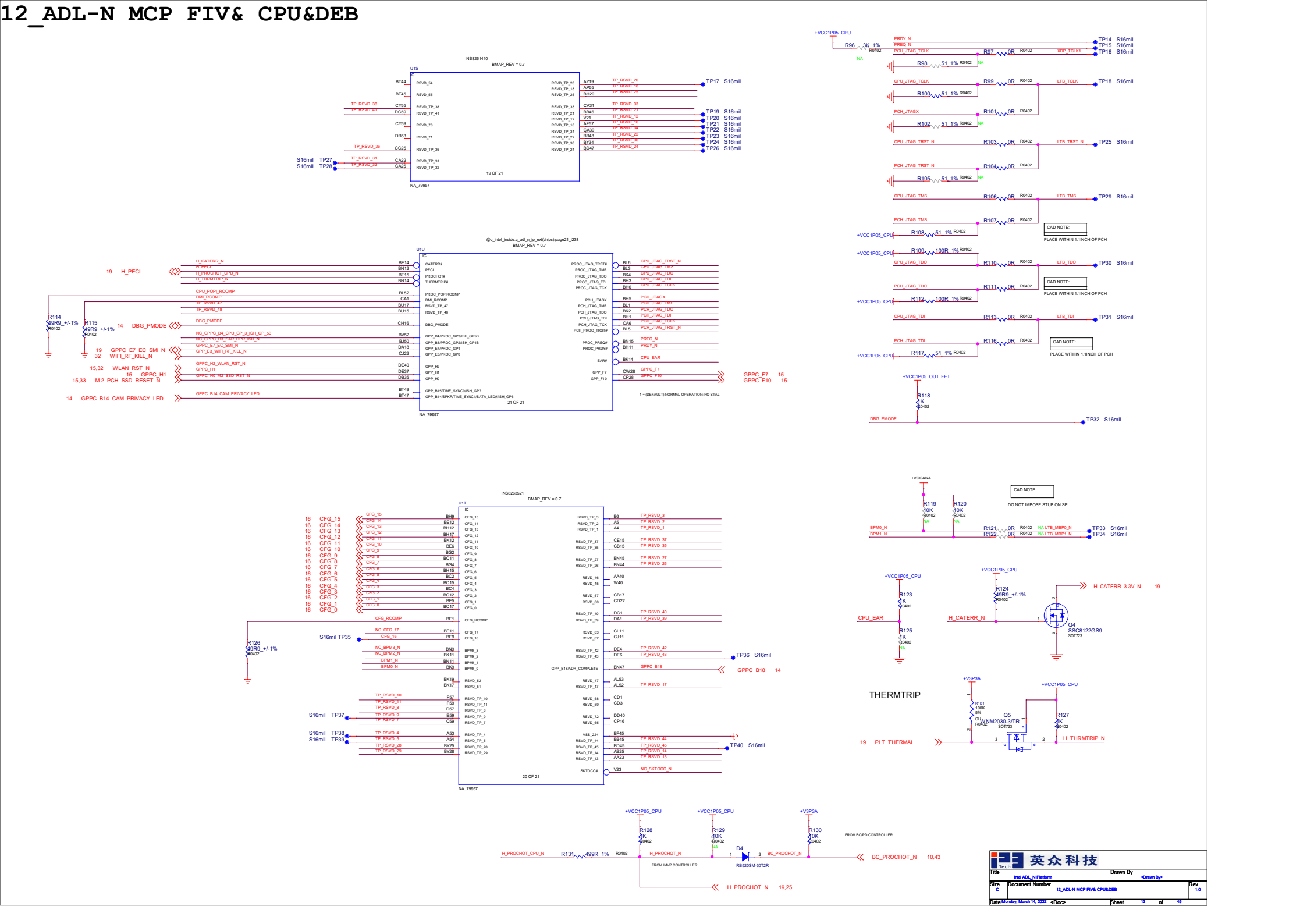
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size	Custom	Document Number	11_ADL-N MCP GND
Rev	1.0		
Date	Monday, March 14, 2022 <Doc>	Sheet	11 of 45

12_ADL-N MCP FIV& CPU&DEB



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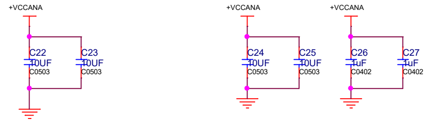
VCCANA PDBOM

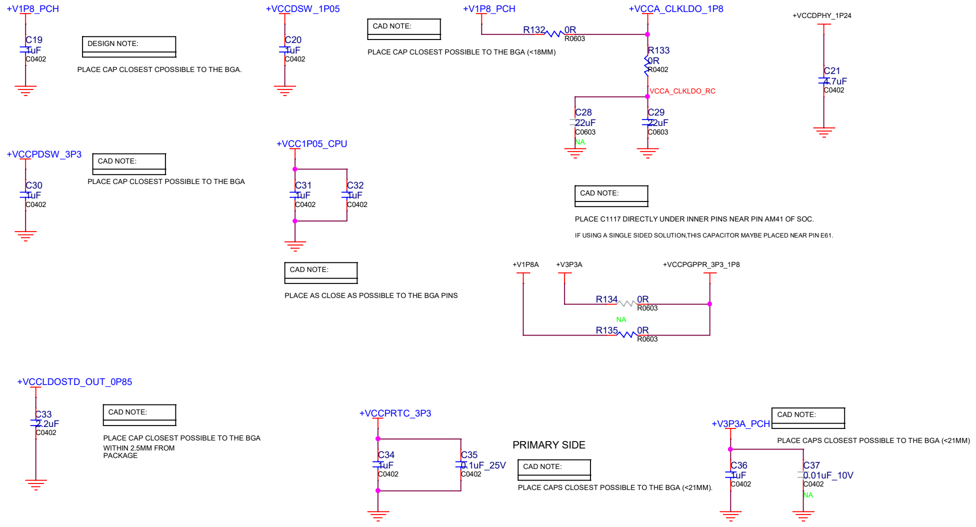


VCCANA - PRIMARY	
10UF 0402	2

VCCANA - SECONDARY	
10UF 0402	2
10UF 0402 - PH	2
1UF 0201	2

PLACE BOTTOM SIDE

PCH_PD BOM

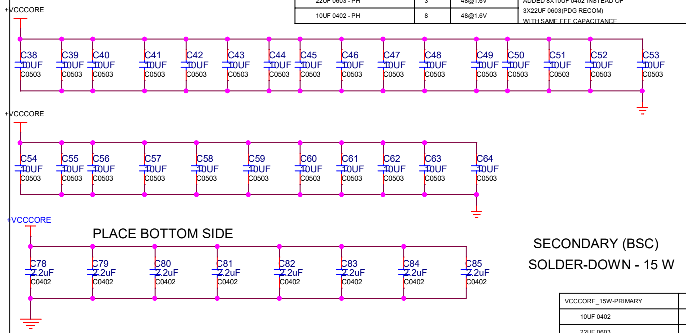


PD_CORE_PD BOM (VCCCORE)

PRIMARY (TSC)

SOLDER-DOWN - 15 W

VCCCORE_15-SECONDARY		EFF CAPACITANCE	COMMENT
10UF 0402	4		
10UF 0402 - PH	3		
22UF 0603 - PH	3	48@1.6V	ADDED 8X10UF 0402 INSTEAD OF 3X22UF 0603(PDG RECOM) WITH SAME EFF CAPACITANCE
10UF 0402 - PH	8	48@1.6V	



PLACE BOTTOM SIDE

SECONDARY (BSC)

SOLDER-DOWN - 15 W

VCCCORE_15W-PRIMARY	
10UF 0402	10
22UF 0603	10

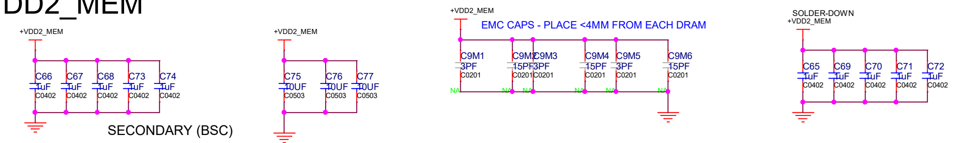
VDD2_MEM

CAPS ADDED TO MEET TARGET IMPEDENCE AFTER FAST PI SIMULATION

SOLDER DOWN

PRIMARY (TSC)

SECONDARY (BSC)

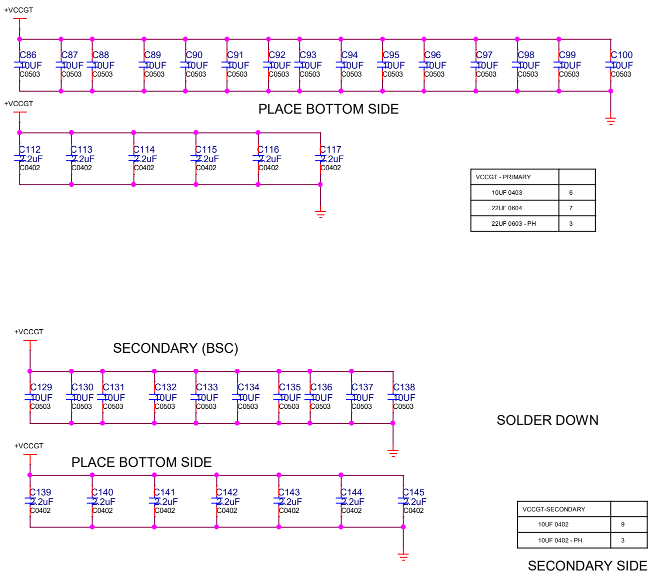


SECONDARY (BSC)

PD_CORE_ PD BOM (GT)

PRIMARY (TSC)

SOLDER DOWN



VCCGT - PRIMARY	
10UF 0403	6
22UF 0604	7
22UF 0603 - PH	3

SOLDER DOWN

VCCGT-SECONDARY	
10UF 0402	9
10UF 0402 - PH	3

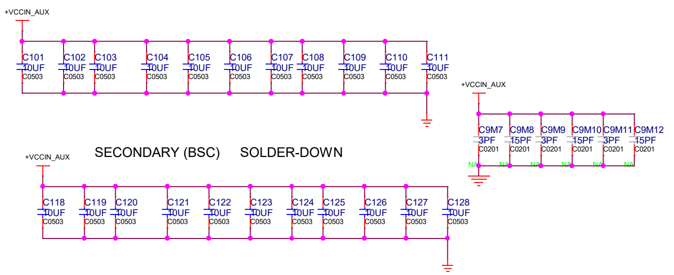
SECONDARY SIDE

VCCIN_AUX

PD_CORE_VCCIN_AUX -PD BOM

PRIMARY (TSC)

SOLDER-DOWN



VCCIN_AUX-PRIMARY	
22UF 0603	10

CAD NOTE:

PLACE TOP SIDE

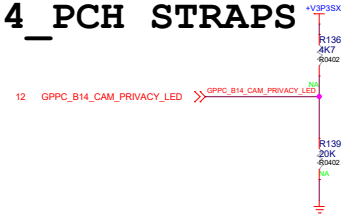
VCCIN_AUX-SECONDARY			
10UF 0402	10		
22UF 0603 - PH	2	29.3@1.8V	ADDED 5 X10UF 0402 INSTEAD OF 2X22UF 0603(PDG RECOM) WITH SAME EFF CAPACITANCE
10UF 0402 - PH	5	29.3@1.8V	

EMC CAPS - PLACE <5MM FROM VCCIN_AUX

CAD NOTE:

PLACE BOTTOM SIDE

14_PCH STRAPS

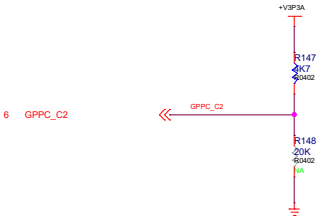


TOP SWAP OVERRIDE

HIGH- TOP SWAP ENABLED
LOW-DISABLED
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

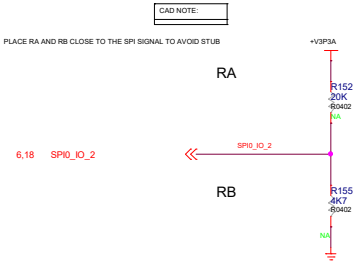
NO REBOOT

HIGH - NO REBOOT
LOW- REBOOT ENABLED
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK



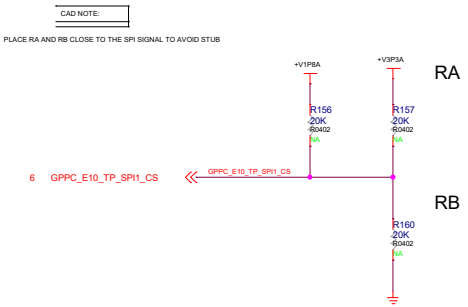
TLS CONFIDENTIALITY

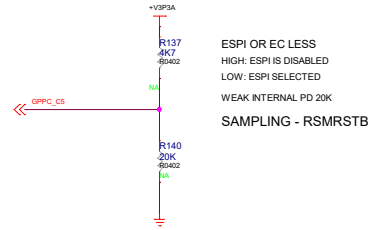
LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB



CONSENT STRAP

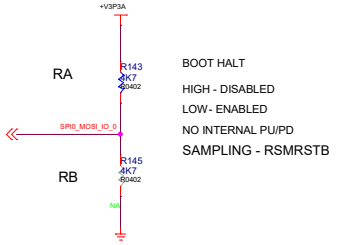
HIGH: DISABLED
LOW: ENABLED
NO INTERNAL PU/PD
SAMPLING - RSMRSTB





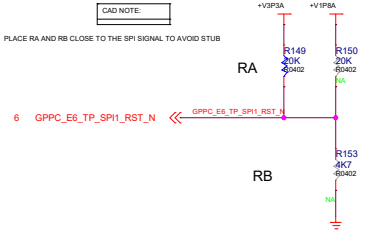
ESPI OR EC LESS

HIGH: ESPI IS DISABLED
LOW: ESPI SELECTED
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB



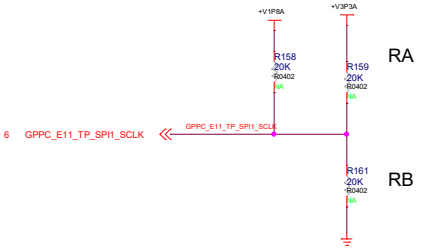
BOOT HALT

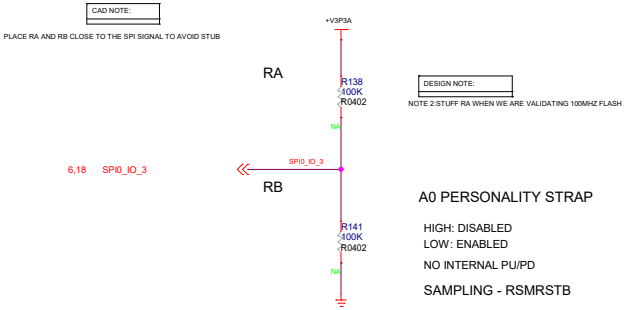
HIGH - DISABLED
LOW- ENABLED
NO INTERNAL PU/PD
SAMPLING - RSMRSTB



JTAG ODT DISABLE

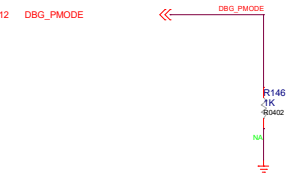
LOW: JTAG ODT DISABLED
HIGH: JTAG ODT ENABLED
NO INTERNAL PU/PD
SAMPLING - RSMRSTB





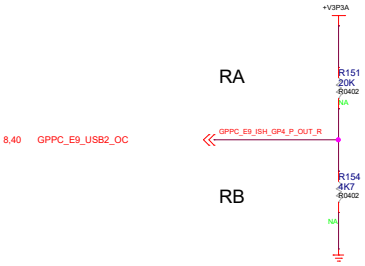
A0 PERSONALITY STRAP

HIGH: DISABLED
LOW: ENABLED
NO INTERNAL PU/PD
SAMPLING - RSMRSTB



DFXTESTMODE

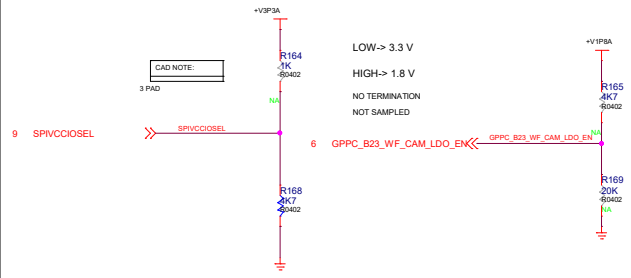
PGDMON
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K
SAMPLING - RSMRSTB



Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 14_PCH STRAPS 1		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 14 of 45	

15_PCH STRAPS 2

STRAP FOR SPI 1.8V/3.3V SELECTION



LOW-> 3.3 V

HIGH-> 1.8 V

NO TERMINATION

NOT SAMPLED

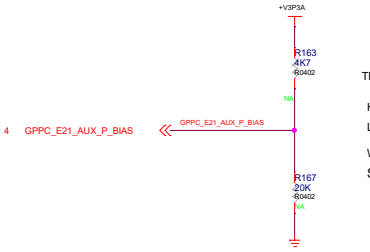
CPUNSSC CLOCK FREQ

HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)

LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB



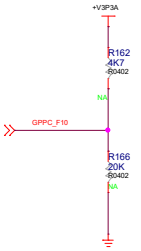
TBT LSX #1 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB



XTAL INPUT MODE

LOW- XTAL ATTACHED (DEFAULT)

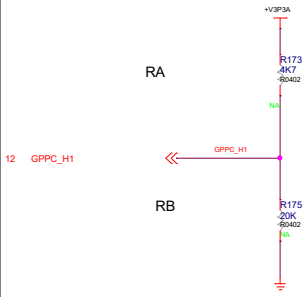
HIGH - SINGLE ENDED CRYSTAL INPUT

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

RA

RB



FOR UNFUSED A0 SILICON STUFF 1-X

GPP_R_2

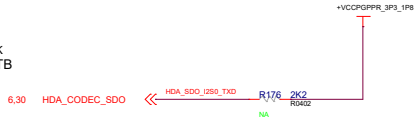
CAD NOTE:

PLACE CLOSE TO THE HDA SIGNAL TO AVOID STUB

BFX STRAP 2- BIT 3

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB



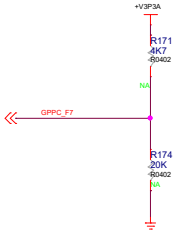
FLASH DESCRIPTOR SECURITY OVERRIDE

HIGH: OVERRIDEN

LOW: SECURITY MEASURES NOT OVERRIDEN

WEAK INTERNAL PD 20K

SAMPLING- PCH_PWROK



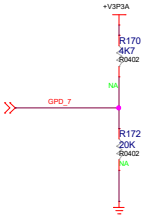
MCRO LDO BYPASS

LOW : NO BYPASS (DEFAULT)

HIGH : LDO BYPASS

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB



SKIP RTC CLOCK STABILIZATION DELAY

LOW- NO BYPASS (DEFAULT)

HIGH - BYPASS/SKIP 95MS RT CLOCK STABILIZATION DELAY

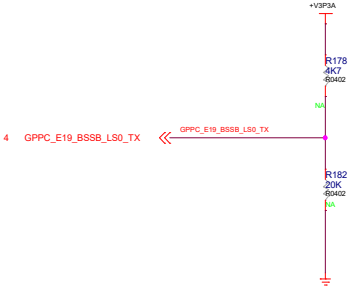
WEAK INTERNAL PD 20K

SAMPLING- DSW_PWROK

BFX STRAP 3- BIT 4

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB



TBT LSX #0 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

BFX STRAP 1- BIT 2

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

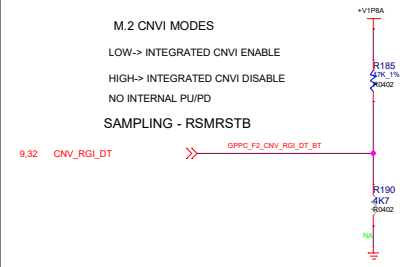
M.2 CNVI MODES

LOW-> INTEGRATED CNVI ENABLE

HIGH-> INTEGRATED CNVI DISABLE

NO INTERNAL PU/PD

SAMPLING - RSMRSTB



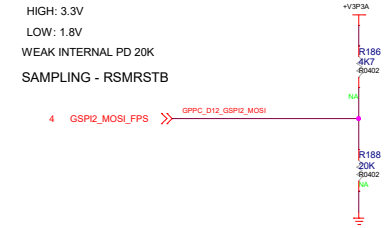
TBT LSX #3 PINS VCCIO CONFIGURATION

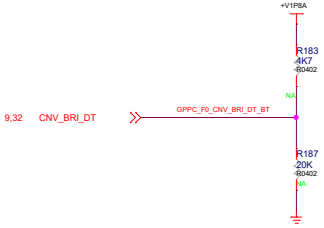
HIGH: 3.3V

LOW: 1.8V

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB





XTAL SEL1

LOW: 38.4/19.2MHZ (DEFAULT)

HIGH = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB

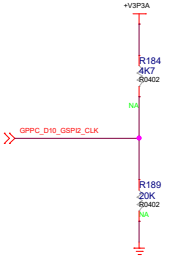
TBT LSX #2 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

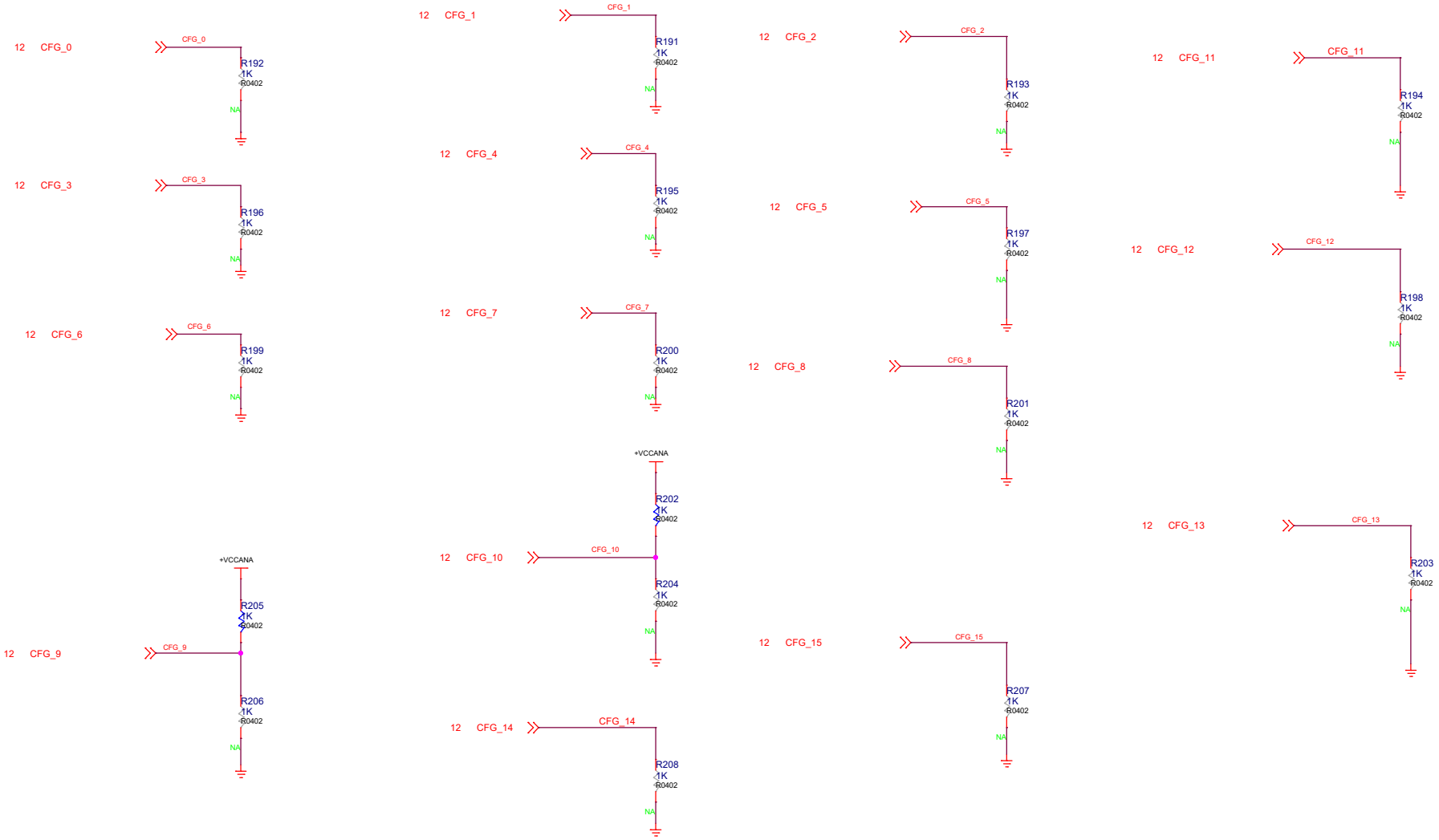
WEAK INTERNAL PD 20K

SAMPLING - RSMRSTB



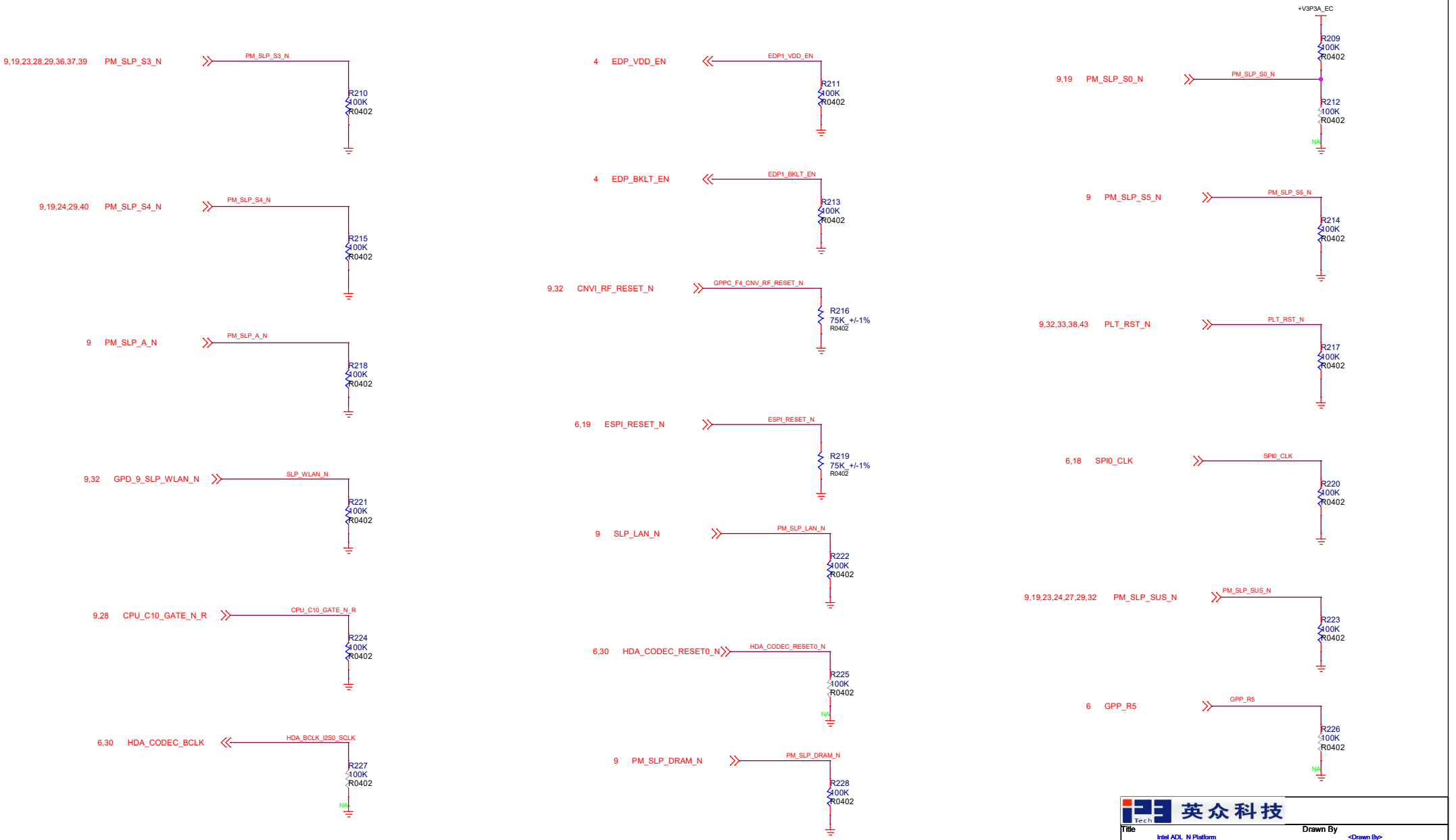
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 15_PCH STRAPS 2		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 15 of 45	

16_CPU_STRAPS



Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size	Custom	Document Number	16_CPU_STRAPS
			Rev 1.0
Date:	Monday, March 14, 2022 <Doc>	Sheet	16 of 45

17_GLITCH FREE CIRCUIT



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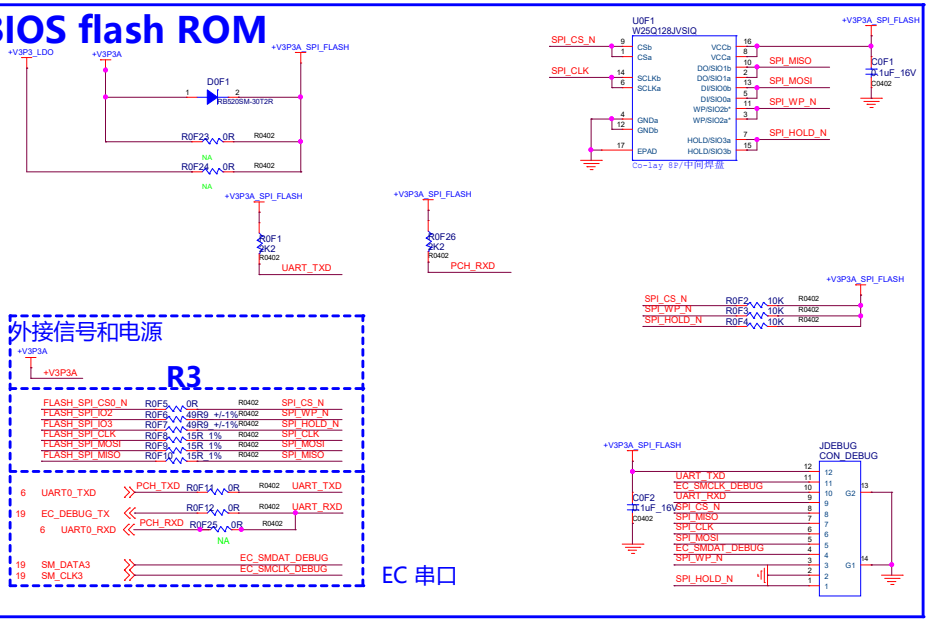
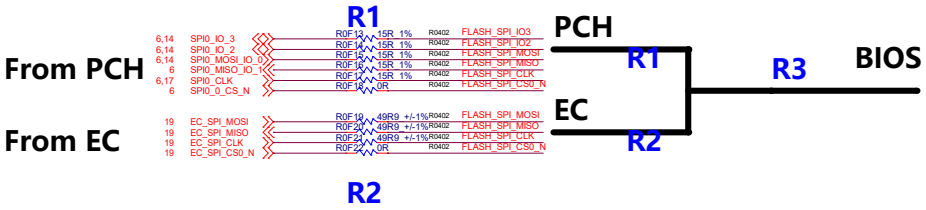
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size	Document Number		Rev
Custom	17_GLITCH FREE CIRCUIT		1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 17 of 45	

18_SYSTEM FLASH

BIOS flash ROM





TPM2.0(INFINEON)

6.18.1.1.7 1-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing

Figure 242. SPI0 1-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Diagram

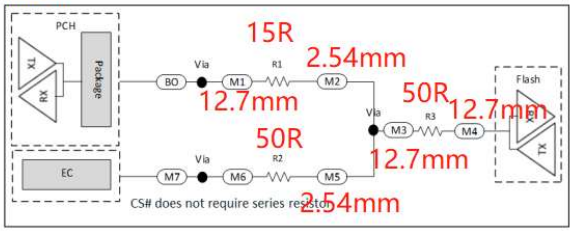
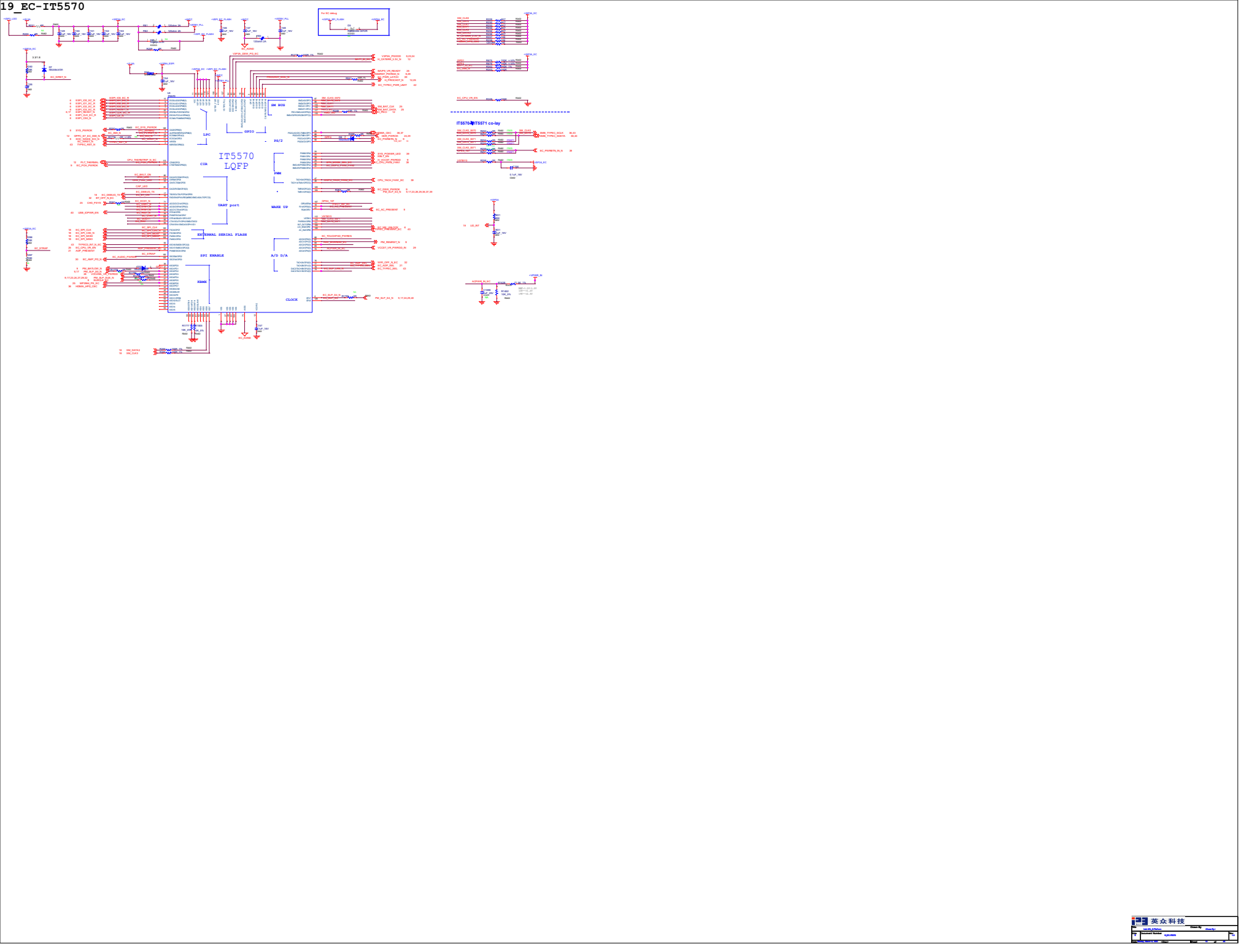


Table 443. 1-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing Notes

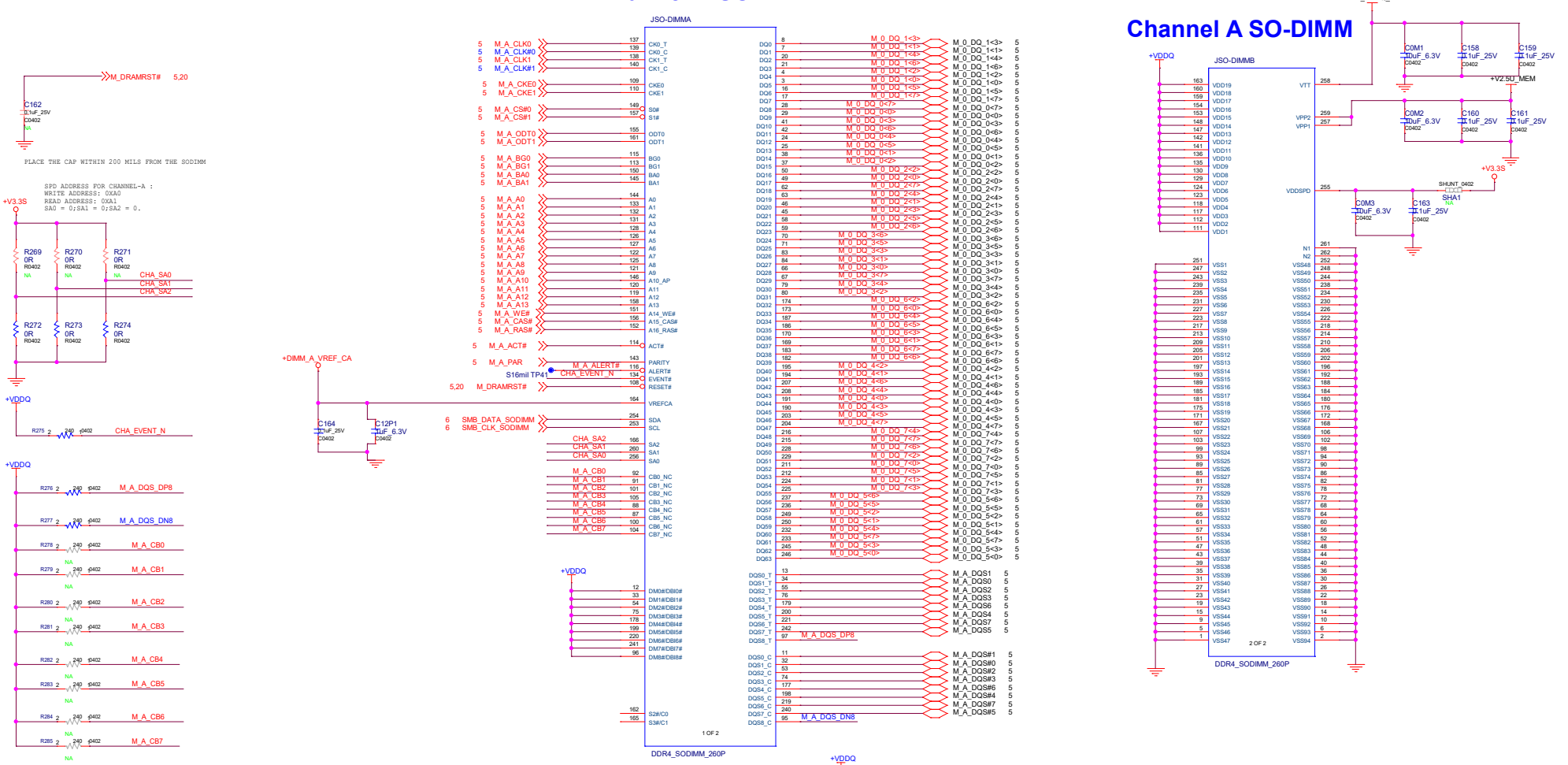
Note	Detail
Number of vias allowed	5
Reference plane	Continuous ground only
Max frequency	50 MHz
EC and PCH branch requirement	Delta between M1 + M2 and M5 + M6 shall not exceed 25.4 mm
R1	0 Ω placeholder for 1.8V and 15Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
R2	50 Ω for 1.8V and 50 Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3.
R3	33 Ω for 1.8V and 50 Ω for 3.3V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2 and SPI0_IO3
Minimum length	[1] M1, M3, M4 and M6: 12.7 mm [2] M2 and M5: 2.54 mm
Device AC timing characteristics	Data input setup time < 2 ns for 1.8V and 3.3V Data input hold time < 3 ns for 1.8V and 3.3V 1.5 ns < CLK to DATA output valid time < 7.5 ns for 1.8V 1.5 ns < CLK to DATA output valid time < 7 ns for 3.3V
Length matching between CLK and DATA/ CS# signals	12.7 mm
Trace spacing between DATA and DATA signals	0.250 mm
Trace spacing between CLK and DATA/ other signals	0.375 mm
Signal name/ list	SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_IO2, SPI0_IO3, SPI0_CS[0:2]#

19_EC-IT5570

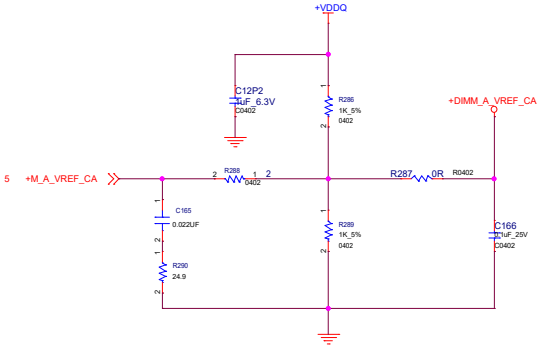

IT5570
LQFP
LPC
GPIO
SM BUS
PS/2
CIR
UART port
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMS
PWM
WAKE UP
A/D D/A
CLOCK
IT5570&IT5571 co-lay

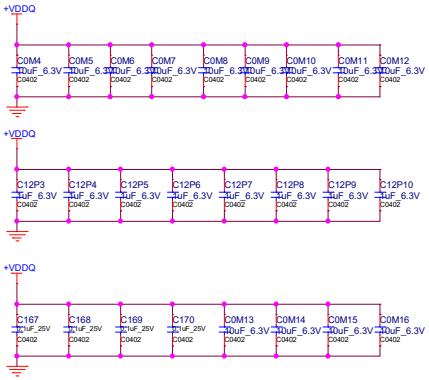
20_DDR4- CH-A

Channel A SO-DIMM

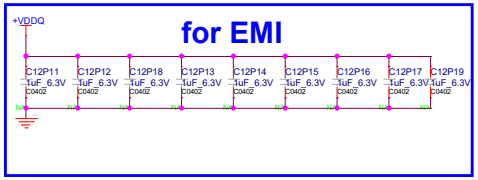


Channel A SO-DIMM



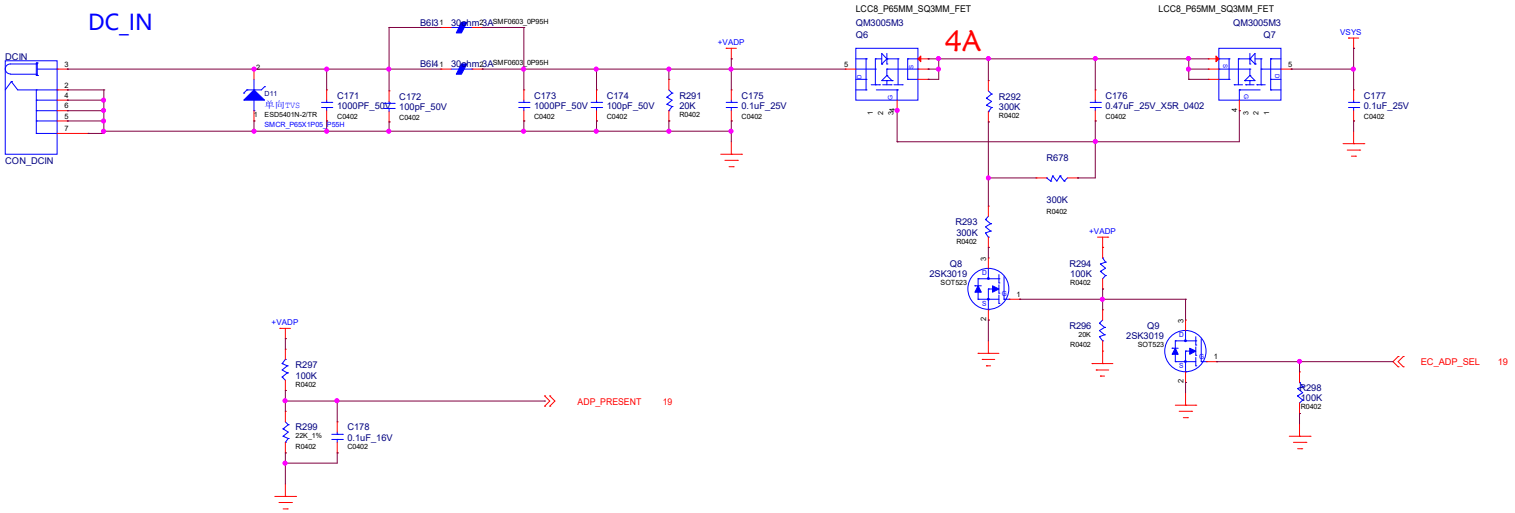


for EMI

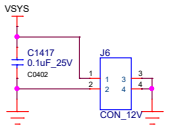


Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 20_DDR4- CH-A		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 20	of 45

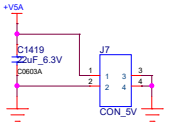
21_DC_IN



预留外部供电19V



预留5V



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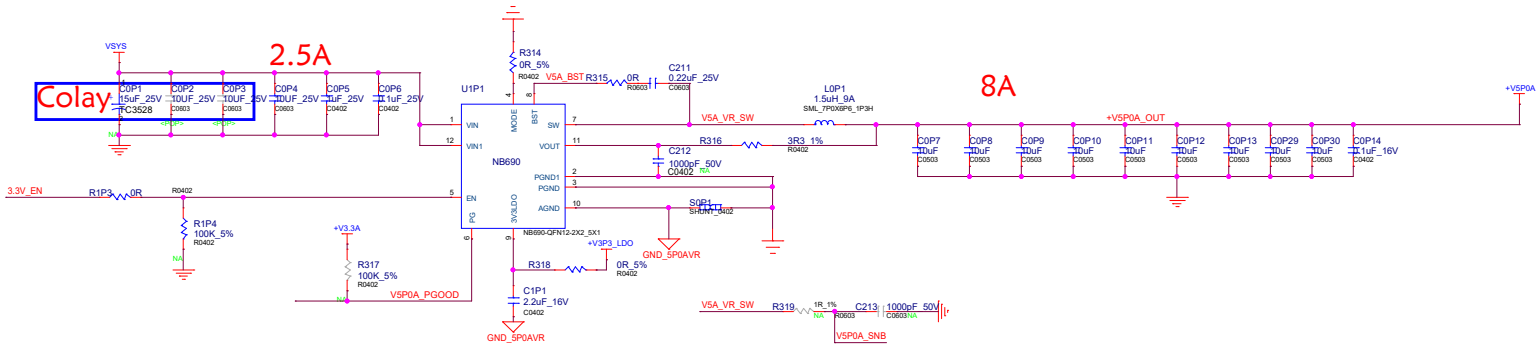
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 21_DC_IN		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 21 of 45	

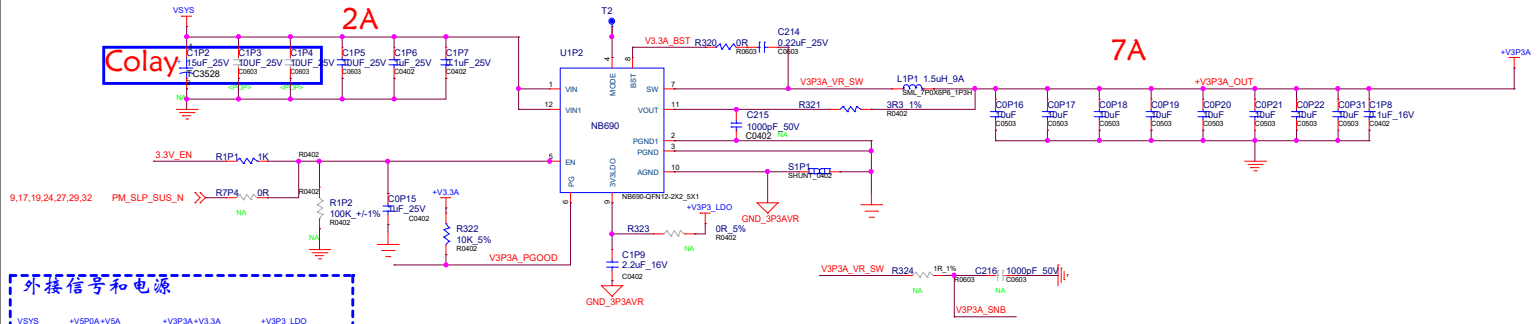
22_PWR_Charger&BAT

23_PWR_+5V/+3V/SX/RTC

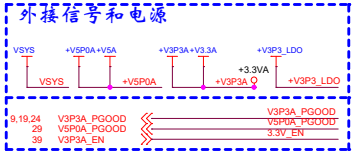
+V5P0A



+V3P3A

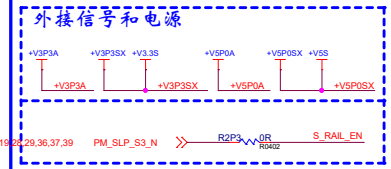


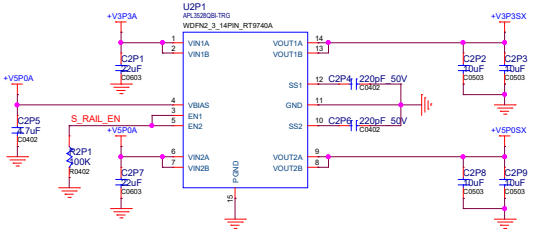
外接信号和电源



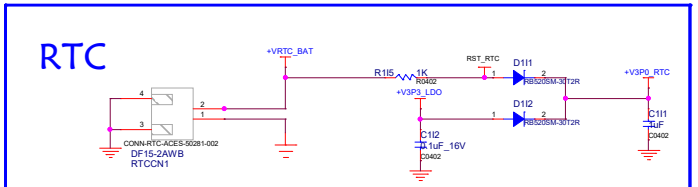
S电

外接信号和电源





RTC



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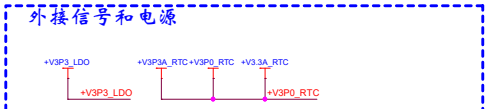

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Size C	Document Number 23_PWR_+5V/+3V/SX/RTC		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 23 of 45	

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24_PWR_+1.8V/VDD_MEM

+V1P8A

3A

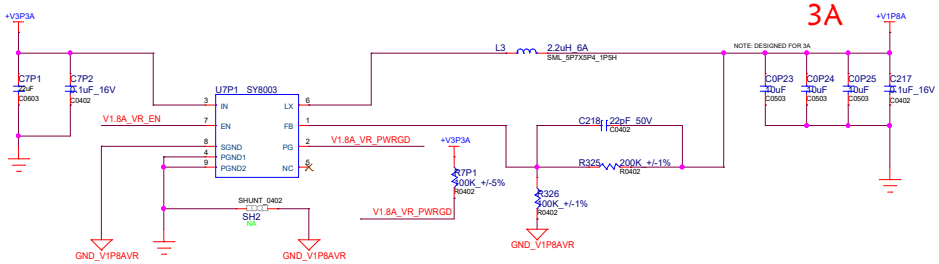
外接信号和电源

+V3P3A +V5P0A +V1P8A +V1P8A

27 V1P8A_PWRGD

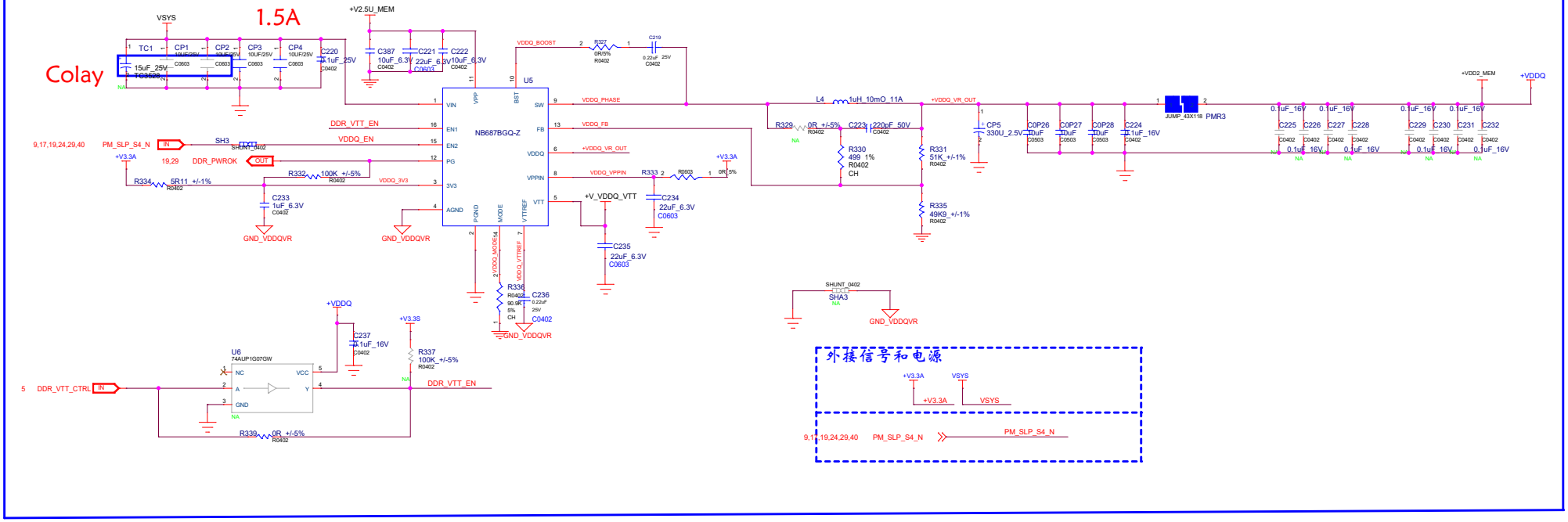
9,19,23 V3P3A_PGOOD

9,17,19,23,27,29,32 PM_SLP_SUS_N



Colay

1.5A

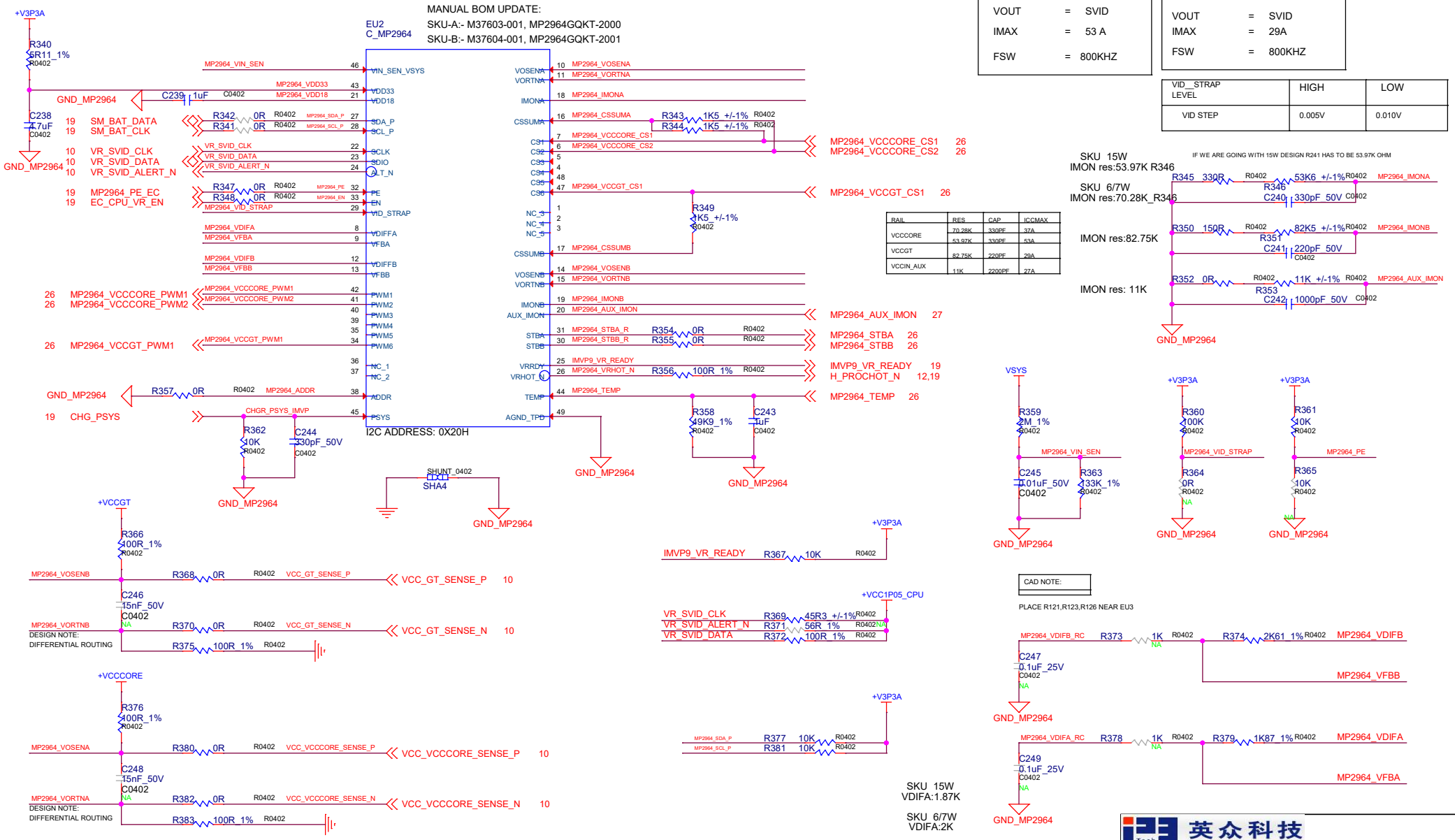


外接信号和电源

+V3.3A VSYS

9,17,19,24,29,40 PM_SLP_S4_N

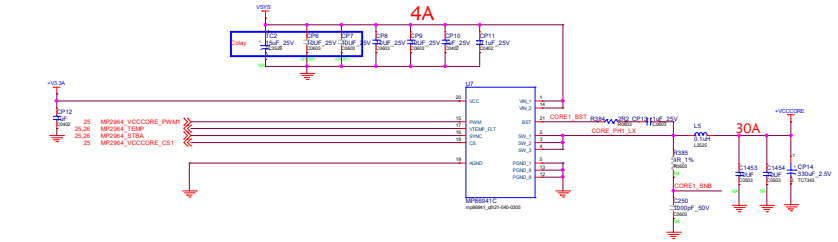
25_PWR_IMVP CONTROLLER

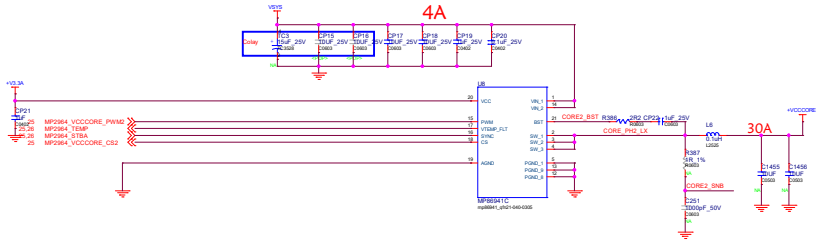


RAIL	RES	CAP	ICCMAX
VCCCORE	70.28K	330PF	37A
	53.97K	330PF	53A
VCCGT	82.75K	220PF	29A
VCCIN_AUX	11K	2200PF	27A

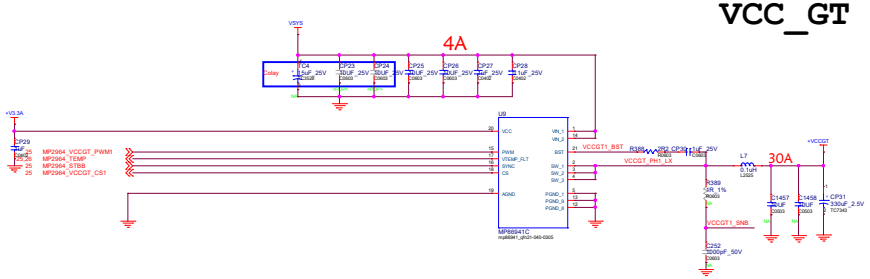
Title	Drawn By
Intel ADL_N Platform	<Drawn By>
Size: B	Document Number: 25_PWR_IMVP CONTROLLER	Rev: 1.0
Date: Monday, March 14, 2022 <Doc>	Sheet 25 of 45

VCC_CORE

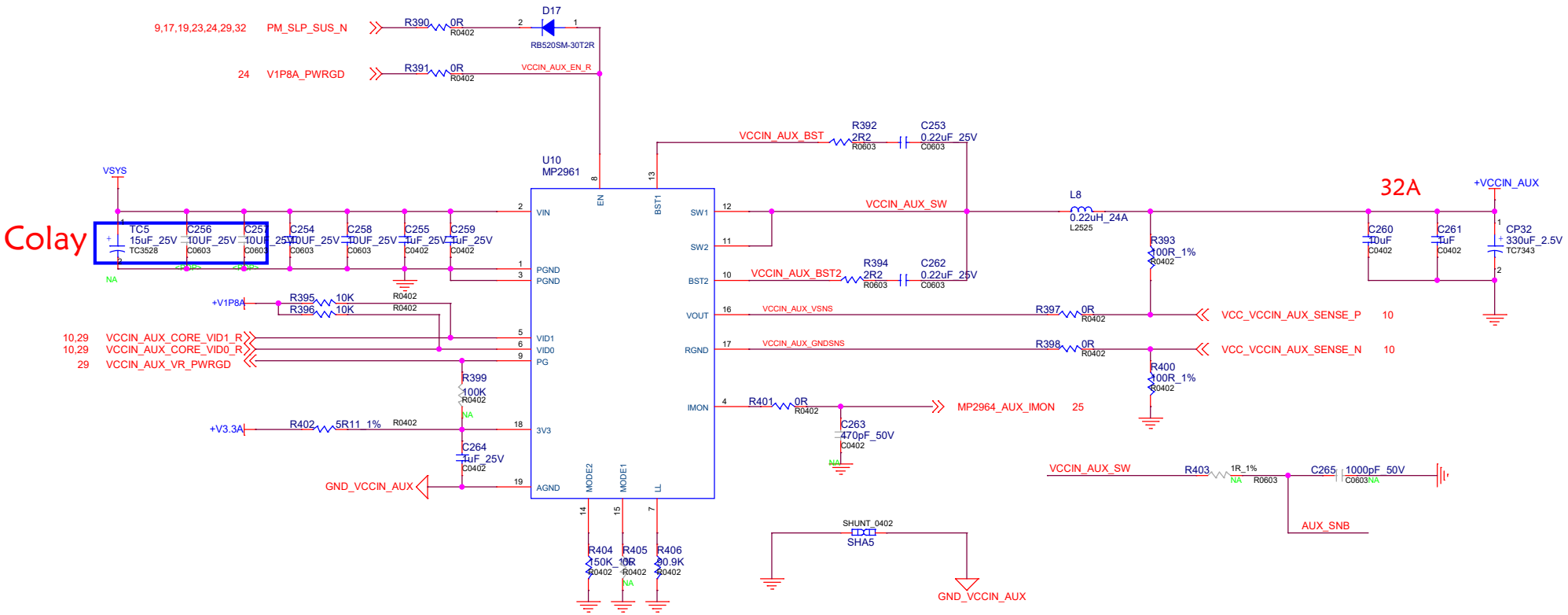




VCC_GT



27_PWR_VCCIN_AUX



PARAMETER	SETTING
OUTPUT VOLTAGE	1.8V
LOAD CURRENT	14A
OCP	16A/PHASE
FREQUENCY	800KHZ
DC_LL	2.5MILLI OHM

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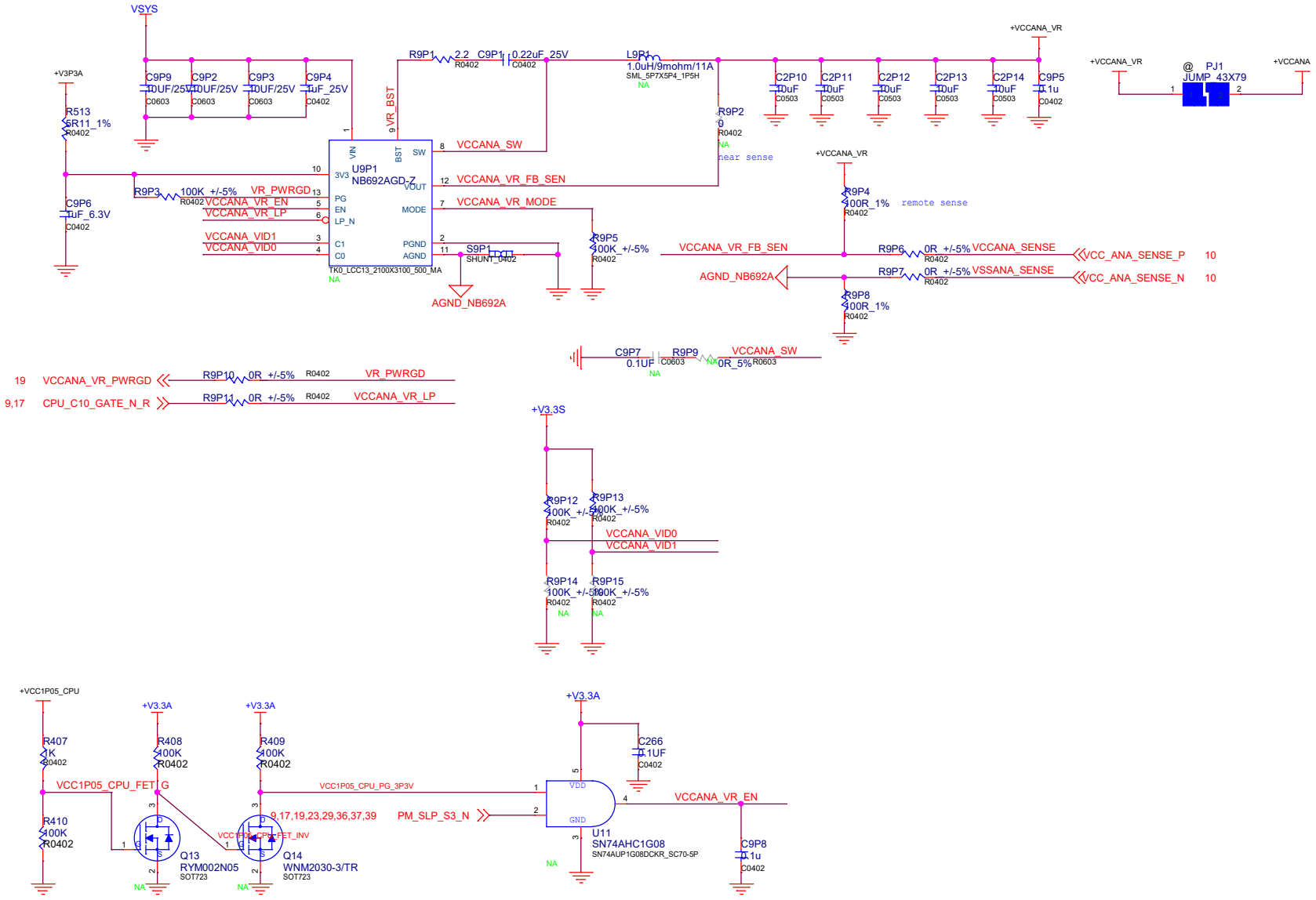
Title: Intel ADL_N Platform	Drawn By: <Drawn By>	
Size: B	Document Number: 27_PWR_VCCIN_AUX	Rev: 1.0
Date: Monday, March 14, 2022 <Doc>	Sheet 27 of 45	

28_VCCANA POWER

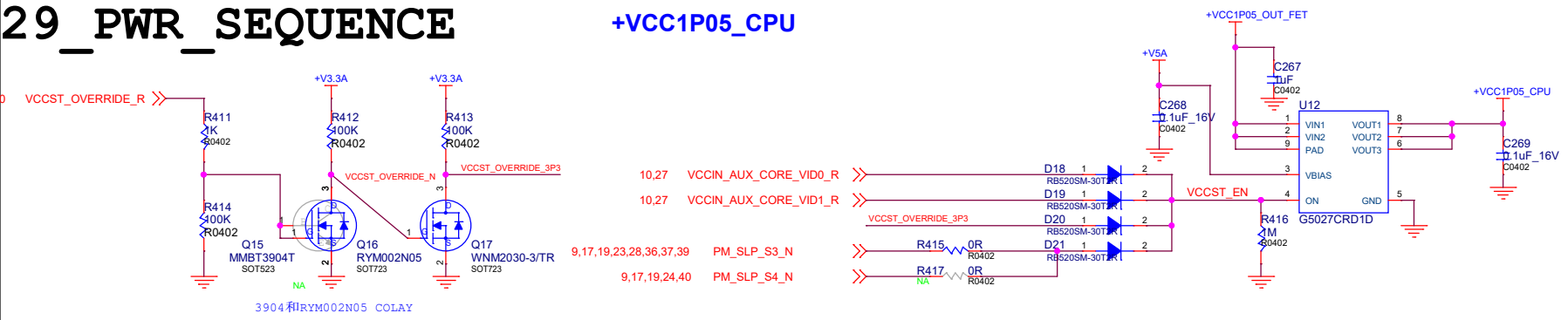
VCCANA	
VOUT	1.05V
SWITCHING FREQUENCY	750 KHZ
ICC MAX	3.6A
VR/MOSFET MPN	NB692D
INDUCTOR MPN	TMPC0315H-1R0MG
INDUCTOR IRMS	3.6A
INDUCTOR ISAT	5.8 A
INDUCTOR DCR(TYP)	41 MILLI OHM



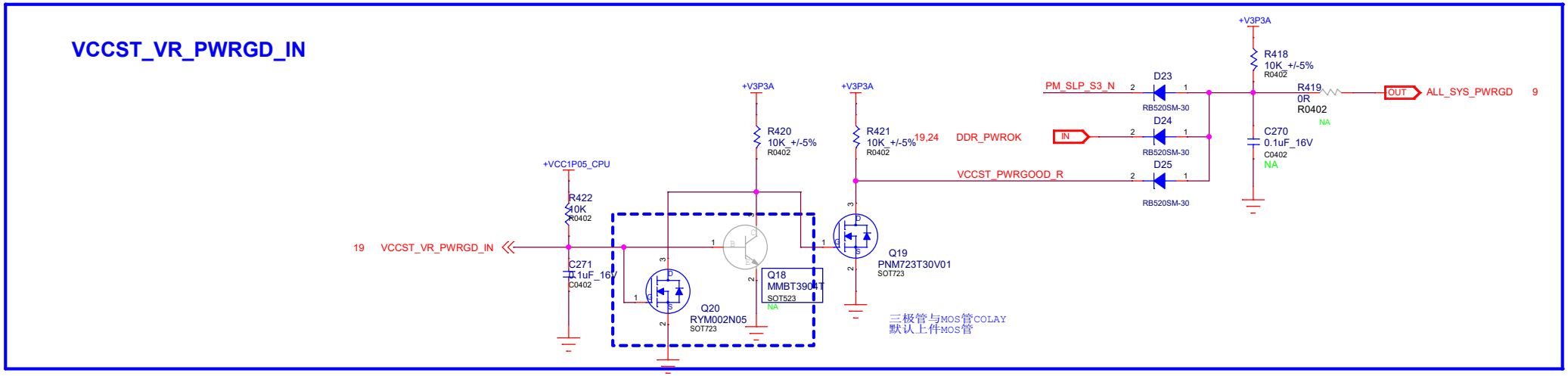
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size B	Document Number 28_VCCANA POWER		Rev 1.0
Date: Monday, March 14, 2022 <Doc>		Sheet 28 of 45	

29_PWR_SEQUENCE

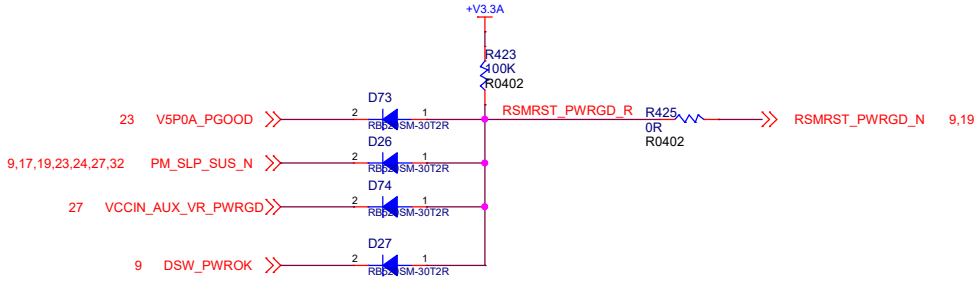
+VCC1P05_CPU



VCCST_VR_PWRGD_IN

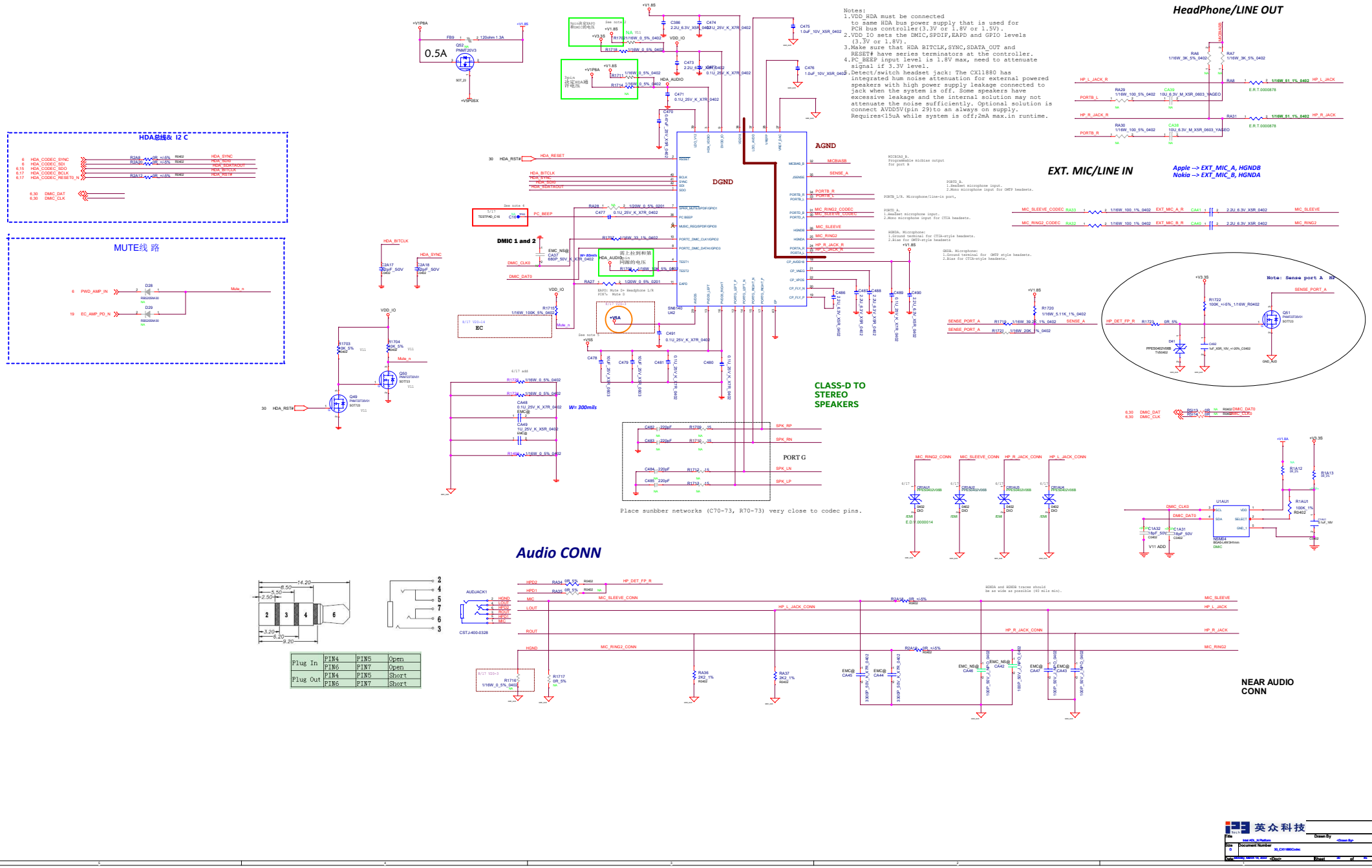


RSMRST PWRGD



Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size B	Document Number 29_PWR_SEQUENCE		Rev 1.0
Date Monday, March 14, 2022 <Doc>		Sheet 29 of 45	

30_SN6140_Codec



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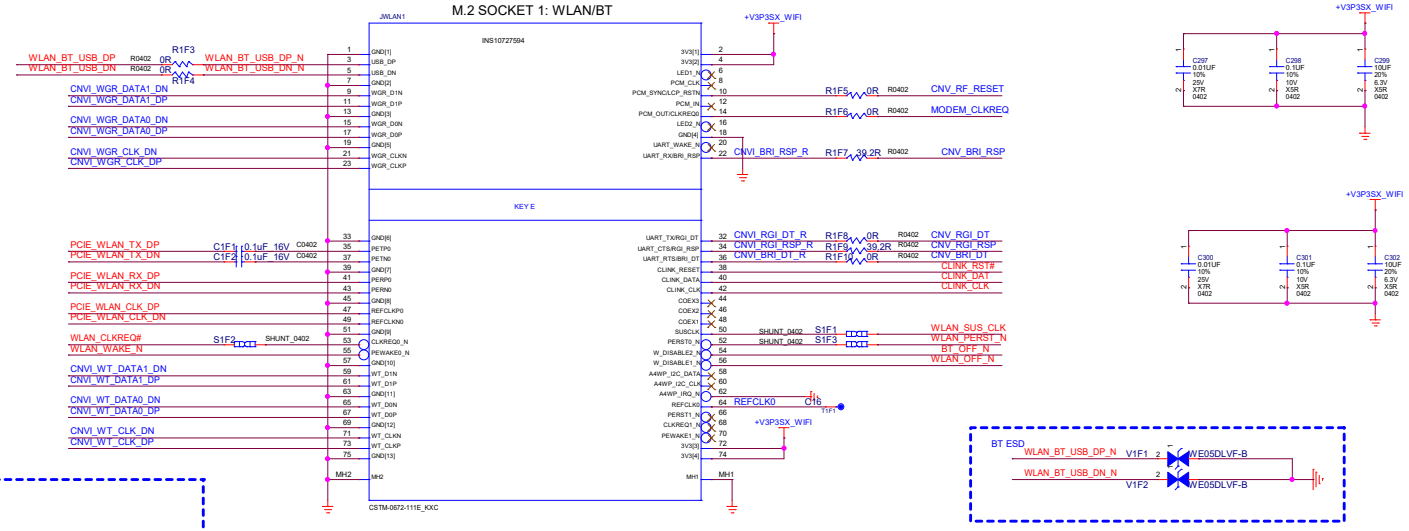
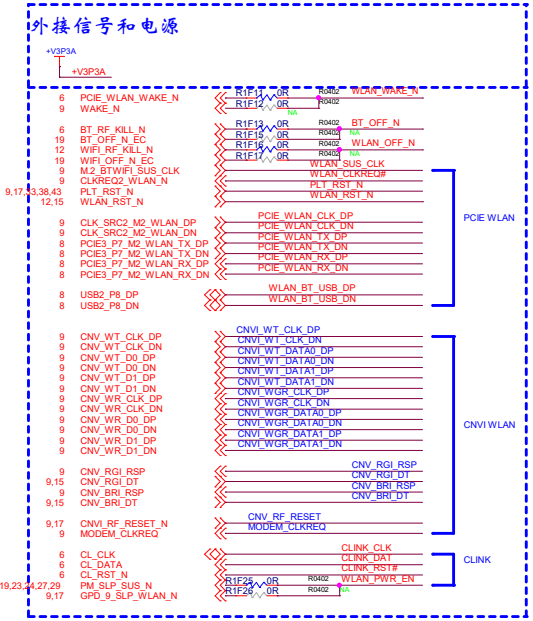
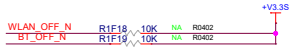
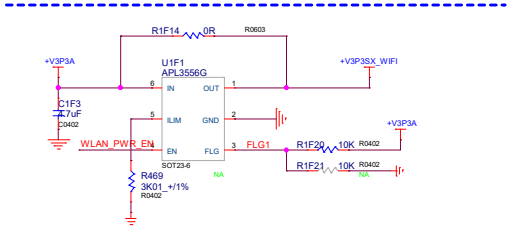
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size: Custom	Document Number: 31_NA		Rev: 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 31 of 45	

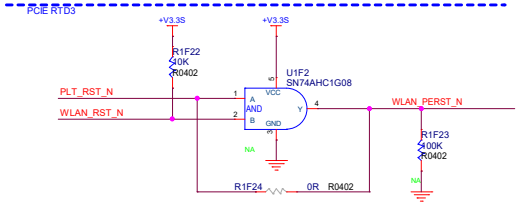
32_WLAN_module





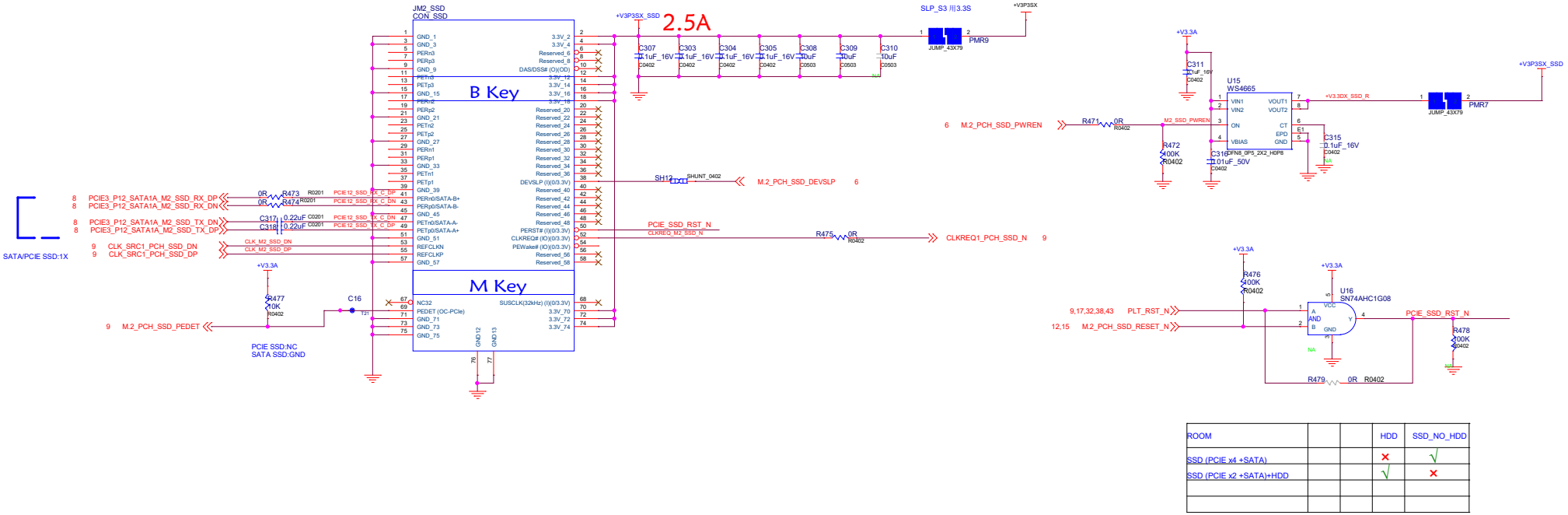






Title	Intel ADL_N Platform	Drawn By <Drawn By>
Size C	Document Number 32_WLAN_module	Rev 1.0
Date: Monday, March 14, 2022 <Doc>	Sheet 32 of 45	

33_CON_M.2_SSD(M)



ROOM			HDD	SSD_NO_HDD
SSD (PCIE x4 +SATA)			×	√
SSD (PCIE x2 +SATA)+HDD			√	×

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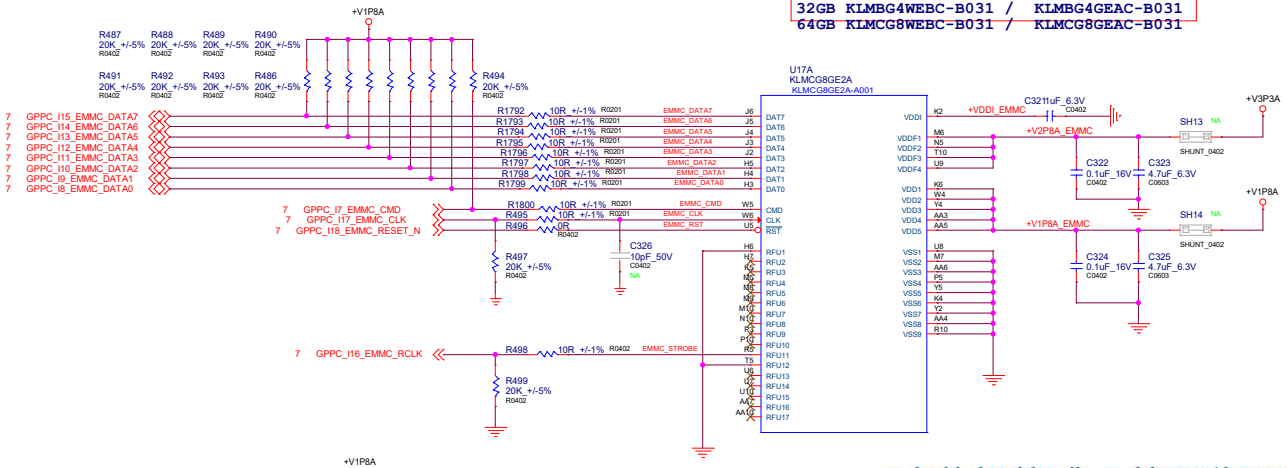
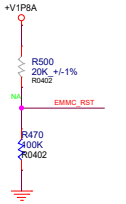
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 33_CON_M.2_SSD(M)		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 33 of 45	

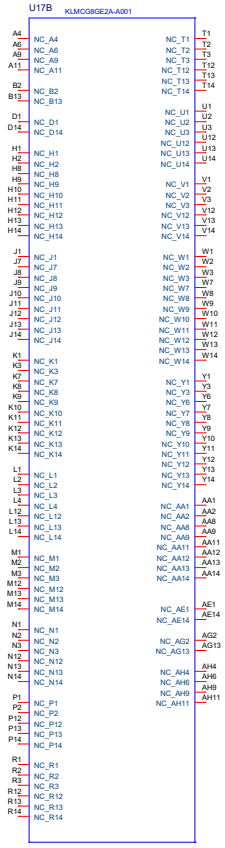
34_EMMC

EMMC

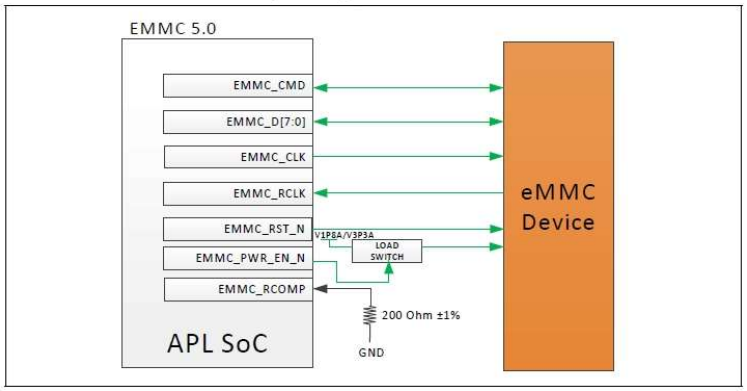
eMMC AVL:
Samsung
16GB KLMAG2WEMB-B031 / KLMAG2GEAC-B031
32GB KLMBG4WEBC-B031 / KLMBG4GEAC-B031
64GB KLMCG8WEBC-B031 / KLMCG8GEAC-B031

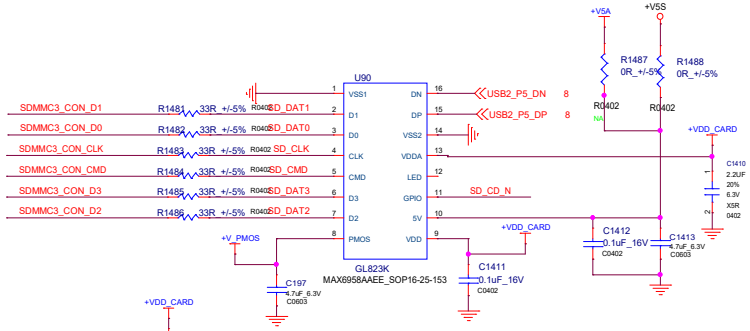


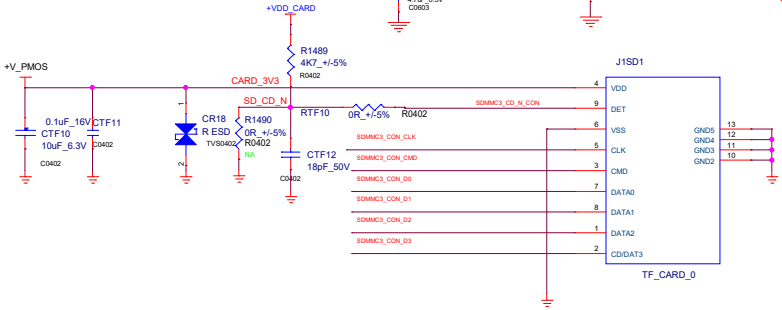


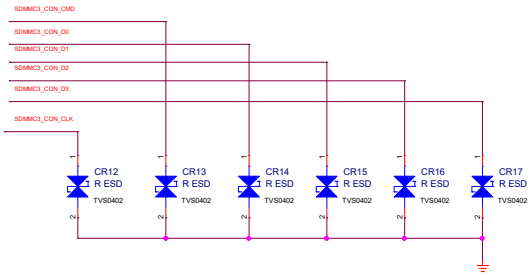


embedded MultiMedia Card (eMMC*) Interface









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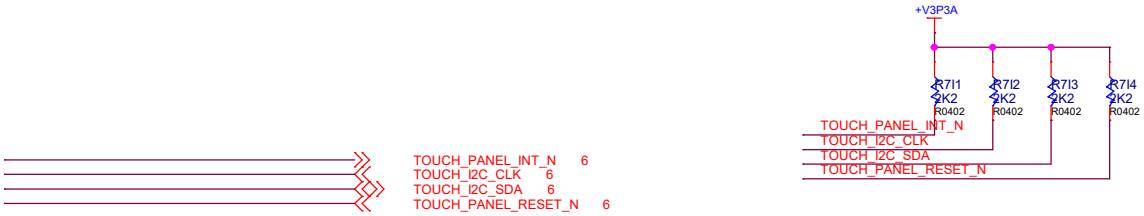
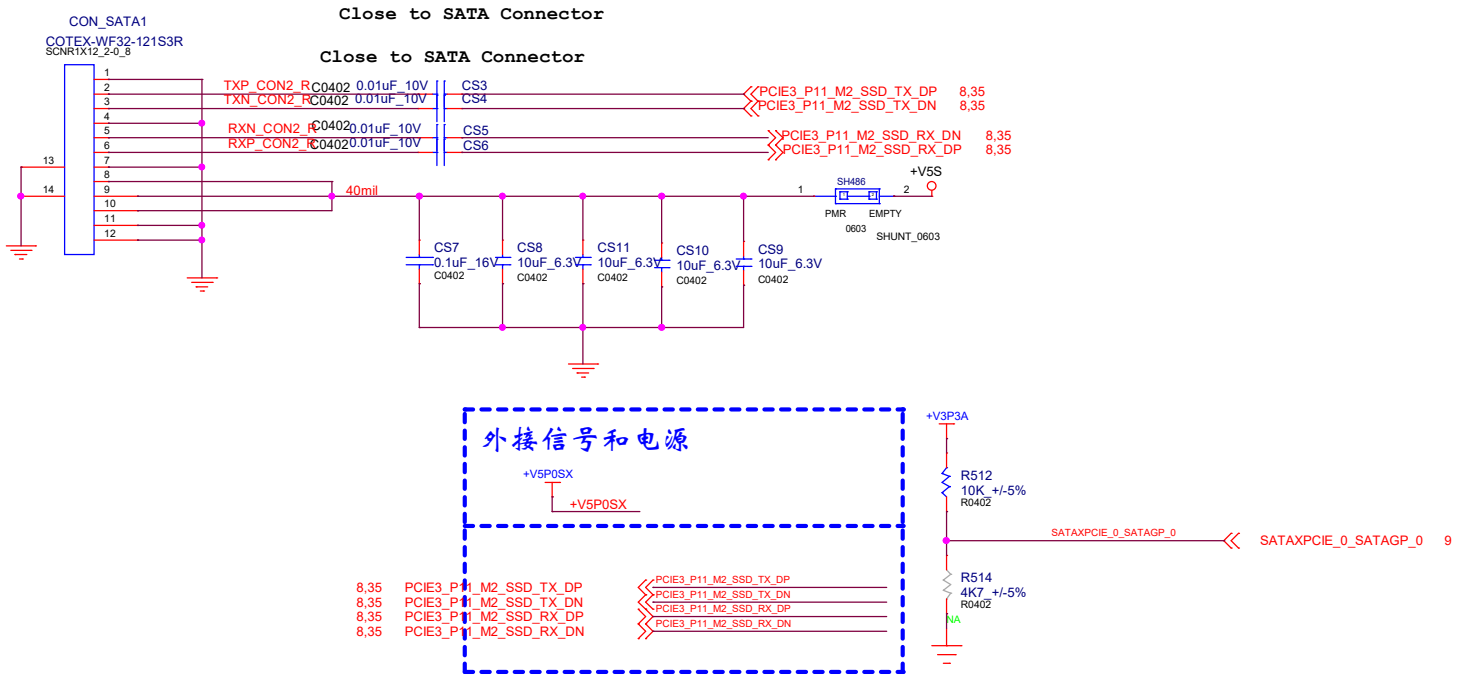
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 34_EMMC_TF		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 34	of 45

35_CON_DB_HDD_LAN

TOUCH PANEL/触摸屏



硬盘连接器/CON_HDD



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Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size B	Document Number 35_CON_HDD		Rev 1.0
Date Monday, March 14, 2022 <Doc>		Sheet 35 of 45	

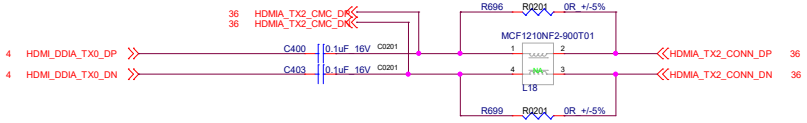
36_CON_LCD

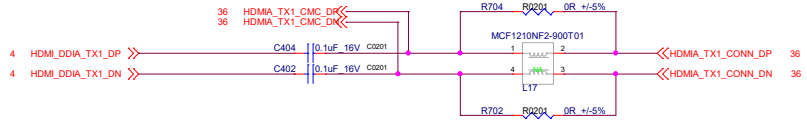
外接信号和电源

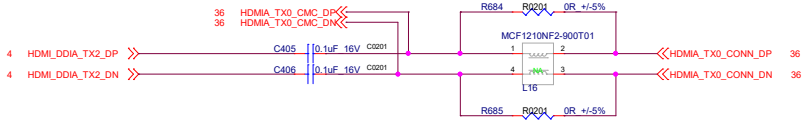
+V3P3SX

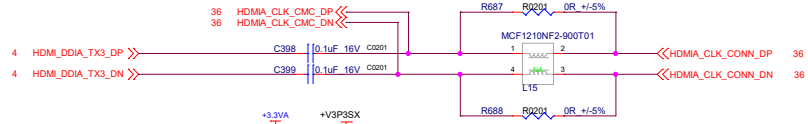
+V5P0SX

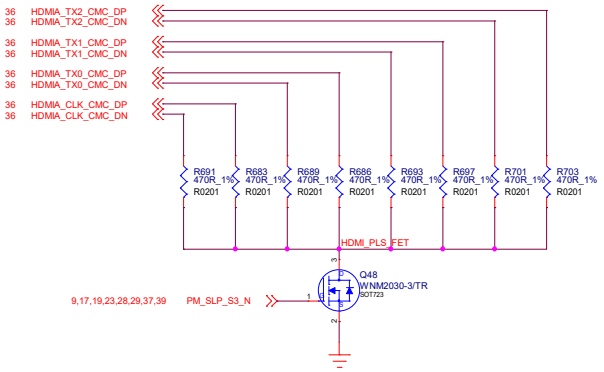
HDMI LEVEL SHIFTERS 1.65Gbps

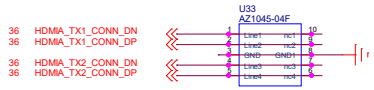


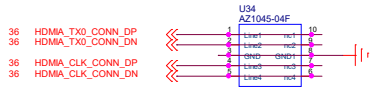


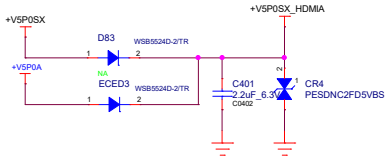


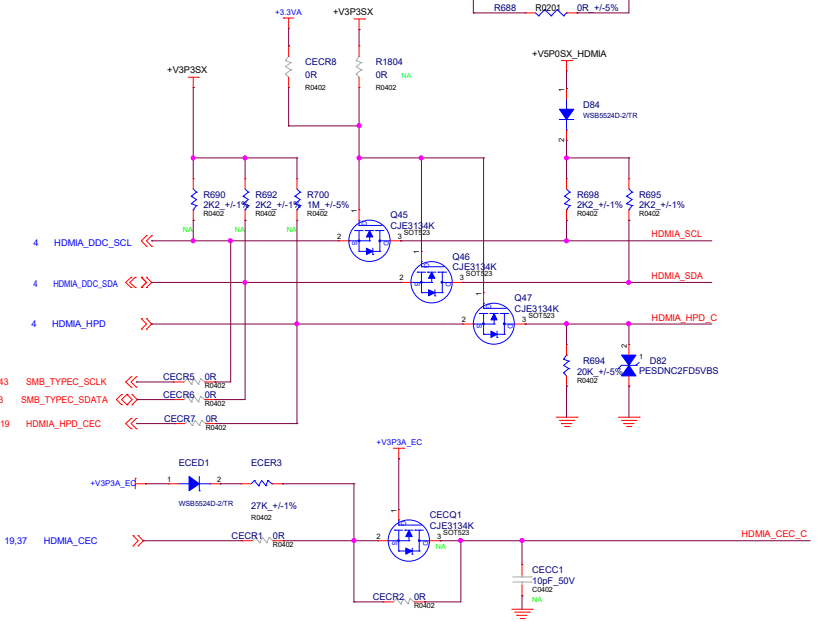




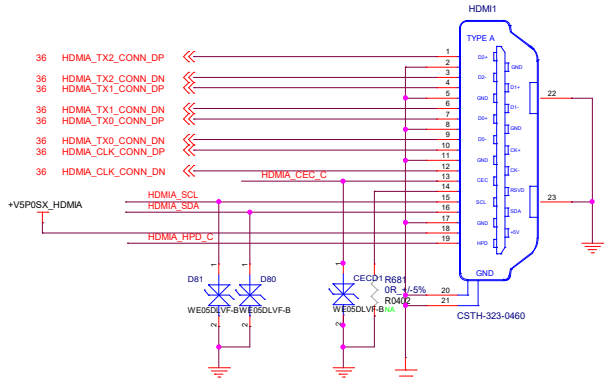








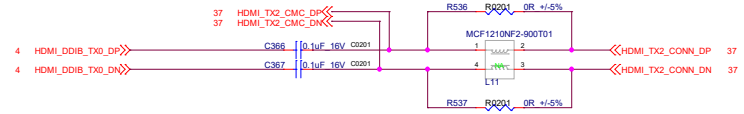
HDMI CONNECTOR

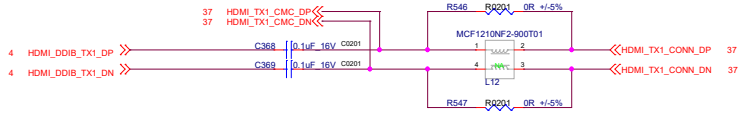


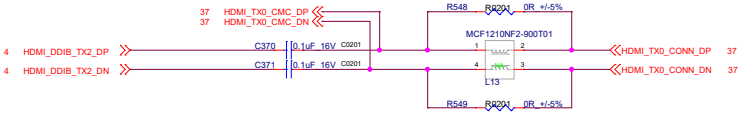
英众科技

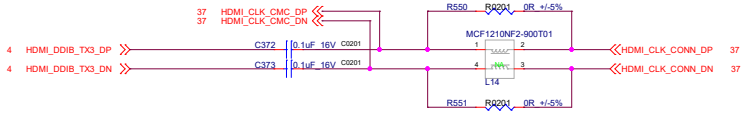
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 36_CON_HDMIA		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 36 of 45	

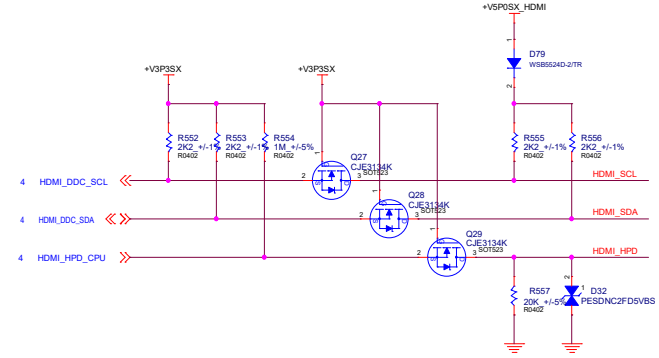
37_CON_HDMI



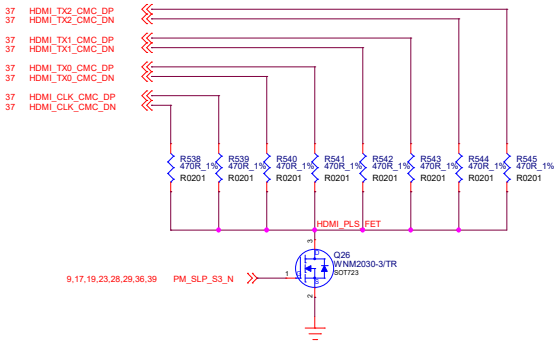


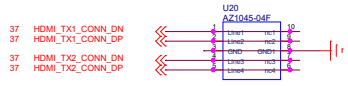


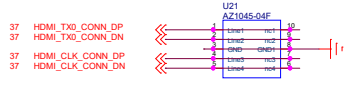


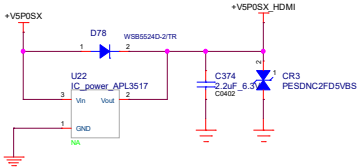


HDMI LEVEL SHIFTERS 1.65Gbps

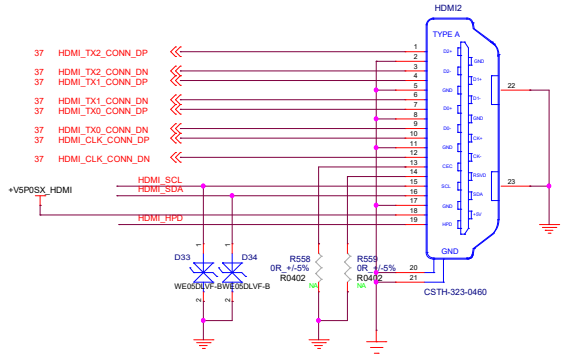








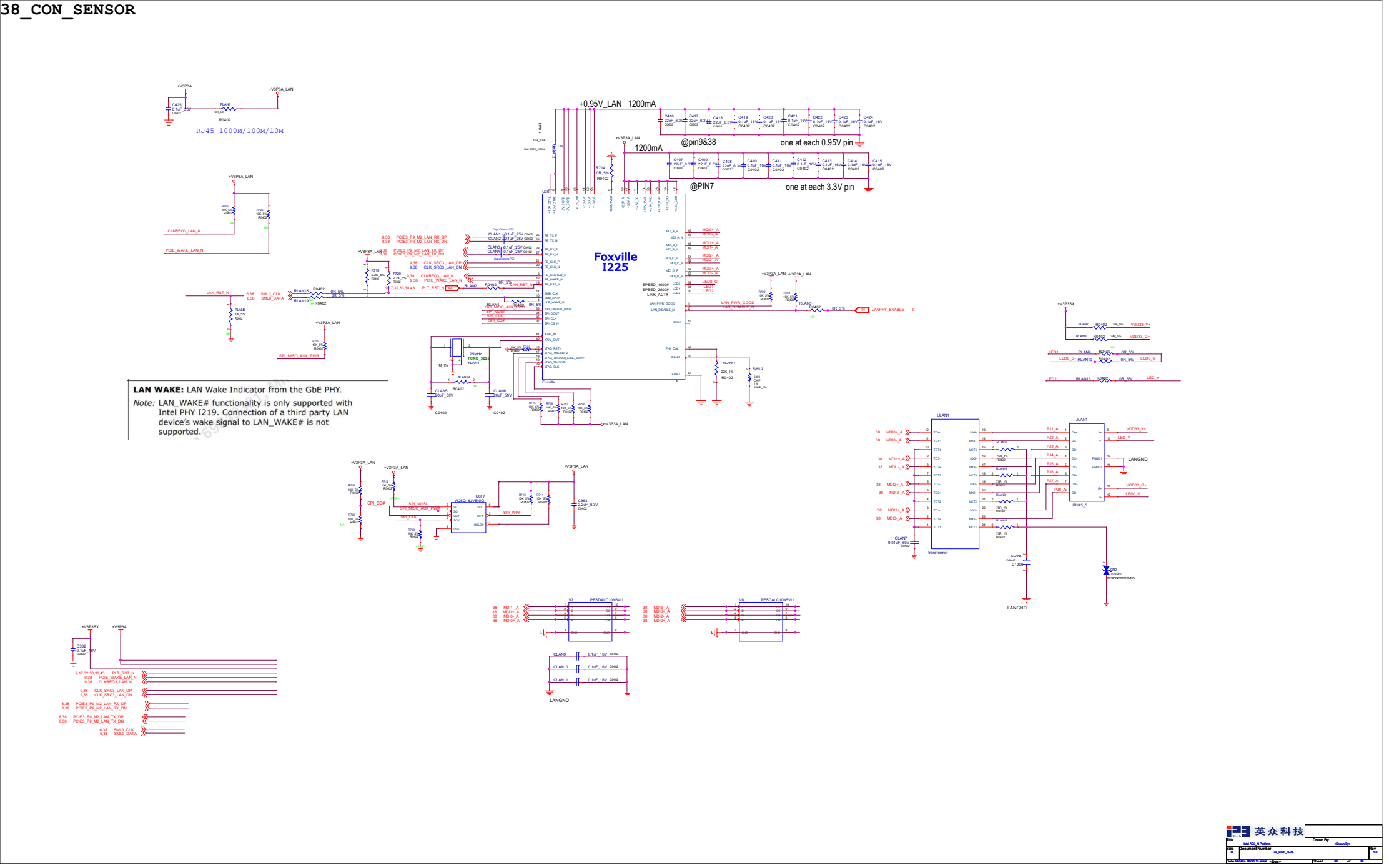
HDMI CONNECTOR



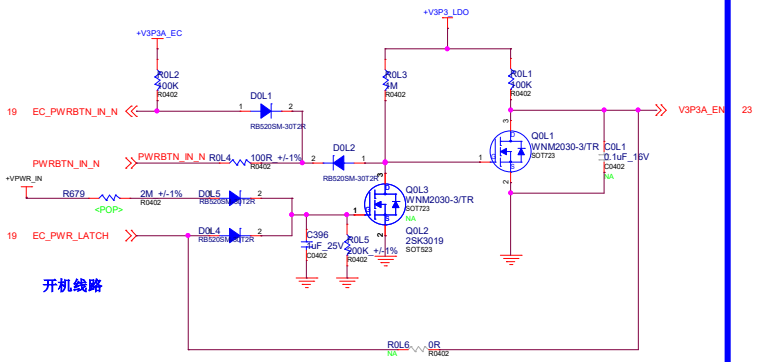
英众科技

Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size A2	Document Number 37_CON_HDMIB		Rev 1.0
Date Monday, March 14, 2022	<Doc>	Sheet 37 of 45	

38_CON_SENSOR

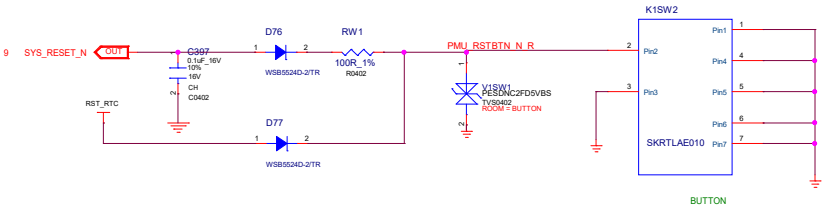


39_CON_KB&PWR_SW&LED



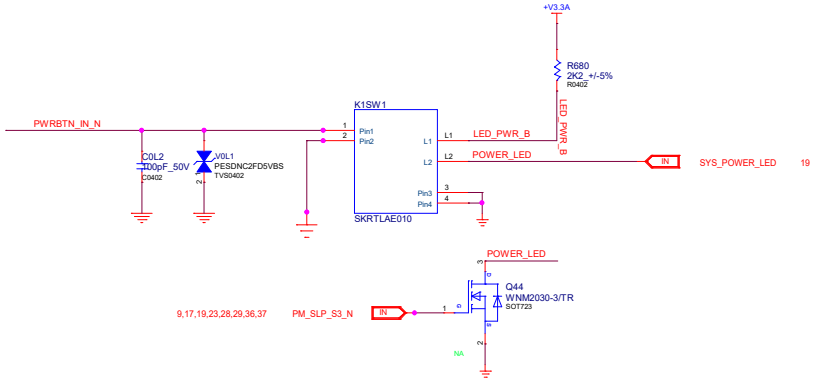
开机线路

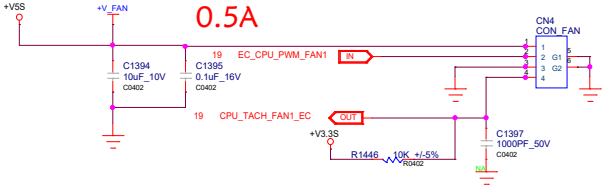
当强制关机时拉LOW

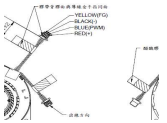


BUTTON

LED控制

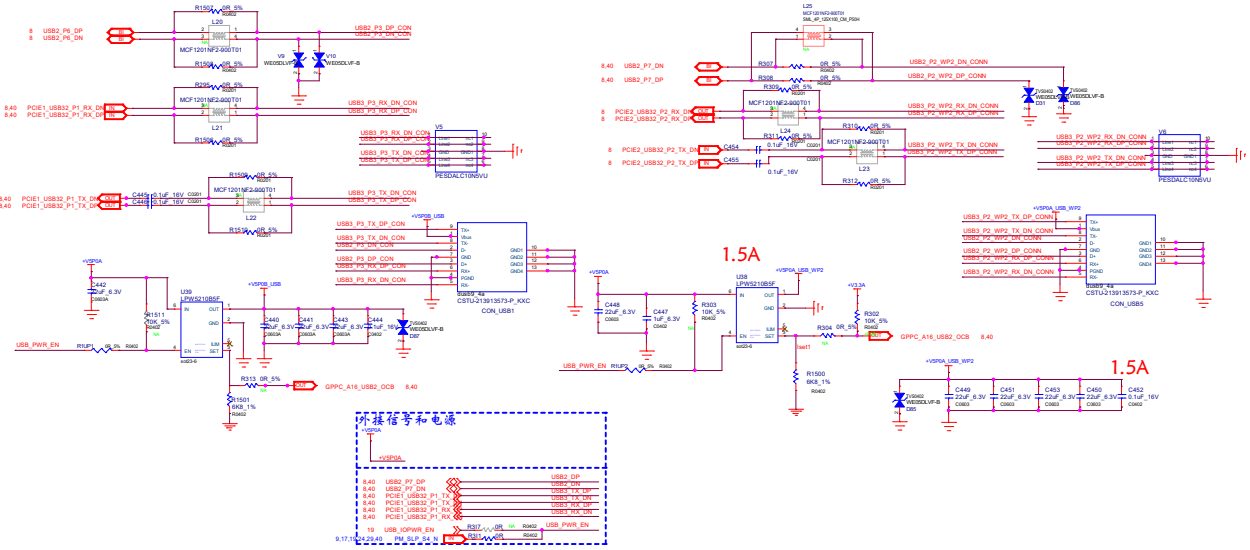




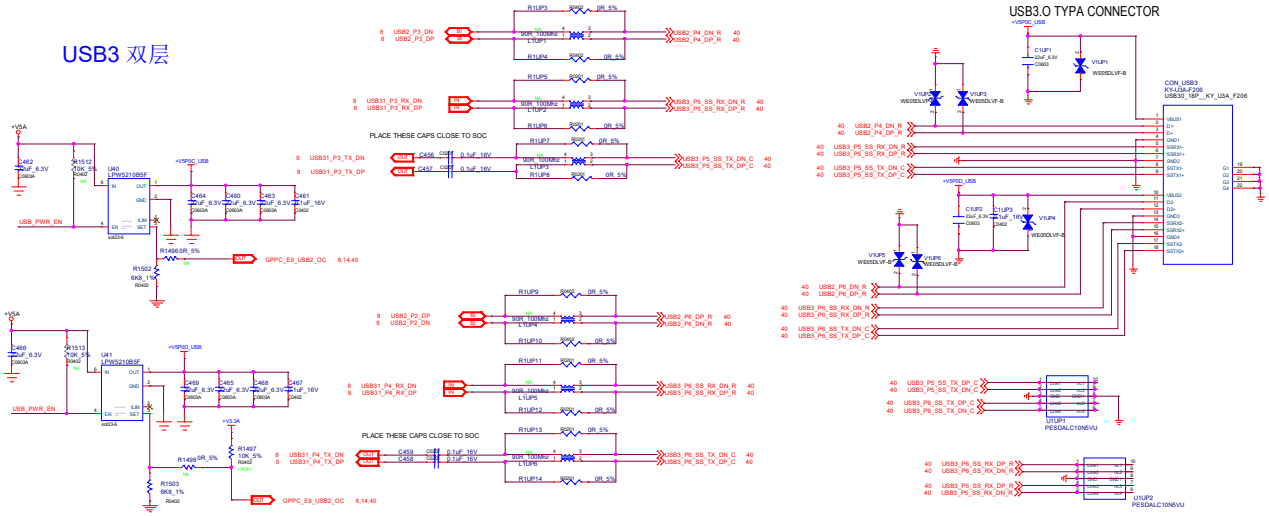


Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 39_PWR_SW&LED_FAN		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 39 of 45	

40_CON_USB30

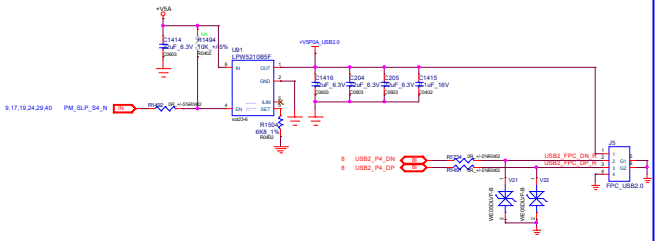


USB3 双层



USB3.0 TYPA CONNECTOR

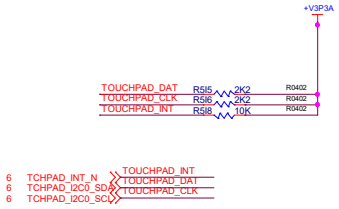
预留USB2.0（FPC）



英众科技

41_CON_TP&FP&FAN&KBLT&LID

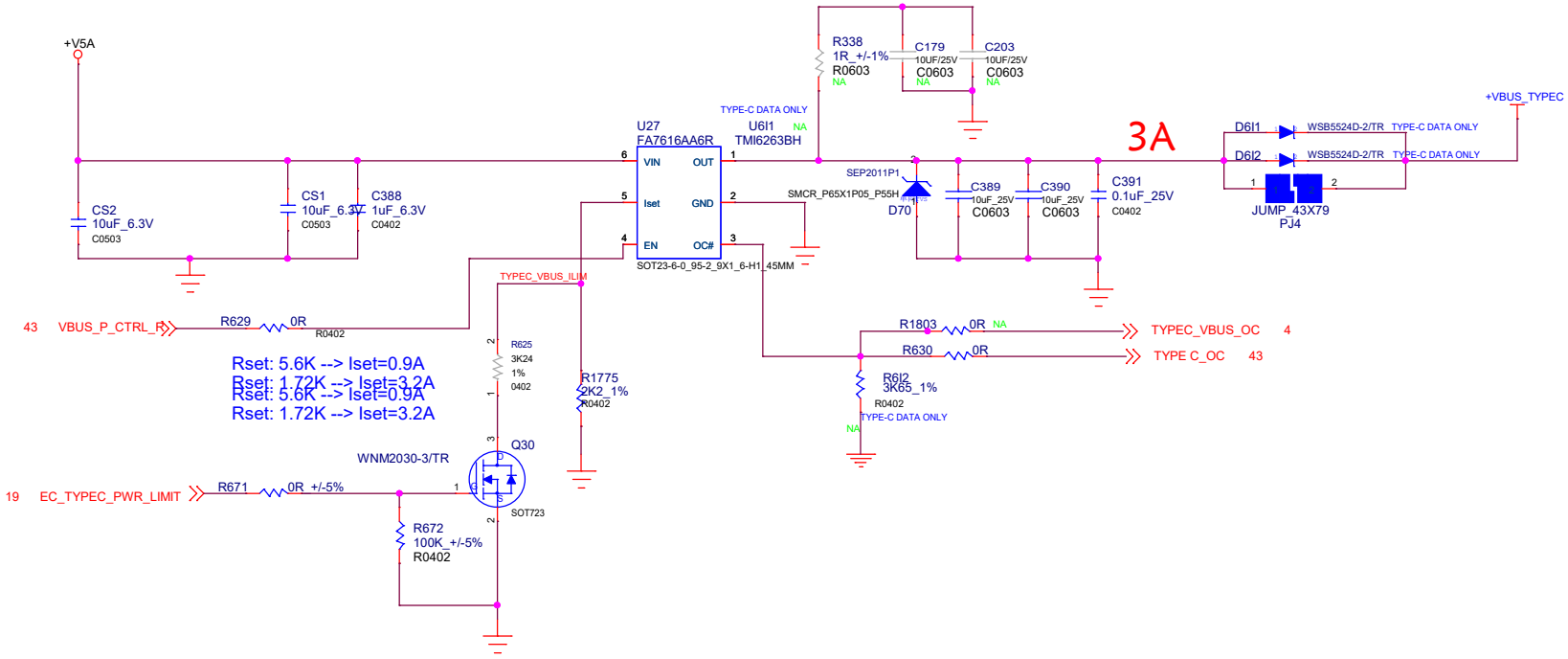
LID/霍尔传感器



英众科技

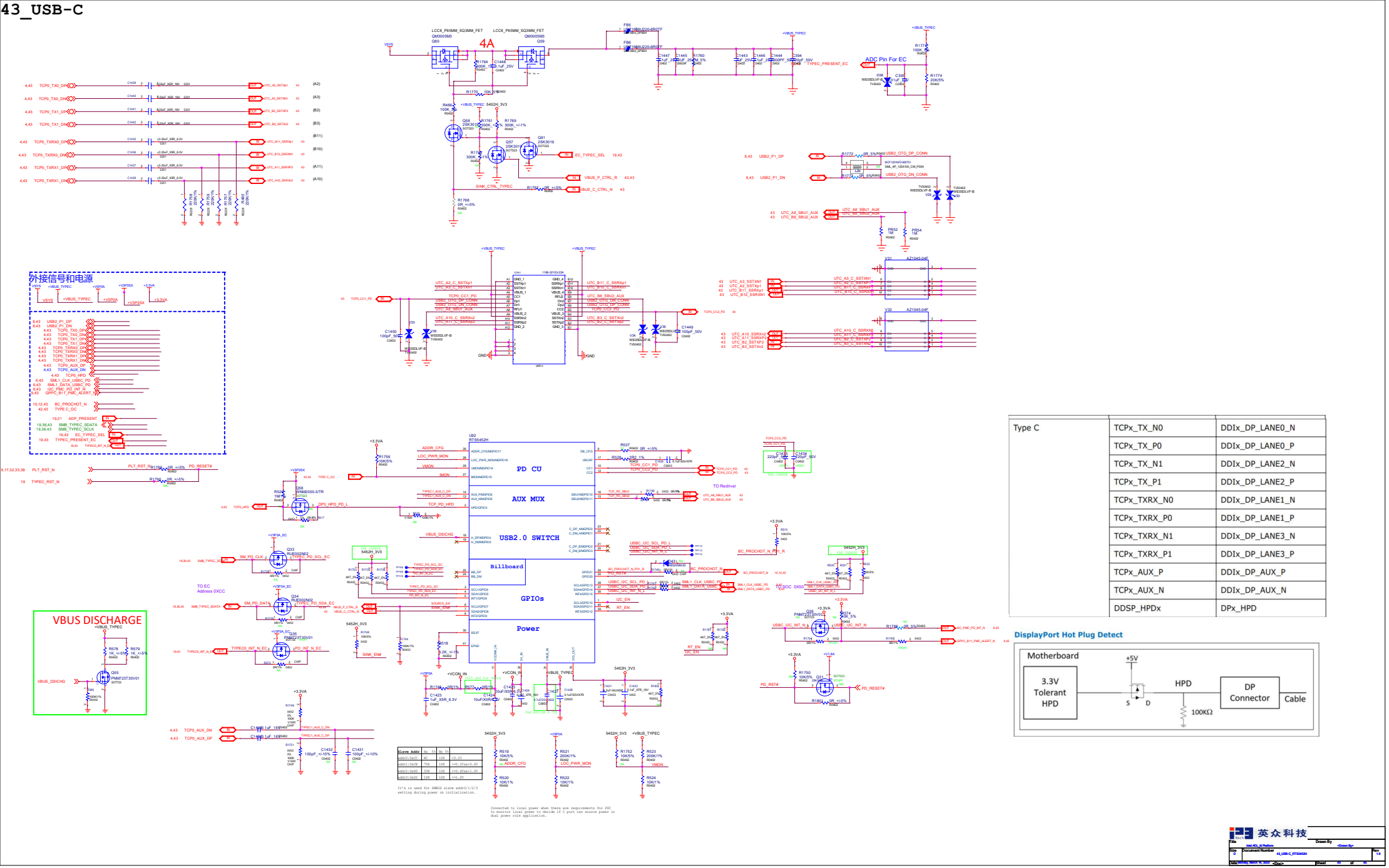
Title	Intel ADL_N Platform	Drawn By	<Drawn By>
Size C	Document Number 41_NA		Rev 1.0
Date: Monday, March 14, 2022	<Doc>	Sheet 41 of 45	

42_USB-C_Power



Title: Intel ADL_N Platform		Drawn By: <Drawn By>	
Size: B	Document Number: 42_USB-C_Power		Rev: 1.0
Date: Monday, March 14, 2022 <Doc>		Sheet 42 of 45	

43_USB-C



Type C	TCPx_TX_N0	DDIx_DP_LANE0_N
	TCPx_TX_P0	DDIx_DP_LANE0_P
	TCPx_TX_N1	DDIx_DP_LANE2_N
	TCPx_TX_P1	DDIx_DP_LANE2_P
	TCPx_TXRX_N0	DDIx_DP_LANE1_N
	TCPx_TXRX_P0	DDIx_DP_LANE1_P
	TCPx_TXRX_N1	DDIx_DP_LANE3_N
	TCPx_TXRX_P1	DDIx_DP_LANE3_P
	TCPx_AUX_P	DDIx_DP_AUX_P
	TCPx_AUX_N	DDIx_DP_AUX_N
	DDSP_HPDx	DPx_HPD

英众科技

V11 Changne list

Page 43: change to +3.3VA from +3.3VS, change to +V3P3SX from +3.3VS(EQ check issue)
Page 23: Q12 NA
Page 42: U6I2 NA
Page 23: R1P4 NA to ment NB690 operates in normal mode
Page 38: R705,R706 NA
Page 26: delete U2, U93,U94 colay,change U7,U8,U9 footprint to mp86941_qfn21-040-0305 from MP86941_QFN21_0D4_3X5_H0D8C
Page 25: mark R379 15W=1.87K, 6W/7W=2K from MPS advice
Page 26: reserve C1453~C1458
Page 39: reserve R0L6 to Q0L1 for EC to control 3P3A
Page 19: R242 net to BATT_ID_EC, EC PIN94 net to EC_SIN1
Page 44: R299 Change to 22K
Page 06: R13,R14 NA
Page 43: Q36,R1788,R574 NA, R1754,R1787 mount, R532 NA
Page 26: DEL +VCCANA_VR due to BIOS can enable FIVR to replace MBVR
(U9P1,L9P1,U11,Q13,Q14 NA)
Page 18: U0F1 change to 16M(W25Q128JVSIQ) from 32M
Page 21:Change C176 to 0.47uF from 0.1uF to delay VSYS to 3ms
Page 36:Change Q47 PIN3 netname to HDMIA_HPD_C form HDMIA_HPD
Page 19:Change EC PIN85 PM_RSMRST_N to PIN67, PIN85 renet: HDMIA_CEC ,
DEL: R244,R246,RT_CHG1,RT_CPU1
Page 36: ADD CEC Circuit
Page 37: ADD CEC Circuit
Page 26: Change R384,R386,R388 to 2.2R from 0R to reduce SW voltage
Page 32: R1F23 NA duplication
Page 33: R478 NA duplication
Page 30: R1711 MOUNT,R1714 NA to ment vender request
Page 25: R342,R341 MOUNT for EC burn MPS FW

45_ME

CPU SCREW

H5
Hole

H6
Hole

H7
Hole

H8
Hole

SSD SCREW

H9
SSD_NUT_MAX
<POP>

WIFI NUT

H14
WIFI_NUT
M.T.N.0000046
NUT_C6_0D3_1

ME Hole

H3
02AP0974
C6_00D2_50
NA

H13
02AP0974
C6_00D2_50
NA

H11
02AP0974
C6_00D2_50
NA

H1
02AP0974
C6_00D2_50
NA

MP1
PingBiZhao

MPCB1
PMIC RAM CPU
PCB

MPCBA1
PMIC RAM CPU
PCBA

MK1
FMARKS
FIDUCIAL_40_PACKAGE
NA

MK2
FMARKS
FIDUCIAL_40_PACKAGE
NA

MK3
FMARKS
FIDUCIAL_40_PACKAGE
NA

MK4
FMARKS
FIDUCIAL_40_PACKAGE
NA

英众科技

Title: Intel ADL_N Platform	Drawn By: <Drawn By>	
Size: B	Document Number: 45_ME	Rev: 1.0
Date: Monday, March 14, 2022 <Doc>	Sheet 45 of 45	