

# Project Name : MPC43

# Platform : INTEL COMPUTE MODULE

### PAGE CONTENT

1. INDEX
2. SYSTEM BLOCK
3. POWER DIAGRAM & SEQUENCE
4. CONN
5. EC
6. ECFLASH
7. Charging
8. TYPE-C PD
9. Type-C\_VBUS\_POWER
10. TYPE-C CONNECTOR
11. HDMI BD
12. FAN
13. CODEC(ALC269Q)/INT MIC/SPKR
14. EXT\_MIC
15. eDP CONN/CAMERA
16. HDMI
17. PWR SW
18. M.2/NGFF/SENSORS
19. TP/LED/Click-pad/USB
20. BATT IN
21. DC IN/Discharge/HOLE
22. 5VA/3.3VA/1.05VA
23. VCC SW/1.5V/HIGH-SPEED CAP
24. History

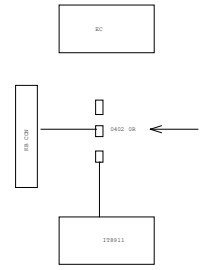
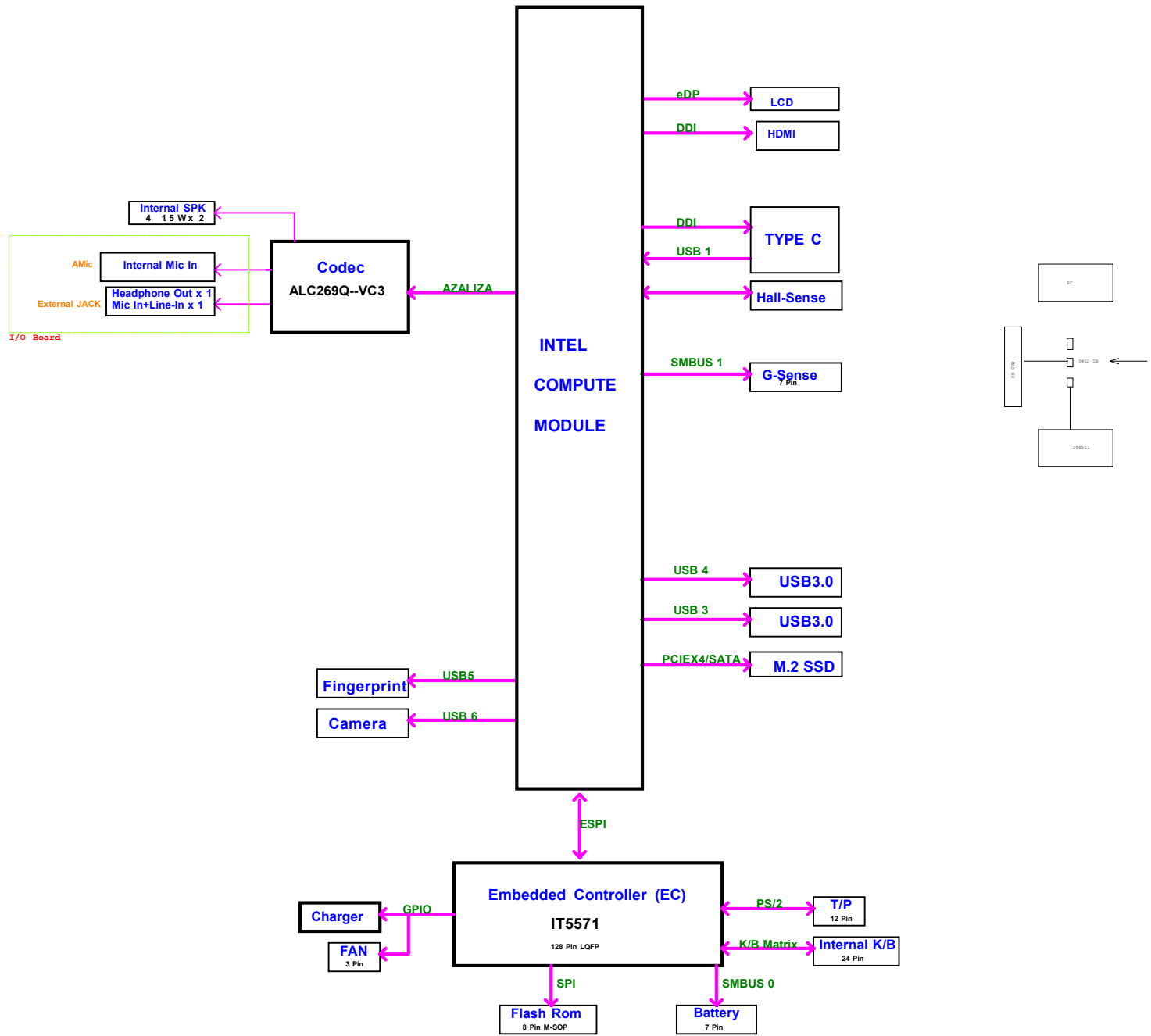
### M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

### Daughter Board Schematic Version Change List

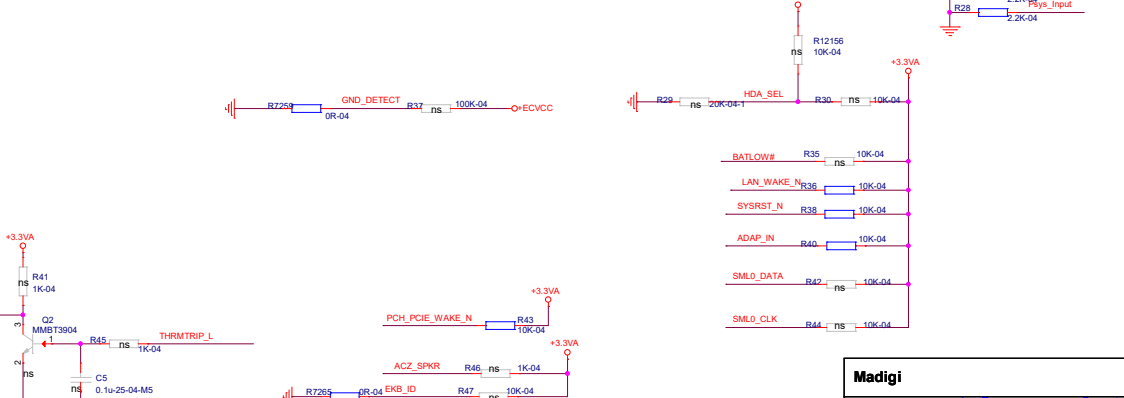
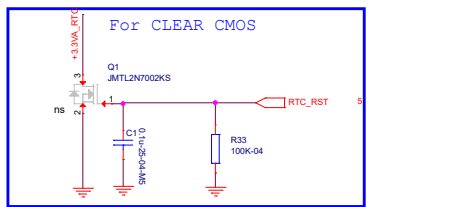
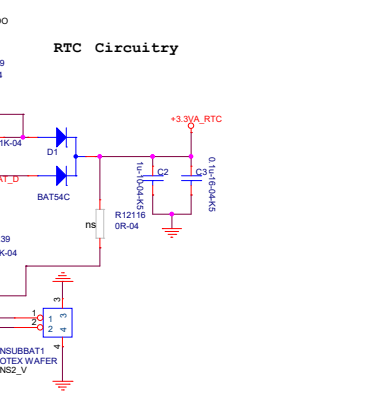
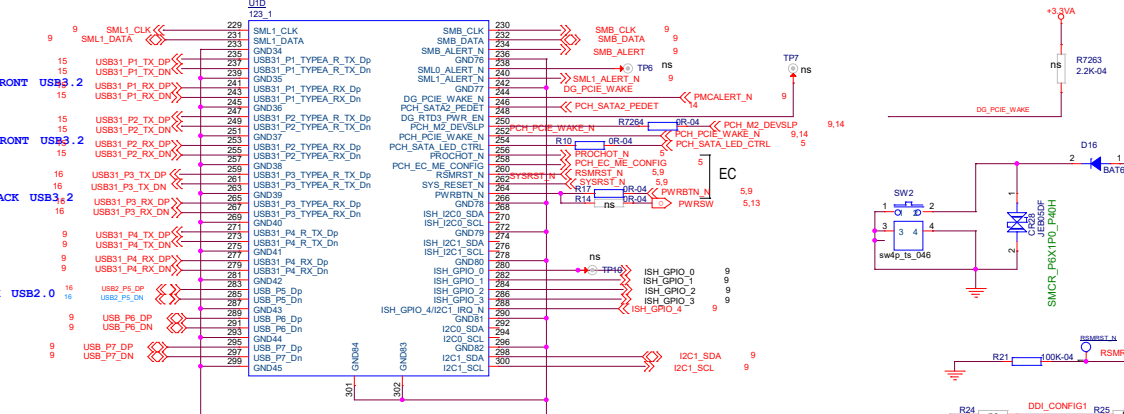
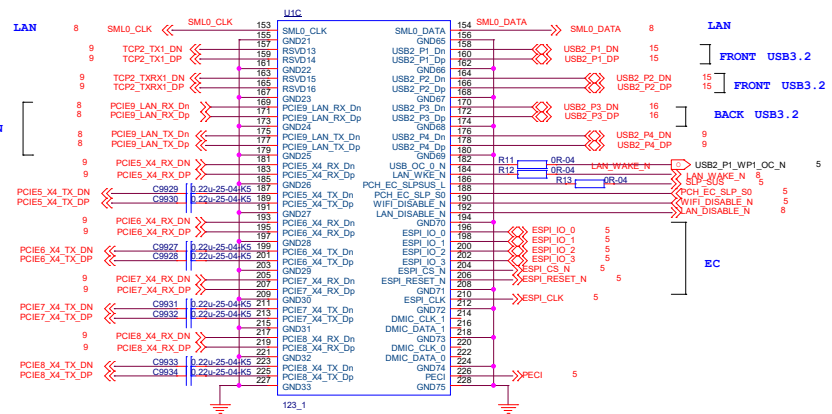
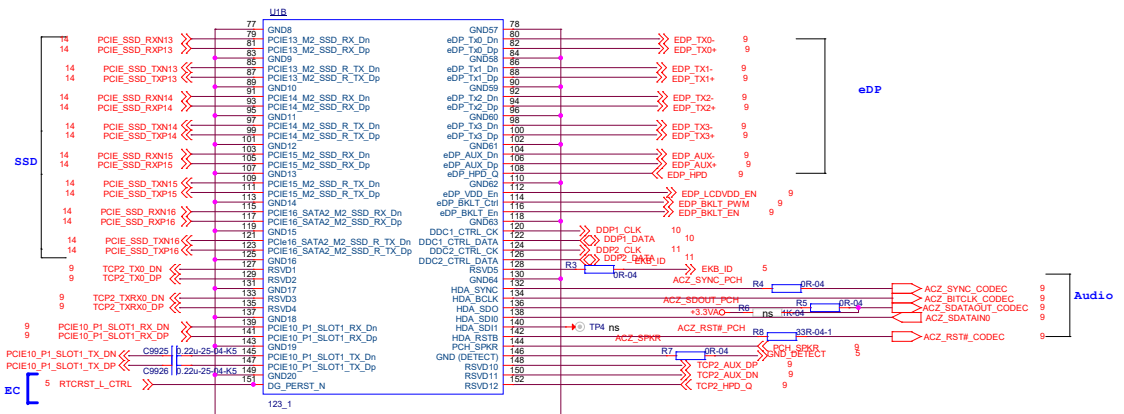
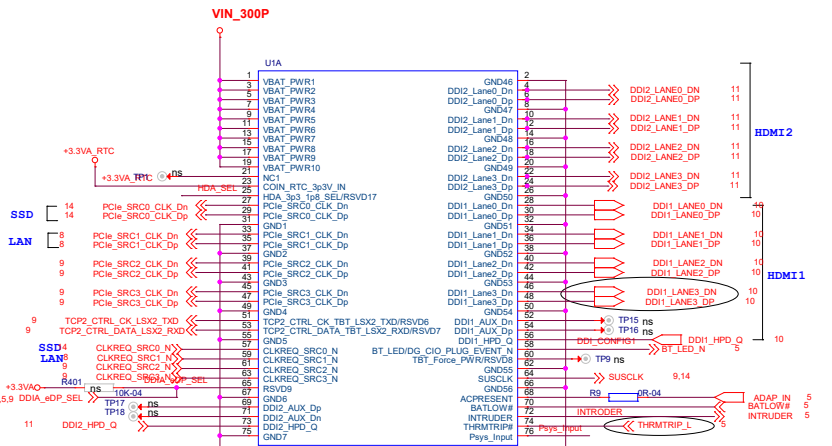
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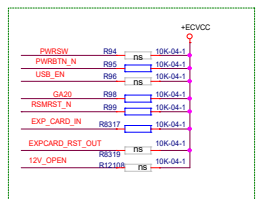
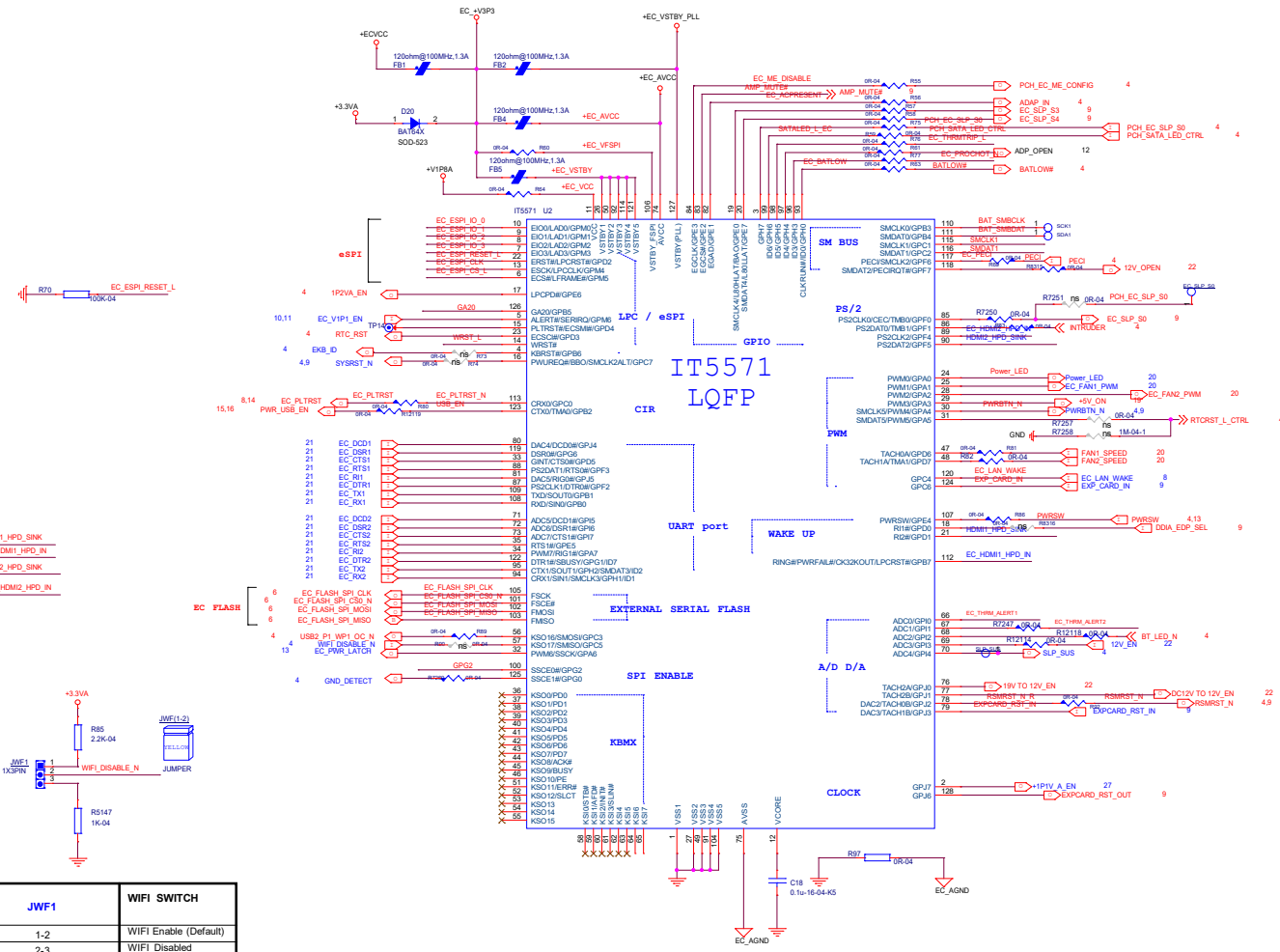
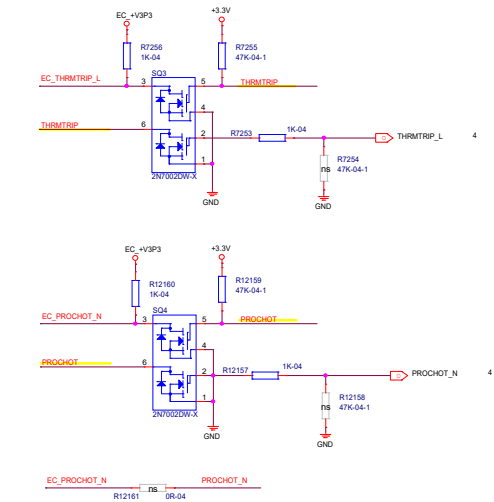
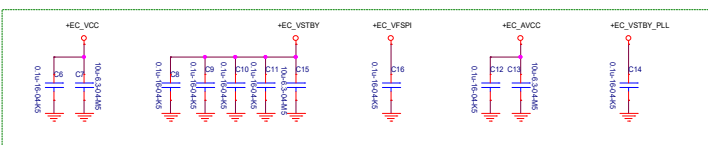
# SYSTEM BLOCK DIAGRAM



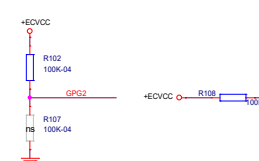
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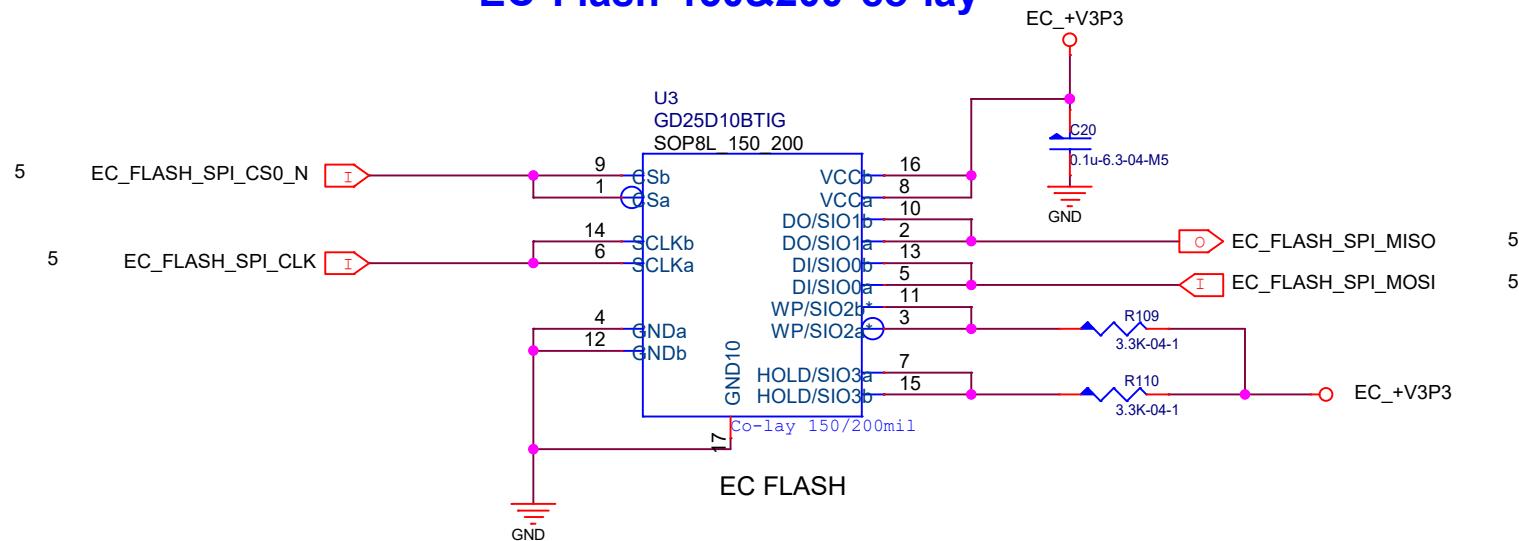


JWF1	WIFI SWITCH
1-2	WiFi Enable (Default)
2-3	WiFi Disabled

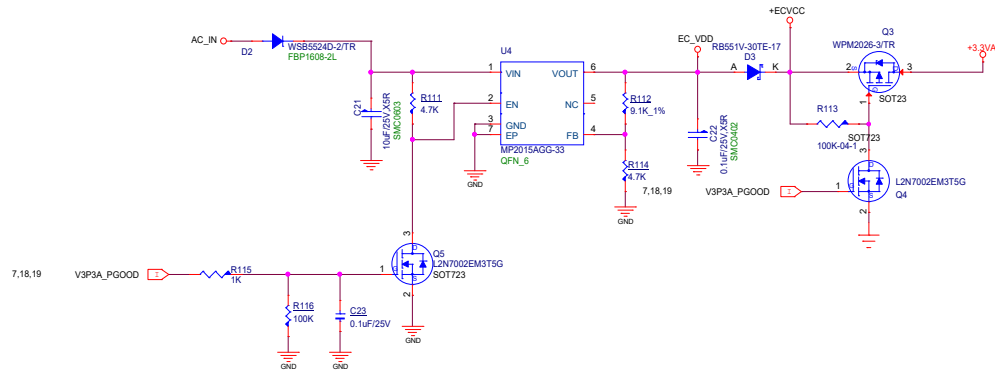


EC -2

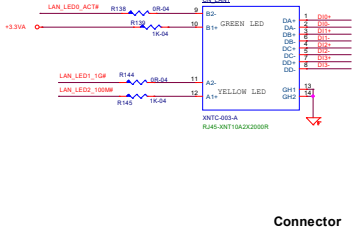
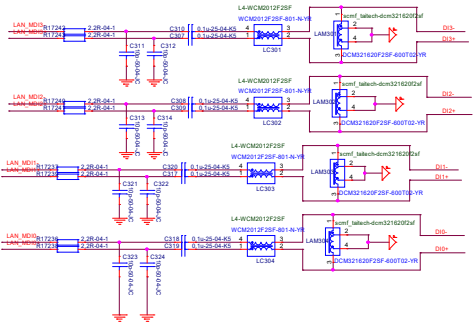
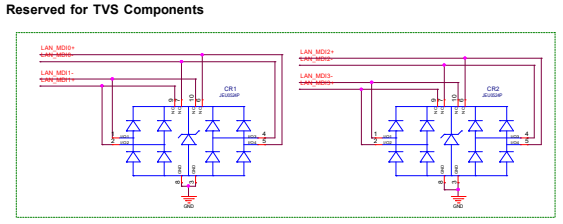
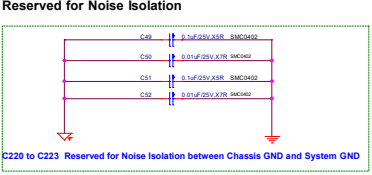
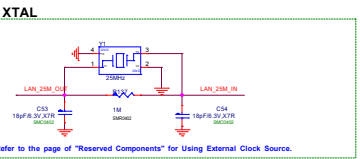
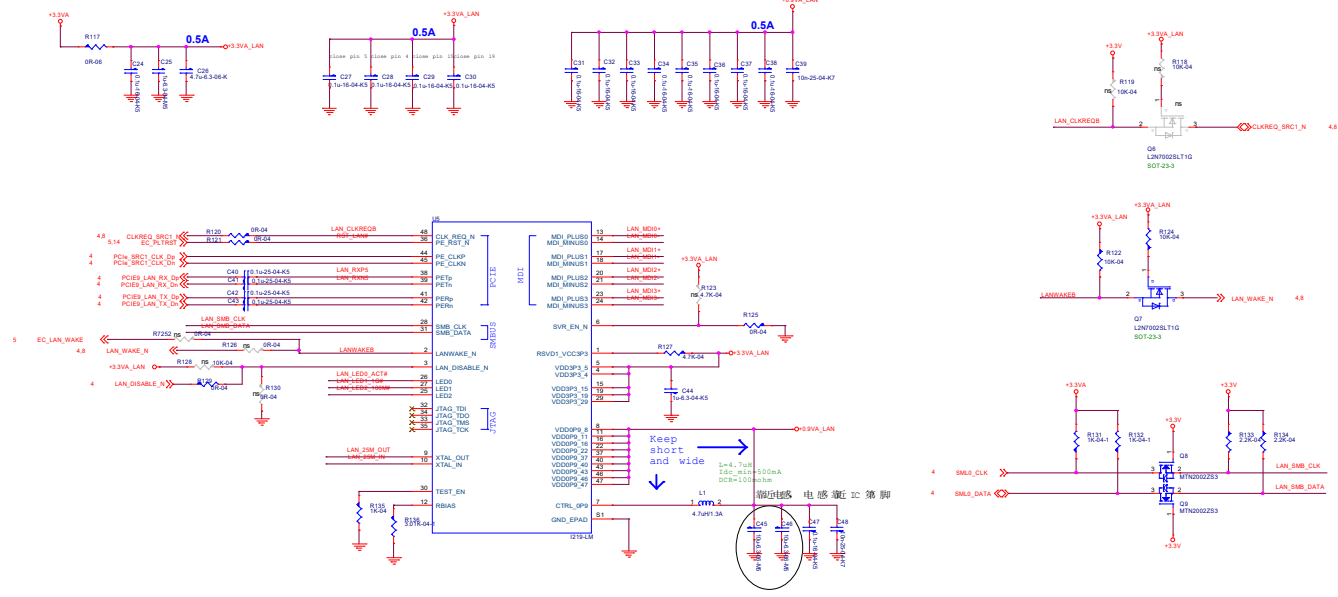
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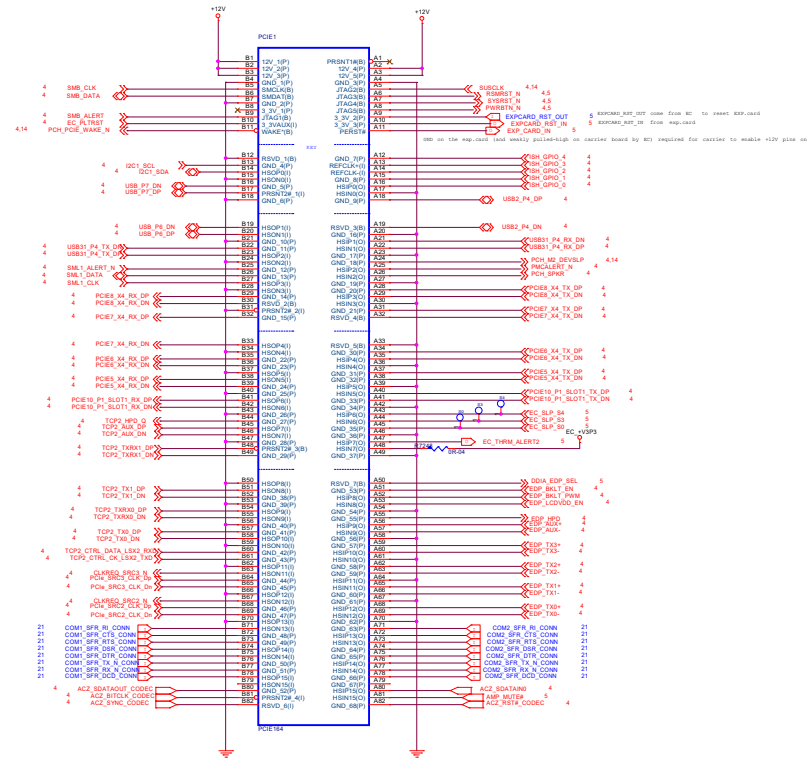
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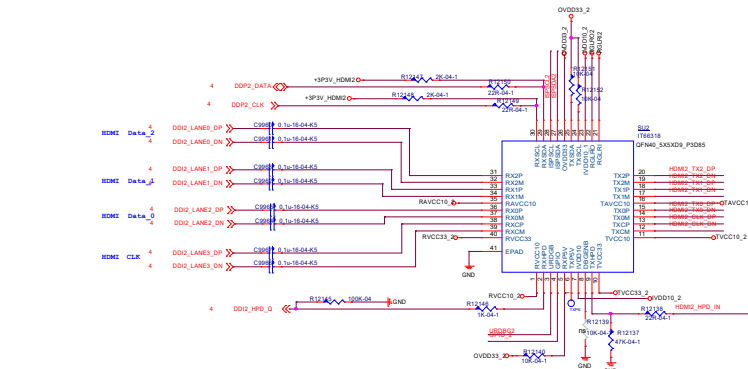
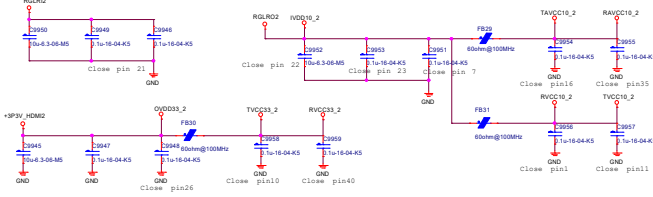
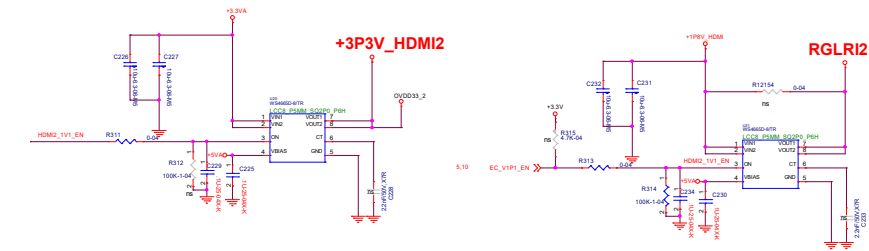
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Page Date	Wednesday, November 23, 2022	Sheet	7 of 30
			Rev V1.0





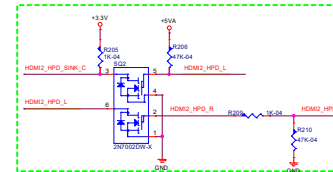
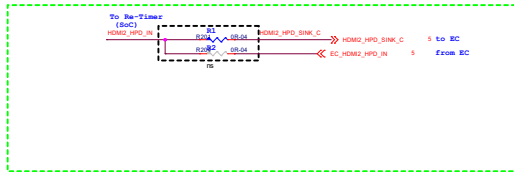
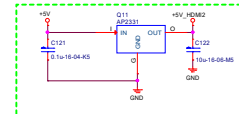
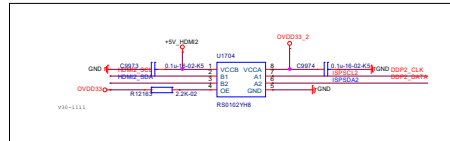
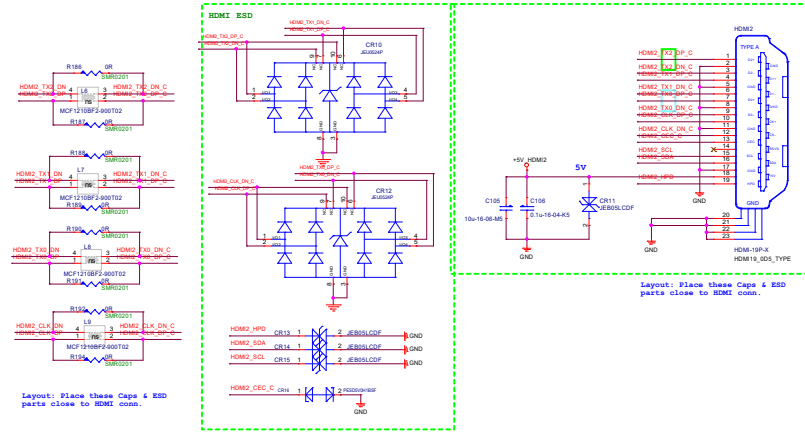
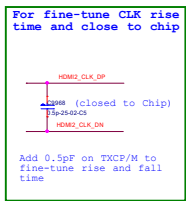


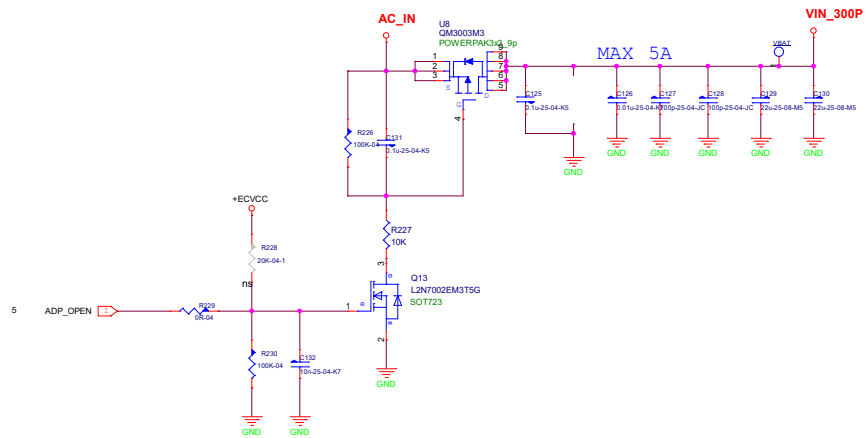
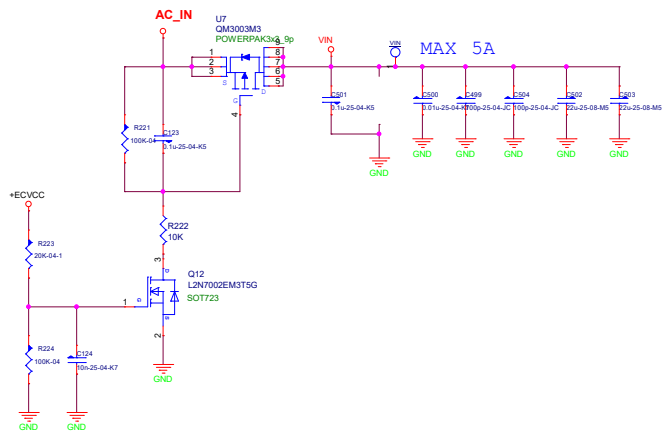




Reserved Trapping Setting

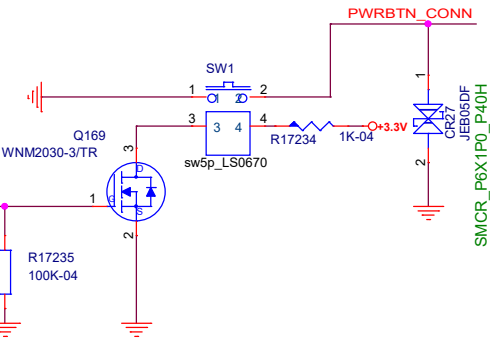
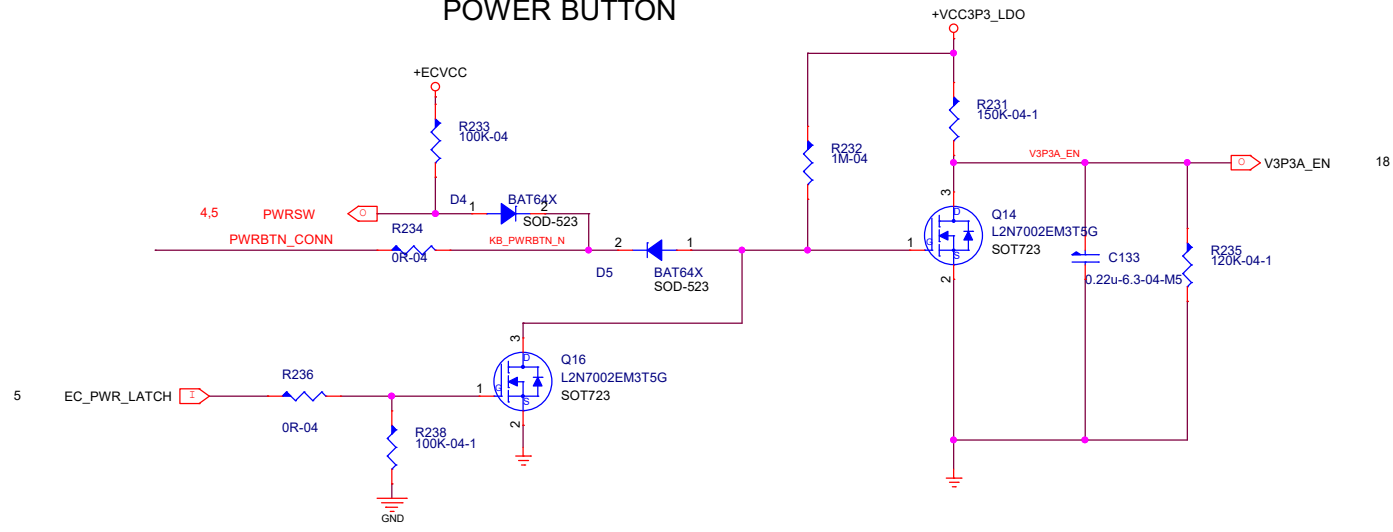
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Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1





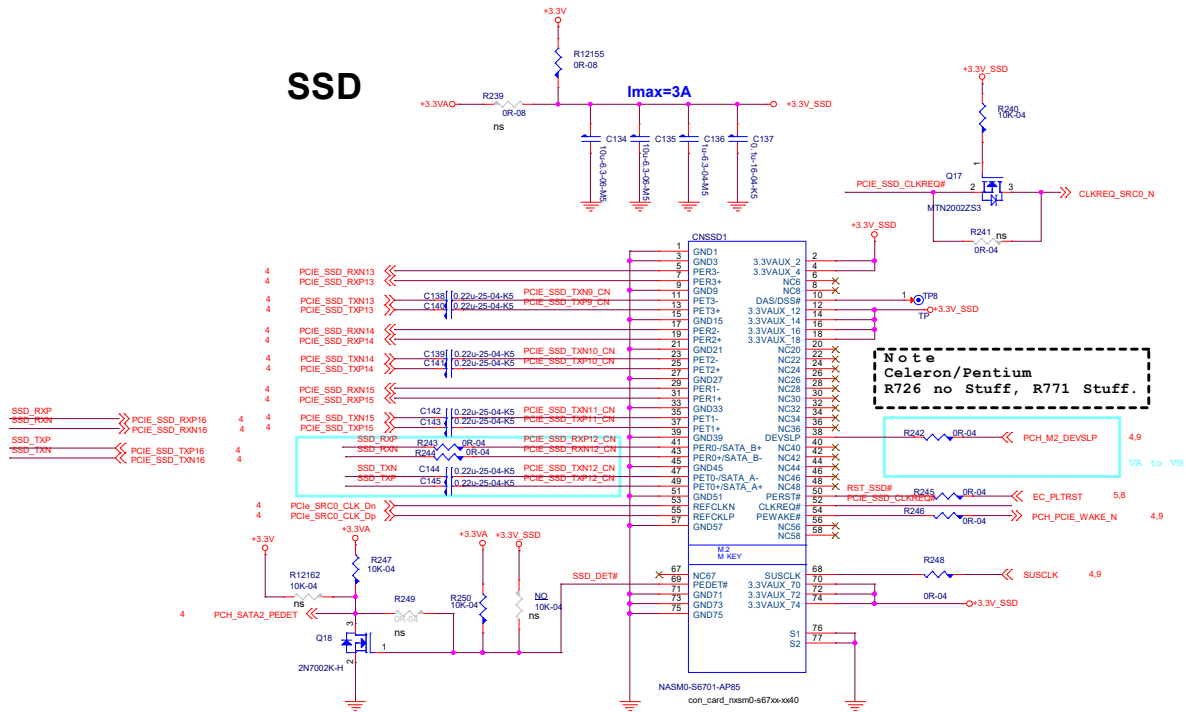
# PWR SW

## POWER BUTTON



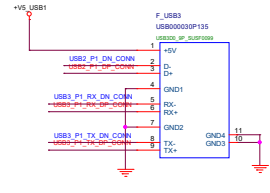
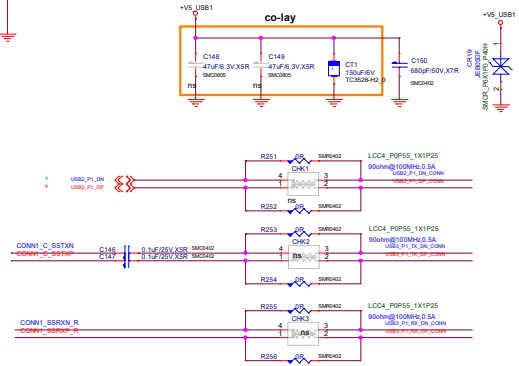
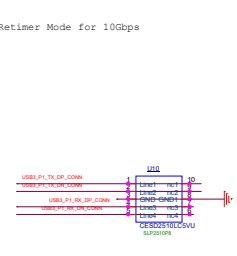
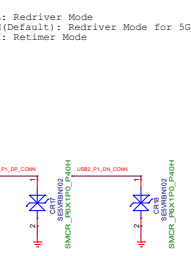
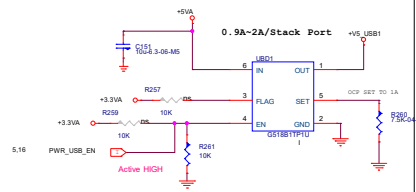
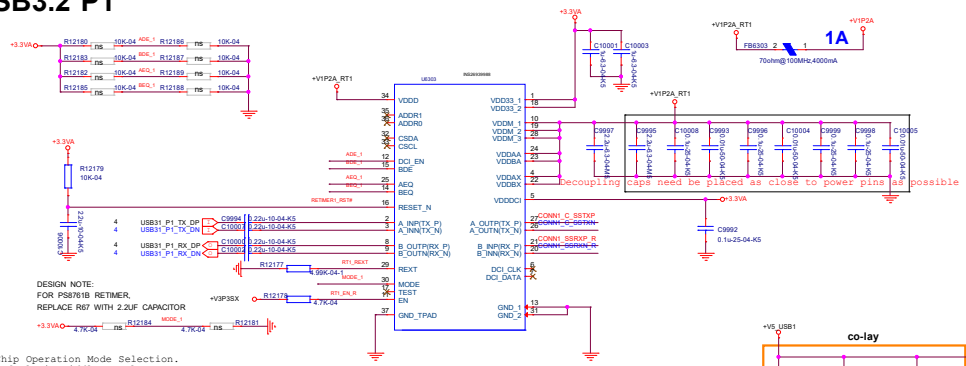
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Page Date	Wednesday, November 23, 2022	Sheet	13 of 30
			Rev V1.0

# SSD

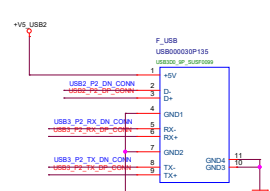
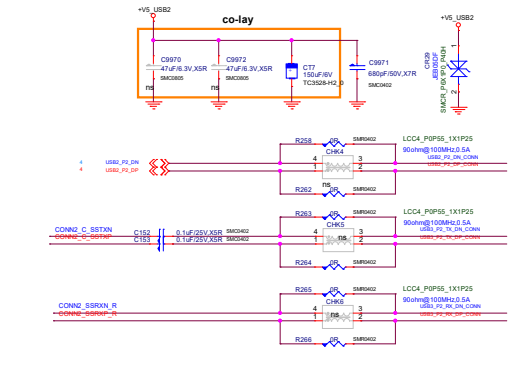
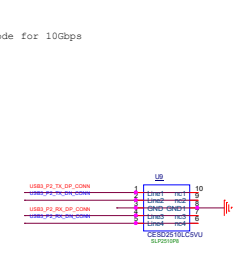
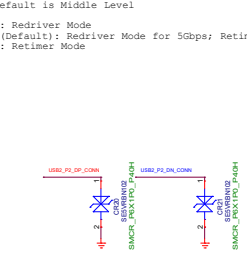
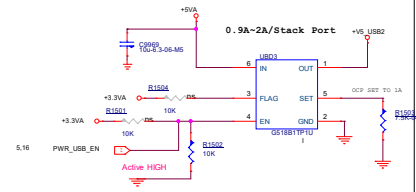
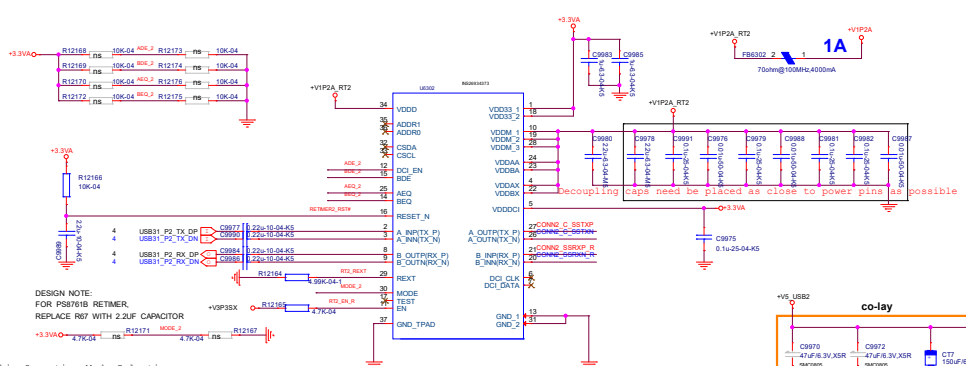


**Note**  
Celeron/Pentium  
R726 no Stuff, R771 Stuff.

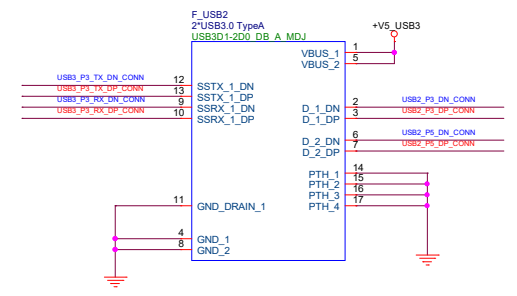
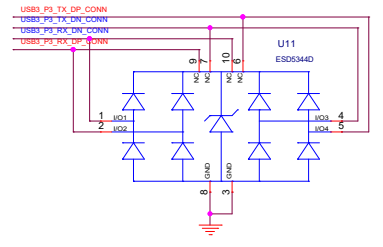
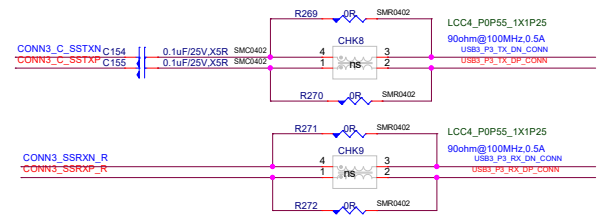
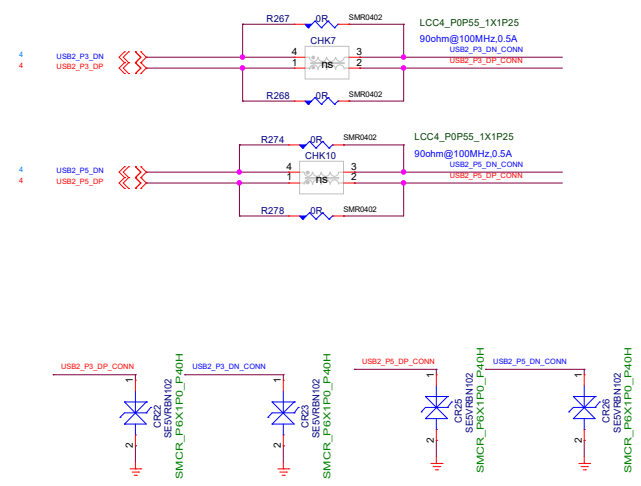
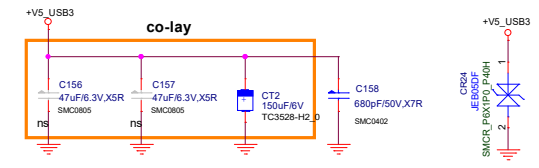
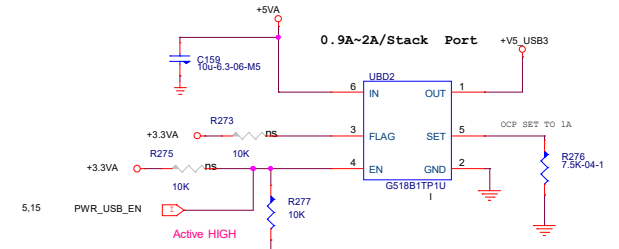
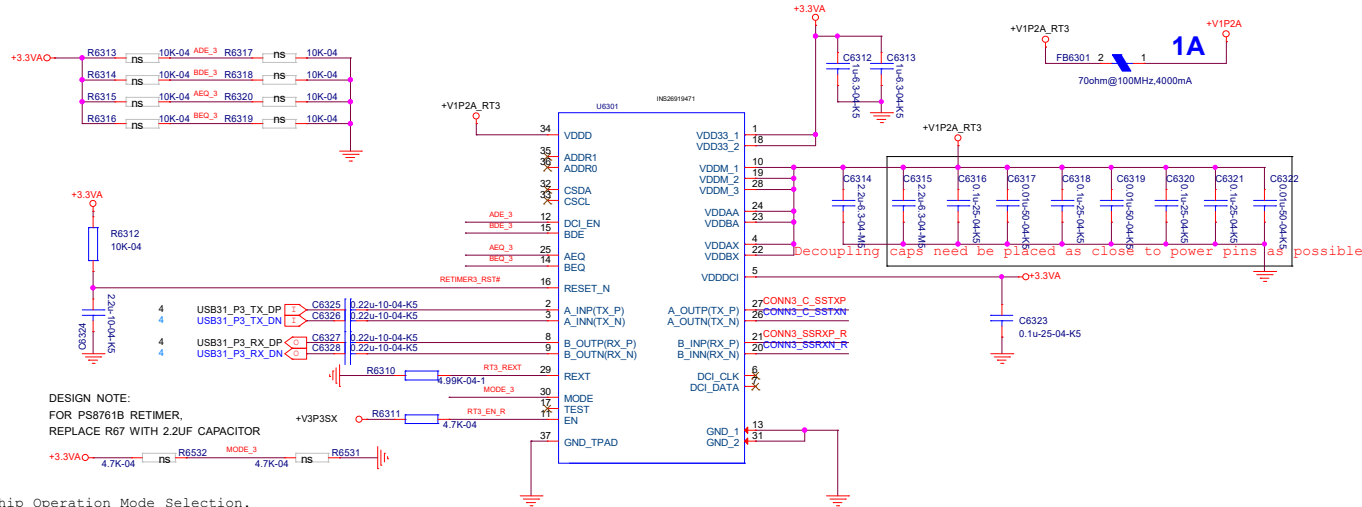
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# USB3.2 P2



# USB3.2 P3

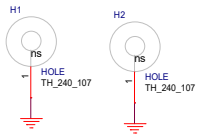
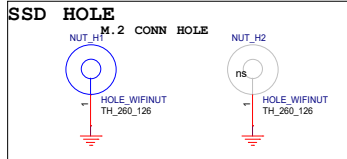
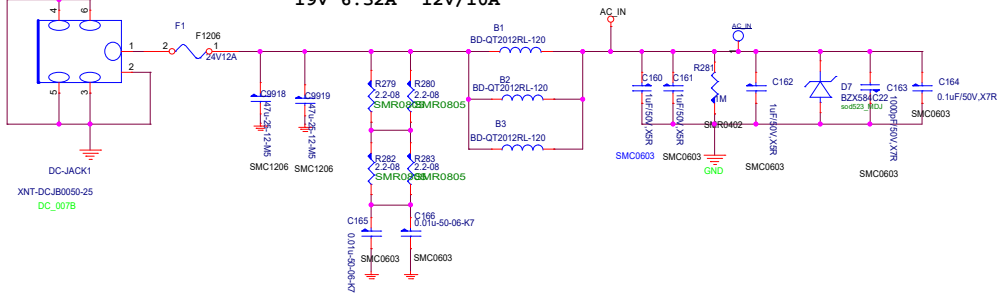


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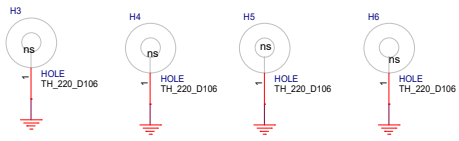


# DC IN 19V/12VDC

19V 6.32A 12V/10A



### SCREW HOLE

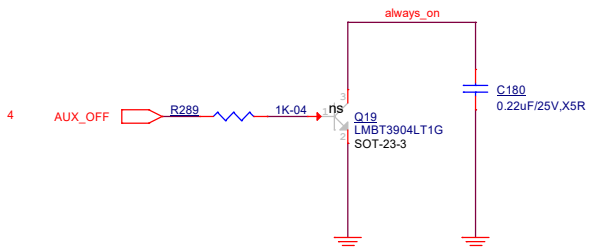
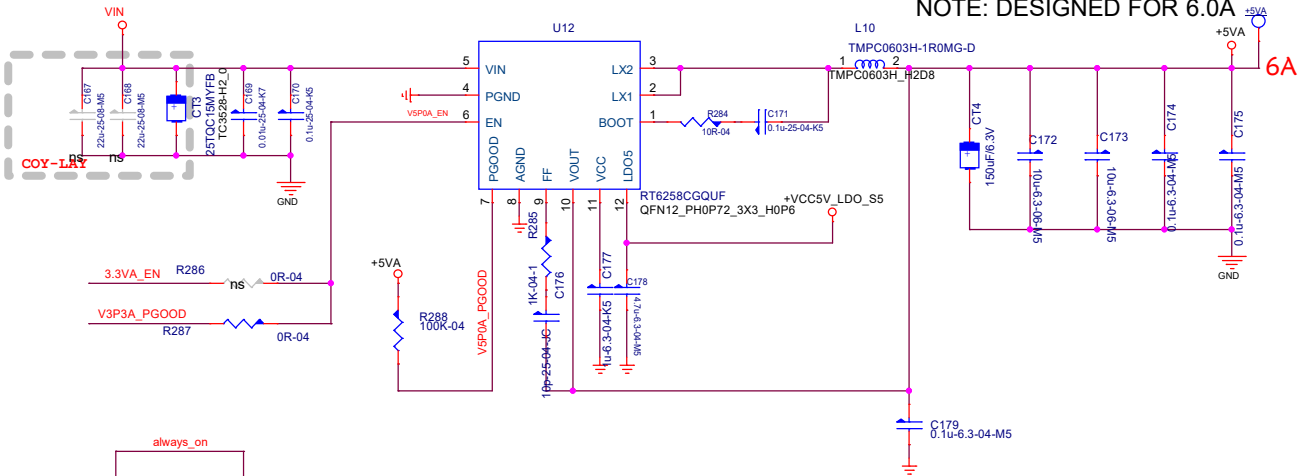


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# 5VA Converter

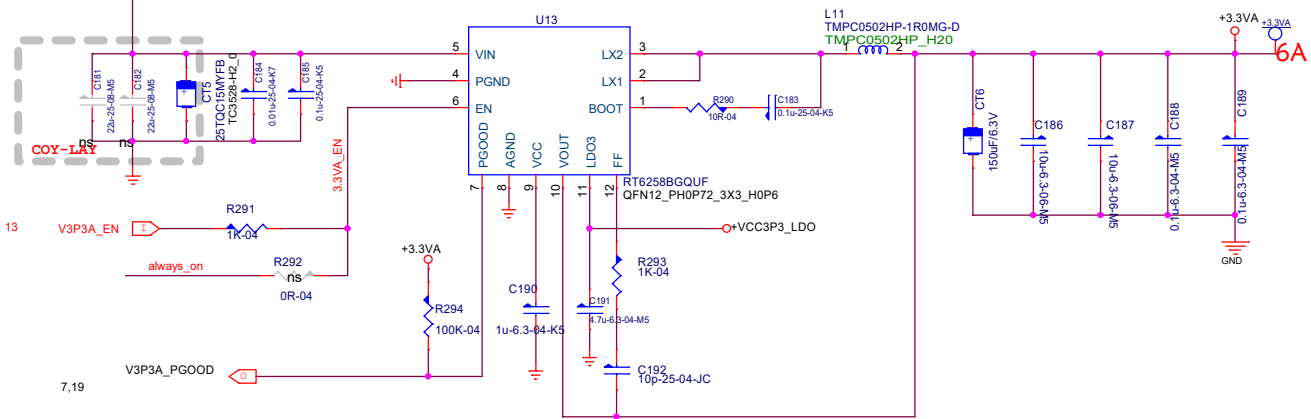
## +V5P0A / +V3P3A POWER SUPPLY

NOTE: DESIGNED FOR 6.0A



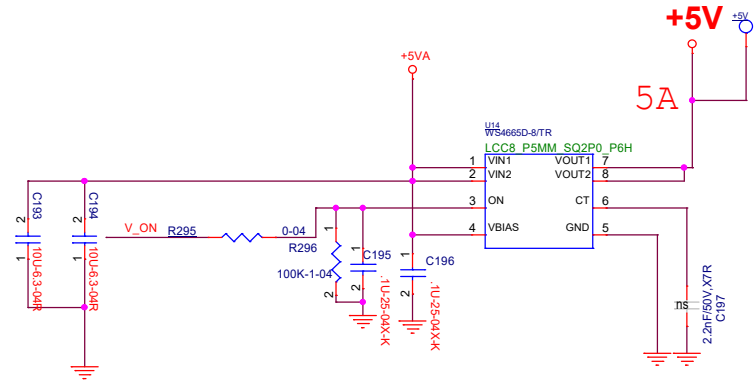
# 3.3VA

NOTE: DESIGNED FOR 5.5A

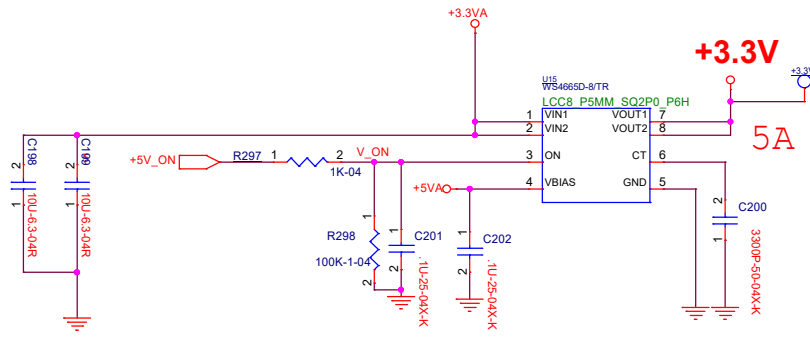


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Page Date	Wednesday, November 23, 2022	Sheet	18 of 30	Rev V1.0

# +5V

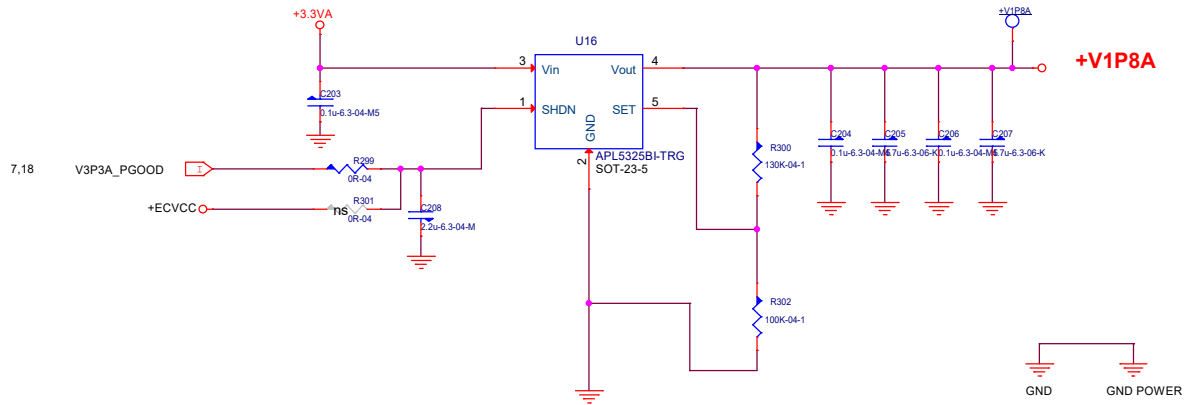


# +3.3V



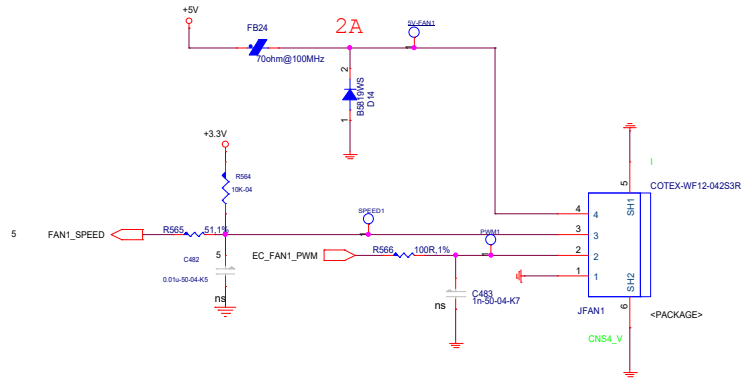
# +V1P8A

$$V_{out} = 0.8 (1 + R1/R2)$$

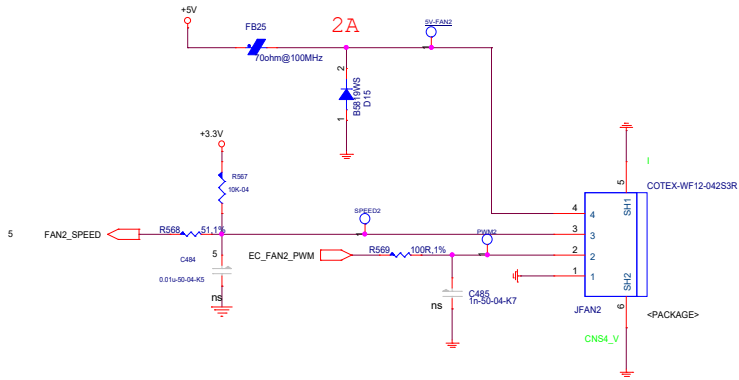


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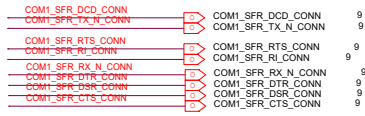
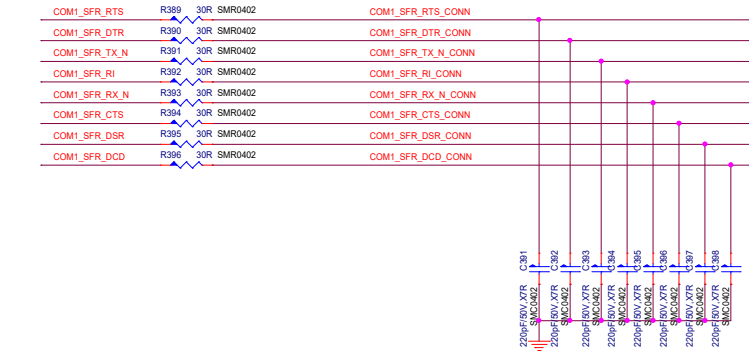
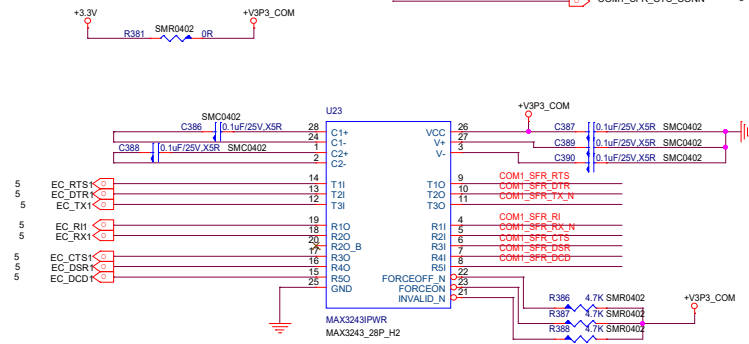
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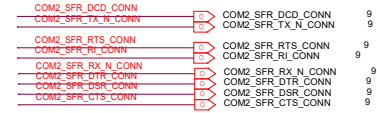
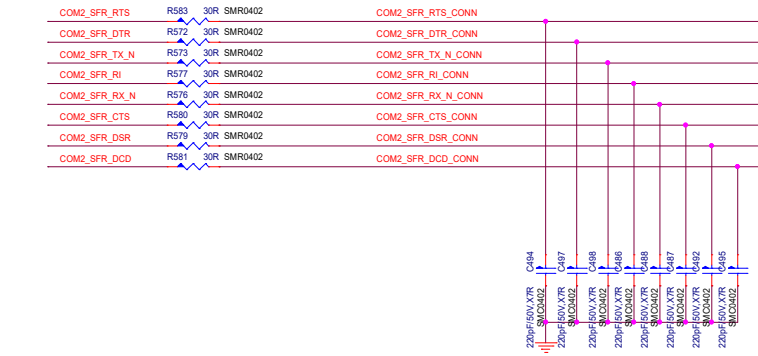
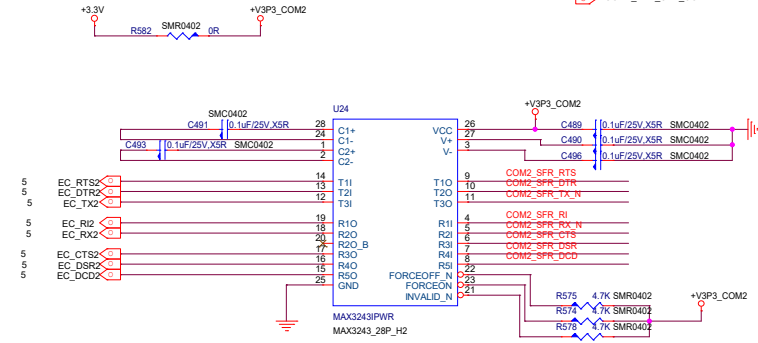
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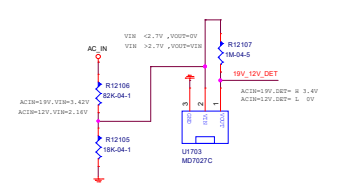
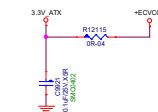
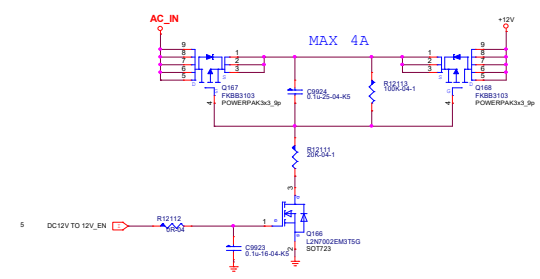
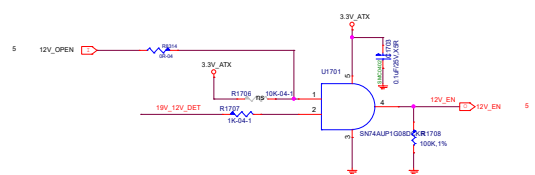
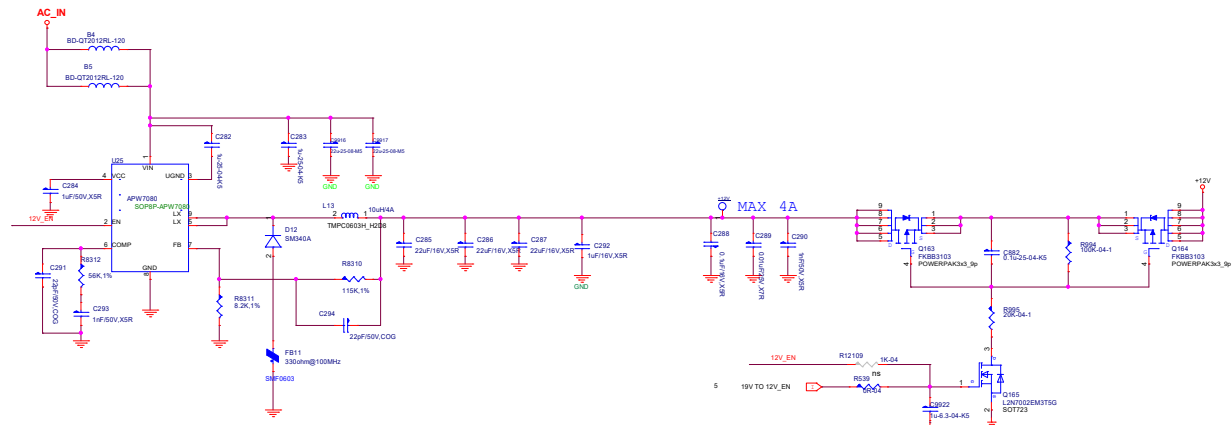


# COM 1



# COM 2





<b>Madigi</b>			
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Project Name	MPC43	Page Name	NC
Document Number		Size	A2
Sheet		Rev	02
Design Date	Wednesday, November 23, 2022	Author	WJSL
Print Date	Wednesday, November 23, 2022	Sheet	23 of 30
			V1.1

5

4

3

2

1

D

D

C

C

B

B

A

A

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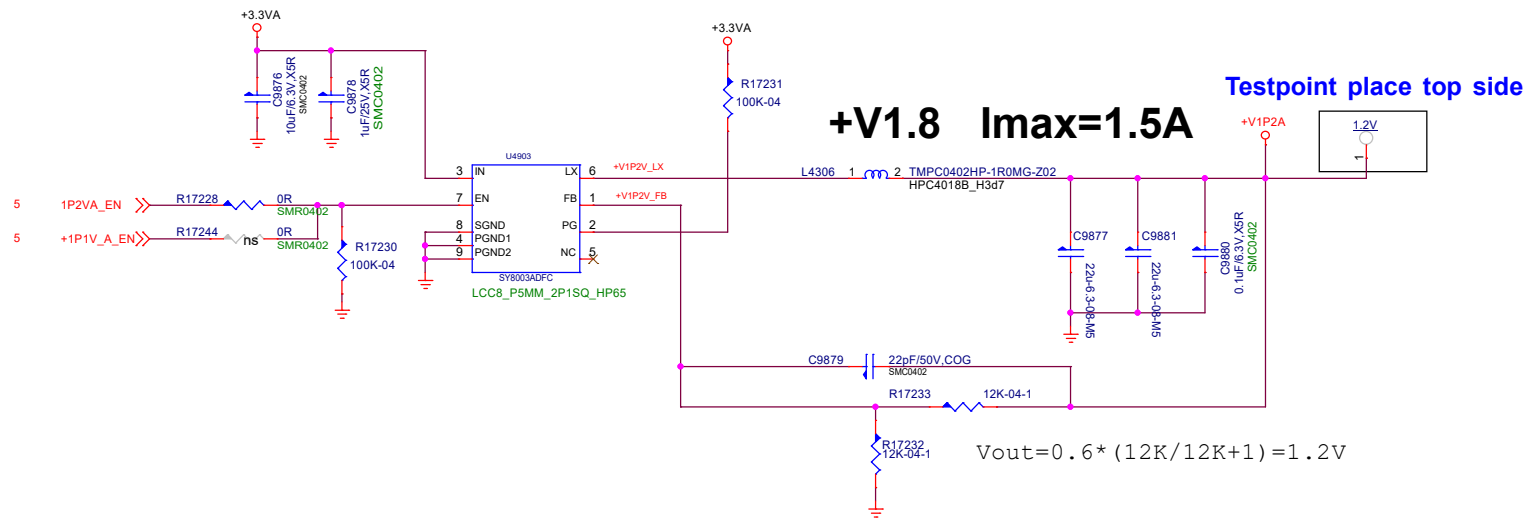
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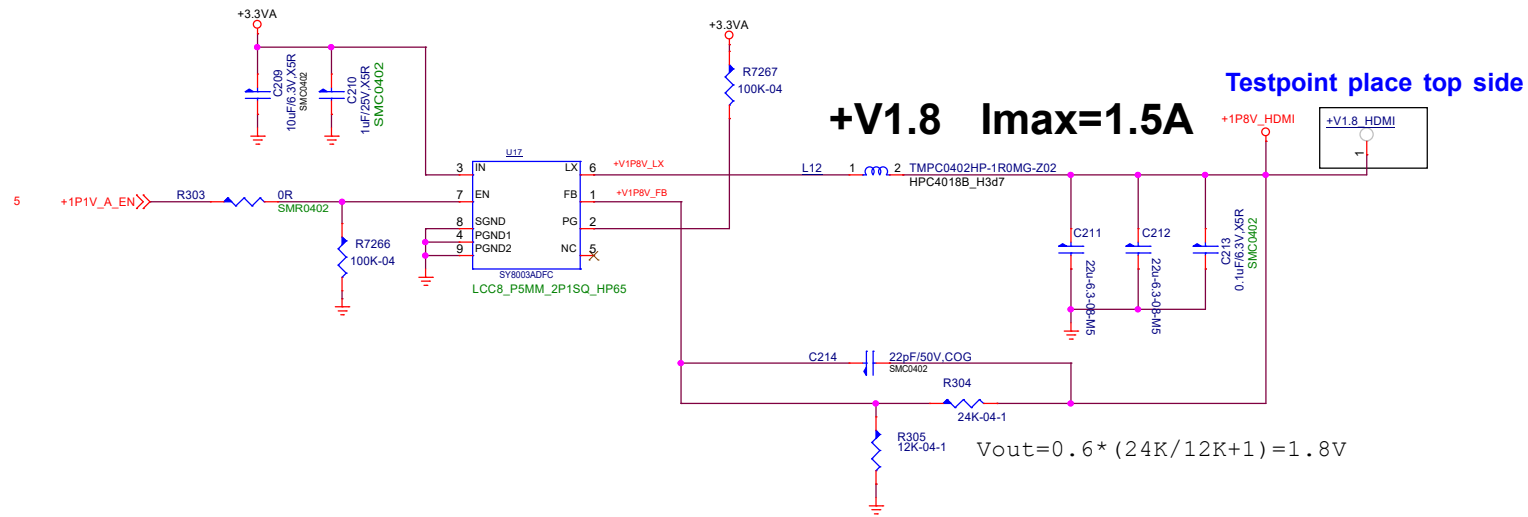


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Project Name	MPC43		
Document Number	Page Name	USB TO PS2 KB	Size
Sheet			A2
Design Date	Wednesday, November 23, 2022	Author	WJSL
Print Date	Wednesday, November 23, 2022	Sheet	26 of 30
			V1.1



<b>Madigi</b>			
Design Title: <b>深圳市迈迪杰科技有限公司</b>			
Project Name: MPC43			
Document Number:	Page Name: 1.2V	Size:	A3
Design Date: Wednesday, November 23, 2022	Author: WUSJ	Rev:	
Page Date: Wednesday, November 23, 2022	Sheet: 26 of 30	Rev:	V1.0

# +1P8V\_HDMI



<b>Madigi</b>			
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Project Name	MPC43		
Document Number	Page Name	+1P1V_HDMI	Size
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Design Date	Wednesday, November 23, 2022	Author	WUSJ
Page Date	Wednesday, November 23, 2022	Sheet	27 of 30
		Rev	V1.0



<b>Madigi</b>			
Design Title <b>深圳市迈迪杰科技有限公司</b>			
Project Name :	MPC43	Size	
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Design Date : Wednesday, November 23, 2022	Author :	WUSJ	Rev
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Document Number	Page Name : TypeC CONN		A3
<Doc>			Rev
Design Date : Wednesday, November 23, 2022	Author : WUSJ		
Page Date : Wednesday, November 23, 2022	Sheet : 29 of 30		V1.0

2022.1.14 V11 版

- 1.P4 HDA\_SEL~~槽~~预留8VA上拉
- 2.P5 EC\_PROCHOT\_N和PROCHOT\_~~槽~~网络,同时~~槽~~o1ay
- 3.P10 DDP1\_CLK~~连~~ISPSC, DDP1\_D~~直~~直连ISSDA。+1P8VHDMI~~槽~~间增加0R电阻~~预~~
- 4.P11 DDP2\_CLK~~连~~ISPSC2, DDP2\_D~~直~~直连ISBDA2。+1P8VHDMI~~槽~~间增加0R~~预~~留
- 5.P14 SSD改3.3~~槽~~同时做3.3V~~槽~~
- 6.P16 BACK USB2.0改用USB\_P5\_DP~~槽~~修改~~槽~~名

2022.2.2.4 增修

- 1.P14 PCH\_SATA2\_PEDDET~~槽~~电由3V~~槽~~改为VA,同时~~槽~~3~~槽~~槽:SSD电改回3.3V来供
- 2.P22 ~~卡~~1~~槽~~槽信号修改, R12109 no s tuff,R539 stuff;~~槽~~DET信号上拉电阻改为1M

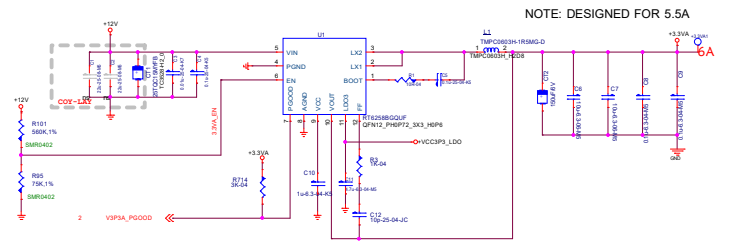
2022.3.4 增修改

- 1.P14 SSD\_DET#~~槽~~槽改+3, ~~槽~~槽, 预留+33V\_SS 做~~槽~~ay

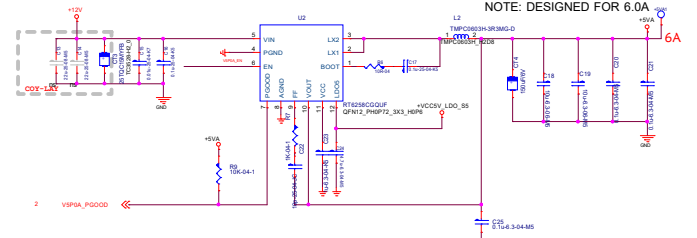
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Design Date : Wednesday, November 23, 2022		Author : WUSJ	Rev
Page Date : Wednesday, November 23, 2022		Sheet : 30 of 30	V1.0

# +V3P3A/+V5P0A POWER SUPPLY

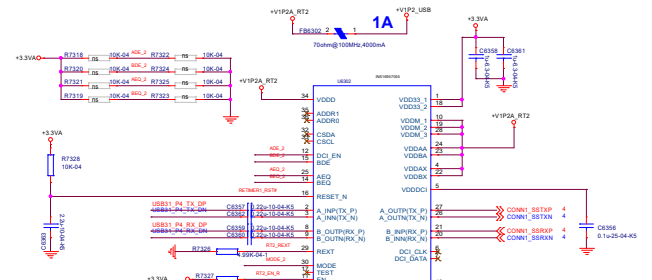
## 3.3VA Converter



## 5VA Converter



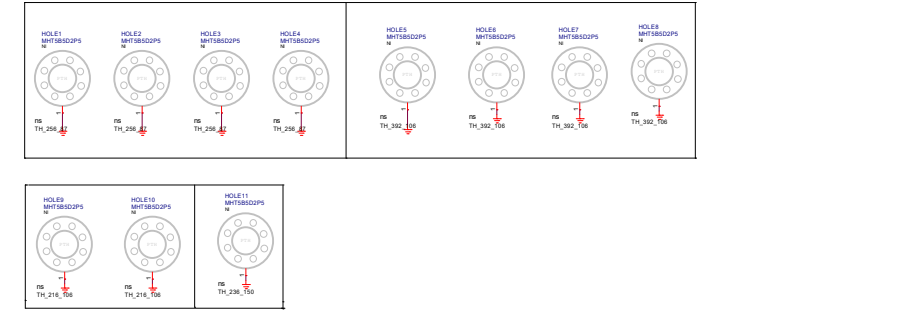
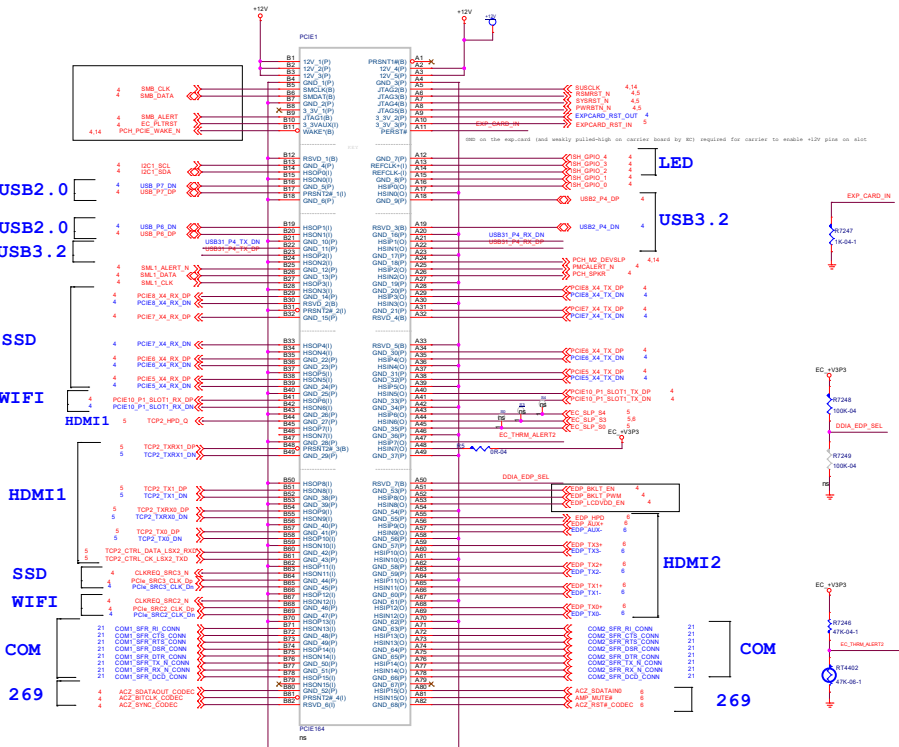
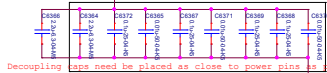
## USB3.0



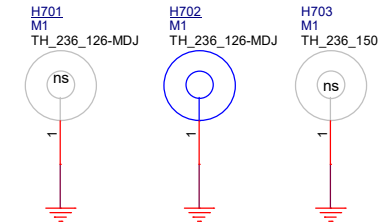
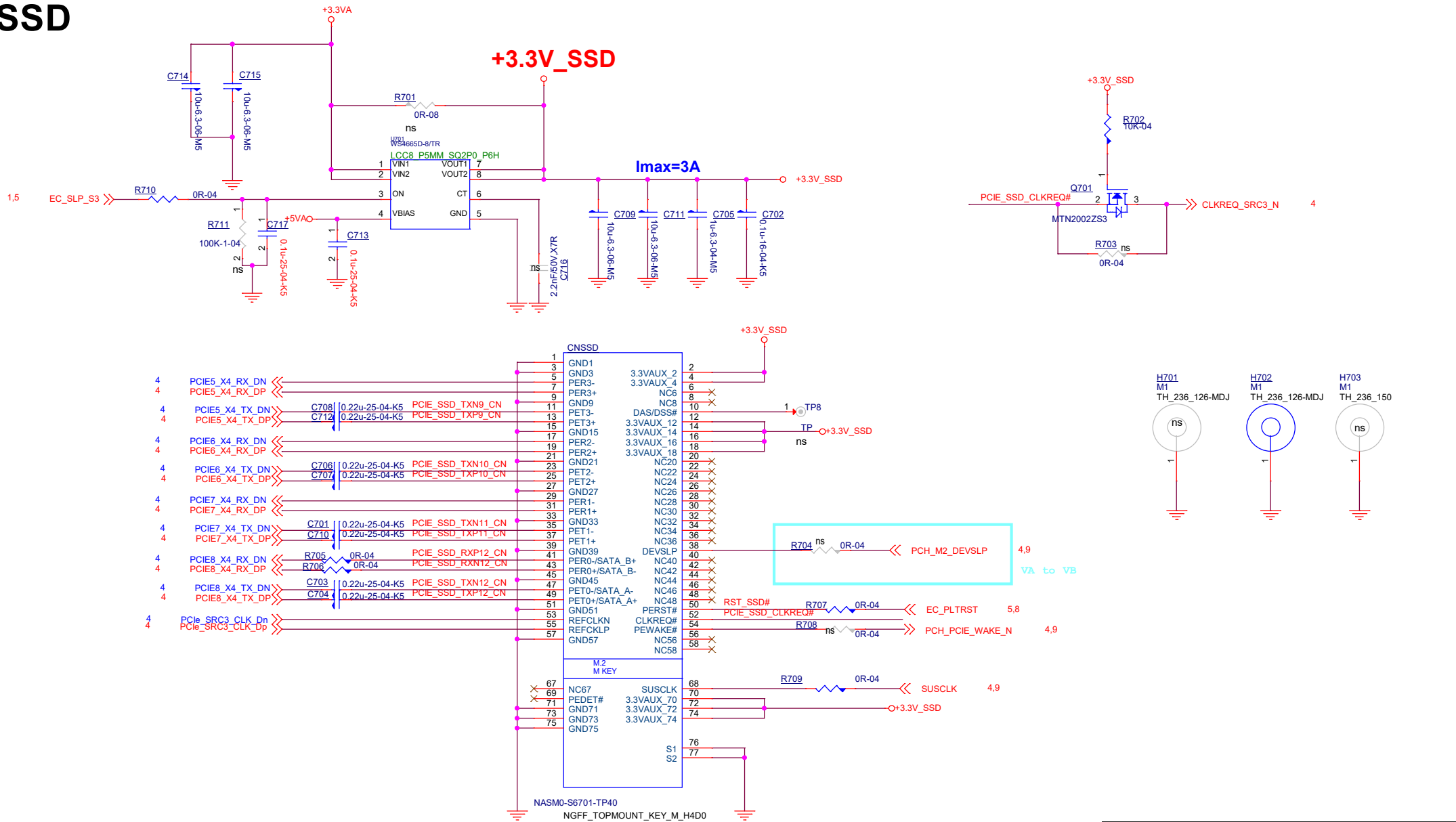
DESIGN NOTE FOR RS728 RETIMER:  
 REPLACE R67 WITH 2.2UF CAPACITOR  
 +3.3VA ← R7328 10K-04  
 ← R7329 10K-04 ← R7330 10K-04  
 ← R7331 10K-04 ← R7332 10K-04

Chip Operation Mode Selection.  
 Default is Middle Level

L: Redriver Mode  
 M(Default): Redriver Mode for 5Gbps; Retimer Mode for 10Gbps  
 R: Retimer Mode



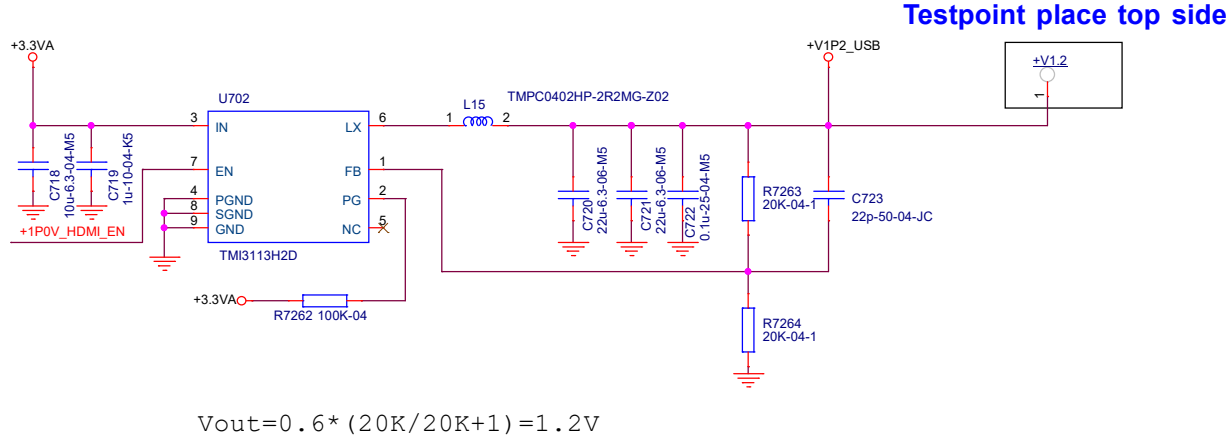
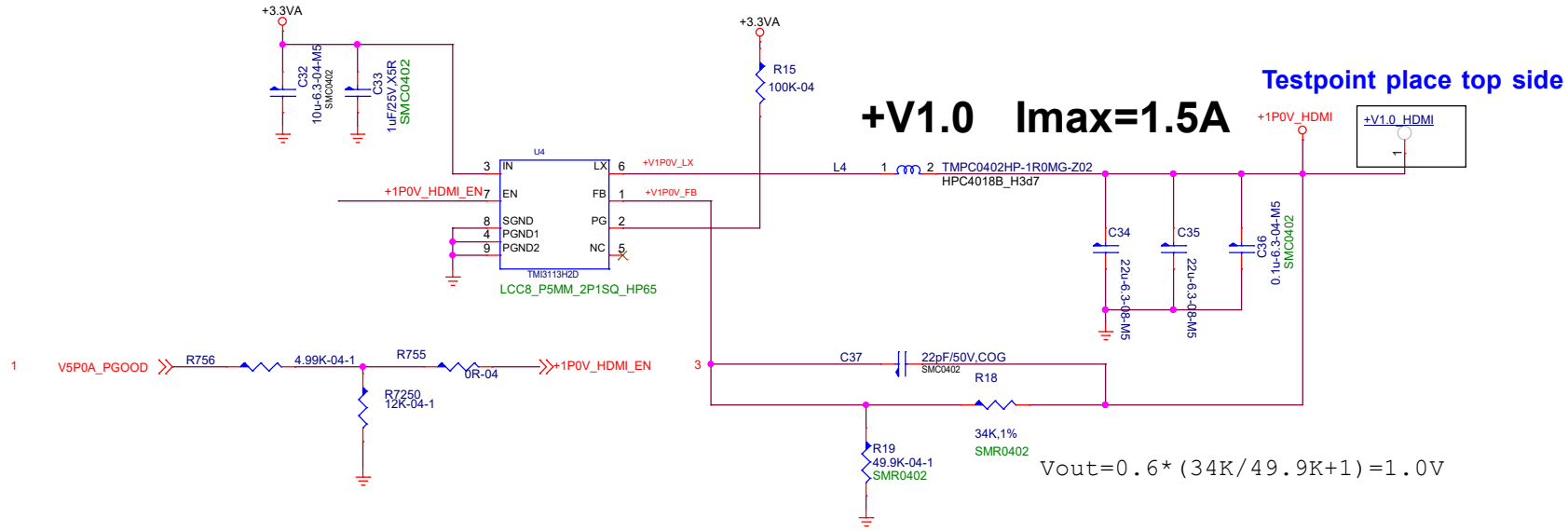
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Size	Document Number	Rev
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Date:	Thursday, March 16, 2023	Sheet 1 of 1

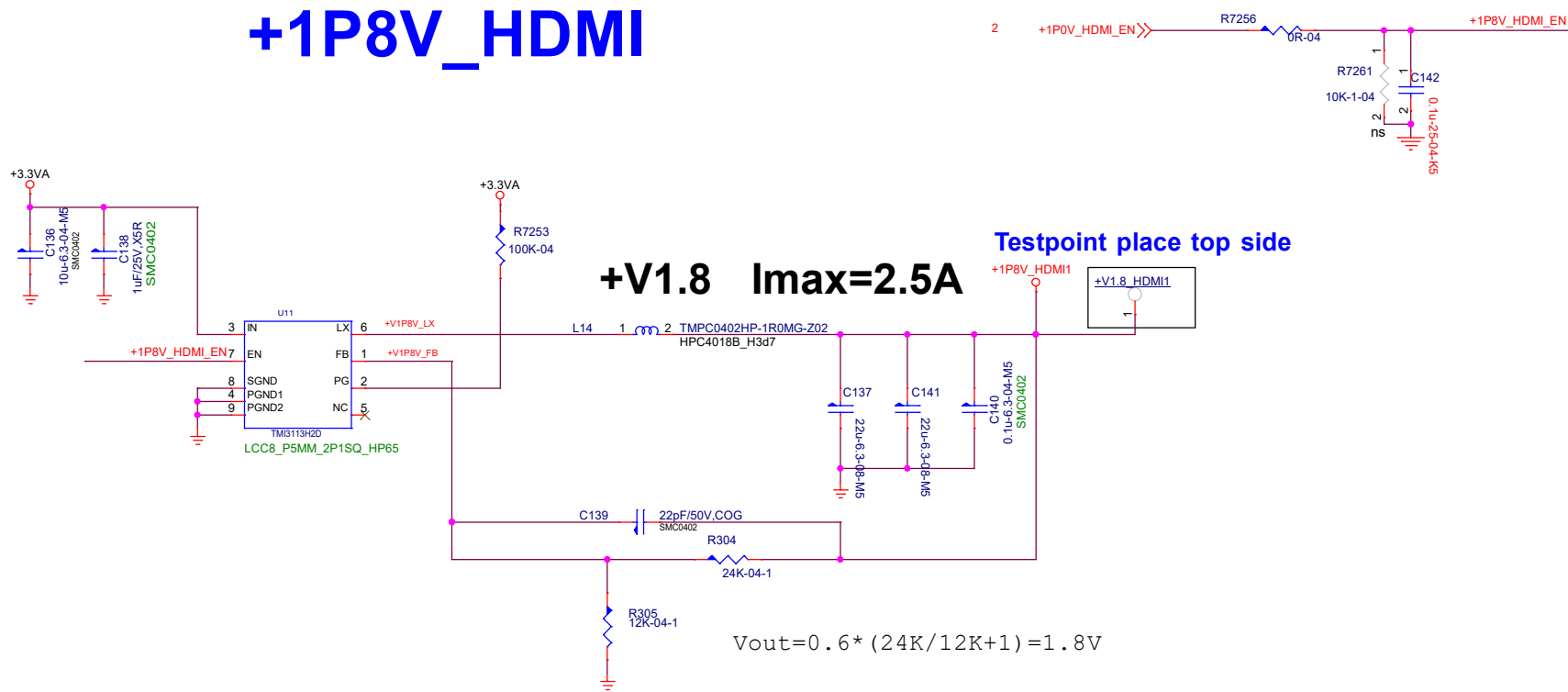


# +1P0V\_HDMI



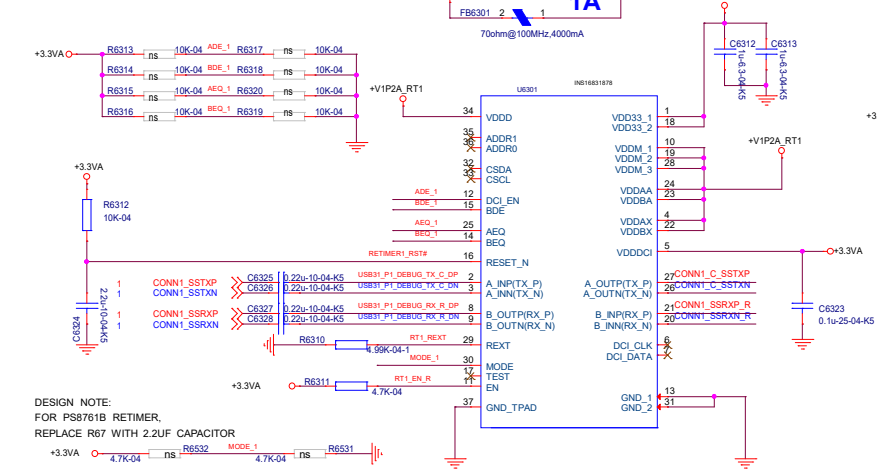
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Title	深圳市迈迪杰科技有限公司	
Size	Document Number	Rev
B	<b>MPC43_Expansion Card</b>	V1.0
Date: Thursday, March 16, 2023	Sheet	2 of 6

# +1P8V\_HDMI



<b>MADIGI</b>		
Title	深圳市迈迪杰科技有限公司	
Size	Document Number	Rev
B	<b>MPC43_Expansion Card</b>	V1.0
Date: Thursday, March 16, 2023	Sheet	3 of 6

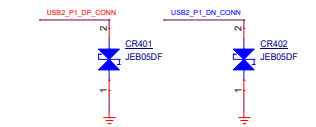
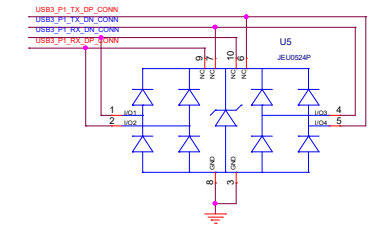
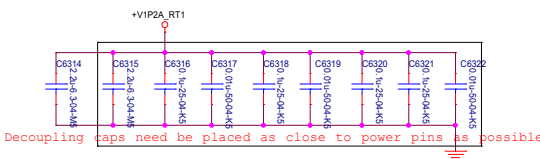
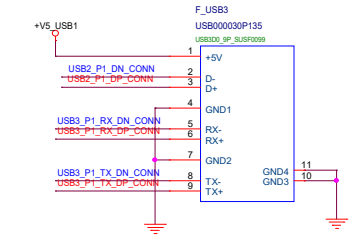
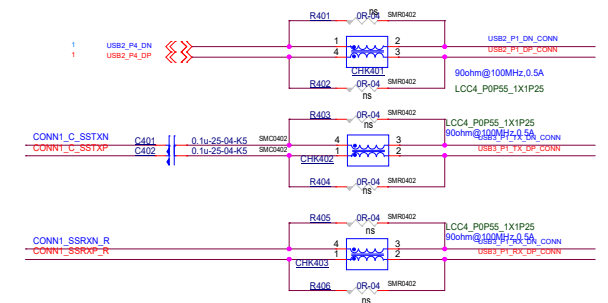
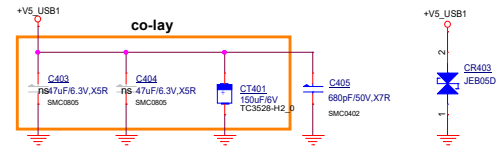
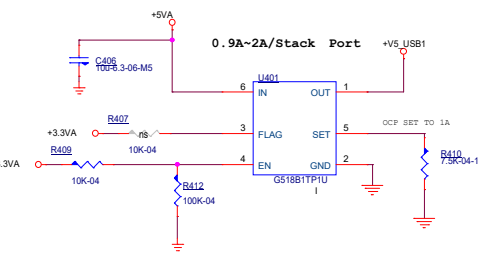
# USB3.0



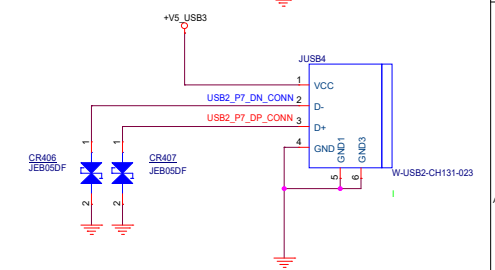
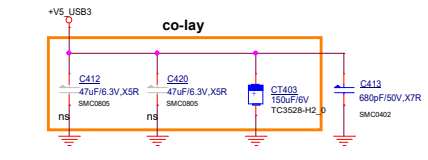
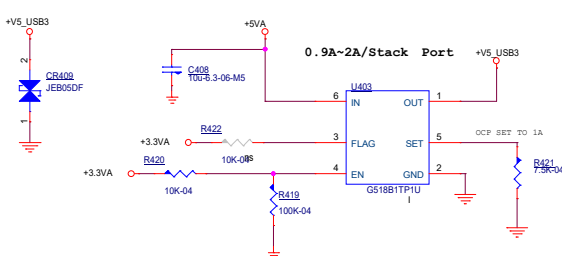
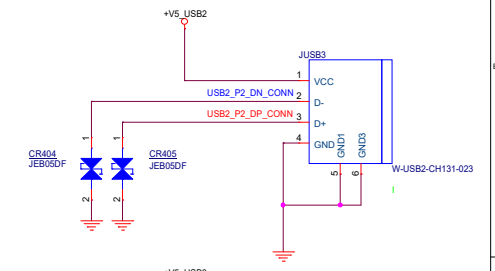
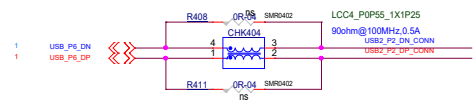
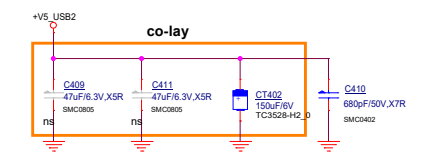
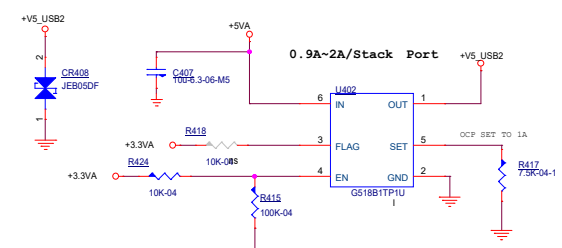
DESIGN NOTE:  
FOR PSB761B RETIMER,  
REPLACE R67 WITH 2.2UF CAPACITOR

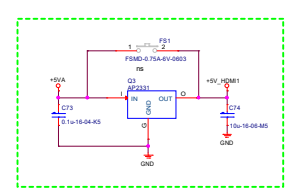
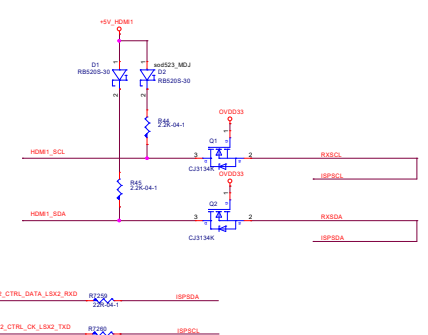
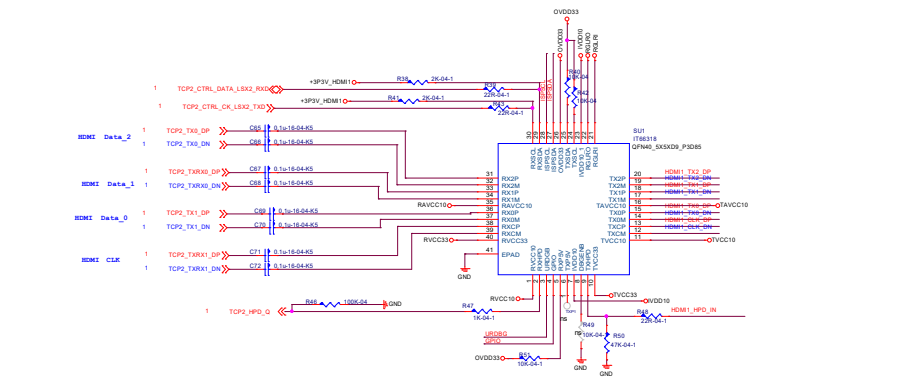
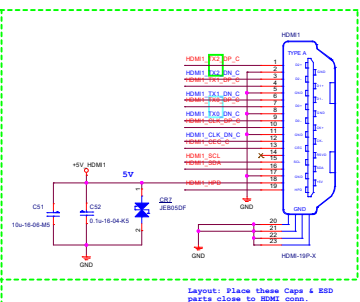
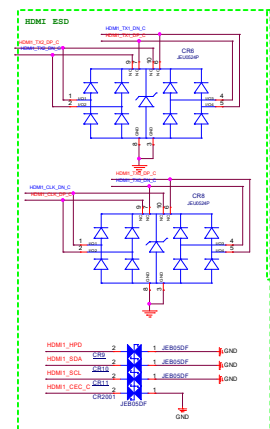
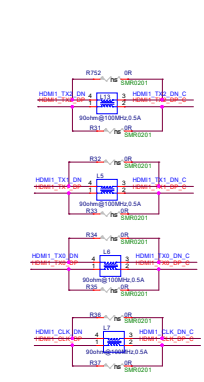
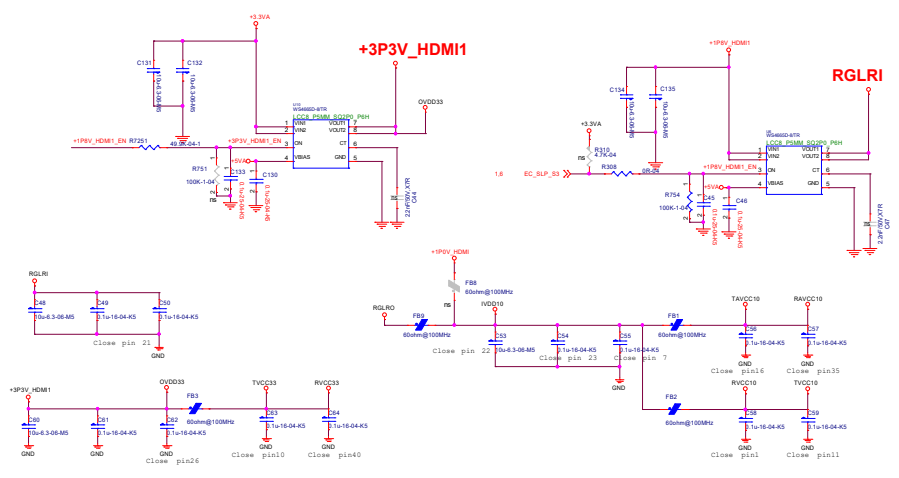
Chip Operation Mode Selection.  
Default is Middle Level

L: Redriver Mode  
M(Default): Redriver Mode for 5Gbps; Retimer Mode for 10Gbps  
H: Retimer Mode



# USB2.0





**Table 48. TCP Port Signal Mapping for HDMI\***

Description	Signal Mapping	
	TCP	HDMI
Main Link (Tx)	TCP_TX0	HDMI Data_2
	TCP_TX1	HDMI Data_0
	TCP_TXRX0	HDMI Data_1
	TCP_TXRX1	HDMI CLK

Note: Apply to TCP ports only.

