PKM8720DF-C13-F10

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

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Contents

1 Module Overview

1.1 General Description

The PKM8720DF-C13-F10 is a multi-radio MCU module. With the open CPU architecture, customers can develop advanced applications running on the dual-core 32-bit MCU. The radio provides support for Wi-Fi 802.11 a/b/g/n in the 2.4GHz/5GHz band and BLE 5.0 communications. The rich set of peripherals and high performance make it an ideal choice for smart homes, industrial automation, consumer electronics, etc.

1.2 Features

Chipset and Memory:

- RTL8720DF-VT1-CG (named RTL8720DF thereafter) chipset embedded, dual-core processor: KM4 up to 200MHz, KM0 up to 20MHz
- KM4 on-chip memory: up to 512KB SRAM
- KM0 on-chip memory: up to 64KB SRAM
- 4MB Flash

Wi-Fi:

- 802.11 a/b/g/n 1x1, 2.4GHz & 5GHz
- Center frequency range of operating channel: 2412MHz ~ 2462MHz, 5180MHz ~ 5240MHz, 5745MHz ~ 5825MHz
- Support 20MHz/40MHz bandwidth, up to the data rate of MCS7
- Wi-Fi WEP, WPA, WPA2, WPA3, WPS; open, shared key, and pair-wise key authentication services
- Support low power Tx/Rx for short-range application
- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)

Bluetooth Low Energy:

- Bluetooth LE: Bluetooth 5.0
- Speed: 1Mbps, and 2Mbps
- Support LE secure connections
- Support LE scatternet
- Support 3 Master links/1 Slave link
- Co-existence RF design between Wi-Fi and Bluetooth

Peripherals:

- 4x UART interface, baud rate up to 6MHz
- 2 x I2C, two speed modes: standard up to 10Kbps, fast up to 400Kbps
- 2 x SDIO Host/SDIO 2.0 Device, clock up to 50MHz
- 3 x SPI Master/Slave, baud rate up to 50MHz
- 1 x USB 2.0 HS/FS/LS mode
- 11 x PWM with configurable duration and duty cycle from 0 ~ 100%
- 19 x programmable GPIOs
- KM4 and KM0 both have a GDMA controller, each with 6 channels

Antenna Option:

- On-board PCB antenna

Operating Conditions:

- Operating input voltage: (3.3 ± 10%)V
- Operating ambient temperature: -40°C to 105°C

2 Module Block Diagram

This module includes the chipset, crystal component, R/L/C components for RF matching, decoupling and RF radio antenna.

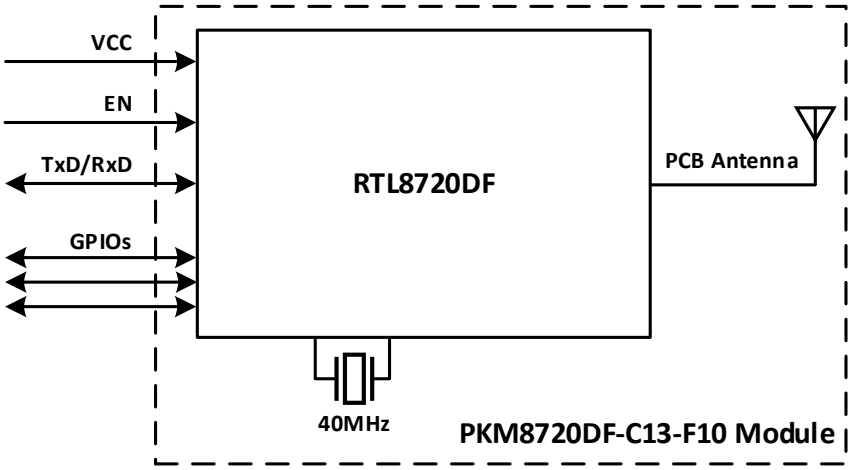


Figure 1. Block Diagram

3 Module Pin Definition

3.1 Module Pin Layout

This module has 22 pins.

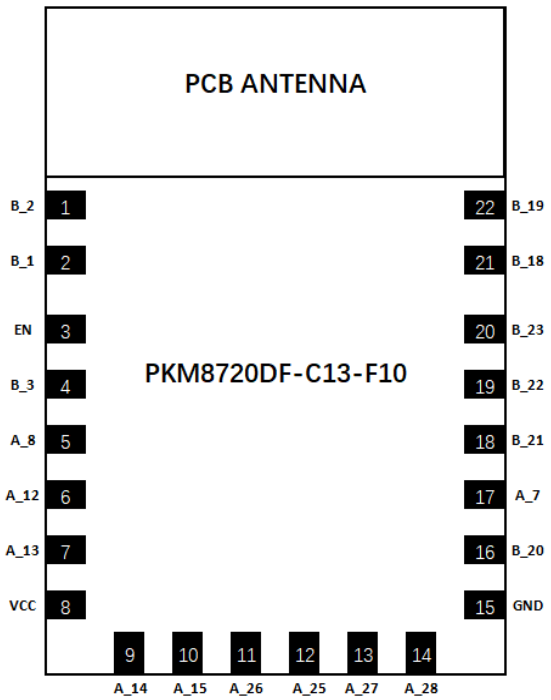


Figure 2. Module Pin Layout (Top View)

3.2 Module Pin Description

3.2.1 Pin Description

Table 1. Pin Description

Pin Name	Pin No.	Type	Description
B_2	1	I/O	GPIOB_2/UART_RXD
B_1	2	I/O	GPIOB_1/UART_TXD
EN	3	I	● High: Enable the chip. ● Low: Module power off.
B_3	4	I/O	GPIOB_3/SWD_CLK
A_8	5	I/O	GPIOA_8/UART_LOG_RXD
A_12	6	I/O	GPIOA_12/SPI_MOSI
A_13	7	I/O	GPIOA_13/SPI_MISO
VCC	8	P	Power Supply
A_14	9	I/O	GPIOA_14/SPI_CLK/UART_RTS
A_15	10	I/O	GPIOA_15/SPI_CS/UART_CTS
A_26	11	I/O	GPIOA_26/HSDP
A_25	12	I/O	GPIOA_25/HSDM
A_27	13	I/O	GPIOA_27/SWD_DAT
A_28	14	I/O	GPIOA_28/RREF
GND	15	P	Ground
B_20	16	I/O	GPIOB_20/SDIO_CMD
A_7	17	I/O	GPIOA_7/UART_LOG_TXD

B_21	18	I/O	GPIOB_21/SDIO_CLK
B_22	19	I/O	GPIOB_22/SDIO_D0
B_23	20	I/O	GPIOB_23/SDIO_D1
B_18	21	I/O	GPIOB_18/SDIO_D2
B_19	22	I/O	GPIOB_19/SDIO_D3

NOTE

- ***P**: power supply*
- ***I**: input*
- ***O**: output*

3.2.2 Strapping Pins

This module has 2 strapping pins.

Table 2. Strapping Pin

Pin Name	Pin No.	Default State	Description
A_7	17	Pull up	1: Normal mode (default) 0: Flash download mode
A_27	13	Pull up	1: Normal mode (default) 0: Test mode

4 RF Characteristic

4.1 Wi-Fi Radio Standard

Table 3. Wi-Fi Radio Standard

Wi-Fi Wireless Standard	Description
Wi-Fi frequency range	● 2412MHz ~ 2462MHz (2.4GHz ISM Band) ● 5180MHz ~ 5240MHz, 5745MHz ~ 5825MHz(5GHz)
Wi-Fi wireless standard	IEEE 802.11 a/b/g/n
Wi-Fi wireless standard Modulation	DSSS, DBPSK, DQPSK, CCK and OFDM (BPSK/QPSK/16-QAM/64-QAM)
Wi-Fi wireless data rate	● 802.11a: 6/9/12/18/24/36/48/54 Mbps ● 802.11b: 1/2/5.5/11 Mbps ● 802.11g: 6/9/12/18/24/36/48/54 Mbps ● 802.11n: HT20 MCS0-7, HT40 MCS0-7

4.1.1 Wi-Fi 2.4GHz Band RF Transmitter Specification

Table 4. Wi-Fi 2.4GHz Transmitter Performance Specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	2412	-	2484	MHz
Tx power at the antenna port for the highest power level (25°C)	1 Mbps DSSS	-	20	-	dBm
	11 Mbps DSSS	-	18	-	dBm
	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	17	-	dBm
	HT20 MCS0	-	18	-	dBm
	HT20 MCS7	-	16	-	dBm
	HT40 MCS0	-	18	-	dBm
	HT40 MCS7	-	16	-	dBm
Tx EVM	1 Mbps DSSS	-	8	-	%
	11 Mbps DSSS	-	8	-	%
	6 Mbps OFDM	-	-5	-	dB
	54 Mbps OFDM	-	-25	-	dB
	HT20 MCS0	-	-5	-	dB
	HT20 MCS7	-	-28	-	dB
	HT40 MCS0	-	-5	-	dB
	HT40 MCS7	-	-28	-	dB
Carrier Suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-	-45	dBm/MHz
	3rd Harmonic	-	-	-45	dBm/MHz

4.1.2 Wi-Fi 2.4GHz Band RF Receiver Specification

Table 5. Wi-Fi 2.4GHz Receiver Performance Specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	2412	-	2484	MHz
802.11b Rx Sensitivity (8% PER)	1 Mbps DSSS	-	-96	-	dBm
	2 Mbps DSSS	-	-94	-	dBm
	5.5 Mbps DSSS	-	-92	-	dBm
	11 Mbps DSSS	-	-89	-	dBm
802.11g Rx Sensitivity (10% PER)	6 Mbps OFDM	-	-93	-	dBm
	9 Mbps OFDM	-	-92	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-88	-	dBm

	24 Mbps OFDM	-	-85	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-77	-	dBm
	54 Mbps OFDM	-	-75	-	dBm
802.11n Rx Sensitivity (10% PER)	HT20 MCS0	-	-93	-	dBm
	HT20 MCS1	-	-90	-	dBm
	HT20 MCS2	-	-87	-	dBm
	HT20 MCS3	-	-84	-	dBm
	HT20 MCS4	-	-81	-	dBm
	HT20 MCS5	-	-76	-	dBm
	HT20 MCS6	-	-75	-	dBm
	HT20 MCS7	-	-73	-	dBm
	HT40 MCS0	-	-91	-	dBm
	HT40 MCS1	-	-87	-	dBm
	HT40 MCS2	-	-84	-	dBm
	HT40 MCS3	-	-81	-	dBm
	HT40 MCS4	-	-78	-	dBm
	HT40 MCS5	-	-73	-	dBm
	HT40 MCS6	-	-72	-	dBm
	HT40 MCS7	-	-70	-	dBm
Maximum Receive Level	1 Mbps DSSS	-	-	0	dBm
	11 Mbps DSSS	-	-	0	dBm
	6Mbps OFDM	-	-	0	dBm
	54Mbps OFDM	-	-	0	dBm
	MCS 0	-	-	0	dBm
	MCS 7	-	-	0	dBm

4.1.3 Wi-Fi 5GHz Band RF Transmitter Specification

Table 6. Wi-Fi 5GHz Transmitter Performance Specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	5180	-	5825	MHz
Tx power at the antenna port for the highest power level (25°C)	6 Mbps OFDM	-	17	-	dBm
	54 Mbps OFDM	-	13	-	dBm
	HT20 MCS0	-	15	-	dBm
	HT20 MCS7	-	12	-	dBm
	HT40 MCS0	-	15	-	dBm
	HT40 MCS7	-	12	-	dBm
Tx EVM	6 Mbps OFDM	-	-5	-	dB
	54 Mbps OFDM	-	-25	-	dB
	HT20 MCS0	-	-5	-	dB
	HT20 MCS7	-	-28	-	dB
	HT40 MCS0	-	-5	-	dB
	HT40 MCS7	-	-28	-	dB
Carrier Suppression		-	-	-30	dBc

4.1.4 Wi-Fi 5GHz Band RF Receiver Specification

Table 7. Wi-Fi 5GHz Receiver Performance Specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	5180	-	5825	MHz
802.11g Rx Sensitivity (10% PER)	6 Mbps OFDM	-	-91	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-90	-	dBm
	18 Mbps OFDM	-	-87	-	dBm
	24 Mbps OFDM	-	-84	-	dBm

	36 Mbps OFDM	-	-81	-	dBm
	48 Mbps OFDM	-	-76	-	dBm
	54 Mbps OFDM	-	-74	-	dBm
802.11n Rx Sensitivity (10% PER)	HT20 MCS0	-	-91	-	dBm
	HT20 MCS1	-	-89	-	dBm
	HT20 MCS2	-	-86	-	dBm
	HT20 MCS3	-	-83	-	dBm
	HT20 MCS4	-	-80	-	dBm
	HT20 MCS5	-	-75	-	dBm
	HT20 MCS6	-	-73	-	dBm
	HT20 MCS7	-	-72	-	dBm
	HT40 MCS0	-	-89	-	dBm
	HT40 MCS1	-	-86	-	dBm
	HT40 MCS2	-	-83	-	dBm
	HT40 MCS3	-	-80	-	dBm
	HT40 MCS4	-	-77	-	dBm
	HT40 MCS5	-	-72	-	dBm
	HT40 MCS6	-	-71	-	dBm
	HT40 MCS7	-	-69	-	dBm
Maximum Receive Level	6Mbps OFDM	-	-	0	dBm
	54Mbps OFDM	-	-	0	dBm
	MCS 0	-	-	0	dBm
	MCS 7	-	-	0	dBm

4.2 Bluetooth LE Radio Standard

4.2.1 Bluetooth LE RF Transmitter Specification

Table 8. Bluetooth LE Transmitter Performance Specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	2402	-	2480	MHz
Tx Output Power	LE1M	-10	4.5	10	dBm
	LE2M				
Modulation Characteristics (LE1M)	ΔF1 Avg.	225	-	275	kHz
	ΔF2 Max.	185	-	-	kHz
	Modulation Index (ΔF2 Avg./ΔF1 Avg.)	0.8	-	-	
Modulation Characteristics (LE2M)	ΔF1 Avg.	450	-	550	kHz
	ΔF2 Max.	370	-	-	kHz
	Modulation Index (ΔF2 Avg./ΔF1 Avg.)	0.8	-	-	
Modulation Characteristics Stable Modulation (LE1M)	ΔF1 Avg.	247.5	-	252.5	kHz
	ΔF2 Max.	185	-	-	kHz
	Modulation Index (ΔF2 Avg./ΔF1 Avg.)	0.8	-	-	
Modulation Characteristics Stable Modulation (LE2M)	ΔF1 Avg.	495	-	505	kHz
	ΔF2 Max.	370	-	-	kHz
	Modulation Index (ΔF2 Avg./ΔF1 Avg.)	0.8	-	-	

4.2.2 Bluetooth LE RF Receiver Specification

Table 9. Bluetooth LE Receiver Performance Specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency Range	-	2402	-	2480	MHz
Rx Sensitivity @30.8% PER	LE1M	-	-99	-	dBm
	LE2M	-	-95	-	

5 Module Electrical Characteristics

5.1 Module Operating Conditions

Table 10. Module Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VCC	Power supply voltage	3.0	3.3	3.6	V
Ta	Ambient operating temperature	-20	-	85	℃
Ts	Storage temperature	-40	-	125	℃

5.2 Module DC Characteristics

Table 11. DC Characteristic (3.3V, 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIH	Input-High Voltage	LVTTL	2.0	-	-	V
VIL	Input-Low Voltage	LVTTL	-	-	0.8	V
VOH	Output-High Voltage	LVTTL	2.4	-	-	V
VOL	Output-Low Voltage	LVTTL	-	-	0.4	V
VT+	Schmitt-trigger High Level	-	1.78	1.87	1.97	V
VT-	Schmitt-trigger Low Level	-	1.36	1.45	1.56	V
IIL	Input-Leakage Current	VIN=3.3V or 0	-10	±1	10	μA

6 Module Schematics

6.1 Module Internal Schematics

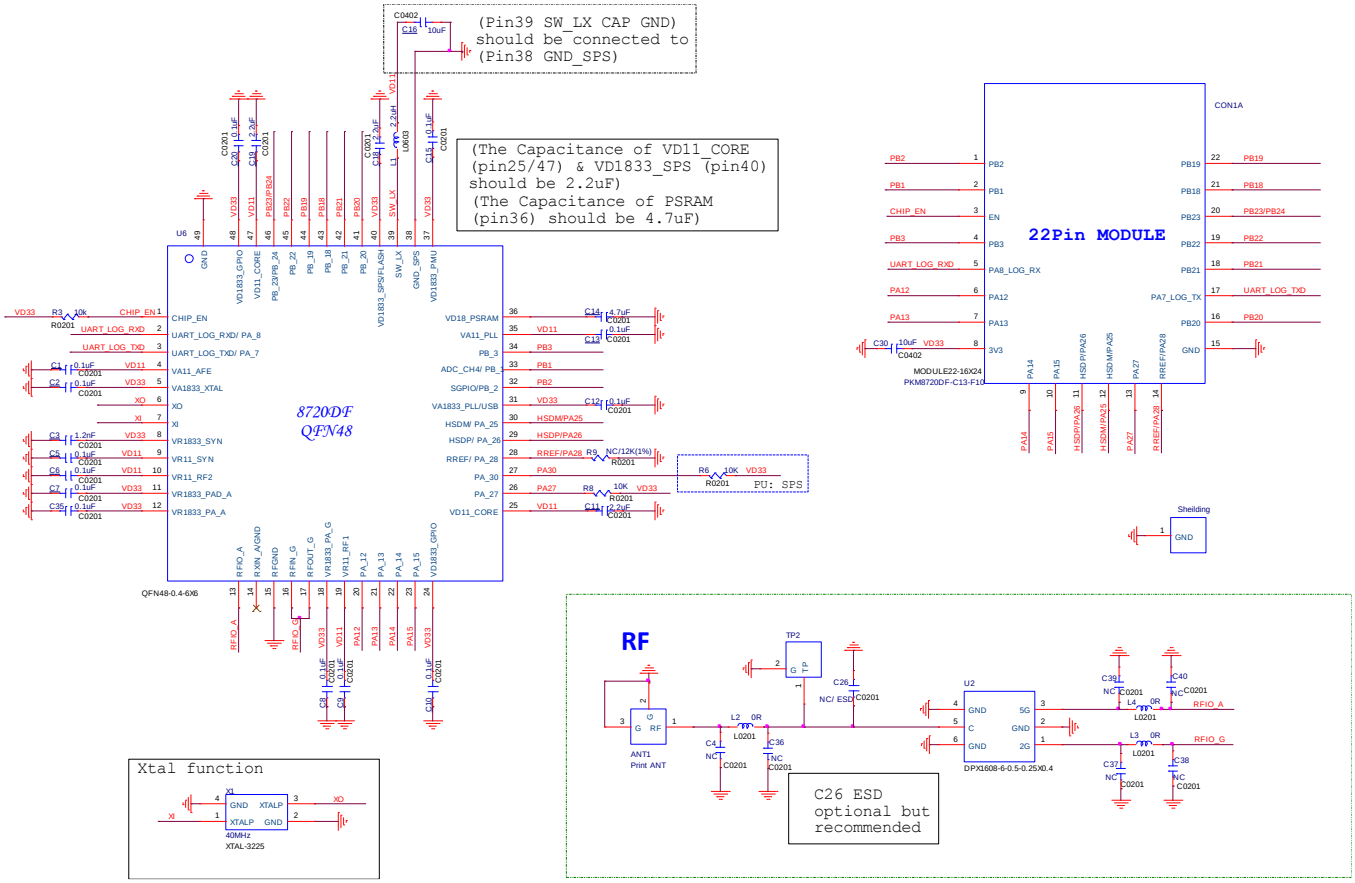


Figure 3. Module internal schematics

6.2 Module Reference Schematics

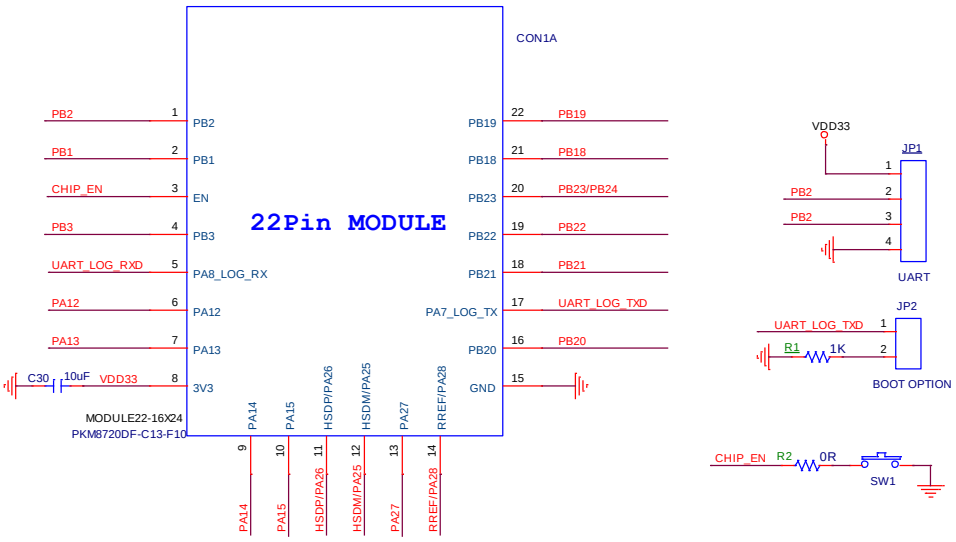


Figure 4. Module Reference schematics

7 Physical Dimensions

Module dimension: 24 ± 0.2mm (L) x 16 ± 0.2mm (W) x 2.3 ± 0.1mm (H)

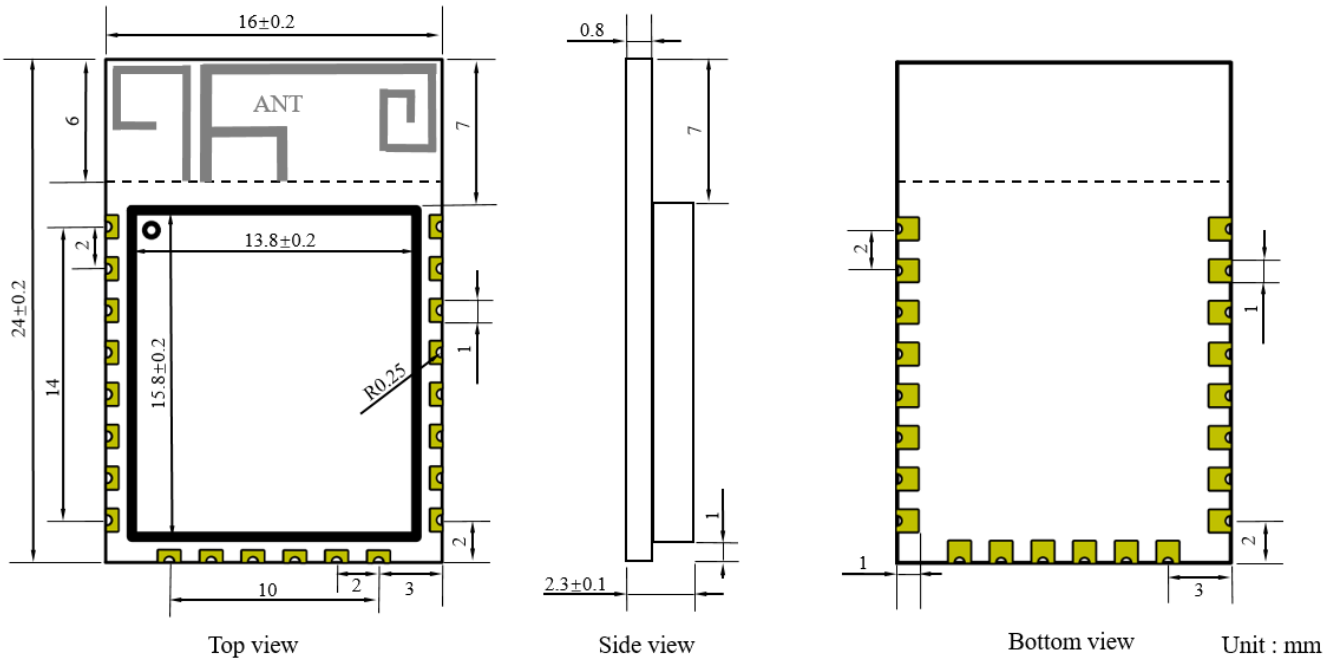


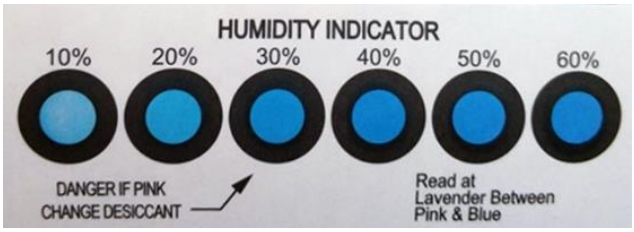
Figure 5. Module Physical Dimensions

8 Product Handling

8.1 Storage Conditions

The storage conditions for a delivered module:

- Moisture sensitive level (MSL): 3
- Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
- Peak package body temperature: 260°C
- A humidity indicator card (HIC) in the packaging bag.



- After bag is opened, the module that will be subjected to reflow solder or other high temperature process must be
  - Mounted within: 168 hours of factory conditions ≤30°C/60% RH, or
  - Stored per J-STD-033
- The module needs to be baked in the following cases:
  - The packaging bag is damaged before unpacking.
  - There is no humidity indicator card (HIC) in the packaging bag.
  - After unpacking, circles of 10% and above on the HIC become pink.
  - The total exposure time has lasted for over 168 hours since unpacking.
  - More than 12 months have passed since the sealing of the bag.
- If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

NOTE

Level and body temperature are defined by IPC/JEDECJ-STD-020.

8.2 Production Instructions

- The PKM8720F-C13-F10 module can be packaged with the SMT process according to the customer's PCB designed to be SMT-packaged. After being unpacked, the module must be soldered within 24 hours. Otherwise, it needs to be put into the drying cupboard where the relative humidity is not greater than 10%; or it needs to be packaged again under vacuum and the exposure time needs to be recorded (the total exposure time cannot exceed 168 hours).
  - SMT devices needed:
    - Mounter
    - SPI
    - Reflow soldering machine
    - Thermal profiler
    - Automated optical inspection (AOI) equipment
  - Baking devices needed:
    - Cabinet oven
    - Anti-electrostatic and heat-resistant trays
    - Anti-electrostatic and heat-resistant gloves
- Baking settings:
  - Temperature: 40°C and ≤ 5% RH for reel package and 125°C and ≤5% RH for tray package (use the heat-resistant tray rather than a plastic container)
  - Time: 168 hours for reel package and 12 hours for tray package
  - Alarm temperature: 50°C for reel package and 135°C for tray package
  - Production-ready temperature after natural cooling: < 36°C
  - Re-baking situation: If a module remains unused for over 168 hours after being baked, it needs to be baked again.
  - If a batch of modules is not baked within 168 hours, do not use the wave soldering to solder them. Because these modules are Level-3 moisture-sensitive devices, they are very likely to get damp when exposed beyond the allowable time. In this case, if they are soldered at high temperatures, it may result in device failure or poor soldering.
- In the whole production process, take electrostatic discharge (ESD) protective measures.

- To guarantee the passing rate, it is recommended to use the SPI and AOI to monitor the quality of solder paste printing and mounting.

8.3 Recommended Oven Temperature Curve

There are some differences between the set temperatures and the actual temperatures. All the temperatures listed in this datasheet are obtained through actual measurements.

For the SMT process, set oven temperatures according to Figure 6.

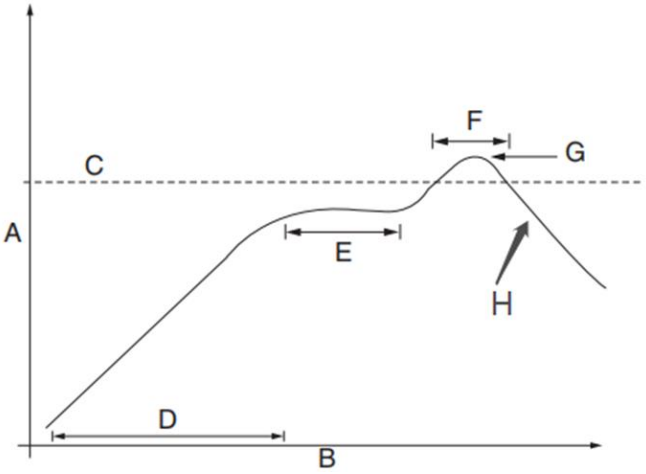


Figure 6. Reflow Soldering Curve Diagram

- D: Rising speed = (1 ~ 3)°C/s, 20°C ~ 150°C, 60s ~ 90s
- E: Average preheating temperature = 150°C ~ 200°C, 60s ~ 120s
- F: Temperature fluctuation > 217°C, 50s to 70s; peak temperature = 235°C ~ 245°C
- H: Drop speed = (1 ~ 4)°C/s

NOTE

Adjust the balance time to ensure the rationalization treatment of gas when tin paste solves. If there are too much gaps on the PCB board, increase the balance time. Considering that the product is long placed in the welding area, to prevent components and bottom plate from damage.

Revision History

Data	Revision	Change Note
2022-12-10	1.0	Initial release

PKM8720DF-C13-F10

Build and Debug Environment Setup – IAR

This document illustrates how to build Realtek low power Wi-Fi software under IAR SDK environment.

1 IAR Build Environment Setup

This chapter illustrates how to setup IAR development environment for Realtek Ameba-D SDK, including building projects, downloading images and debugging.

1.1 Requirement

1.1.1 IAR Embedded Workbench

IAR provides an IDE environment for code building, downloading, and debugging. Check “IAR Embedded Workbench” on http://www.iar.com/, and a trail version is available for 30 days.

Note: To support ARMv8-M with Security Extension (Ameba-D HS CPU, also called KM4), IAR version must be 8.30 or higher.

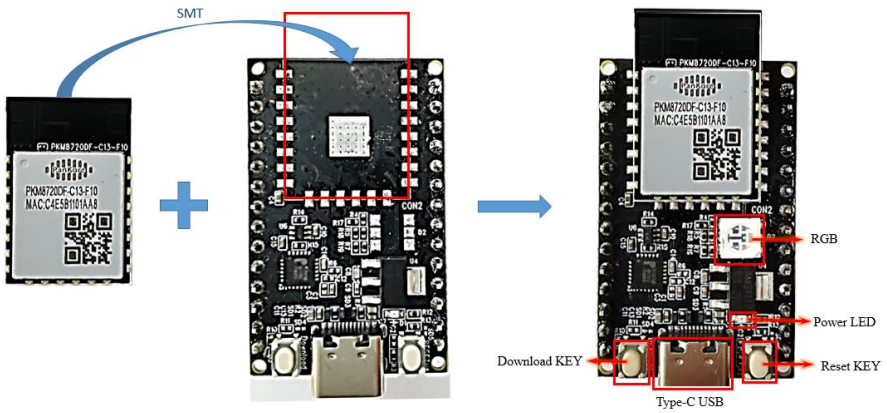
1.1.2 J-Link

If you need to download images or debug code for Ameba-D with IAR, then a J-Link adapter is necessary.

Note: For Ameba-D CPU, the J-Link version must be v9 or higher.

1.1.3 Module or Development Board

PKE8720DF-C13-F10 is a development board designed by Realsil. The PKM8720DF-C13-F10 module is directly attached to the development board, and development board is designed with USB, RGB, LED and key. These peripherals communicate with the module through GPIOs, and the development board can be connected to the computer through USB. The module and peripherals can be controlled and tested by commands from the computer.
After the module is installed, it can communicate with the computer to verify whether it is installed correctly, such as controlling the wifi/BT on the module to TX/RX, or controlling GPIOs to make RGB appear in different colors to determine whether the corresponding GPIOs control is normal. Below is an explanation of module WIFI testing.



1.2 Hardware Configuration

The hardware block diagram of Ameba-D demo board is shown in Fig 1-1.

- USB TO UART: supply power and print logs, baud rate is 115200 bps.
- SWD: SWD interface, used for image downloading and debugging with IAR.
- Reset button: reset Ameba-D to run firmware after IAR completes downloading.

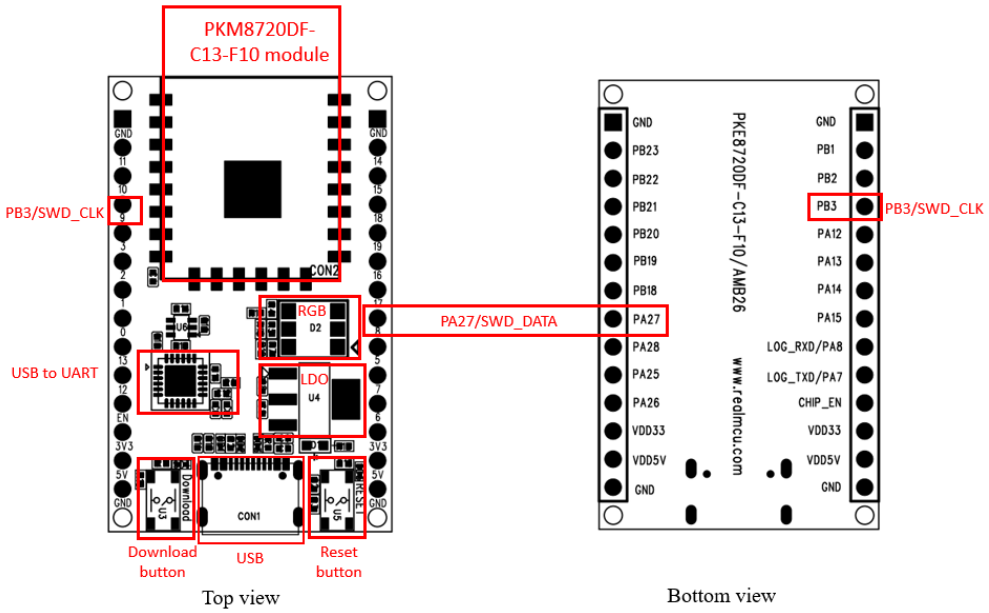


Fig 1-1 Ameba-D demo board

1.2.1 Antenna description

The DUT has one types of antenna, both of which are 2.4 & 5GHz dual band antennas. The information is as follows. PIFA & Dipole antennas are connected with module by RF test point.

1) PCB Onboard Antenna, 2.4G peak gain 2.4dbi, 5G peak gain 3.8dbi.

1.2.2 Connecting with J-Link

Refer to Fig 1-2 and Fig 1-3 to connect Ameba-D SWD interface with J-Link.

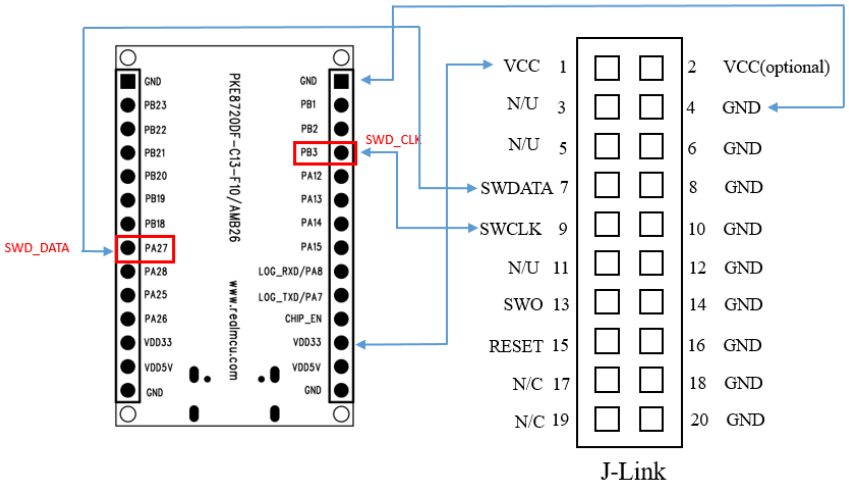


Fig 1-2 J-Link and SWD connection diagram

Fig 1-3 J-Link and Ameba-D SWD connection

1.3 How to Use IAR SDK?

1.3.1 IAR Project Introduction

Because Ameba-D is a dual-core CPU platform, two workspaces are provided to build for each core in **project\realtek_amebaD_va0_example\EWARM-RELEASE**.

- Project_lp_release.eww (KM0 workspace) contains the following projects:
  - km0_bootloader
  - km0_application
- Project_hp_release.eww (KM4 workspace) contains the following projects:
  - km4_bootloader
  - km4_application
  - km4_secure

Each project in KM4 workspace has different build configurations, as Table 1-1 shows.

Table 1-1 Build configurations for KM4 project

Project	Build Configuration	Configure TrustZone	Enable MP
km4_bootloader	km4_bootloader - is[1]	N	N
	km4_bootloader - tz[2]	Y	N
km4_application	km4_application - is	N	N
	km4_application - tz	Y	N
	km4_application - is (mp[3])	N	Y
	km4_application - tz (mp)	Y	Y
km4_secure	km4_secure - tz	Y	N
	km4_secure - tz (mp)	Y	Y

Note:

1. The configuration items with “-is” are ignore secure configuration, which are designed for applications that do not use TrustZone.
2. The configuration items with “-tz” are TrustZone configuration, which are designed for applications that use TrustZone.
3. The configuration items with “mp” are mass production configuration, which are designed for generating MP image.

- For applications that do not use TrustZone, users should apply ignore secure configurations as Table 1-2 shows. The km4_secure project which contains Trustzone-protected code, is not used.
- For applications that use TrustZone, users should apply TrustZone configurations as Table 1-2 shows.

Table 1-2 Configurations for project with/without TrustZone

Project	TrustZone	Normal Image	MP Image
km4_bootloader	N	km4_bootloader - is	km4_bootloader - is
	Y	km4_bootloader - tz	km4_bootloader - tz
km4_application	N	km4_application - is	km4_application - is (mp)
	Y	km4_application - tz	km4_application - tz (mp)
km4_secure	Y	km4_secure - tz	km4_secure - tz (mp)

At the top of the Workspace window, there is a drop-down list where you can choose a build configuration for a specific project.

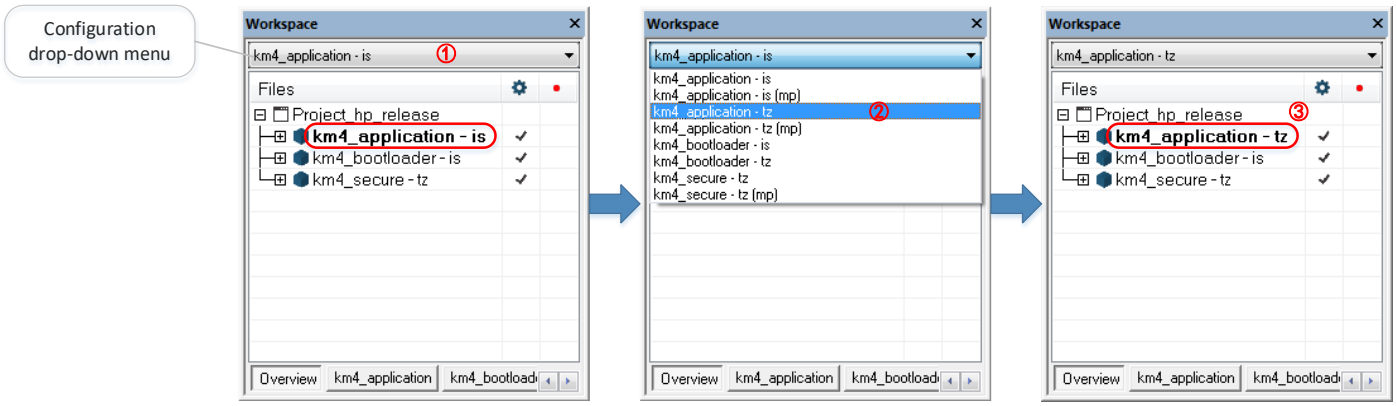


Fig 1-4 How to choose a build configuration

1.3.2 IAR Build

When building SDK for the first time, you should build both KM0 project and KM4 project. Other times, you only need to rebuild the modified project.

1.3.2.1 Building KM0 Project

The following steps show how to build KM0 project:

(1) Open **project\realtek_amebaD_va0_example\EWARM-RELEASE\Project_lp_release.eww**.

(2) Make sure km0_bootloader and km0_application are in Workspace. Click **Project** > **Options**, **General Options** > **Target** > **Processor Variant** > **Core**, verify the CPU configurations according to Fig 1-5.

(3) Right click the project and choose “Rebuild All”, as Fig 1-6 shows. The km0_bootloader and km0_application should compile in order.

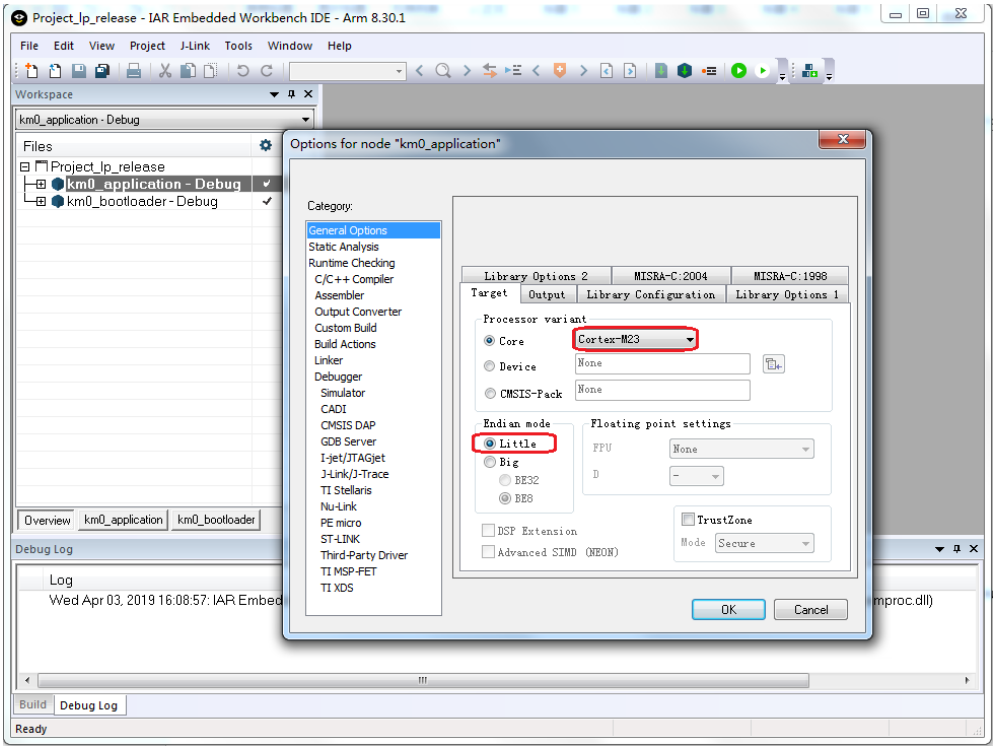


Fig 1-5 KM0 processor options

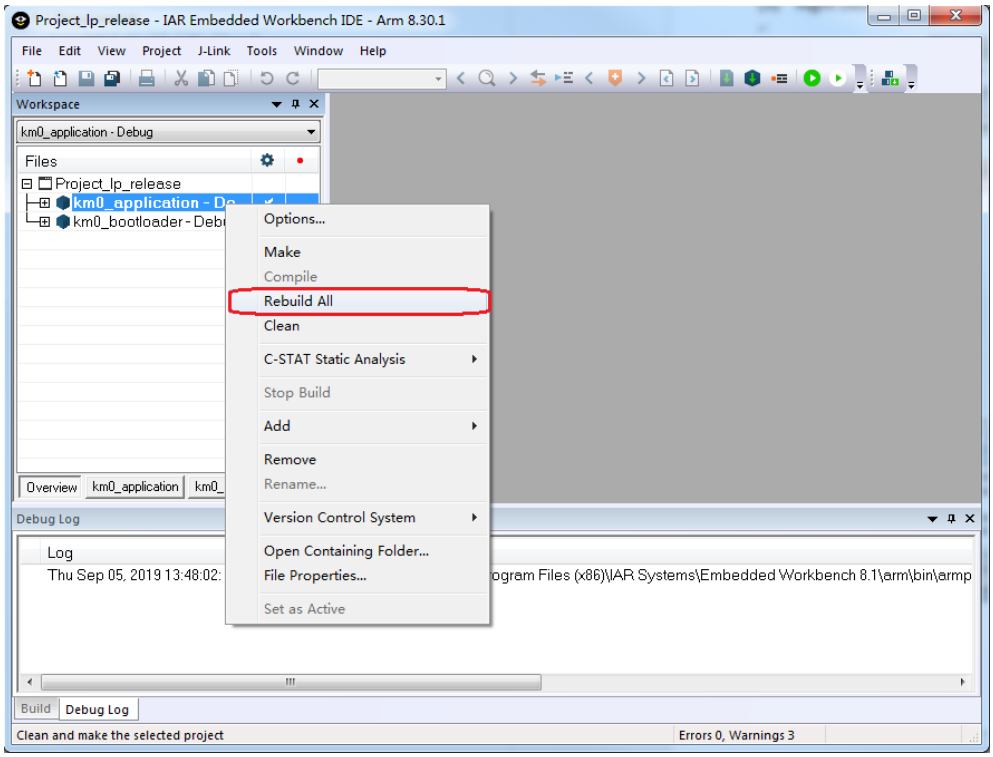
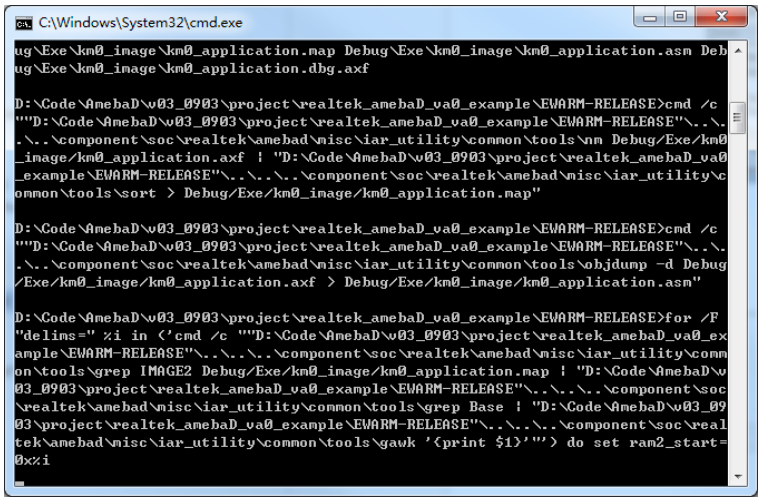


Fig 1-6 Building KM0 project

Note: After building each project, IAR will pop up a command prompt window to execute post-build action to generate images from executable files. This may takes several seconds. Don't stop it while it is in progress. After post-build action is completed, the window would disappear automatically.



(4) After compile, the images km0_boot_all.bin and km0_image2_all.bin can be seen in **project\realtek_amebaD_va0_example\EWARM-RELEASE\Debug\Exe\km0_image**.

1.3.2.2 Building KM4 Project

The following steps show how to build KM4 project:

(1) Open project\realtek_amebaD_va0_example\EWARM-RELEASE\Project_hp_release.eww.

(2) Refer to 1.3.1 and choose the build configurations for each project according to your application.

(3) Click **Project** > **Options**, **General Options** > **Target** > **Processor Variant** > **Core**, verify the CPU configurations according to Fig 1-7.

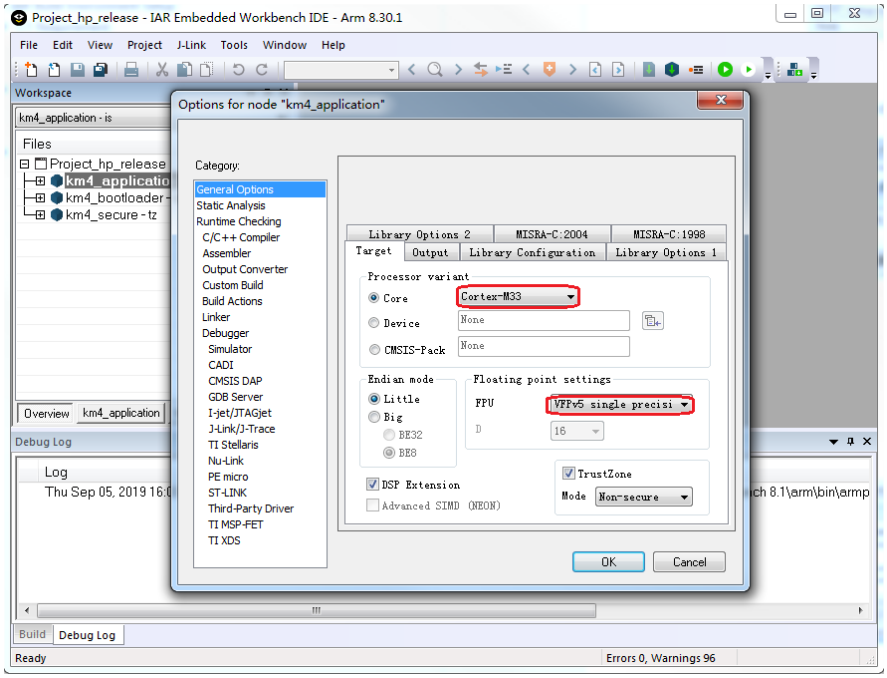


Fig 1-7 KM4 processor options

(4) Right click the project and choose “Rebuild All”, as Fig 1-8 shows. The km4_bootloader, km4_secure and km4_application should compile in order.

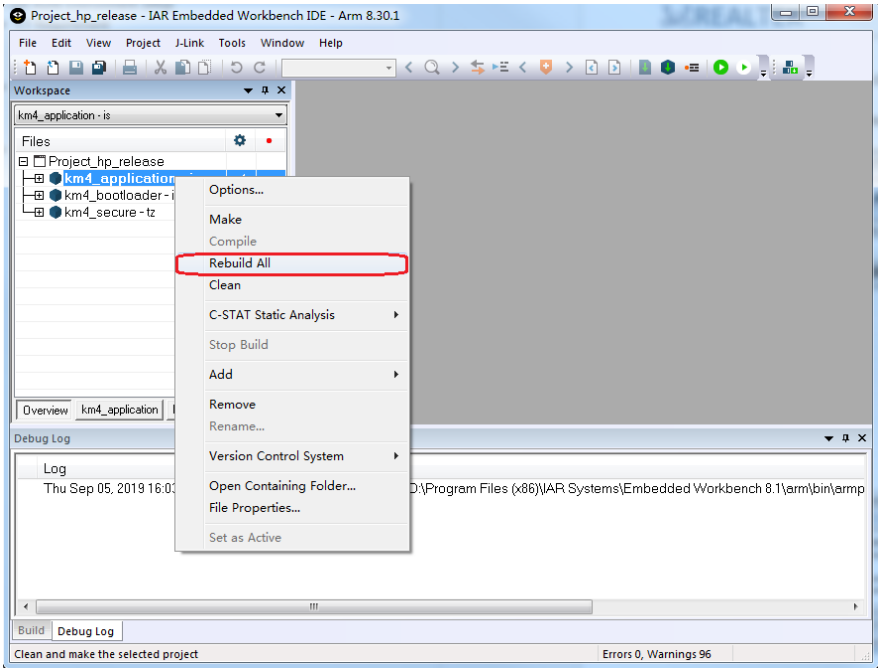
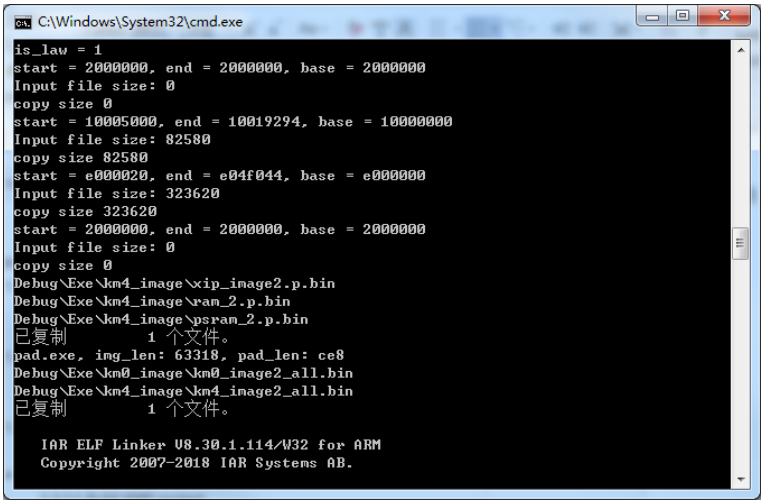


Fig 1-8 Building KM4 project

Note:

- When TrustZone is enable, the km4_secure project must be built before the km4_application project. When TrustZone is not used, there is no need to compile the km4_secure project.
- After building each project, IAR will pop up a command prompt window shown in the figure below to execute post-build action to generate images from executable files. This may takes several seconds. Don’t stop it while it is in progress. After post-build action is completed, the window would disappear automatically.



(5) After compile, the images km4_boot_all.bin and km0_km4_image2.bin can be seen in **project\realtek_amebaD_va0_example\EWARM-RELEASE\Debug\Exe\km4_image**. For MP configurations, the km0_km4_image2_mp.bin would be generated instead.

1.3.3 IAR Download

The generated images can be downloaded in two ways:

- IAR J-Link SWD (introduced in the next section)
- Ameba-D ImageTool, refer to Image Tool User Guide for more information.

Ameba-D demo board supports using J-Link SWD to download and debug. Image of each project can be download individually.

Note: Considering KM4 is powered-on by KM0, you should make sure that KM0 has boot up already before downloading images to KM4. Otherwise, for J-Link, J-Link can't connect to KM4 and show the error message as Fig 1-9 shows.

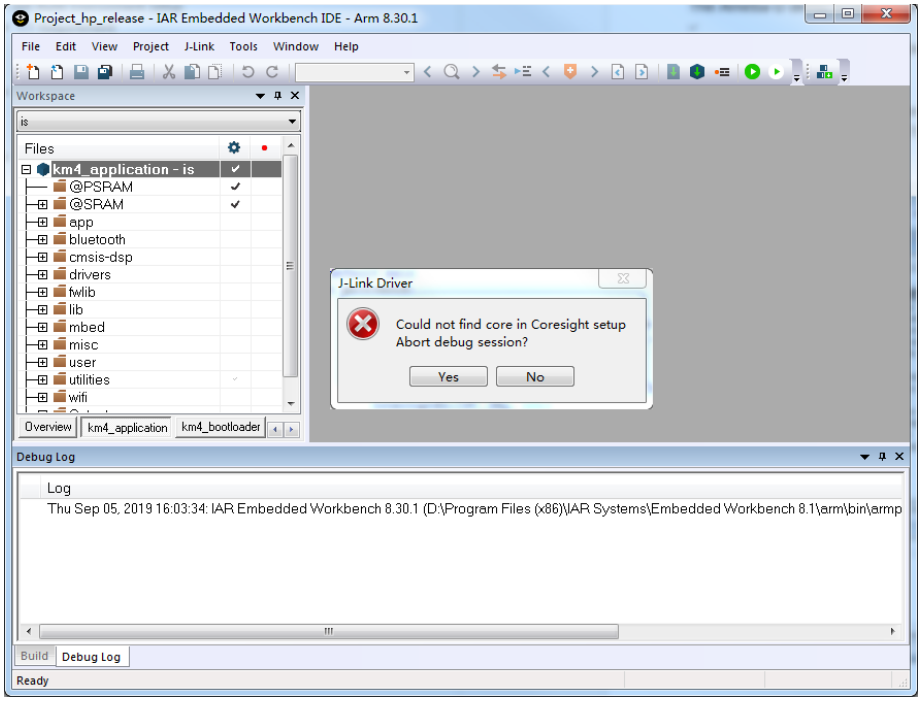


Fig 1-9 J-Link cannot find KM4

As a result, if the Flash memory is empty, the sequence to download images is:

(1) Download for km0_bootloader and km0_application projects
(2) Click **Reset** button on demo board to make KM0 boots up
(3) Download for km4_bootloader and km4_application projects

During development, if Flash memory is not empty and KM0 can boot up successfully, then you can download updated images to KM4 directly, and there is no need to re-download for KM0.

The following steps show how to download image for the target project with IAR. If there is an error like Fig 1-17 displayed in IAR window, refer to 1.3.4.2.

(1) Choose the target project display in Workspace window, for example, km4_bootloader as Fig 1-10 shows.
(2) If using J-link debugger, check whether the J-link debugger setting is correct.
    a) Click **Project** > **Options** > **Debugger** > **Setup** > **Driver**, and choose "J-Link/J-Trace", as Fig 1-11 shows.
    b) Click **Debugger** > **J-Link/J-Trace** > **Connection** > **Interface**, and choose "SWD", as Fig 1-12 shows.

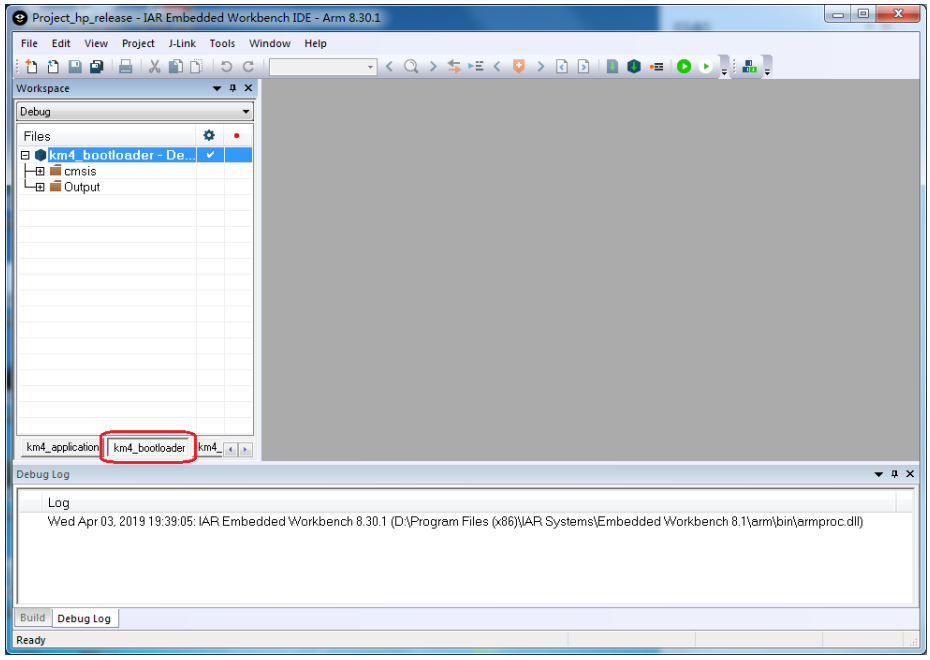


Fig 1-10 Switching to the target project view

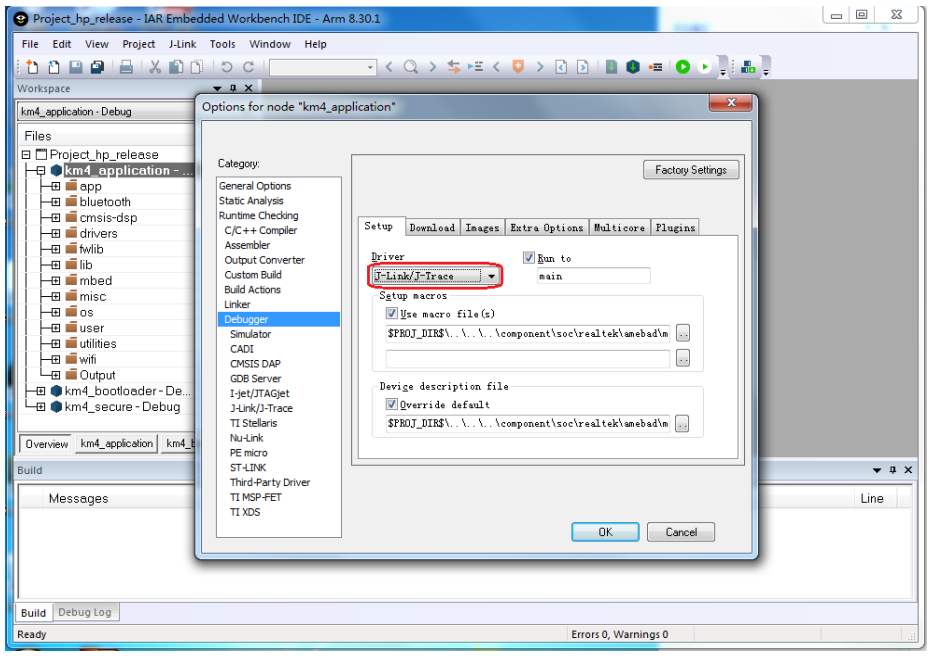


Fig 1-11 J-Link debugger setup

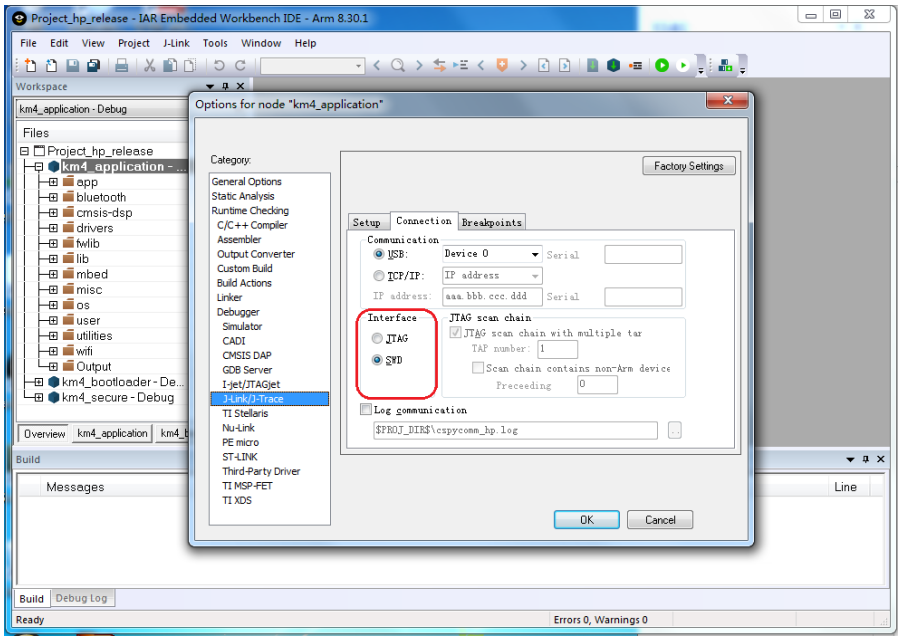


Fig 1-12 J-Link interface setup

(3) Click **Project** > **Download** > **Download active application**, image downloading starts.
When downloading, Ameba-D prints the log, as Fig 1-13 shows. You can check the log to see if download is successful.

```
[FlashInit] image_size:f48, link_address:8000000, flags:0
[FlashErase] block_start:0, block_size:1000
[FlashWrite] block_start:0, offset_into_block:0, count:f48
[FlashInit] image_size:82000, link_address:8006000, flags:0
[FlashErase] block_start:6000, block_size:1000
[FlashErase] block_start:7000, block_size:1000
[FlashErase] block_start:8000, block_size:1000
[FlashErase] block_start:9000, block_size:1000
[FlashErase] block_start:a000, block_size:1000
[FlashErase] block_start:b000, block_size:1000
[FlashErase] block_start:c000, block_size:1000
[FlashErase] block_start:d000, block_size:1000
[FlashErase] block_start:e000, block_size:1000
[FlashErase] block_start:f000, block_size:1000
[FlashErase] block_start:10000, block_size:1000
[FlashErase] block_start:11000, block_size:1000
[FlashWrite] block_start:6000, offset_into_block:0, count:c000
[FlashErase] block_start:12000, block_size:1000
[FlashErase] block_start:13000, block_size:1000
[FlashErase] block_start:14000, block_size:1000
[FlashErase] block_start:15000, block_size:1000
[FlashErase] block_start:16000, block_size:1000
[FlashErase] block_start:17000, block_size:1000
[FlashErase] block_start:18000, block_size:1000
[FlashErase] block_start:19000, block_size:1000
[FlashErase] block_start:1a000, block_size:1000
[FlashErase] block_start:1b000, block_size:1000
[FlashErase] block_start:1c000, block_size:1000
[FlashErase] block_start:1d000, block_size:1000
[FlashWrite] block_start:12000, offset_into_block:0, count:c000
[FlashErase] block_start:1e000, block_size:1000
[FlashErase] block_start:1f000, block_size:1000
[FlashErase] block_start:20000, block_size:1000
[FlashErase] block_start:21000, block_size:1000
[FlashErase] block_start:22000, block_size:1000
[FlashErase] block_start:23000, block_size:1000
[FlashErase] block_start:24000, block_size:1000
```

Fig 1-13 Downloading log

(4) You can also erase all parts of the Flash memory if necessary.

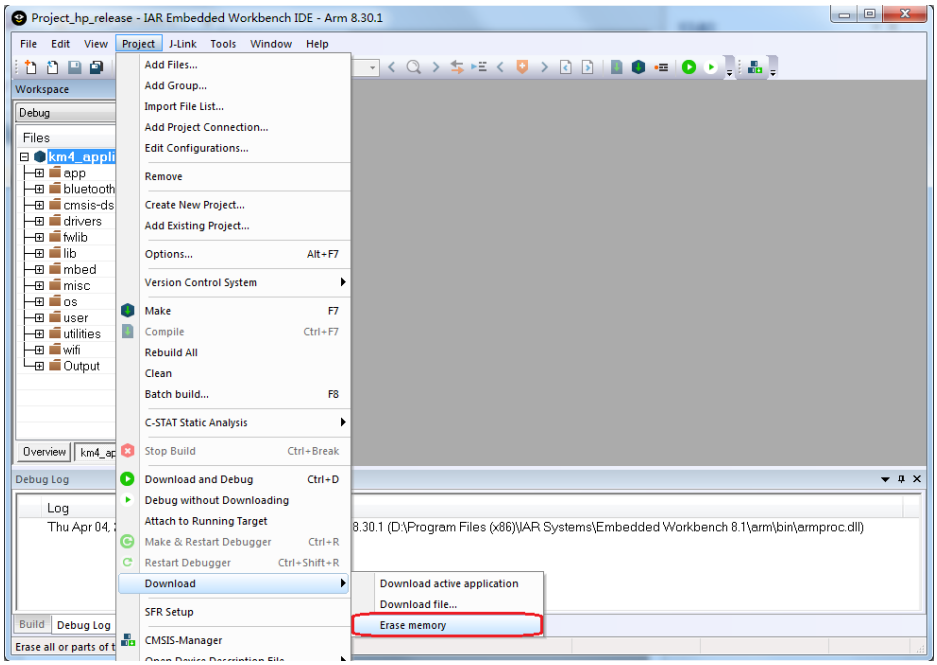


Fig 1-14 Erasing Flash memory

1.3.4 IAR Debug

You can debug or trace KM0 and KM4 system individually with J-Link SWD.

Note: Considering KM4 is power-on by KM0, you should make sure that KM0 has already boot up before debug KM4. For KM0, there is no such requirement because KM0 is power-on immediately after reset.

1.3.4.1 J-Link Debug

Follow the steps to debug and trace code of target project with IAR by J-Link:

(1) Set the target project as active project and verify the debugger configurations as step (1) and (2).

(2) Click **Project** > **Download and Debug** or **Project** > **Debug without Downloading**.

- Download and Debug: downloads the application and debug the project object file. If necessary, a make will be performed before download to ensure the project is up to date.
- Debug without Downloading: debug the project object file

(3) When starting IAR C-SPY to debug, it will firstly reset the target CPU and run to the main function, as Fig 1-15 shows.

(4) Toggles a breakpoint at the statement or instruction that contains or is located near the cursor in the source window. The “Toggle Breakpoint” button is on the debug toolbar, as Fig 1-16 shows.

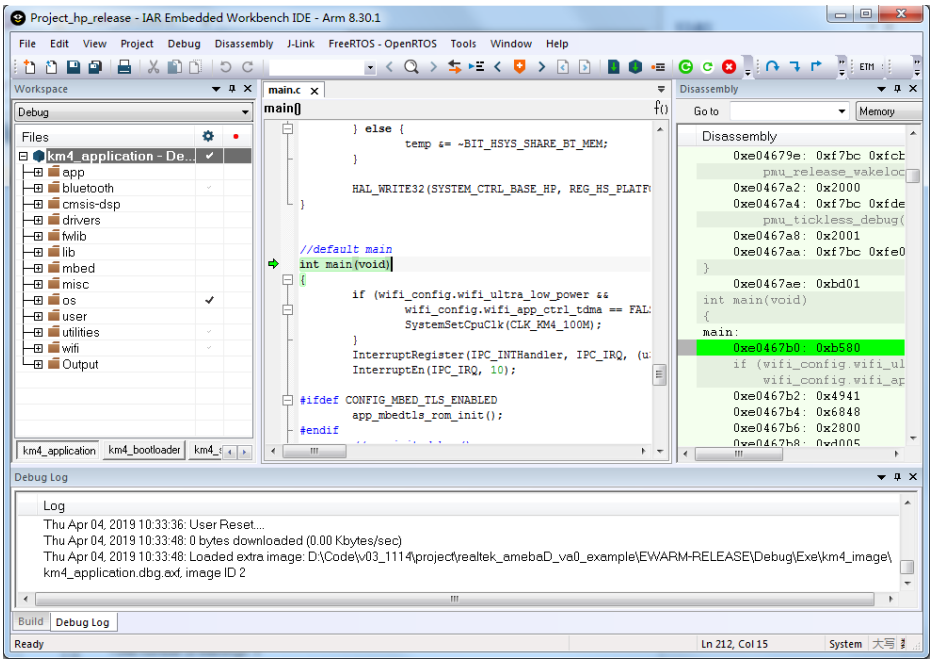


Fig 1-15 Running to main() when debug

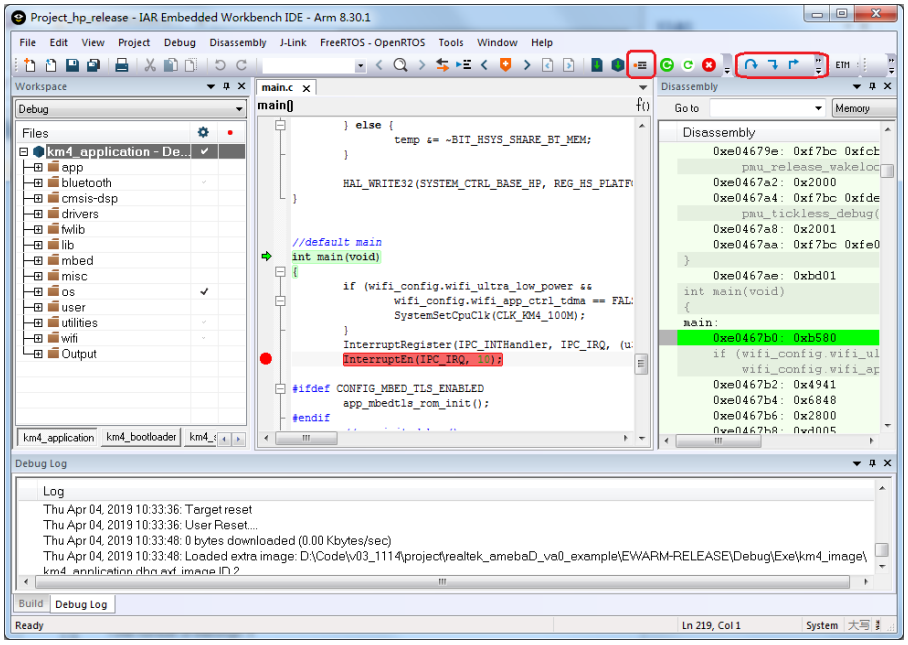


Fig 1-16 Toggle breakpoint

(5) You can trace code step by step with “Step Into” or “Go” until triggering a breakpoint. These function buttons are available on toolbar.

1.3.4.2 IAR Debug or Download Error

Because Ameba-D has two CPU cores, and a post-build script will be run after make, sometimes the debug or download thread cannot get the correct AXF file for debug or download, the error like Fig 1-17 happens.

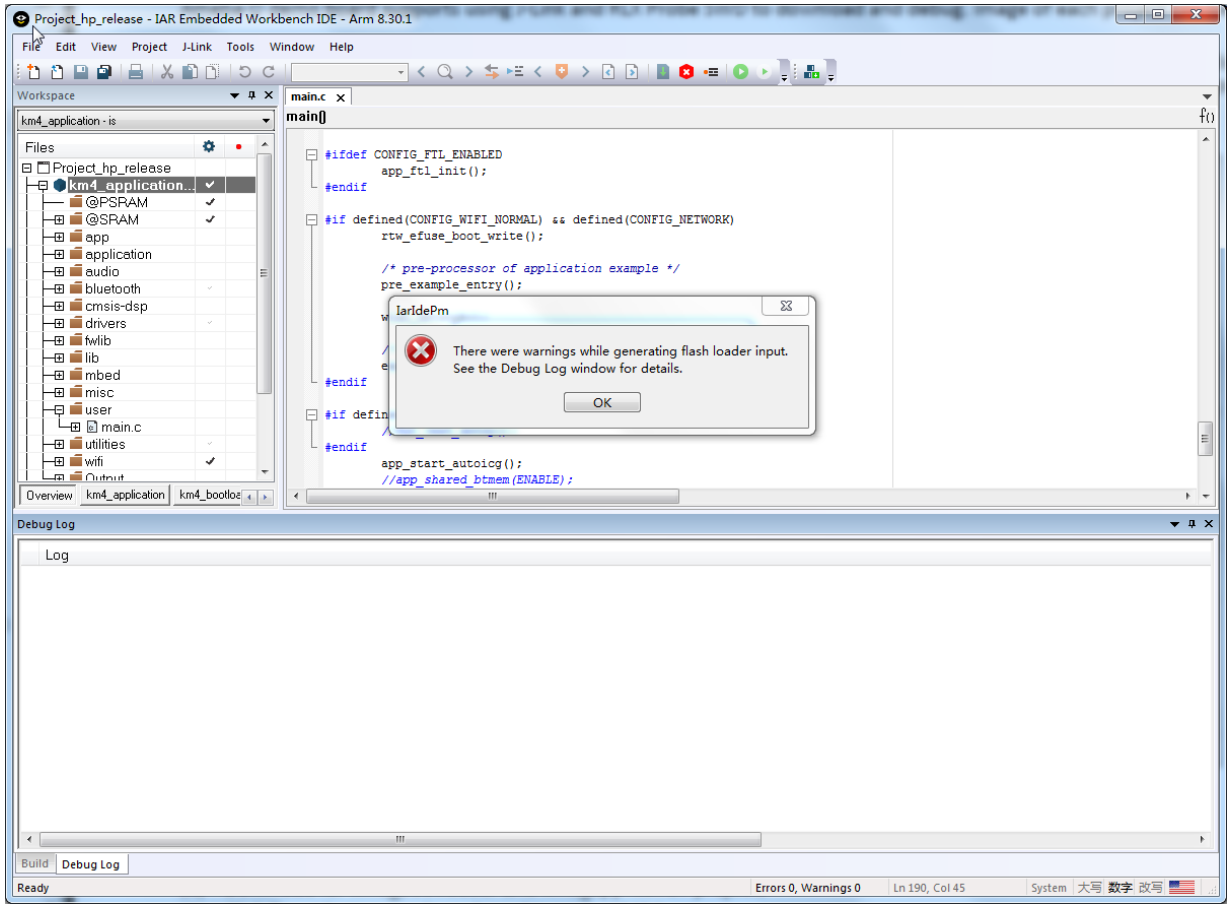


Fig 1-17 IAR debug or download error

To avoid this error, you should build manually before debug or download, and disable auto-build from **Tools** > **Options** > **Project** > **Make before debugging**, as Fig 1-18 shows.

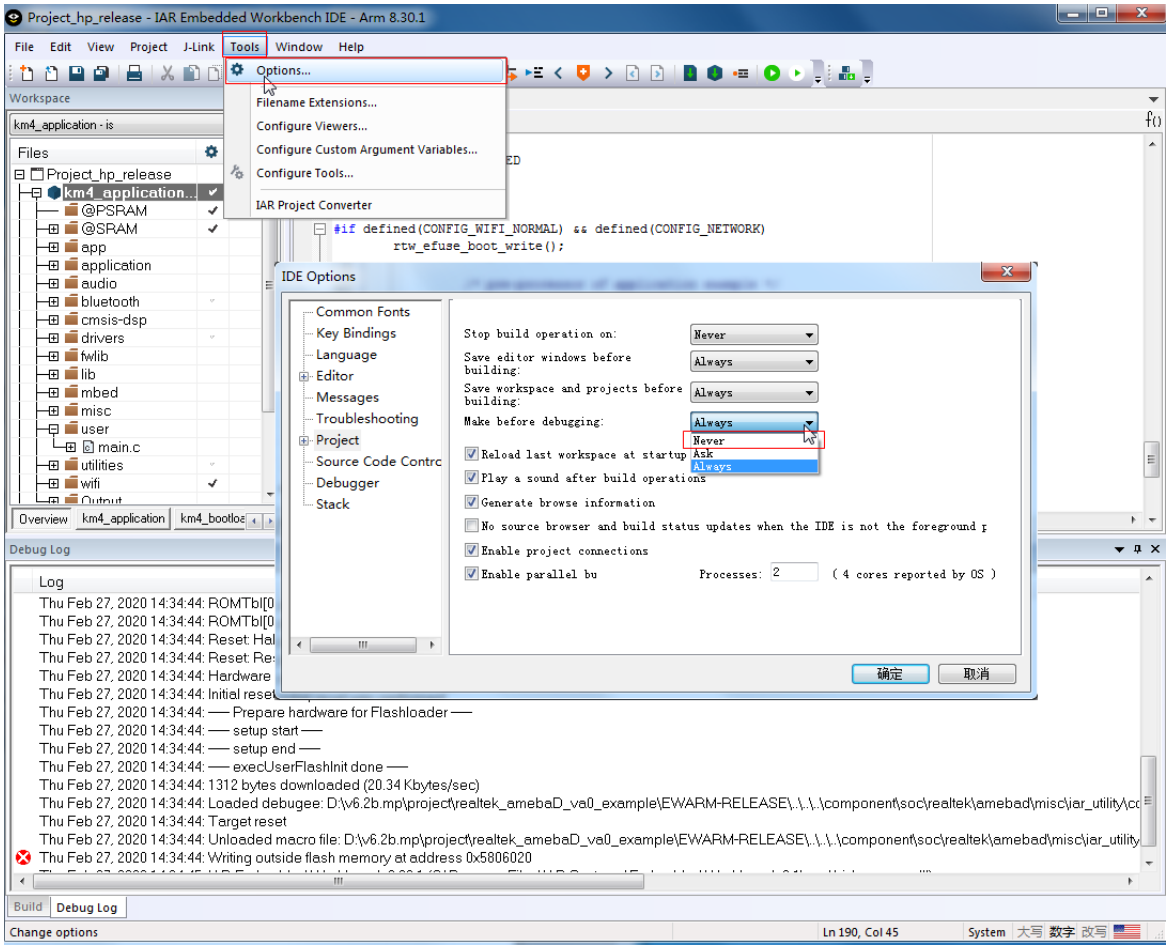


Fig 1-18 IDE options

1.3.5 IAR Memory Configuration

1.3.5.1 Configuring Memory from IAR IDE

In order to allow users to manage memory flexibly, there are some configurations to put some code into certain memory region.
In IAR workspace, there are “@PSRAM” and “@SRAM” group. The code in “@PSRAM” group would be linked and loaded into PSRAM, and the code in “@SRAM” group would be linked and loaded into SRAM. The rest of code will be placed on Flash and execute in place.

Note: Considering only SRAM and PSRAM contains secure regions, the code in km4_secure project should be placed either in “@PSRAM” or in “@SRAM”. It can’t be placed outside these two groups.

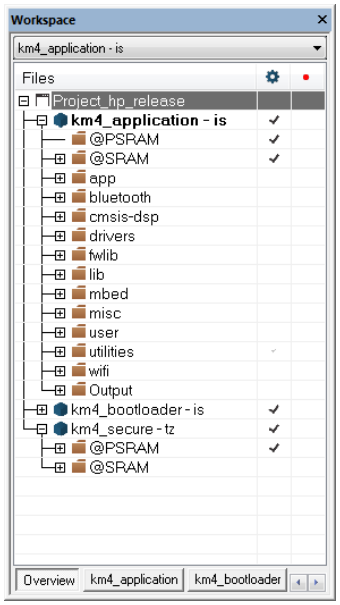


Fig 1-19 Memory location configuration

1.3.5.2 Configuring Memory from ICF File

IAR uses ICF (IAR Configuration File) to configure memory allocation, so users can configure memory allocation by ICF file.

ICF file of Ameba-D location:

- "project\realtek_amebaD_va0_example\EWARM-RELEASE\ rtl8721dhp_image2_is.icf" for ignore secure project
- "project\realtek_amebaD_va0_example\EWARM-RELEASE\ rtl8721dhp_image2_tz.icf" for TrustZone project

If having a good understand of the format of ICF, users can modify the section location in ICF file.

1.4 How to Build Sample Code?

The example source code is located in **project\realtek_amebaD_va0_example\example_sources**. To build sample code, you should copy the "main.c" file in the target example to **project\realtek_amebaD_va0_example\src\src_hp** and replace the original one.

For example, you can copy "main.c" from **project\realtek_amebaD_va0_example\example_sources\I2C\mbed\i2c_int_mode\src** to use i2c_int_mode example code, as Fig 1-20 shows.

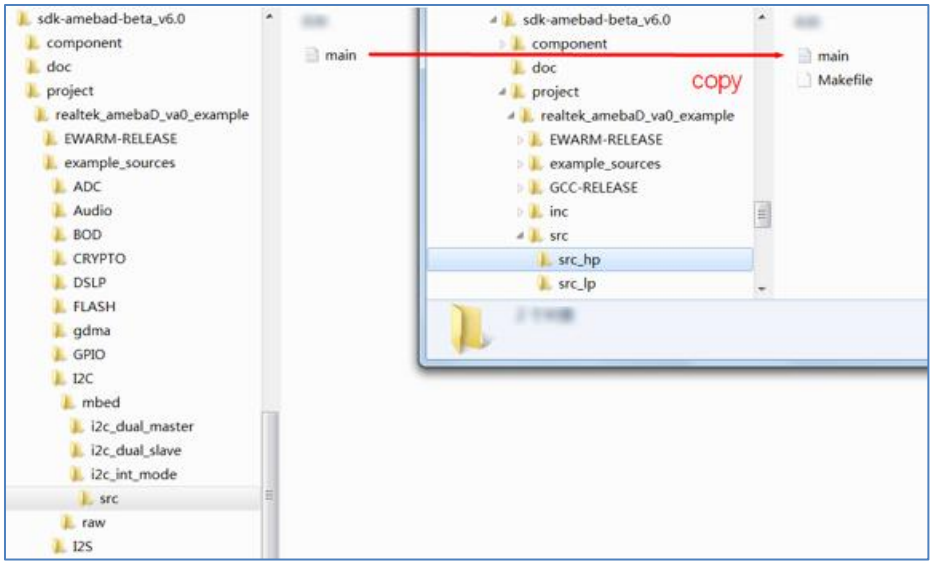
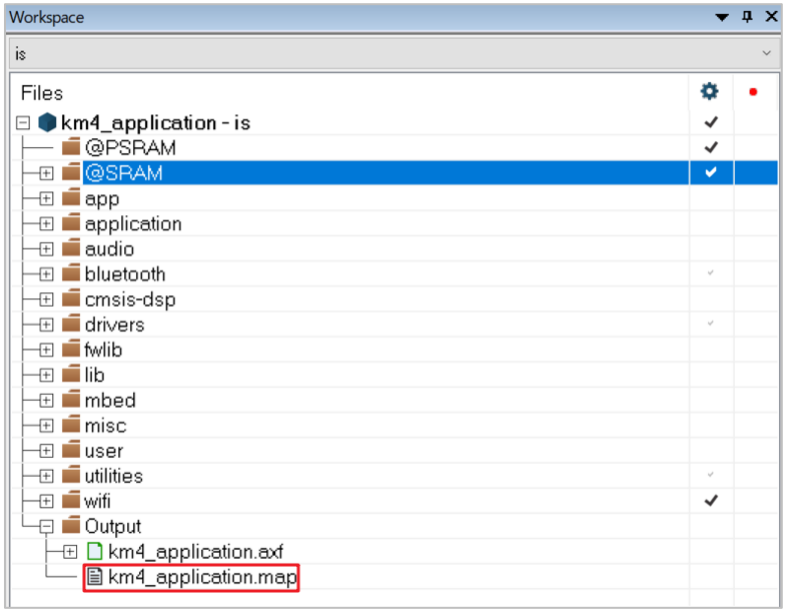


Fig 1-20 Building sample code

1.5 Used Memory Size Calculation

This section explains how to calculate used memory size by users in IAR project, whose version is IAR 8.30.1 or higher. You can refer to "km4_application.map" to observe them after project build. This file can be found in the following folders:

- Project folder: project\realtek_amebaD_va0_example\EWARM-RELEASE\Debug\List\km4_application
- IAR GUI's folder: Output



1.5.1 Memory Section

- A7 (PSRAM): This section is read-write data in PSRAM (0x2000000 to 0x23FFFFF).
- BTTRACE: This section is reserved for BTTRACE.
- A5 (XIP): This section is read-only data in XIP.

- A4 (SRAM): This section is read-write data in SRAM.
- P1 (SRAM): This is BSS section in SRAM.

1.5.2 Memory Size

1.5.2.1 Memory Size in SRAM

There are two sections resident in SRAM, which are A4 and P1. As we can see from the map file, for standard SDK, these two sections use almost all of the memory space from SRAM (476KB).

- A4 has size 0x17ad7.

```
"A4":                                       0x17ad7
  IMAGE2                          0x1000'5000  0x17ad7  <Block>
    .ram image2.entry             0x1000'5000    0x20  <Block>
      .image2.entry.data  rw data 0x1000'5000     0xc  rtl8721dhp app start.o [1]
```

- P1 has size 0x5dfc8.

```
"P1":                                       0x5dfc8
  .ram heap.data                  0x1001'cae0  0x50000  <Block>
    .ram image2.bfsram.data
                                  0x1001'cae0  0x50000  <Block>
      .bfsram.data        uninit  0x1001'cae0  0x50000  freertos heap5 config.o [1]
```

So totally 0x17ad7 + 0x5dfc8 = 470K bytes memory in SRAM is used.

The total SRAM space is defined in project\realtek_amebaD_va0_example\EWARM-RELEASE\rtl8721d_memory_layout_is.icf.

```
define symbol __ICFEDIT_region_HS_BD_RAM_NS_start__          = 0x10005000;
define symbol __ICFEDIT_region_HS_BD_RAM_NS_end__            = 0x1007C000-1;
```

For this case, the total size of SRAM is 0x1007C000 – 0x10005000 = 0x77000 = 476K bytes, there is still 6K (= 476K – 470K) bytes free SRAM space.

1.5.2.2 Memory Size in PSRAM

There is one section in PSRAM called A7, the memory space from PSRAM (4MB).

A7 has size 0x54800.

```
"A7":                                       0x54800
  IMG2 PSRAM                    0x200'0000      0x0  <Block>
  .psram ns.bss                 0x200'0000  0x54800  <Block>
    .psram.bss                  0x200'0000  0x54800  <Block>
      .psram.bss          uninit  0x200'0000  0x54800  rtw opt skbuf.o [1]
```

So totally 0x54800 = 338K bytes memory in PSRAM is used.

1.5.2.3 Memory Size in XIP

XIP can only place text section, so there is only one section called A5.

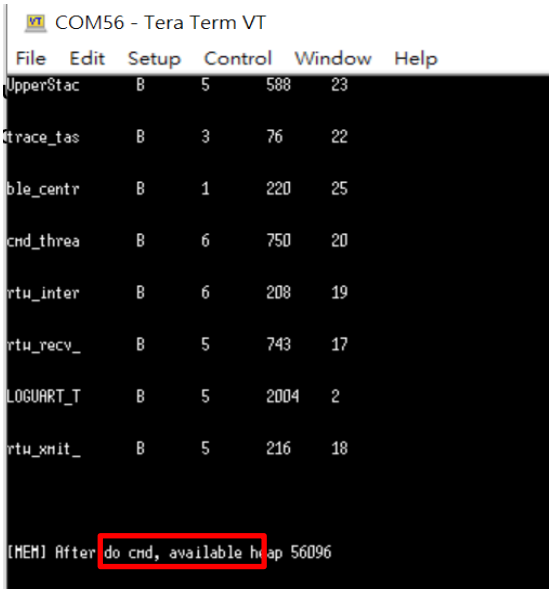
A5 has size 0x8afe8.

```
"A5":                                          0x8afe8
  .xip image2.text                 0xe00'0020  0x8afe8  <Block>
    .text                  ro code  0xe00'0020     0xfc  app task.o [1]
    .text.os msg queue create intern
                           ro code  0xe00'011c     0x40  os msg.o [2]
```

So totally 0x8afe8 = 555K bytes memory in XIP is used.

1.5.2.4 Available Heap Size

When calculating total used memory size, available heap size after WLAN association and BT connection needs to be considered. In the above case, it is 56096 bytes.



Finally, you can use total SRAM 476K bytes to subtract these sections of memory to obtain totally free global memory and free heap in SRAM.

Formula is as below:

- SRAM free global memory: 476K – “A4” – “P1” = 476*1024 – 96983 – 384968= 5473 (bytes)
- Available heap: 56096 bytes.
- Totally free SRAM memory and heap: 5473 + 56096 = 61569 (bytes)
- Totally free PSRAM memory: 4*1024*1024 – 338 * 1024 (A7) = 3848192 (bytes)

1.6 warning

1.6.1 Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

IMPORTANT NOTE:
FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device and its antenna(s) must not be co-located with any other transmitters except in accordance with FCC multi-transmitter product procedures.
Refering to the multi-transmitter policy, multiple-transmitter(s) and module(s) can be operated simultaneously without C2PC.

This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated.
Additional testing and certification may be necessary when multiple modules are used.

List of applicable FCC rules
This module has been tested and found to comply with 15. 249, 15.247 and 15.407 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

USERS MANUAL OF THE END PRODUCT:
In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied. The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. If the size of the end product is smaller than 8x10cm, then additional FCC part 15.19 statement is required to be available in the users manual: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains TX FCC ID: 2BASB-PKM8720DFC ". If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.