

1 OF 22

*CPU_ADE_P_1744P

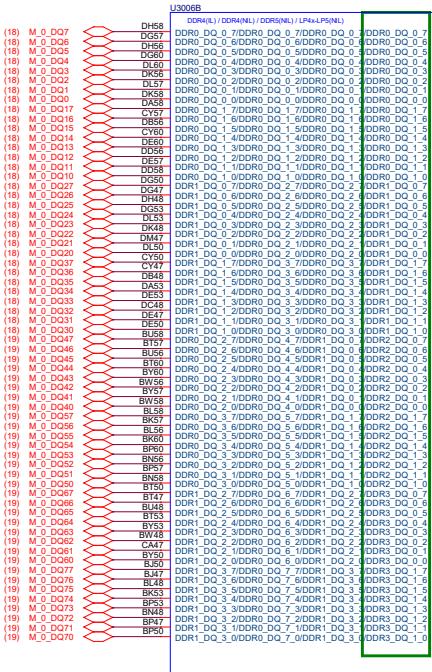
DDI Port Signal Mapping for HDMI*

Description	Signal Mapping		
	DDI	HDMI (Default non-reversed)	HDMI (Reversed)
Main Link (Tx)	DDI_TX0	HDMI Data_2	HDMI CLK
	DDI_TX1	HDMI Data_1	HDMI Data_0
	DDI_TX2	HDMI Data_0	HDMI Data_1
	DDI_TX3	HDMI CLK	HDMI Data_2

20220701a

ALDER LAKE Processor LPDDR4x

J-BDDBA (NTT)



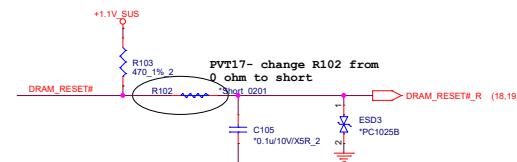
3.05.03

SVD_1
SVD_2
SVD_3
SVD_4
SVD_6
SVD_7
SVD_8
SVD_9
SVD_10
SVD_13
SVD_15
SVD_16
SVD_20

— 1 —

OF 22

— 1 —



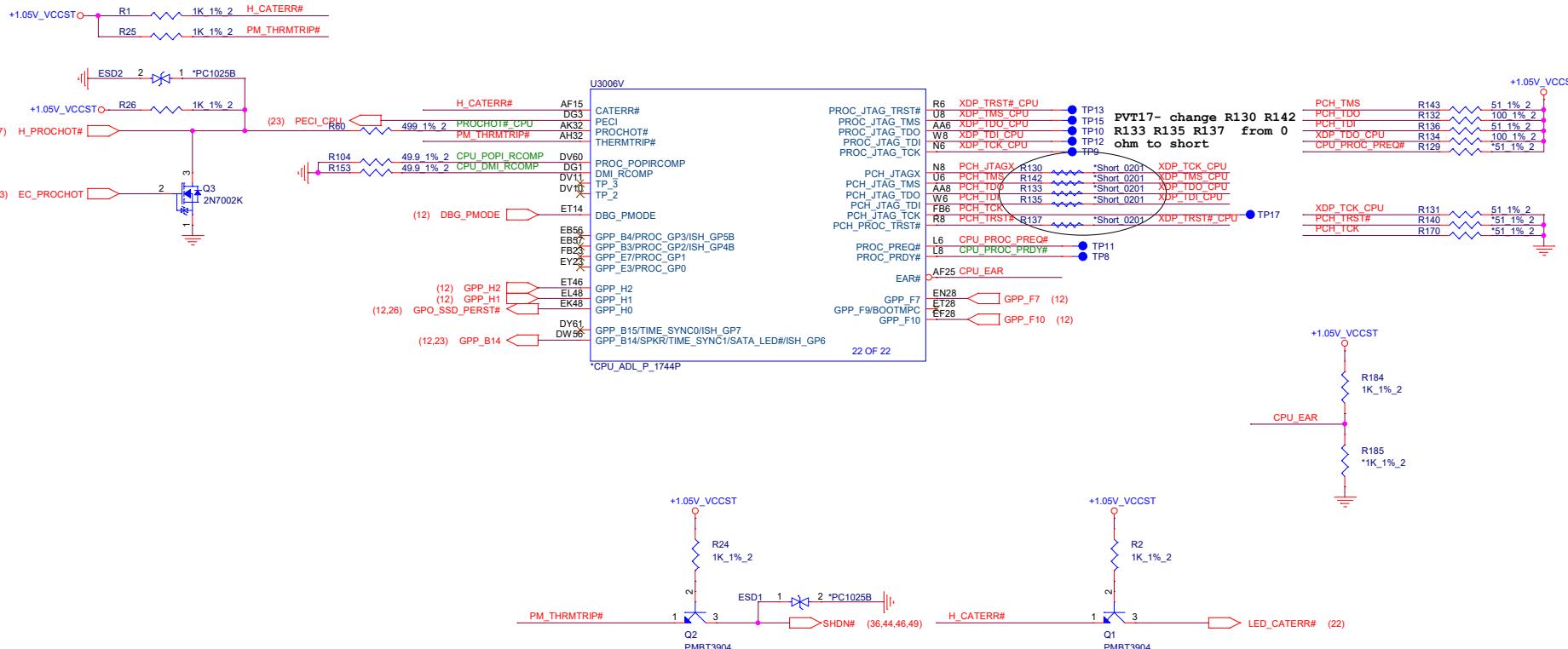
This part should not contain any substances which are specified in EM-

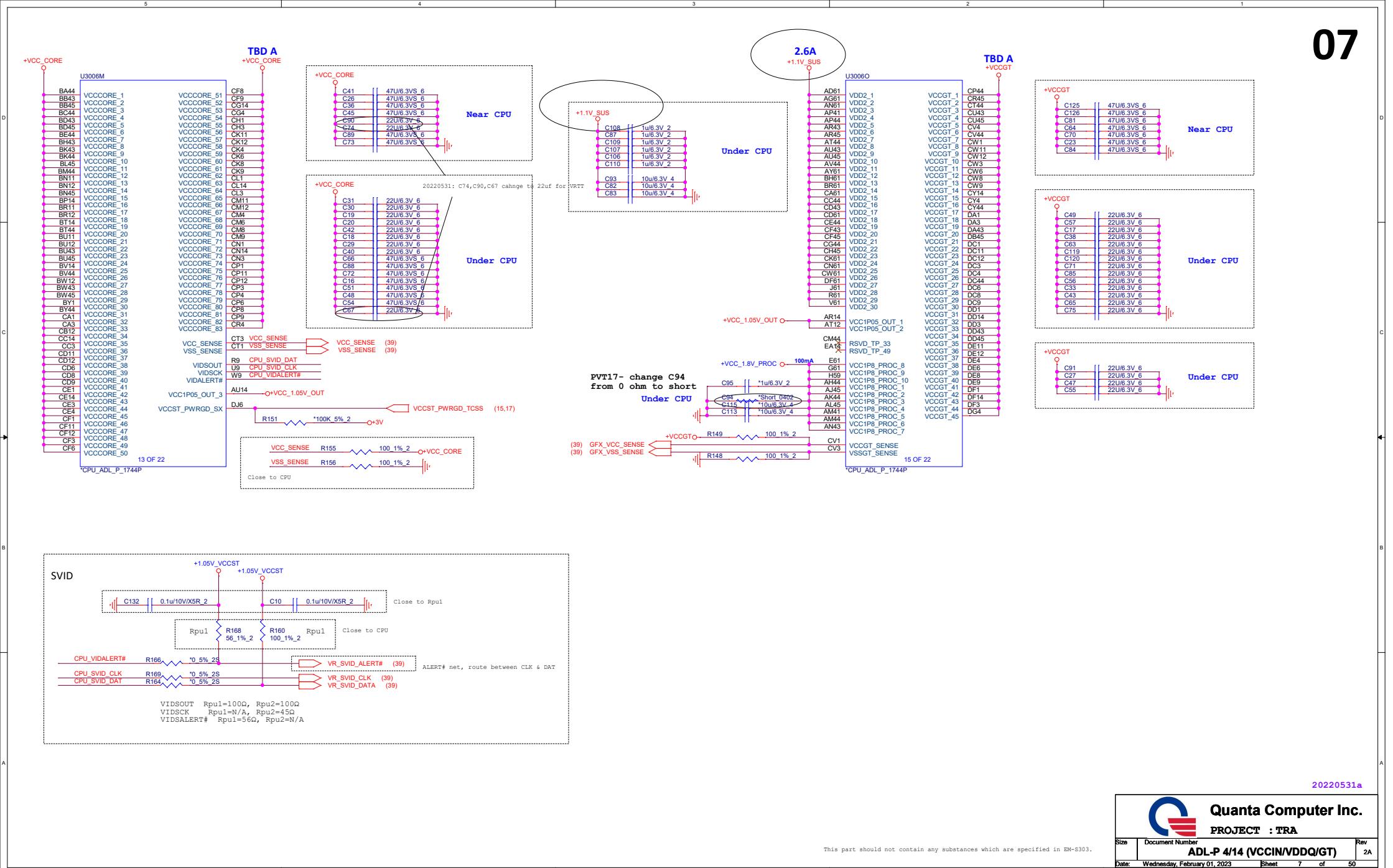
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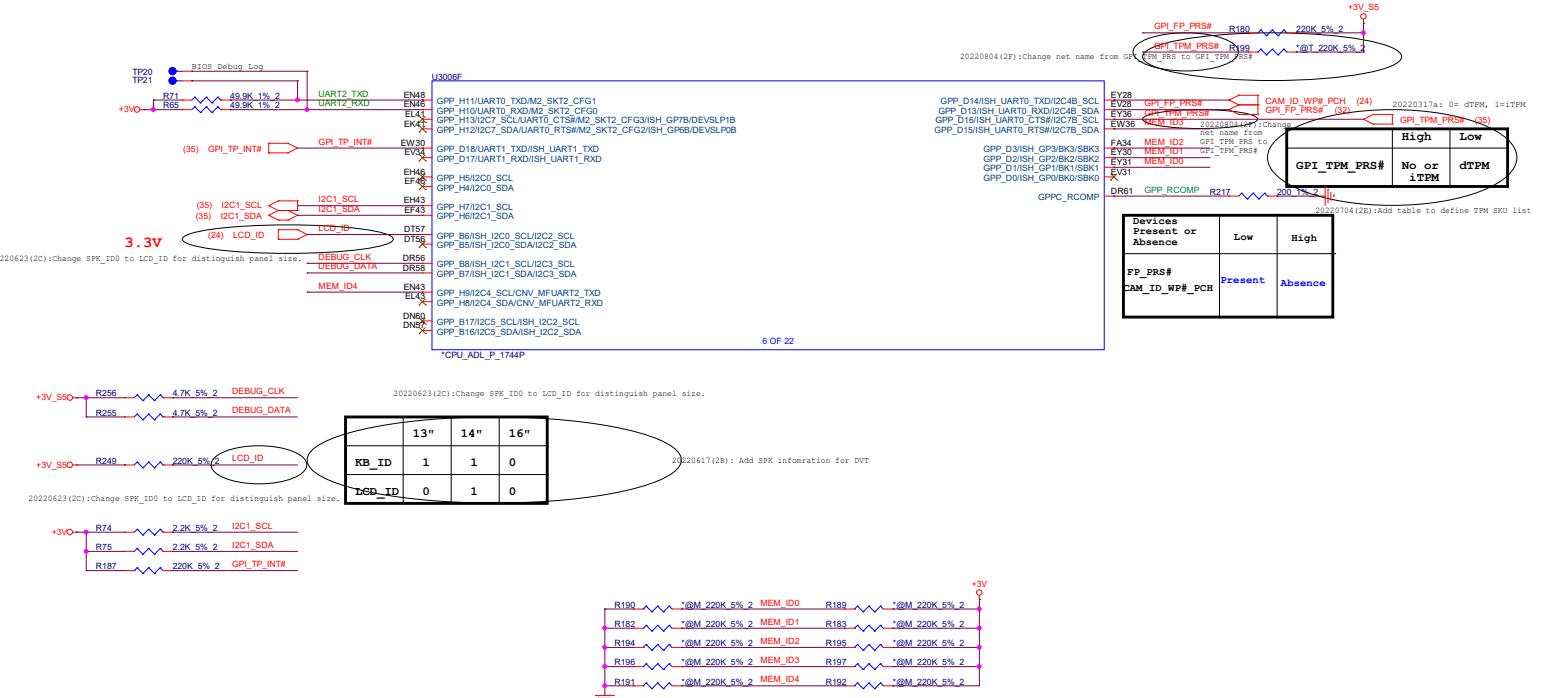
Quanta Computer Inc.
PROJECT : TRA

Size	Document Number	Rev.
303.	ADL-P 2/14 (DDR4 I/F)	1.

Date: Wednesday, October 01, 2014 Sheet: 1 of 50







LPDDR4 Memory Strap

System Memory Size (byte)	Part capacity(bit)	Vendor Part Number	Quanta P/N	ID4	ID3	ID2	ID1	ID0	Memory Fre(MHZ)
Samsung 8GB	Samsung 16Gb	K4U6E3S4AB-MGCL	AKD5RZST571	0	0	1	1	1	4266MHz
Samsung 16GB	Samsung 32Gb/DDP	K4UBE3D4AB-MGCL	AKD5PZST566	0	1	0	0	0	4266MHz
Samsung 32GB	Samsung 64Gb/QDP	K4UCE3Q4AB-MGCL	AKD5QZST544	0	1	0	0	1	4266MHz
Micron 8GB	Micron 16Gb/SDP	MT53E512M32D1NP-046 WT:B	AKD5RZSTL24	0	1	0	1	0	4266MHz
Micron 16GB	Micron 32Gb/DDP	MT53E1G32D2NP-046 WT:B	AKD5SWDTL36	0	1	0	1	1	4266MHz
Micron 32GB	Micron 64Gb/QDP	MT53E2G32D4NQ-046 WT:C	AKD5QWUTL11	0	1	1	0	0	4266MHz
Hynix 8GB	Hynix 16Gb	H54G46CYRBX267	AKD5RGSTW09	0	1	1	0	1	4266MHz
Hynix 16GB	Hynix 32Gb/DDP	H54G56CYRBX247	AKD5SGSTW11	0	1	1	1	0	4266MHz
Hynix 32GB	Hynix 64Gb	H54G68CYRBX248	AKD5TGSTW02	0	1	1	1	1	4266MHz

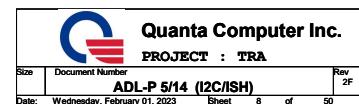
DDR4 Memory Strap

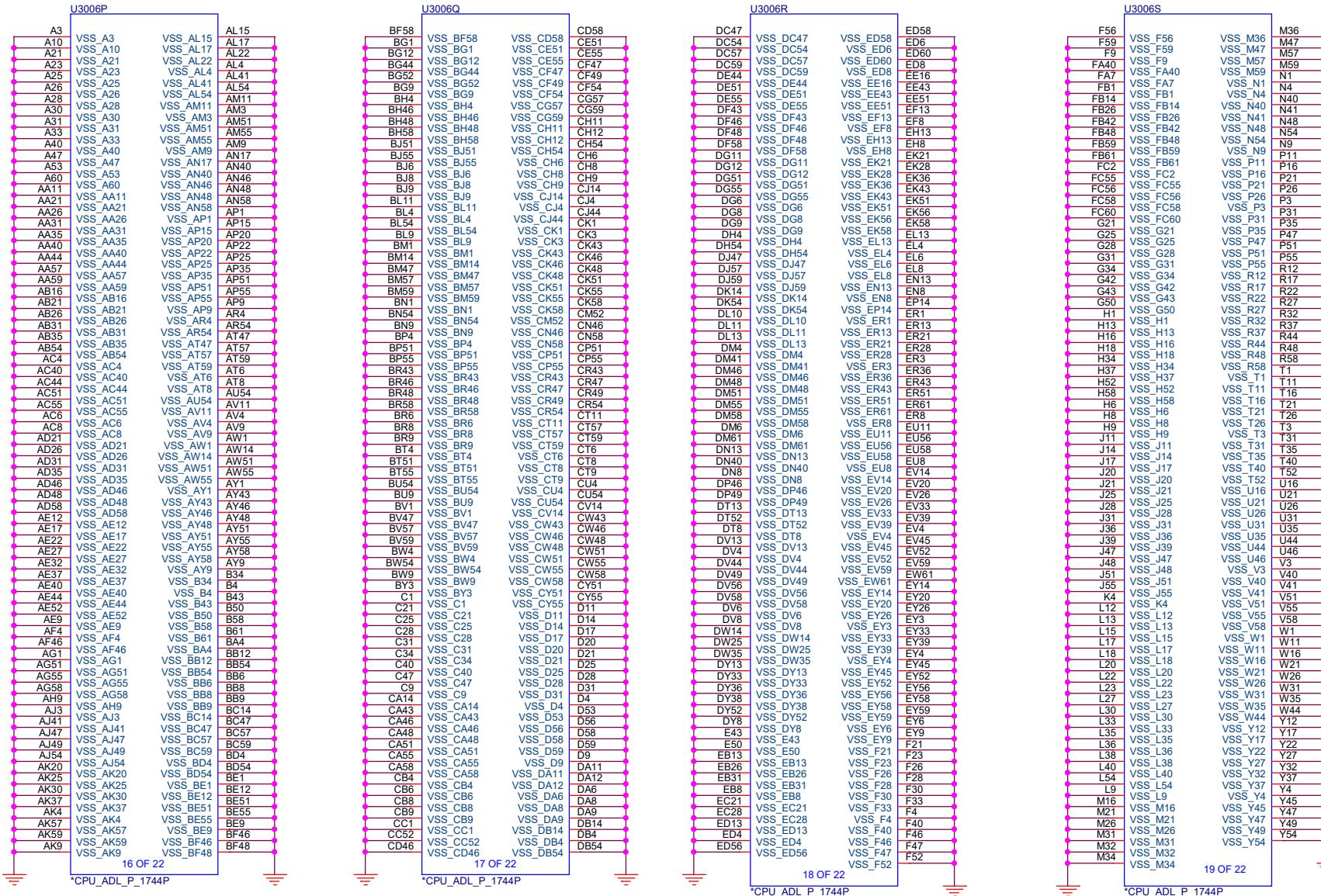
System Memory Size (byte)	Part capacity(bit)	Vendor Part Number	Quanta P/N	ID4	ID3	ID2	ID1	ID0	Memory Fre(MHZ)
Samsung 8GB	SDP 16Gb x16 (T7:NC)	K4AA1G165WB-BCWE	AKD5LGUT517	0	0	0	0	0	3200MHz
Samsung 16GB	DDP 32Gb x16 (T7:VSS)	K4ABG165WB-MCWE	AKD5SGST518	0	0	0	0	1	3200MHz
Micron 8GB	SDP 16Gb x16 (T7:NC)	MT40A1G16TB-062E:F	AKD5RGSTL25	0	0	0	1	0	3200MHz
Micron 16GB	DDP 32Gb x16 (T7:NC)	MT40A2G16SKL-062E:B	AKD5SGSTL04	0	0	0	1	1	3200MHz
Hynix 8GB	SDP 16Gb x16 (T7:NC)	H5ANAG6NCJR-XNC	AKD5RGUTW38	0	0	1	0	0	3200MHz
Hynix 16GB	DDP 32Gb x16 (T7:VSS)	H5ANBG6NCMR-XNC	AKD5SGSTW12	0	0	1	0	1	3200MHz
Micron 16GB	DDP 32Gb x16 (T7:NC)	MT40A2G16TB-062E:F	AKD5SGSTL07	0	0	1	1	0	3200MHz

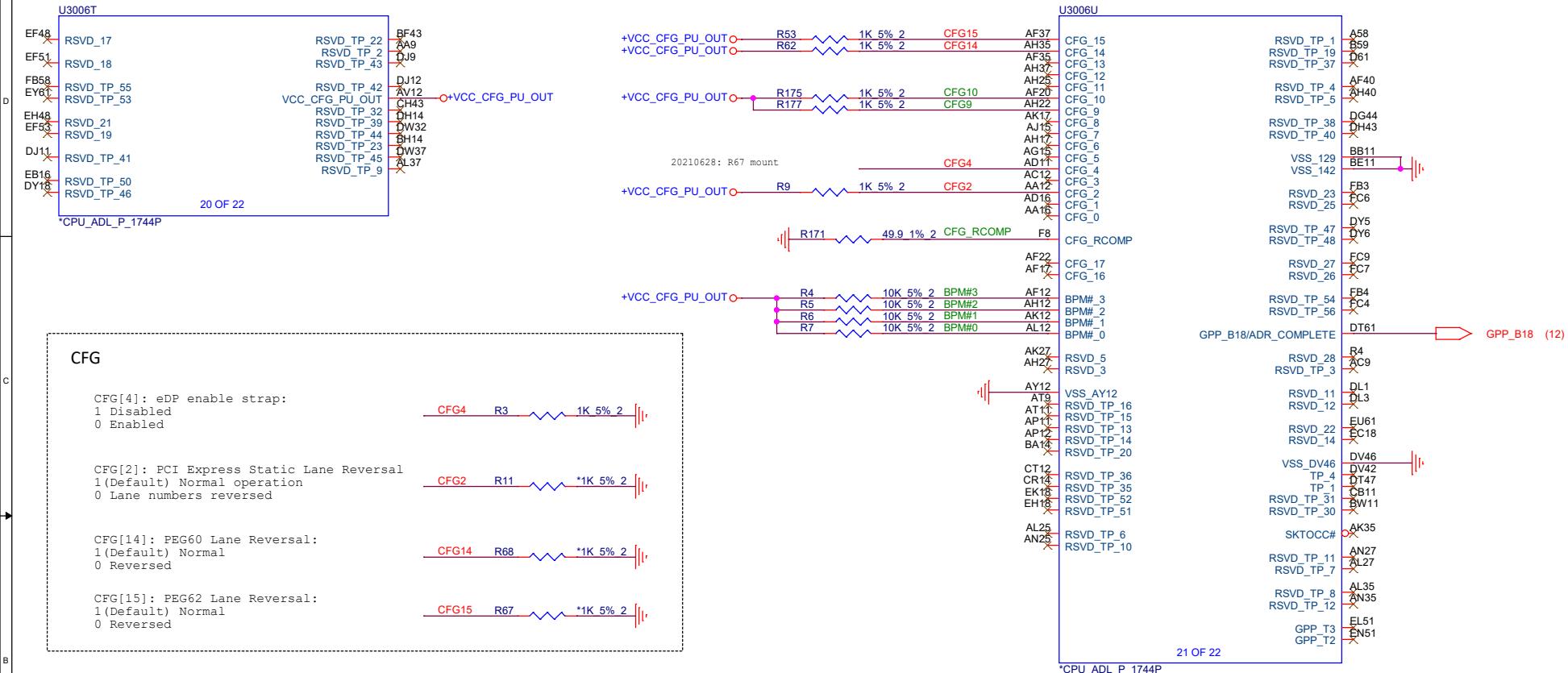
20220629(2D):Add memory for new Micron 16G

This part should not contain any substances which are specified in EM-S303.

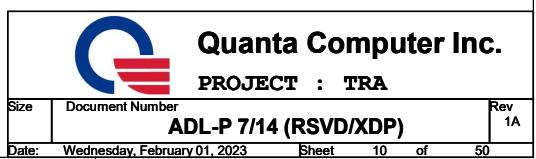
20220804a

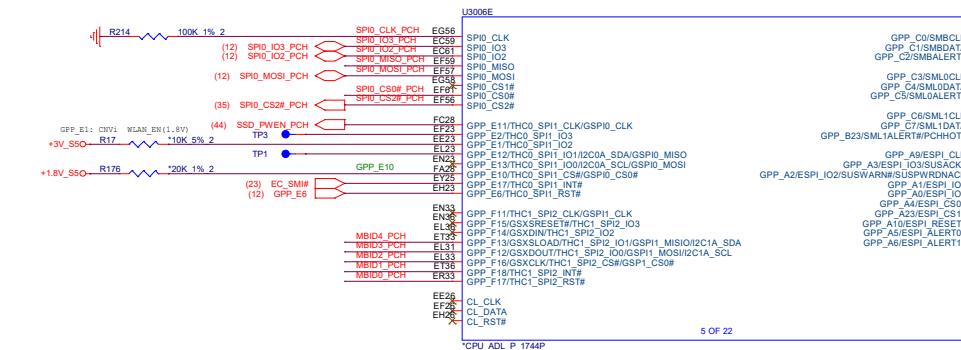






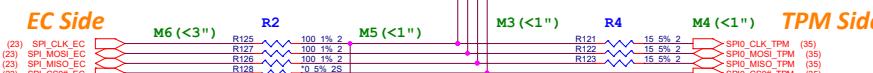
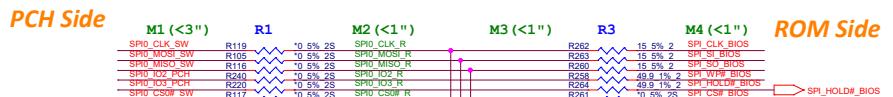
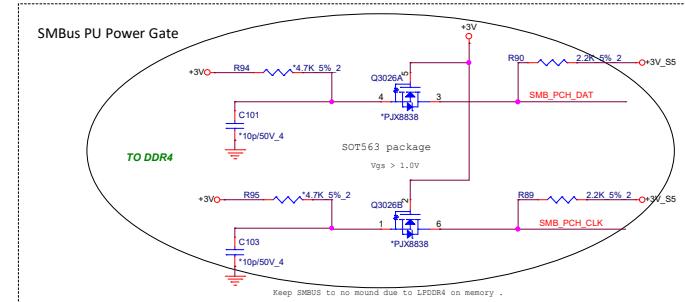
20220216d





R179 → R181
 R63 → R59
 R51 → R50
 R66 → R58

Resistors need to place on CPU side



$$(M1+M2) = (M5+M6) \leq \pm 2.5'$$

M1 / M3 / M4 / M6 > 0.5"

$$M2/M5 > 0.1''$$

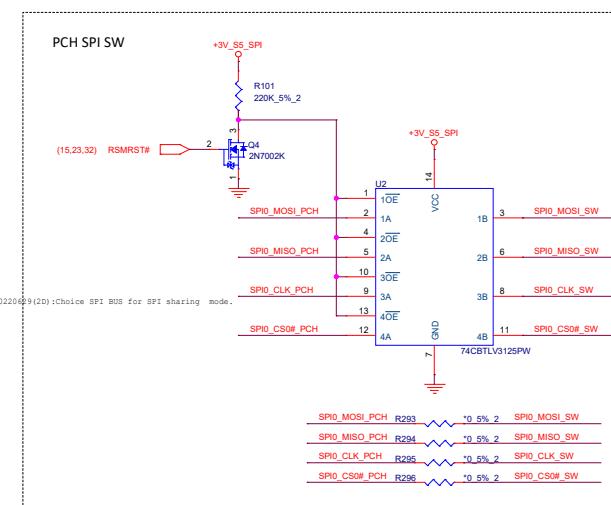
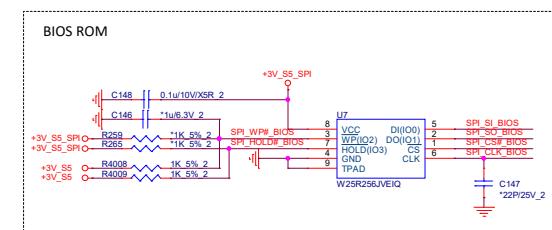
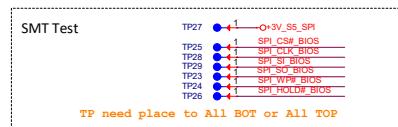
CLK - DATA/CS# <= +-0.5"

B1 : 0 ohm (3-3V) - 0 ohm (1-8V)

R2: 100 ohm (3.3V), 50 ohm (1.8V)

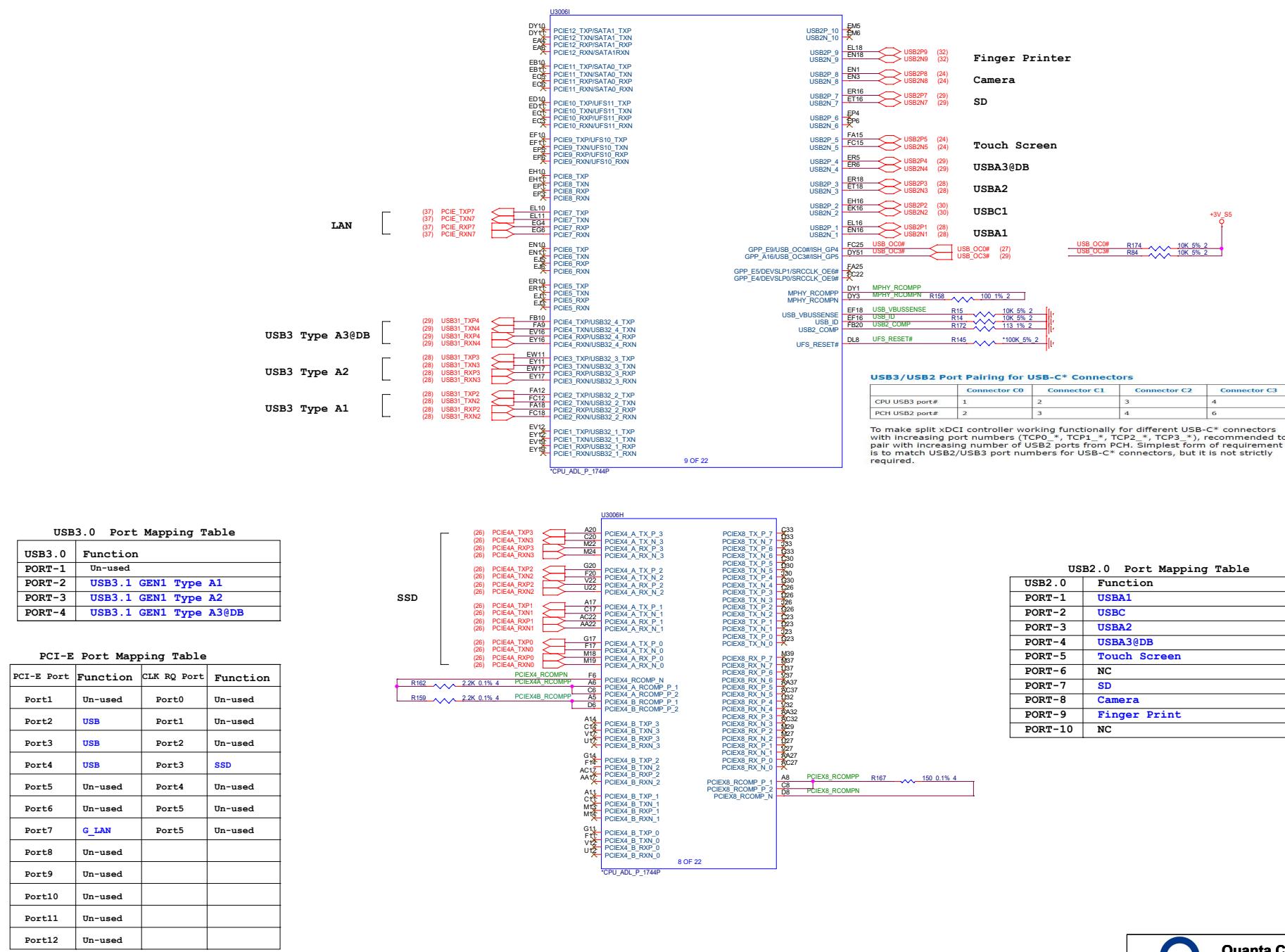
R3: 15 ohm(3.3V), 15 ohm(1.8V)

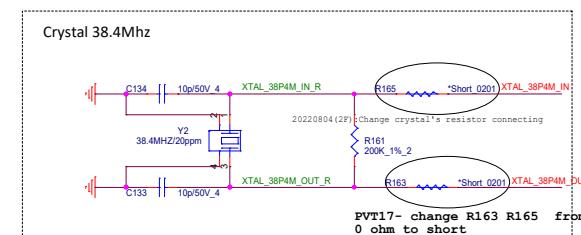
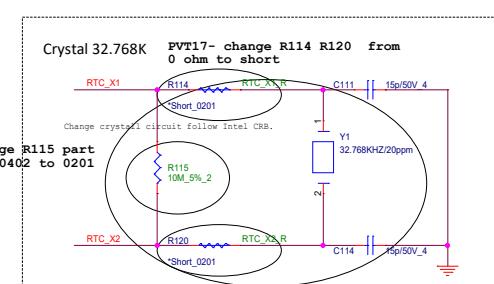
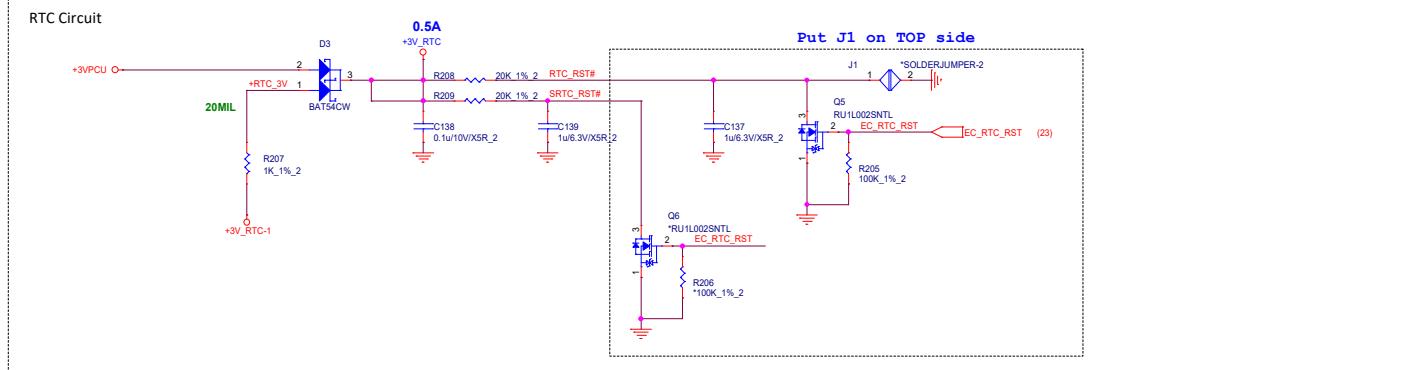
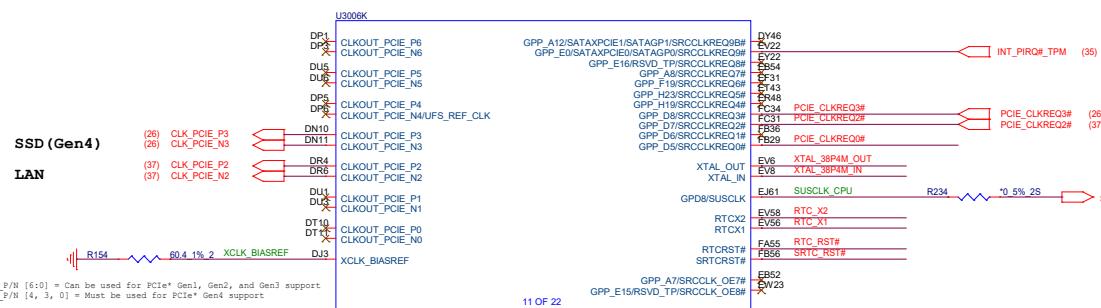
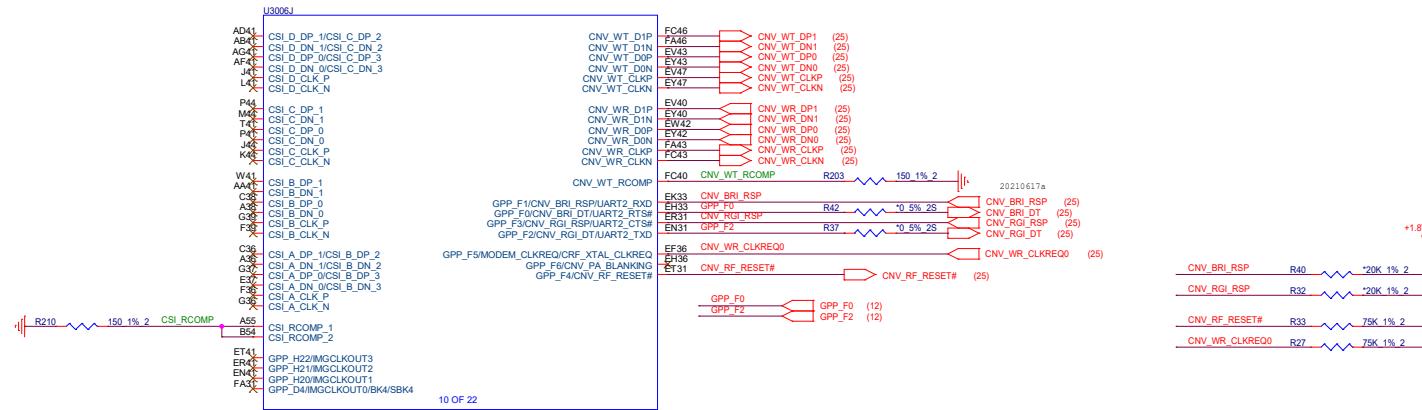
R4: 15 Ohm(3.3V), 15 Ohm(1.8V)

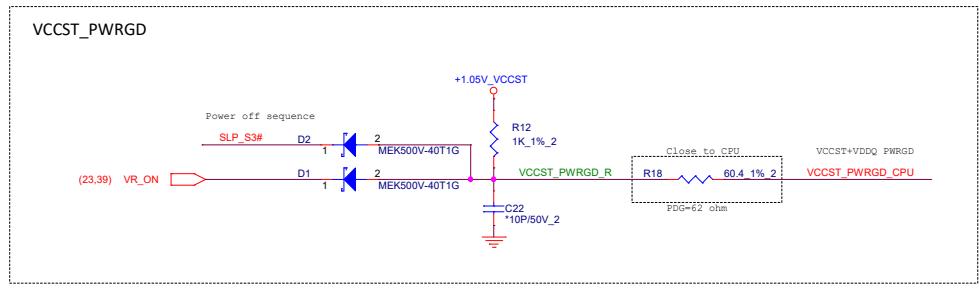
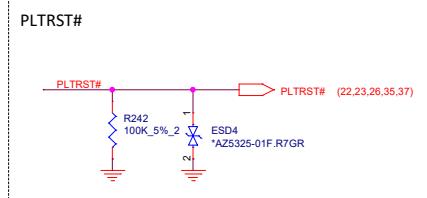
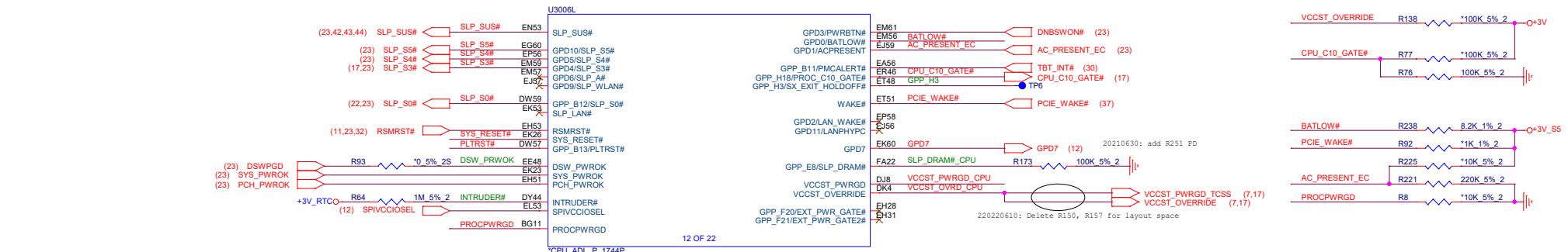
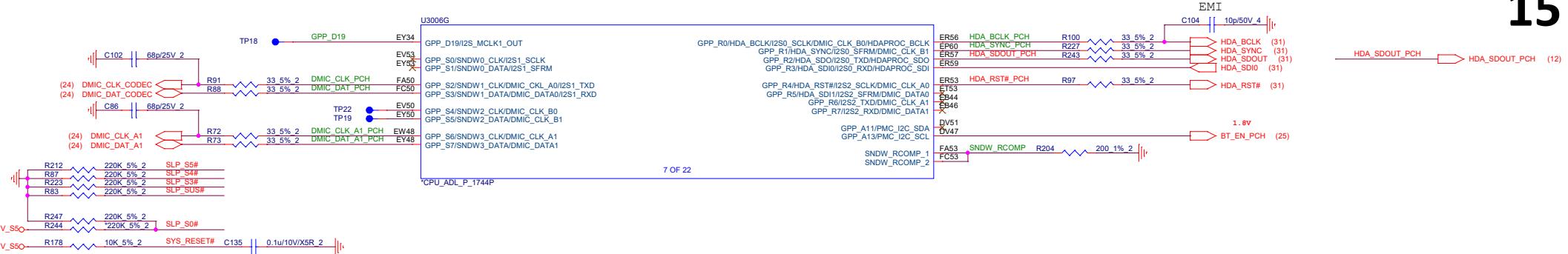


GPIO	Usage	Sampled	PU/PD	Strap
GPP_B14	TOP SWAP 1: Enable 0: Disable(Default)	PCH_PWROK	20K PD (INT)	+3V_O R250 *4.7K 5% 2 R248 *20K 1% 2 GPP_B14 (6.23)
GPP_B18	NO Reboot 1: Enable 0: Disable(Default)	PCH_PWROK	20K PD (INT)	+3V_O R254 *4.7K 5% 2 R251 *20K 1% 2 GPP_B18 (10)
GPP_C2	TLS CONFIDENTIALITY 1: Enable 0: Disable(Default)	RSMRST#	20K PD (INT)	+3V_S5_O R35 *4.7K 5% 2 +1.8V_S5_O R31 *4.7K 5% 2 R36 *20K 1% 2 SMB_ALERT# (11)
GPP_C5(0) GPP_H0(1) GPP_H1(2) GPP_H2(3)	Boot Configuration 0000:BIOS/CSME on SPI, eSPI enable 0010:BIOS/CSME on SPI, eSPI disable 0100:BIOS/CSME on eSPI 1100:BIOS on eSPI, CSME on SPI	RSMRST#	20K PD (INT) 20K PD (INT) 20K PD (INT) 20K PD (INT)	+3V_S5_O R54 *4.7K 5% 2 R55 *20K 1% 2 R80 *4.7K 5% 2 R81 *20K 1% 2 R57 *4.7K 5% 2 R58 *20K 1% 2 R56 *4.7K 5% 2 R59 *20K 1% 2 GPP_C5 (11) GPP_H0 (6.26) GPP_H1 (6) GPP_H2 (6)
SPI0_MOSI	Reserved	RSMRST#	4.7K PU@EDS	+3V_S5_O R216 *4.7K 5% 2 R215 *4.7K 5% 2 SPI0_MOSI_STRAP R211 1K 5% 2 SPI0_MOSI_PCH (11)
GPP_D10	DDP3 I2C Power Configuration 1: DDP3 I2C/TBT_LSX2=3.3V 0: DDP3 I2C/TBT_LSX2=1.8V	RSMRST#	20K PD (INT)	+3V_S5_O R200 *4.7K 5% 2 R198 *20K 1% 2 TBT_LSX2_RXD (4) GPP_D10
GPP_D12	DDP4 I2C Power Configuration 1: DDP4 I2C/TBT_LSX3=3.3V 0: DDP4 I2C/TBT_LSX3=1.8V	RSMRST#	20K PD (INT)	+3V_S5_O R201 *4.7K 5% 2 R202 *20K 1% 2 GPP_D12 (4.30)
GPP_B23	CPUNSSC Clock Frequency 1: 19.2MHz 0: 38.4MHz(Default)	RSMRST#	20K PD (INT)	+3V_S5_O R38 *4.7K 5% 2 R39 *20K 1% 2 GPP_B23 (11)
SPI0_IO2	Reserved	RSMRST#	100K PU@3.3V(EXT) 75K PU@1.8V(EXT)	+3V_S5_O R233 *100K 1% 2 R224 *4.7K 5% 2 SPI0_IO2_STRAP R235 1K 5% 2 SPI0_IO2_PCH (11)
SPI0_IO3	Reserved	RSMRST#	100K PU@3.3V(EXT) 75K PU@1.8V(EXT)	+3V_S5_O R218 *100K 1% 2 R219 *4.7K 5% 2 SPI0_IO3_PCH (11)
GPP_R2	Flash Security Override 1: Disable 0: Enable(Default)	PCH_PWROK	20K PD (INT)	+3V_S5_O R239 *4.7K 5% 2 R228 *1K 5% 2 HDA_SDOUT_PCH (15) (23) MEFW_WP
GPP_E6	Reserved	RSMRST#	100K PU@3.3V(EXT) 75K PU@1.8V(EXT)	+3V_S5_O R34 *20K 1% 2 R41 *20K 1% 2 R28 *4.7K 5% 2 GPP_E6 (11)
GPP_E19	DDP1 I2C Power Configuration 1: DDP1 I2C/TBT_LSX0=3.3V 0: DDP1 I2C/TBT_LSX0=1.8V	RSMRST#	20K PD (INT)	+3V_S5_O R22 *4.7K 5% 2 R23 *20K 1% 2 TBT_LSX0_RXD (4) GPP_E19
GPP_E21	DDP2 I2C Power Configuration 1: DDP2 I2C/TBT_LSX1=3.3V 0: DDP2 I2C/TBT_LSX1=1.8V	RSMRST#	20K PD (INT)	+3V_S5_O R20 *4.7K 5% 2 R19 *20K 1% 2 GPP_E21 (4)
DBG_PMODE	Reserved	RSMRST#	20K PU (INT)	+1.05V_OUT_FET R10 1K 5% 2 R13 *20K 1% 2 DBG_PMODE (6)
GPD7	Reserved	DSW_PWROK	20K PD (INT)	+3V_S5_O R226 *4.7K 5% 2 R222 *20K 1% 2 GPD7 (15)
GPP_F0	X'tal Frequency Selection 1: 24MHz 0: 38.4MHz(Default)	RSMRST#	20K PD (INT)	+1.8V_S5_O R45 *4.7K 5% 2 R43 *20K 1% 2 GPP_F0 (14)
GPP_F2	M2 CNVi Mode Select 1: Integrated CNVi Disable 0: Integrated CNVi Enable	RSMRST#	Note:Intel WiFi module ;PU down 1K ohm Platform is Pull high 100K ohm Weak PU(EXT)	+1.8V_S5_O R30 *100K 5% 2 R29 *4.7K 5% 2 GPP_F2 (14)
GPP_F7	Reserved	RSMRST#	20K PD (INT)	TP4 GPP_F7 (6)
GPP_F10	Reserved	RSMRST#	20K PD (INT)	TP5 GPP_F10 (6)
SPIVCCIOSEL	SPI Operation Voltage 1: SPI Voltage =1.8V 0: SPI Voltage =3.3V	DSW_PWROK	4.7K PU@DSW_PWROK (EXT) 4.7K PD@GND (EXT)	+3V_S5_O R99 *1K 5% 2 R98 *10K 1% 2 SPIVCCIOSEL (15)

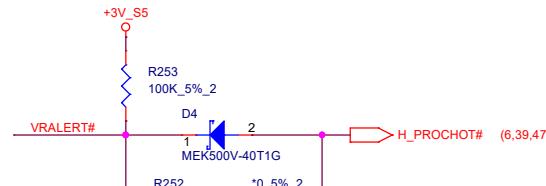
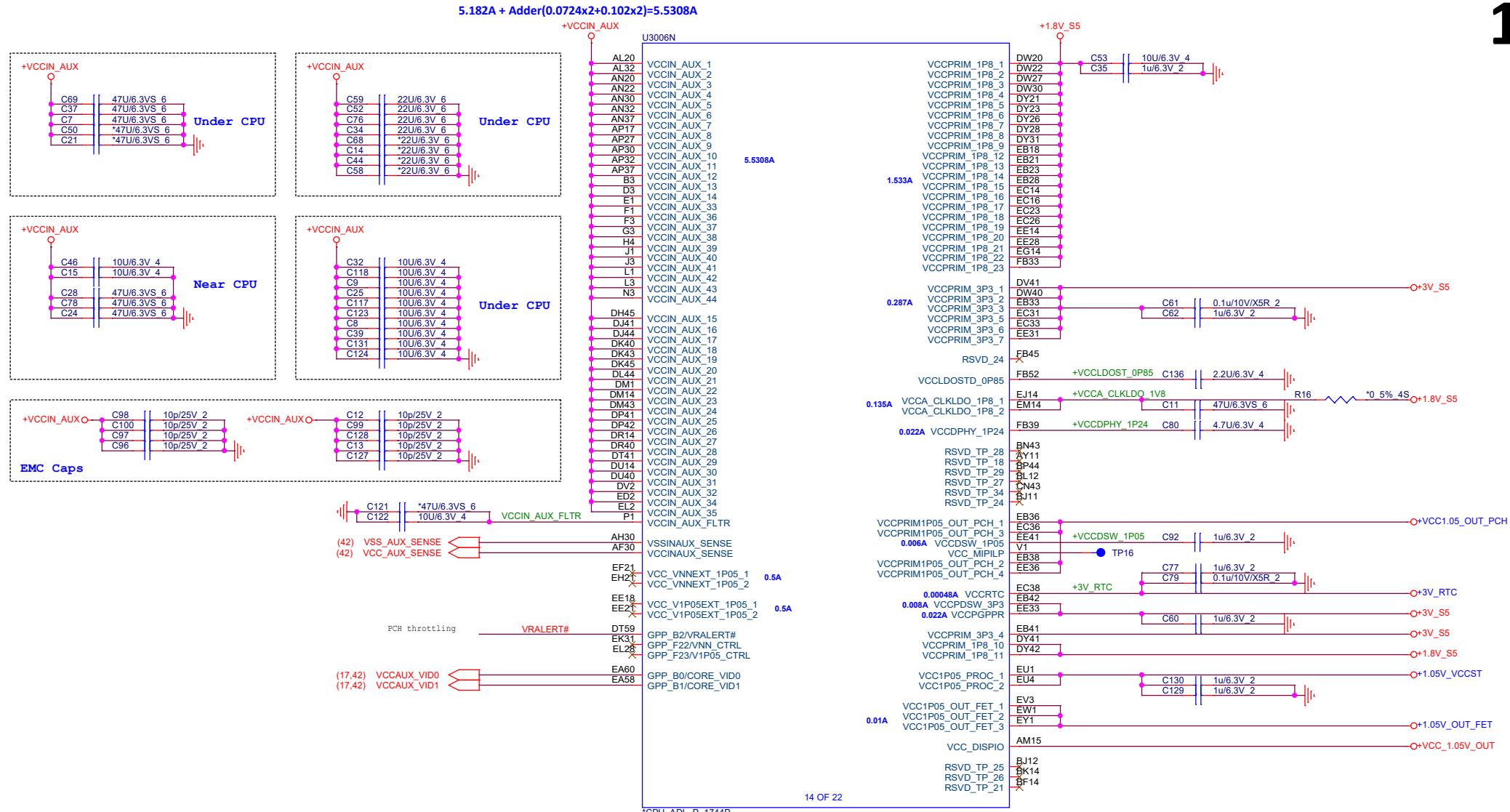
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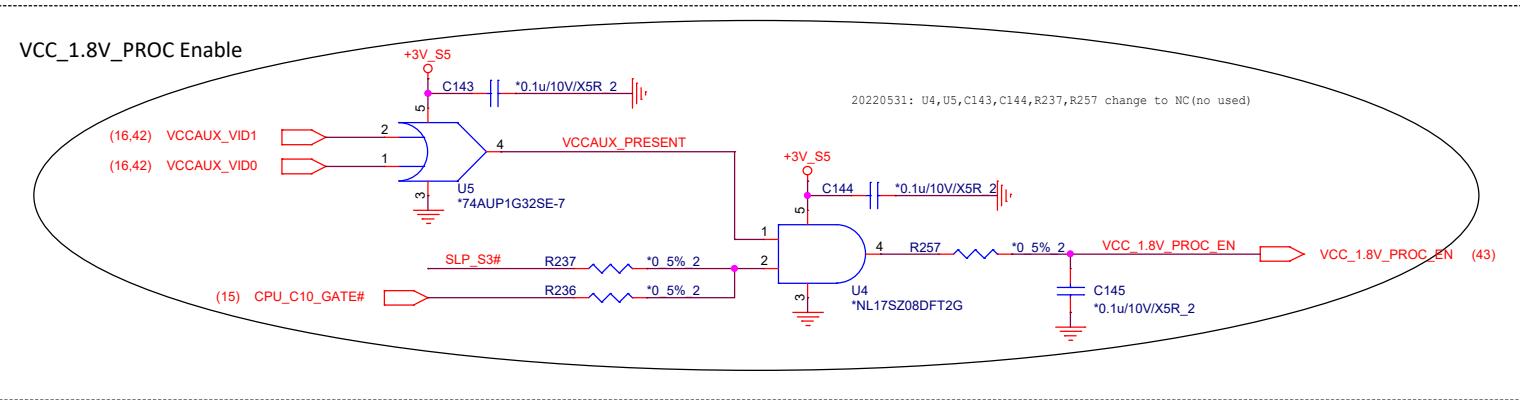
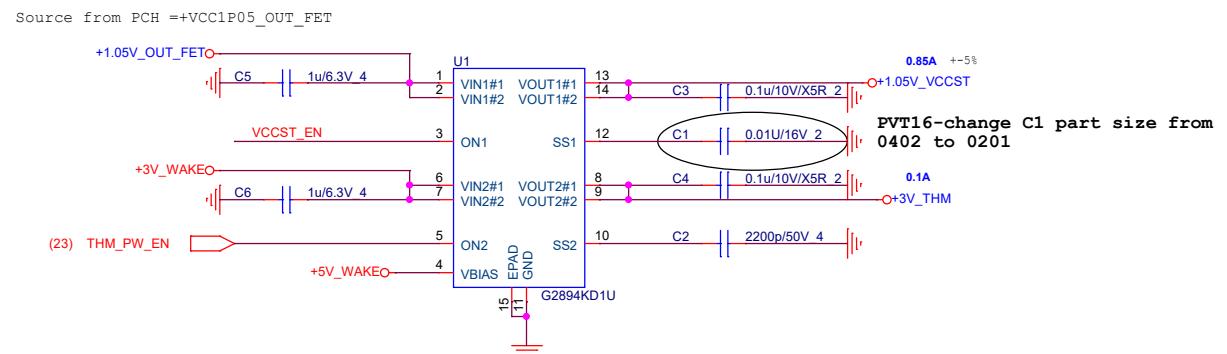
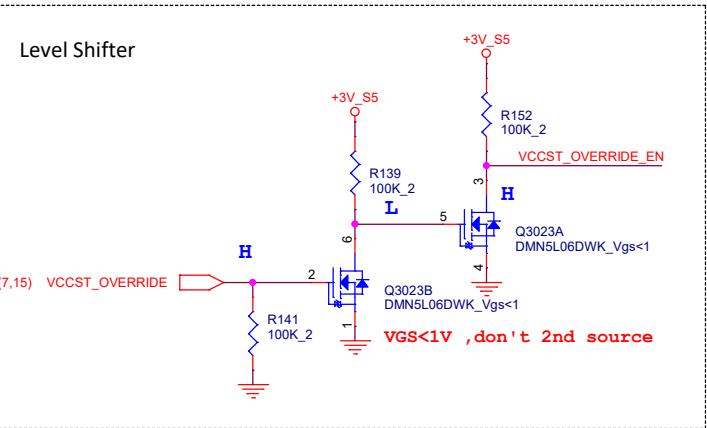
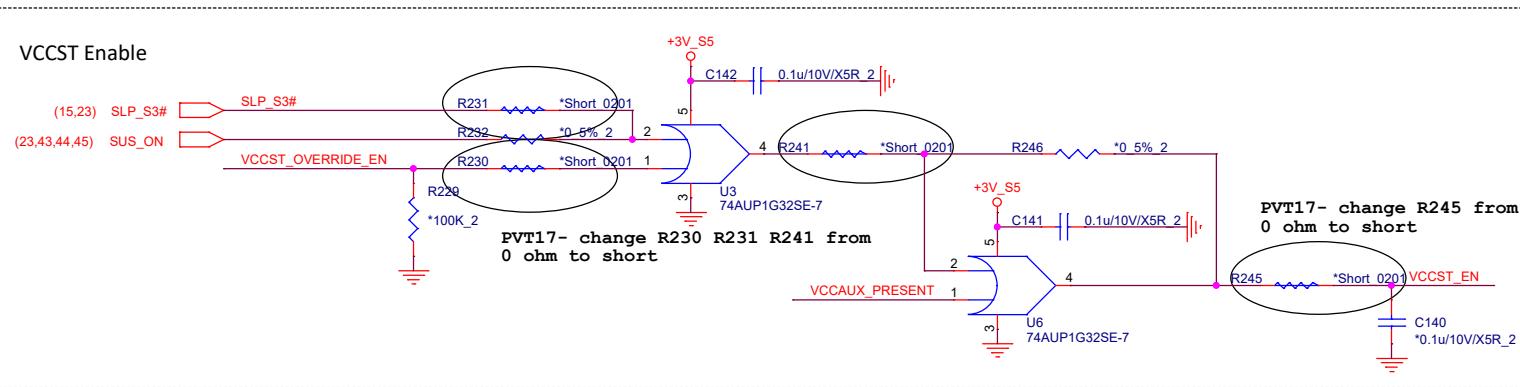




This part should not contain any substances which are specified in EM-S303.



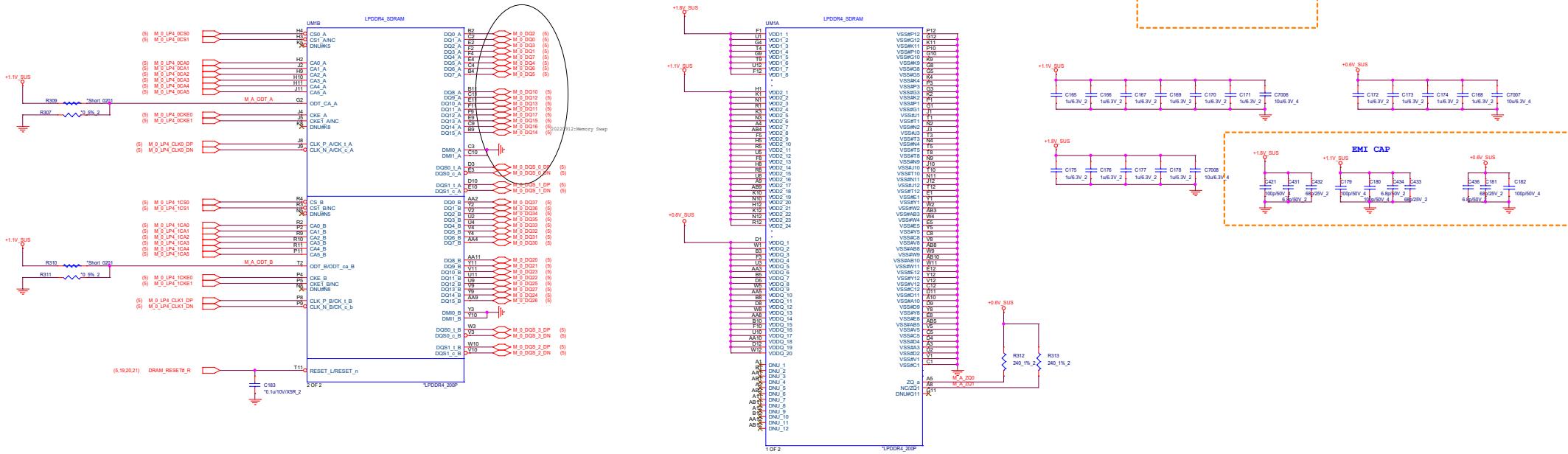
This part should not contain any substances which are specified in EM-S303



This part should not contain any substances which are specified in EM-S303.

Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

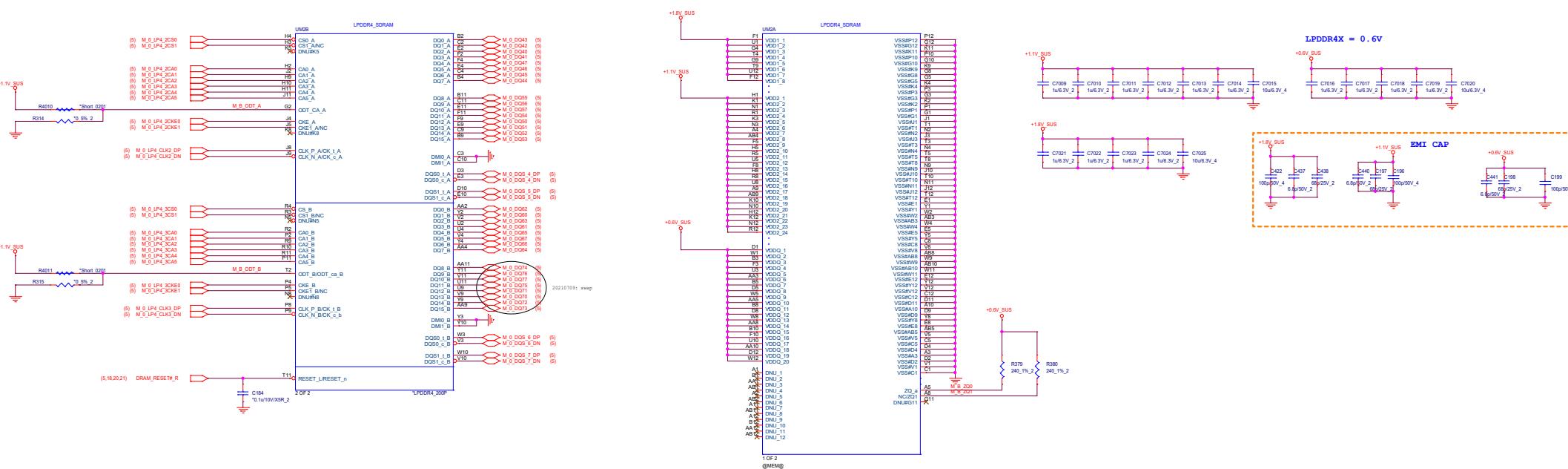
LPDDR4 CH-A



This part should not contain any substances which are specified in

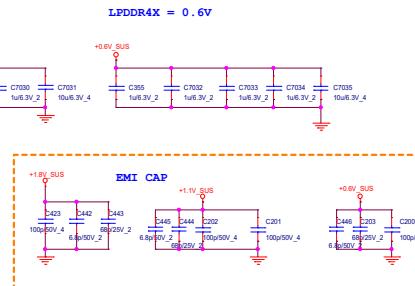
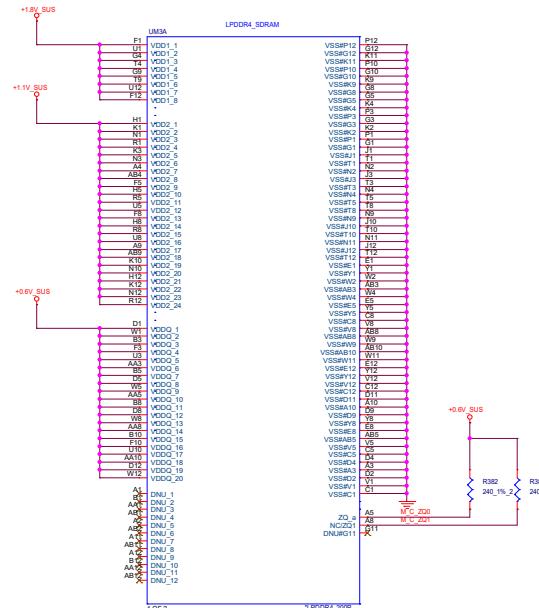
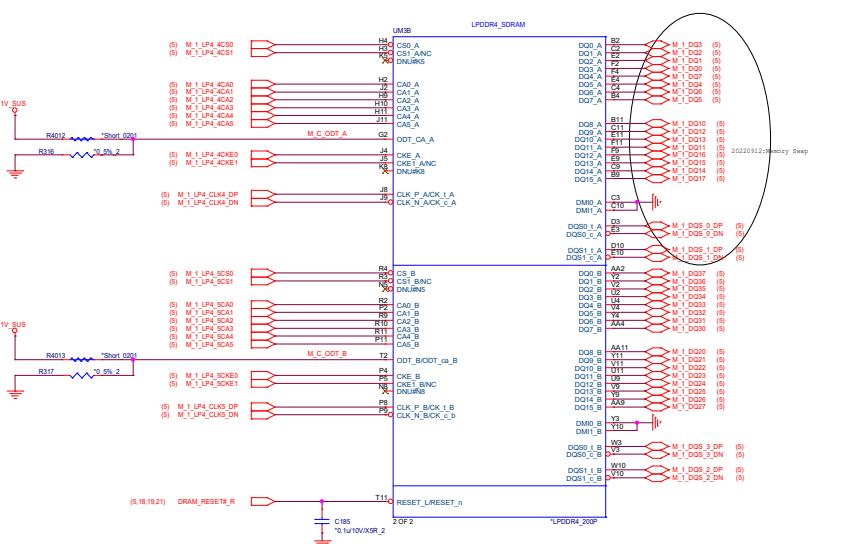
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0 5s

LPDDR4 CH-B



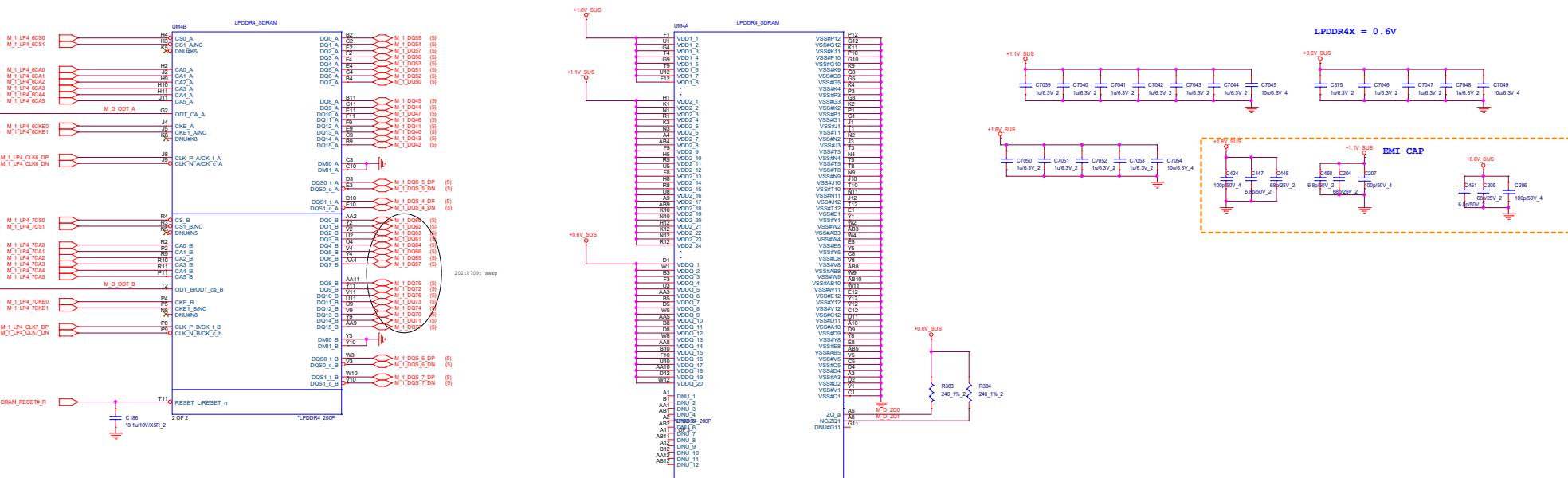
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-C

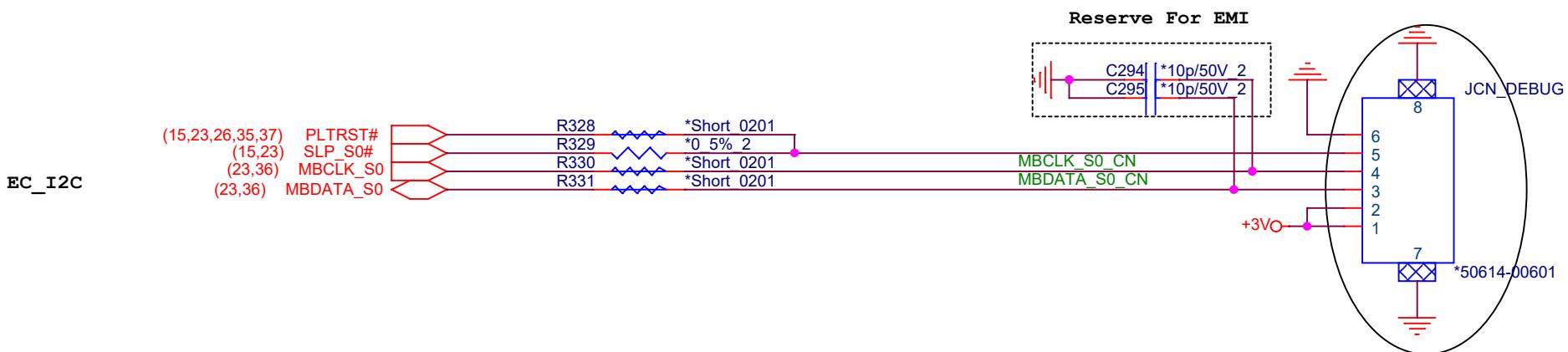


Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-D

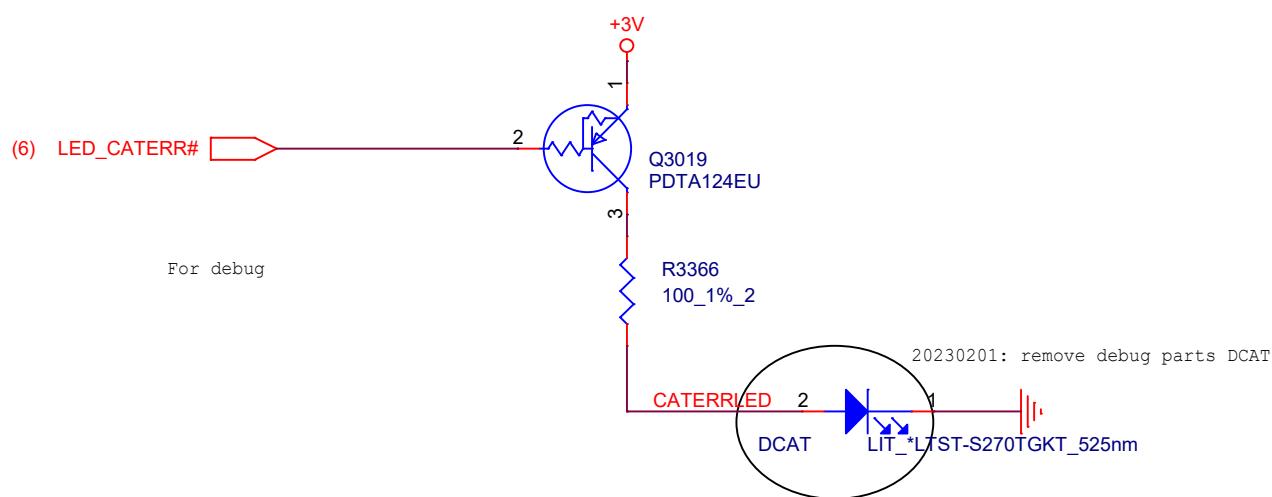


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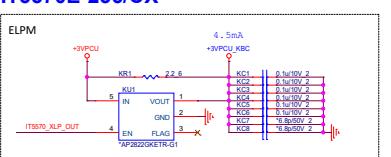


CATERR LED

20230201: remove debug parts JCN_DEBUG



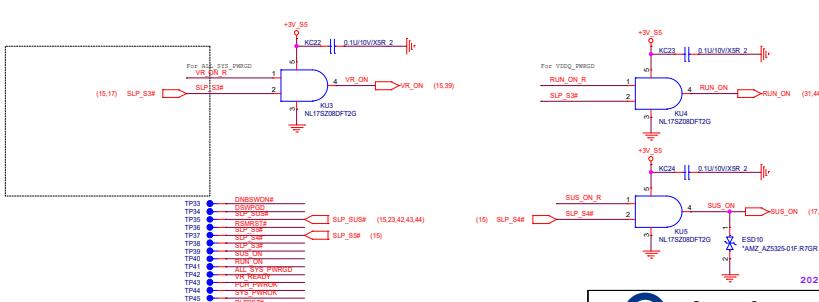
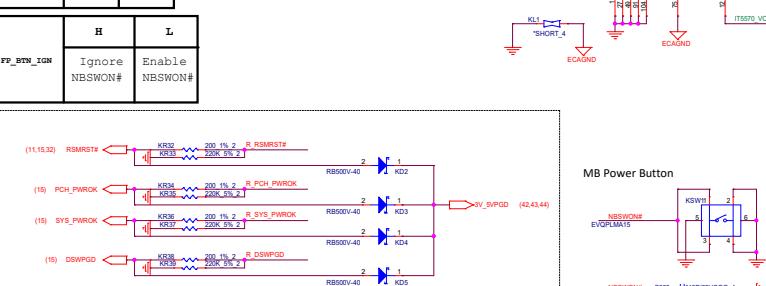
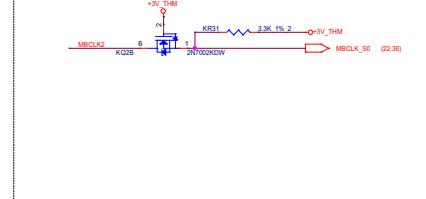
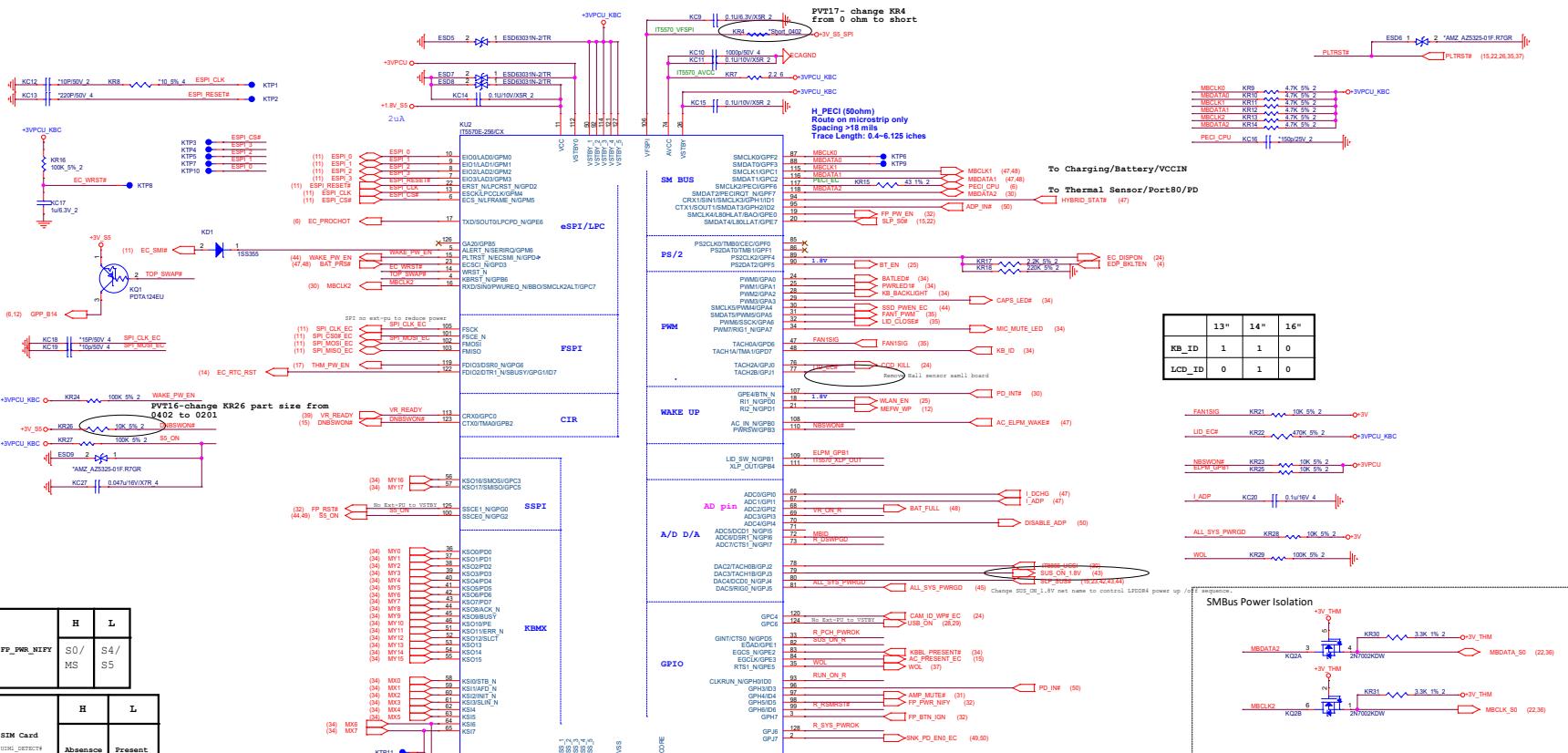
20220303b



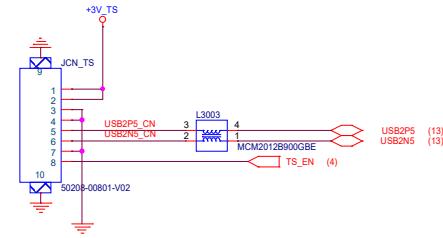
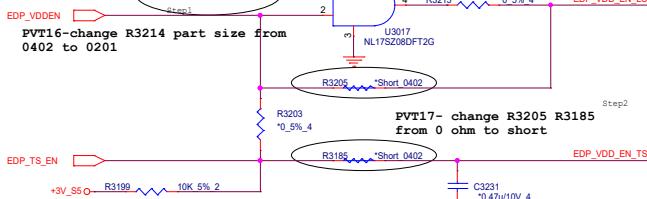
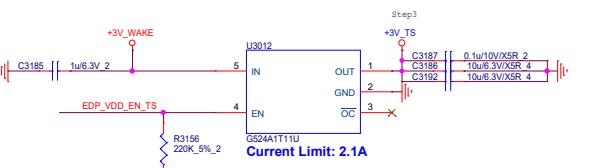
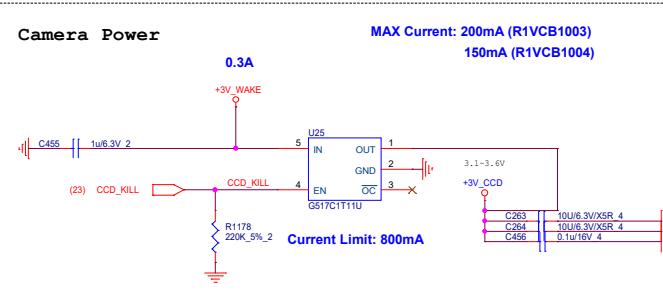
MBID		TRA EVT	TRA DVT	TRA DVT15	TRA DVT2	TBD PV1	TBD PV2
	KR3	X	220K	82K	220K	220K	150K
	KR2	100K	82K	X	47K	133K	180K

20221103: 3m Update KB ID (KR2/KR3) for PVTI stage

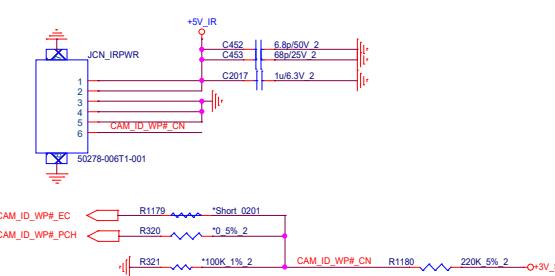
20221201: 3m Update MB ID(XR2/XR3) for PVT2 stage



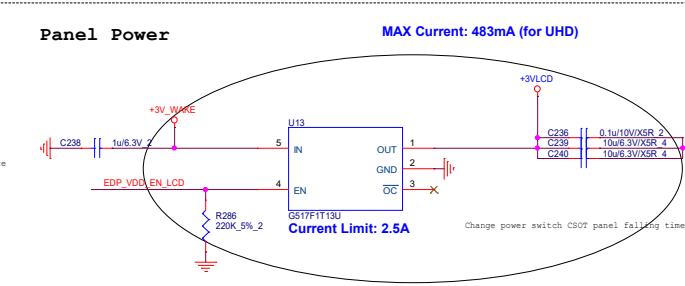
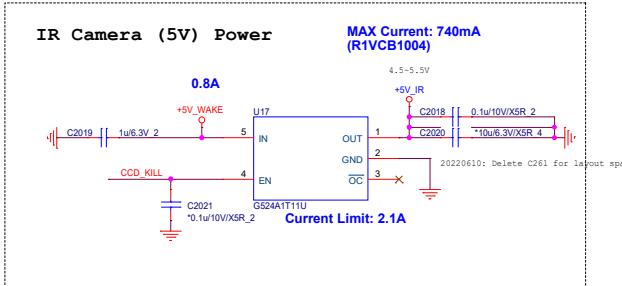
For HD/Hello Camera



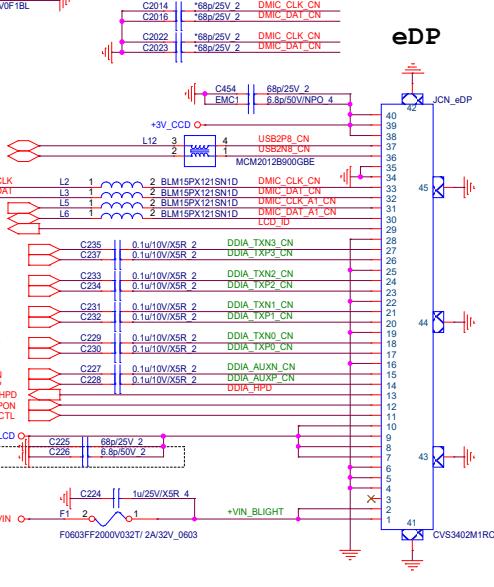
For Hello Camera

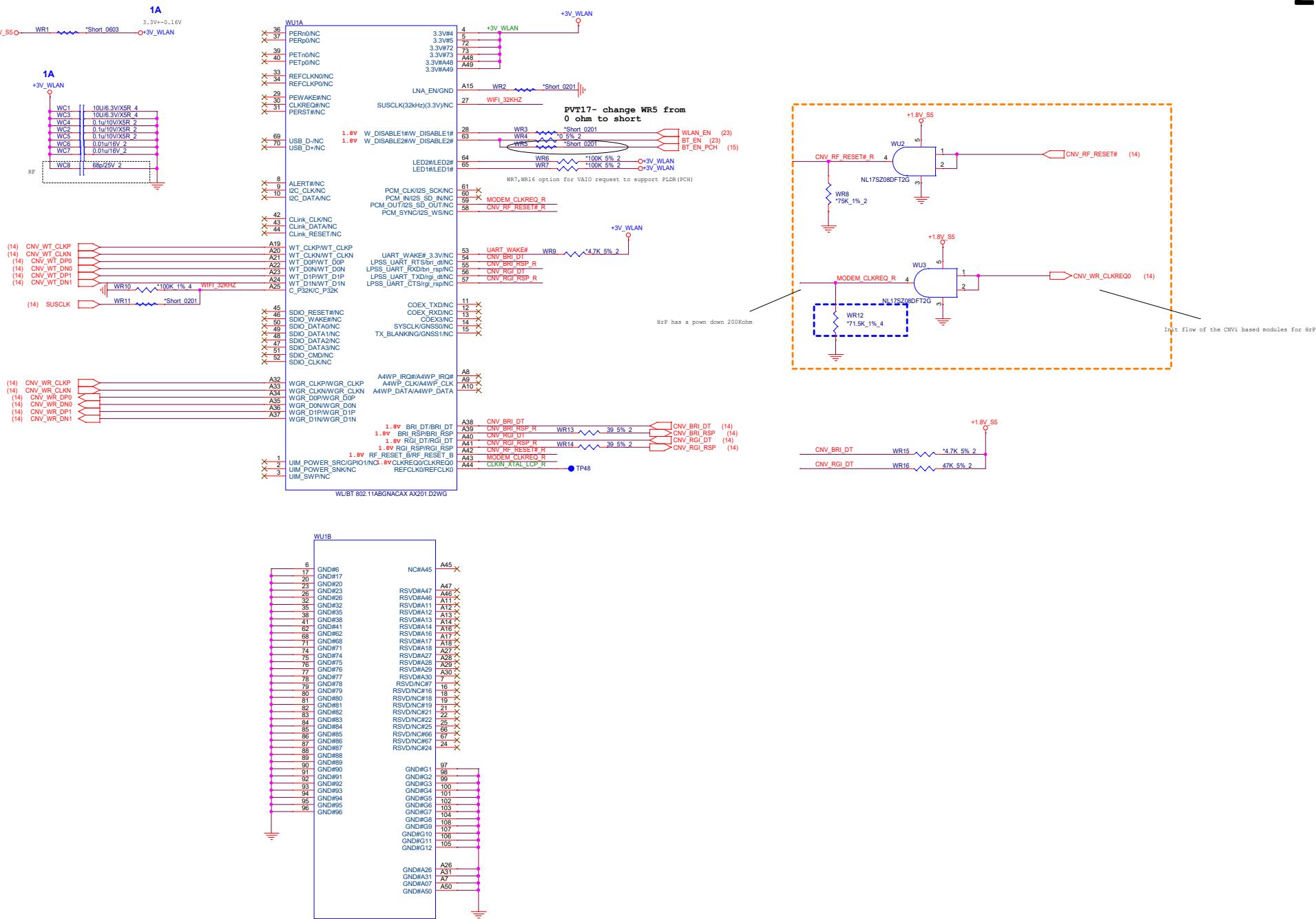


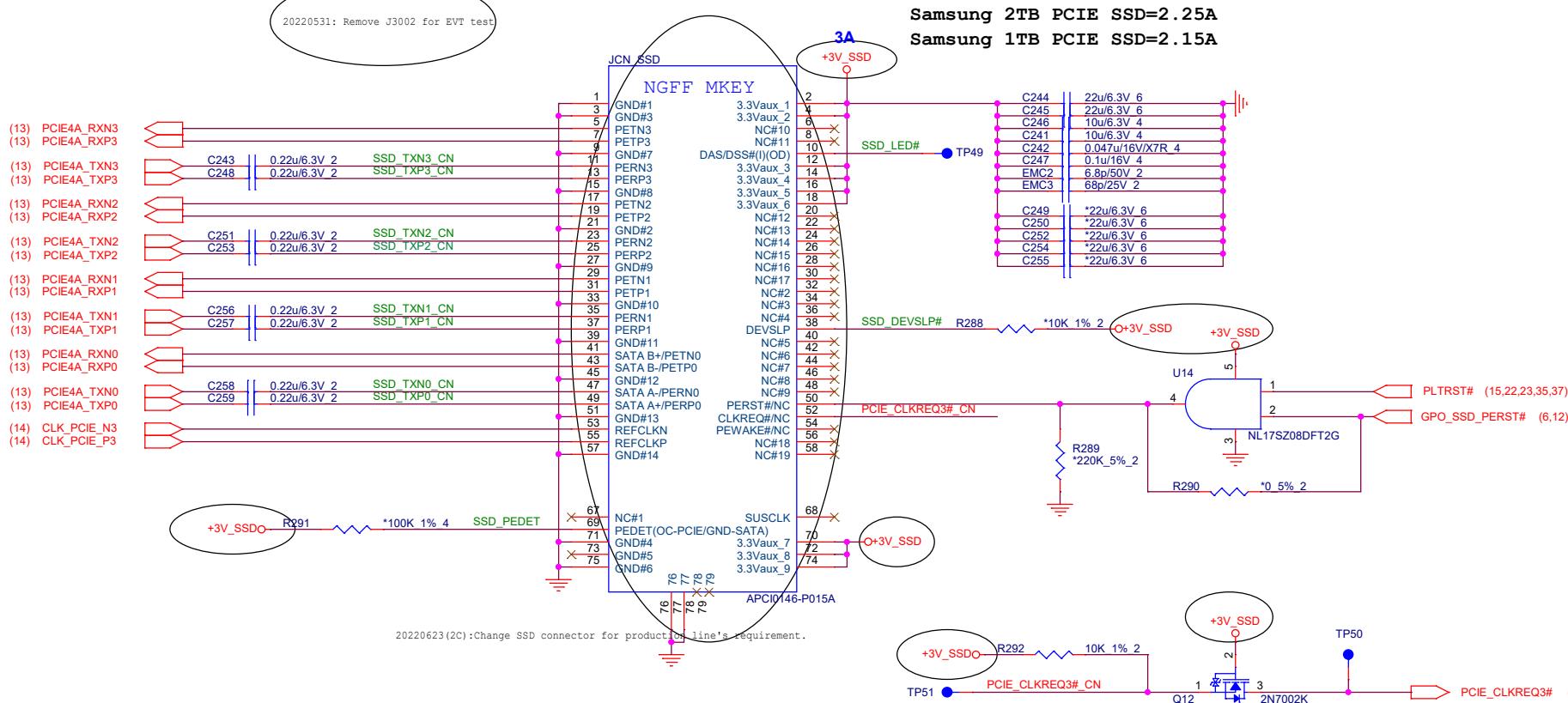
Host GPIO Direction	Host GPIO Value	Connected Camera	Result
IN	LOW	Hello cam	Hello cam detected
IN	HIGH	HD cam	HD cam detected
OUT	LOW	Hello cam	Write protected
OUT	HIGH	Hello cam	Write enabled



This part should not contain any substances which are specified in EM-S303.

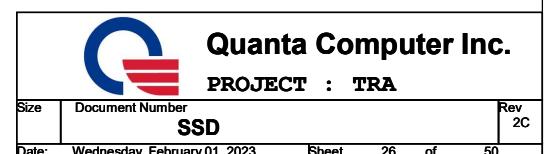






Size	I/F	Module ME	Vendor	Vendor PN
128GB	PCIE3		Samsung	MZVLQ128HCHQ-00B07
256GB	PCIE3		Samsung	MZVLQ256HBJD-00B07
512GB	PCIE3		Samsung	MZVLQ512HBLU-00B07
256GB	PCIE4		Samsung	MZVL2256HCHQ-00B07
512GB	PCIE4		Samsung	MZVL2512HCJQ-00B07

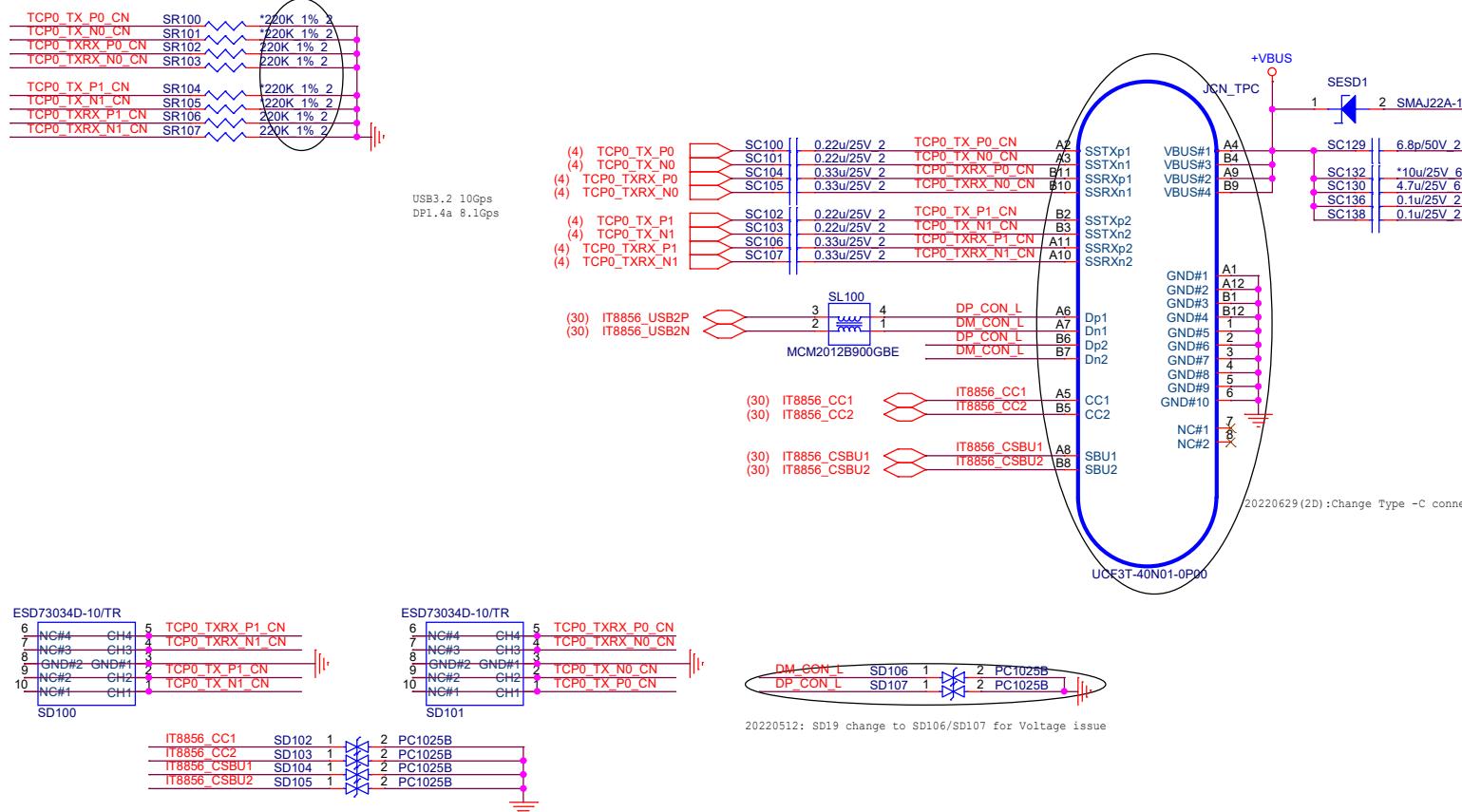
20220623a



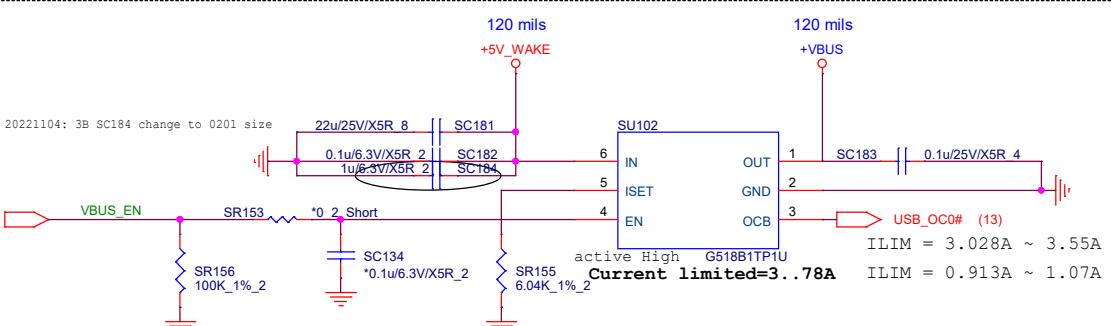
This part should not contain any substances which are specified in EM-S303.

USB Type-C

20220531: remove SR100, SR101, SR104, SR105 for SI

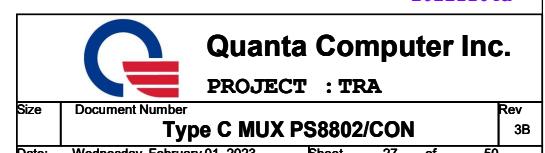


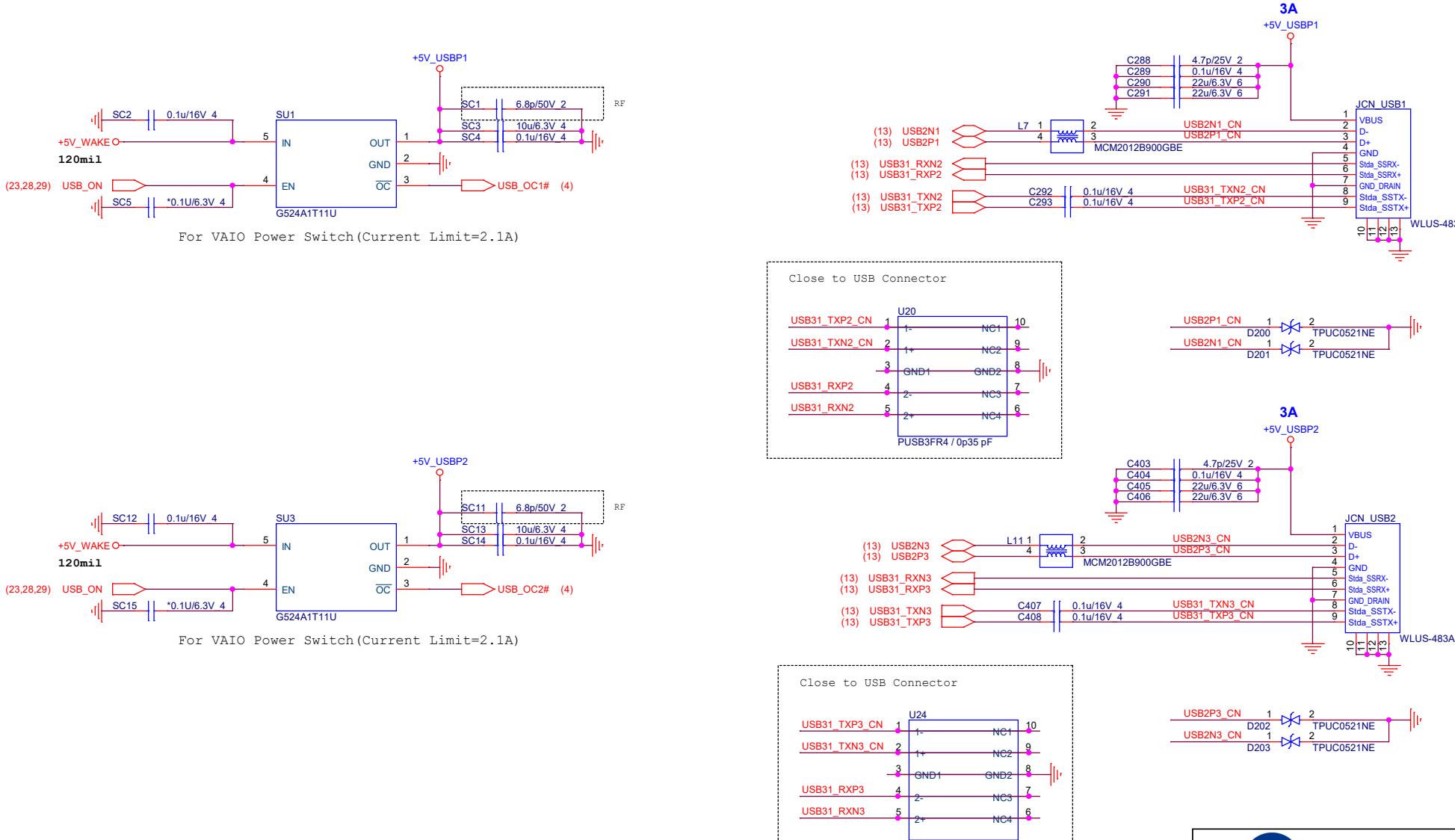
VBUS



This part should not contain any substances which are specified in EM-S303.

20221104a

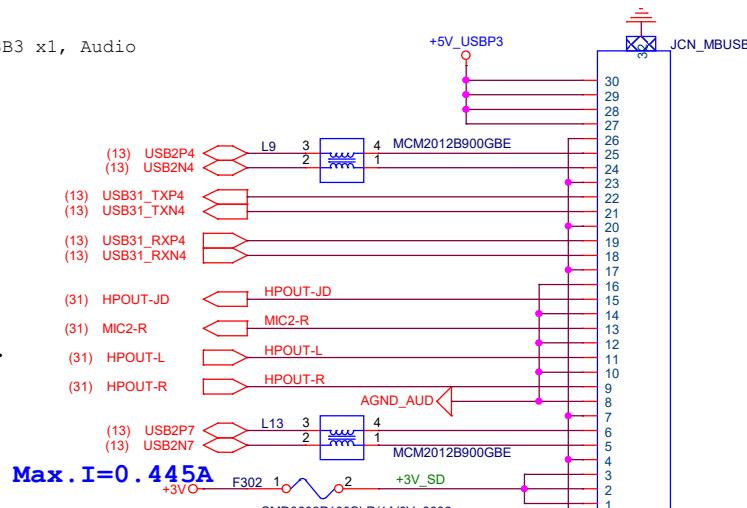




This part should not contain any substances which are specified in EM-S303.

Remove Hall sensor samll board

Micro SD, USB3 x1, Audio



change pin 31 of JCN_MBUSB for Audio AGND_AUD sharp.

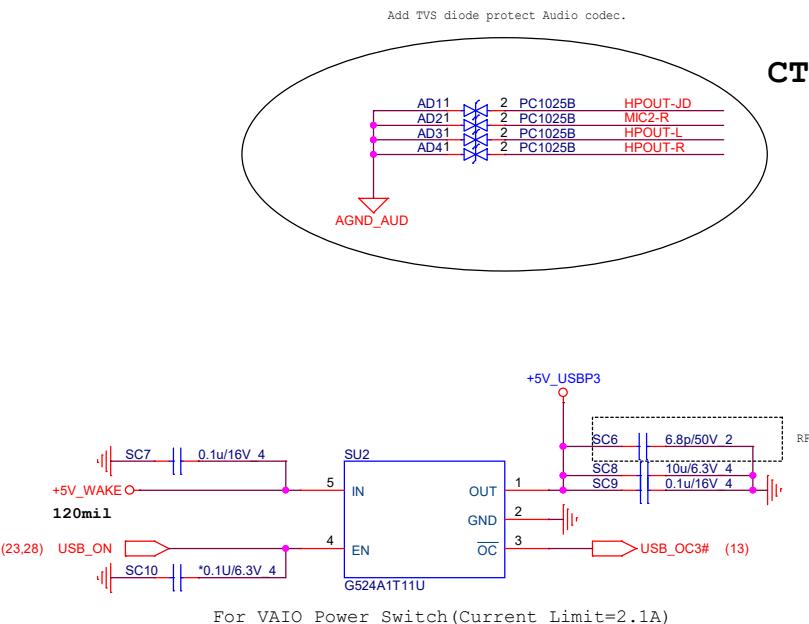
20220304a

Quanta Computer Inc.

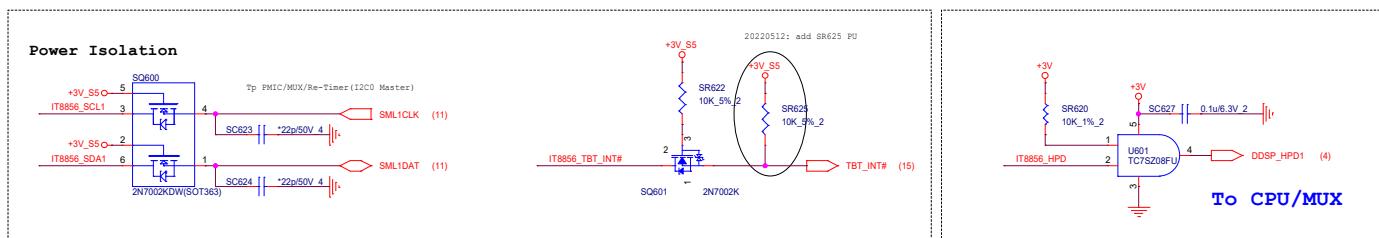
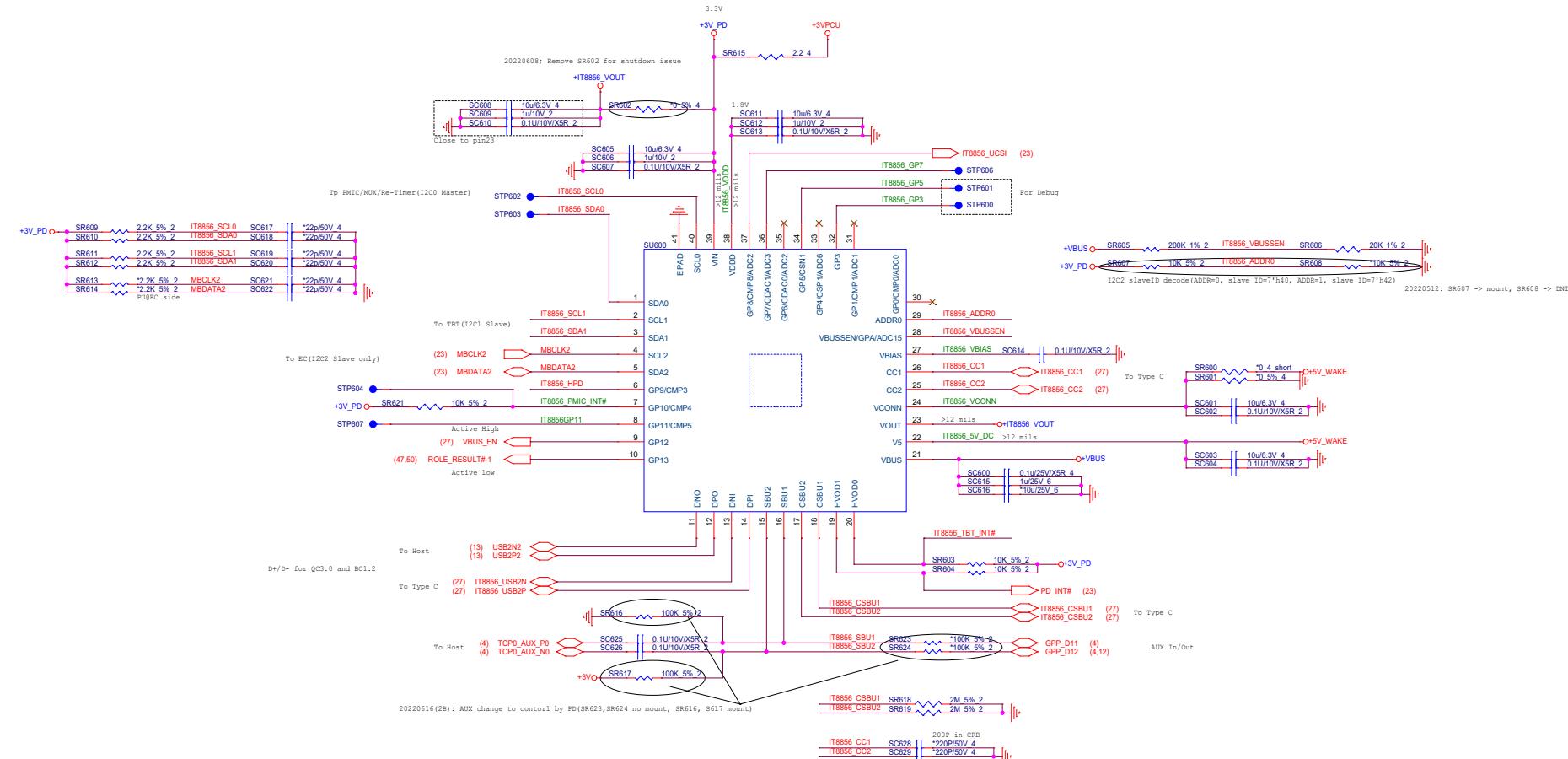
PROJECT : TRA

Size	Document Number	Rev
	MB to USB/SENSOR	3A

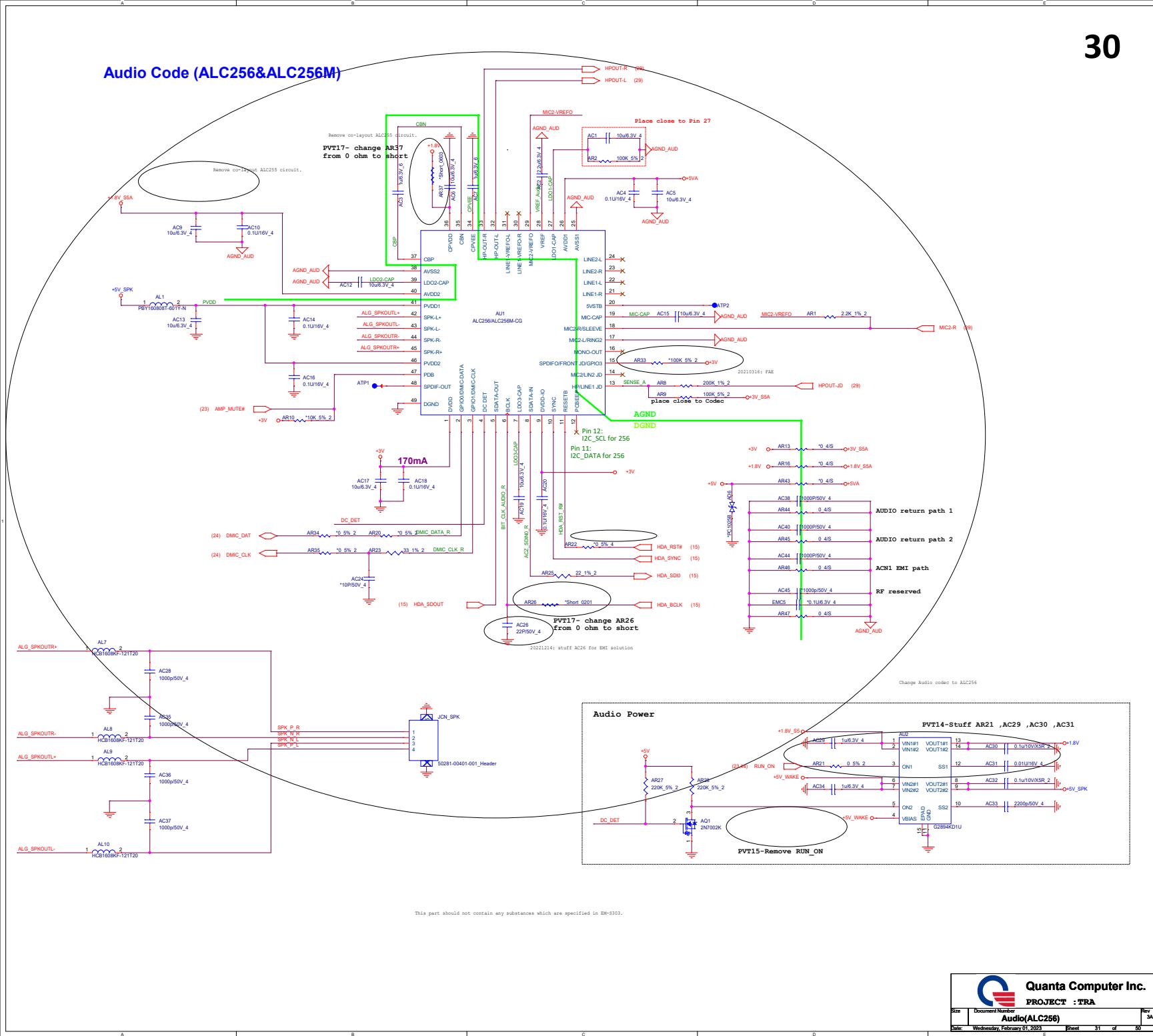
This part should not contain any substances which are specified in EM-S303.



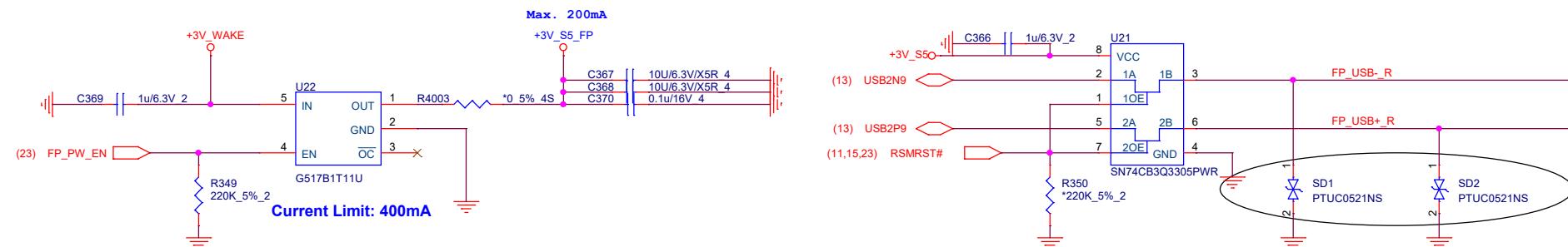
CTIA TRRS Headset



Audio Code (ALC256&ALC256M)

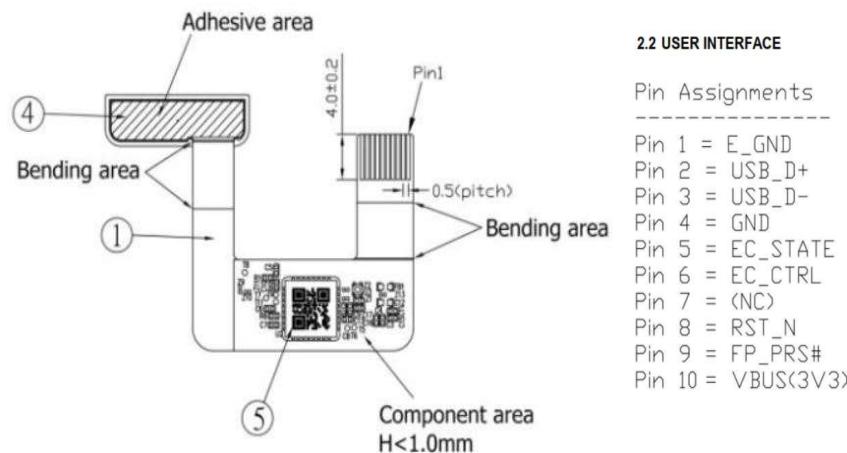


Fingerprint Power/BUS SW



20221129: add SD1 SD2 2nd source PTUC0521NS(BC0521NS200) / PESD5V0F1BSF (BC5V0F1BZ02)

Bottm view

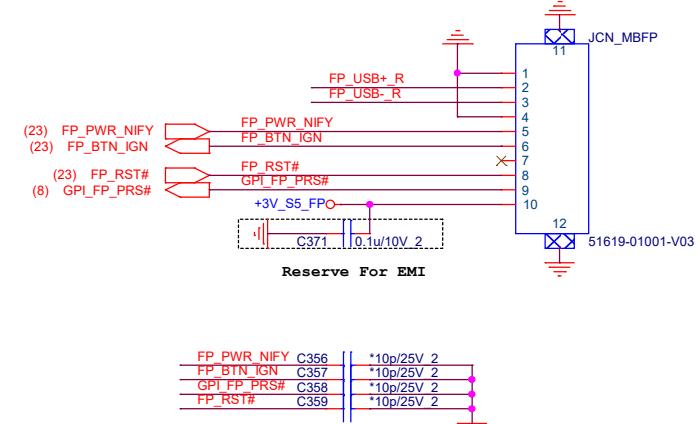


Pull-up & Pull-down Resistors

FP_PRS# (FP presence pin)	
High	Non Fingerprint SKU
Low	Fingerprint SKU

MB Pull UP 100K , Fingerprint Module pull down 10K

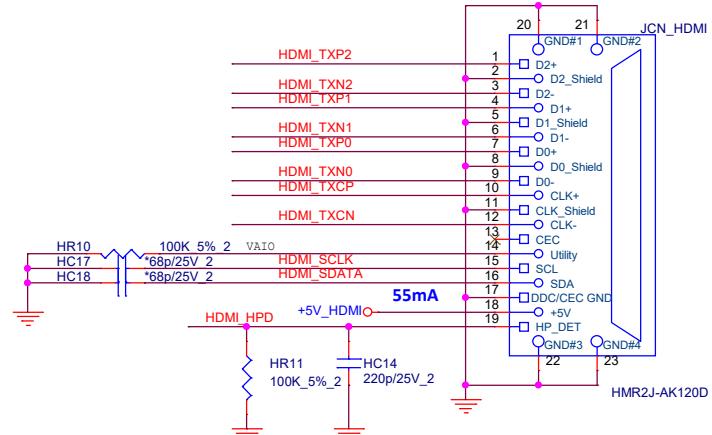
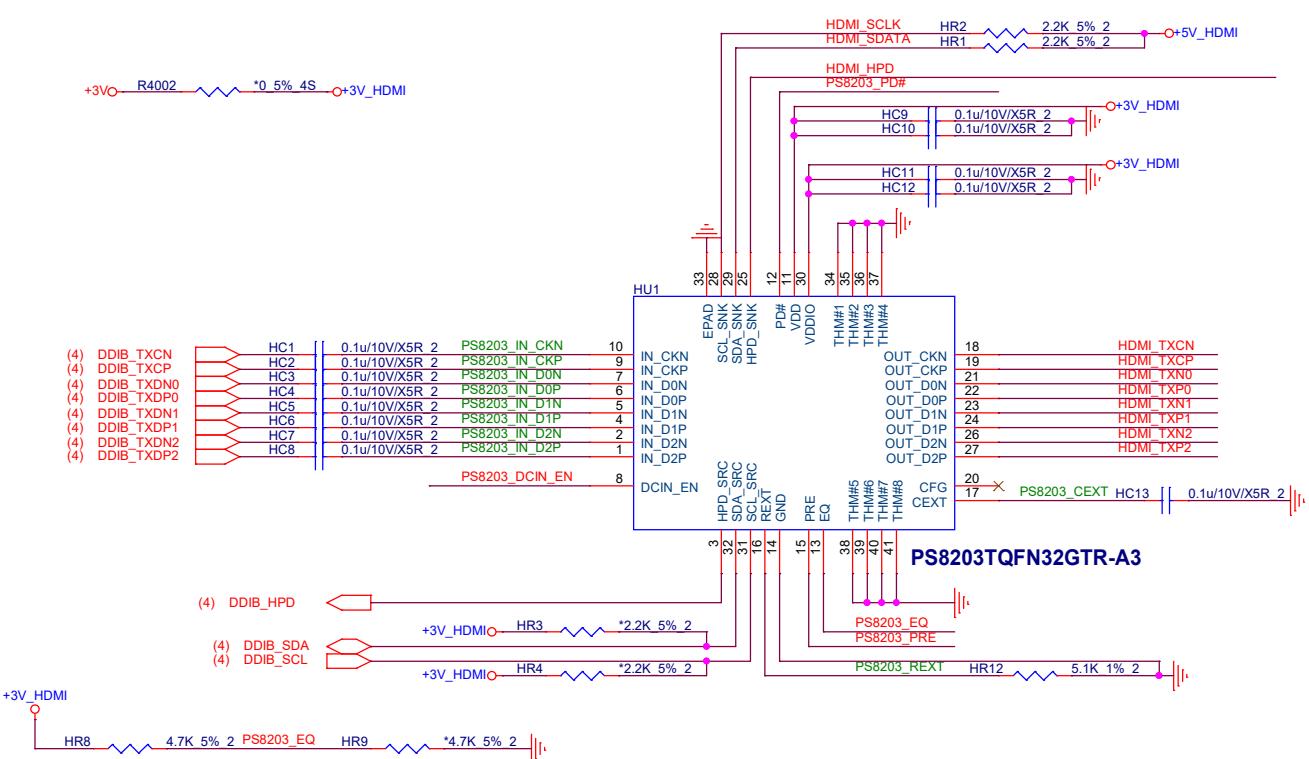
Fingerprint Module



20220317a

Quanta Computer Inc.	
PROJECT : TRA	
Size	Document Number
MB to FP	
Date: Wednesday, February 01, 2023	Rev 1A
Sheet 32	of 50

This part should not contain any substances which are specified in EM-S303.

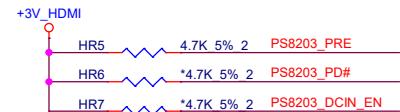
HDMI 1.4b

EQ = Receiver equalization setting; Internal pull down at~150Kohm, 3.3V I/O

L : Programmable EQ for channel loss up to 12.4dB @ 3.0Gbps (default)

H : Programmable EQ for channel loss up to 4.3dB @ 3.0Gbps

M : Programmable EQ for channel loss up to 8.6dB @ 3.0Gbps



PRE = Output pre-emphasis setting for data; Internal pull down at~150Kohm, 3.3V I/O

L : No pre-emphasis (default)

H : 2.5dB pre-emphasis

PD# = Chip power down, Active LOW; Internal pull up at~150Kohm, 3.3V I/O

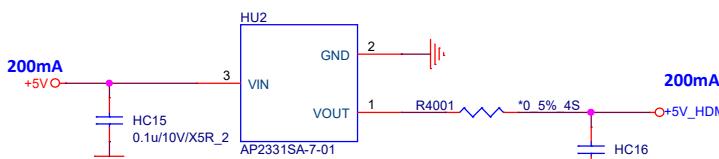
H : Normal operation (default)

L : Chip power down

DCIN_EN = DC coupling enable; Internal pull down at~150Kohm, 3.3V I/O

L : AC coupling (default)

H : DC coupling input



This part should not contain any substances which are specified in EM-S303.

20220602a

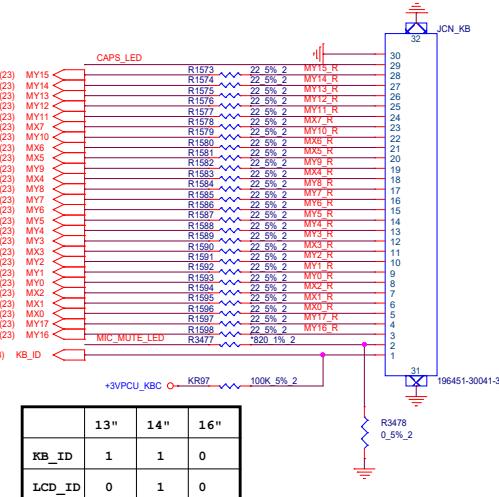
	Quanta Computer Inc.
	PROJECT : TRA
Size	Document Number
	HDMI 1.4b PS8203A

Date: Wednesday, February 01, 2023

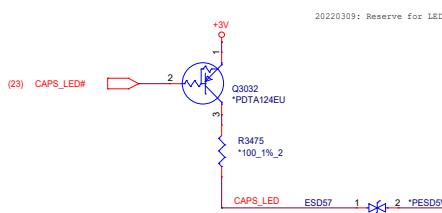
Sheet 1 of 33 of 50

Rev 2A

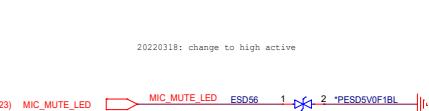
Keyboard Connector



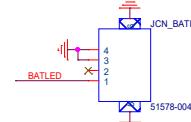
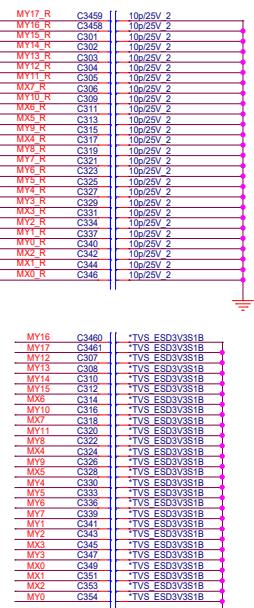
CAPS LED (Reserve)



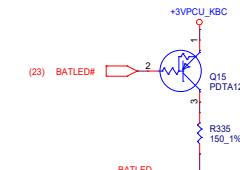
MIC LED (Reserve)



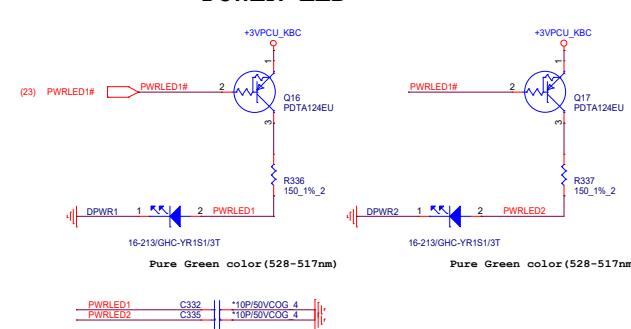
LED



BATTERY LED



POWER LED

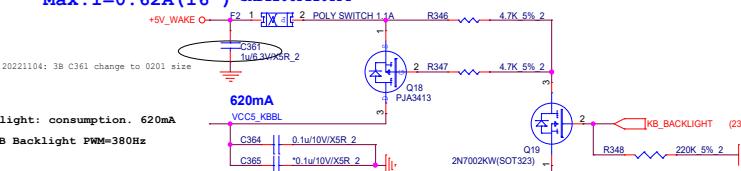


Keyboard Backlight

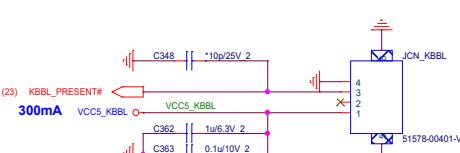
Test case	Pattern6
F2 Temp. (C)	43.7

Temperature	40C	50C
Fuse I- hold current (A)	0.92	0.83

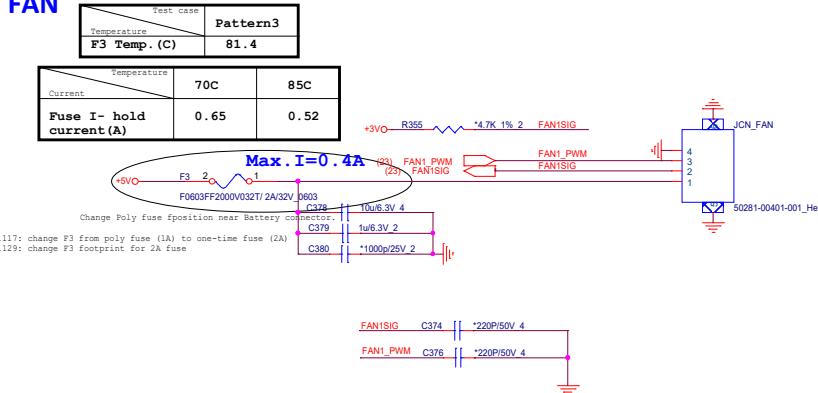
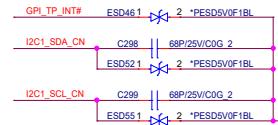
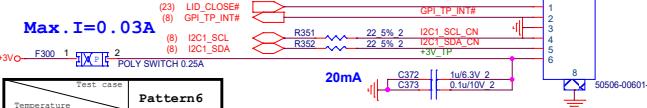
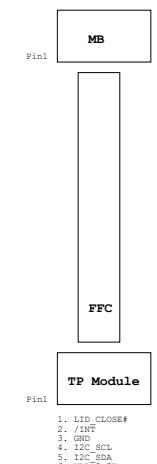
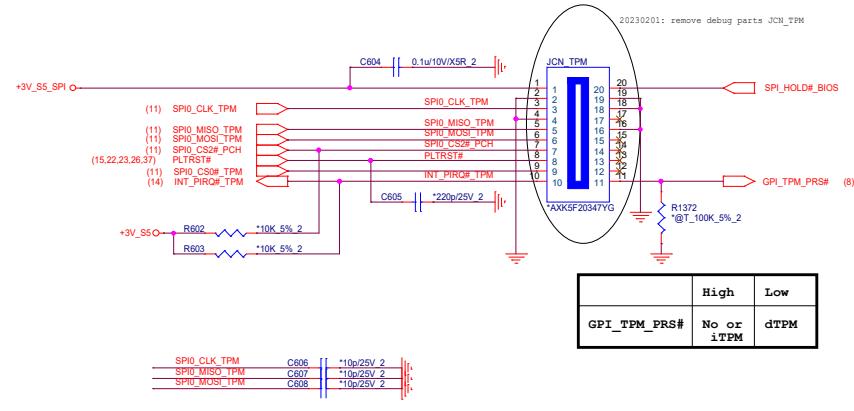
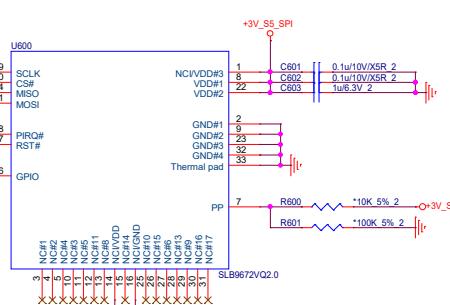
Max. I=0.62A (16") SMD1206P110TFT



KB Backlight Connector

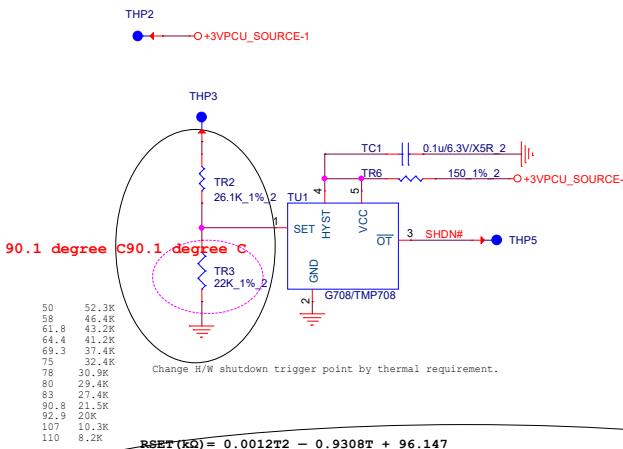


20221104a

FAN**TouchPAD****TPM****TPM on Board**

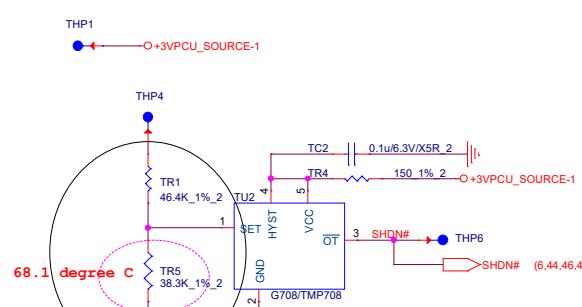
H/W Thermal Protect

As close as possible to CPU

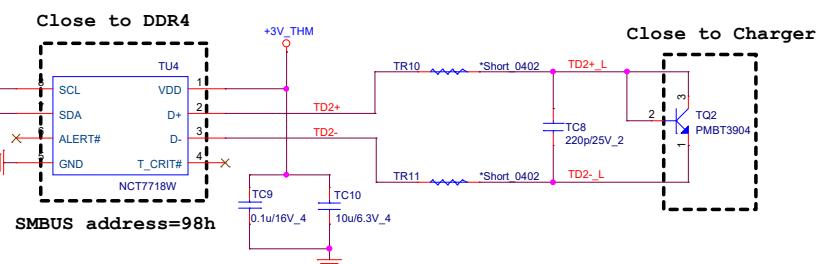
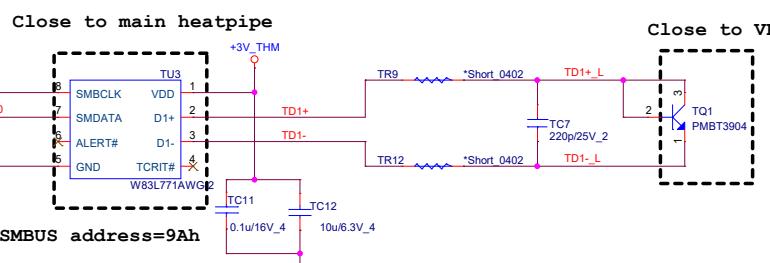


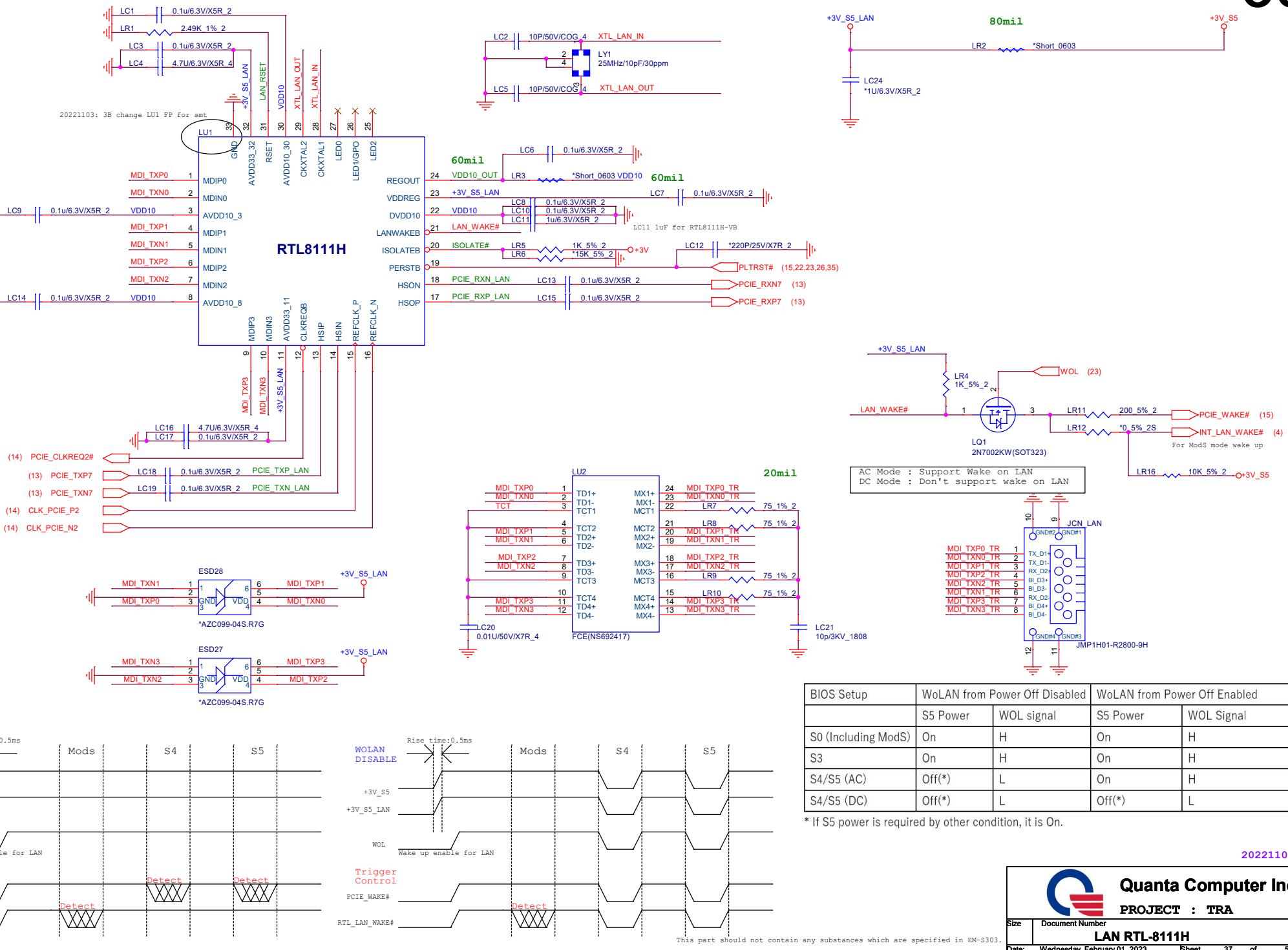
UMA SKU					
Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near USB3 CN sensor temp	68.1	TR5=38.3K	TR5=38.3K		
Near CPU sensor temp	90.1	TR3=22K	TR3=22K		

Thermally far from heat source

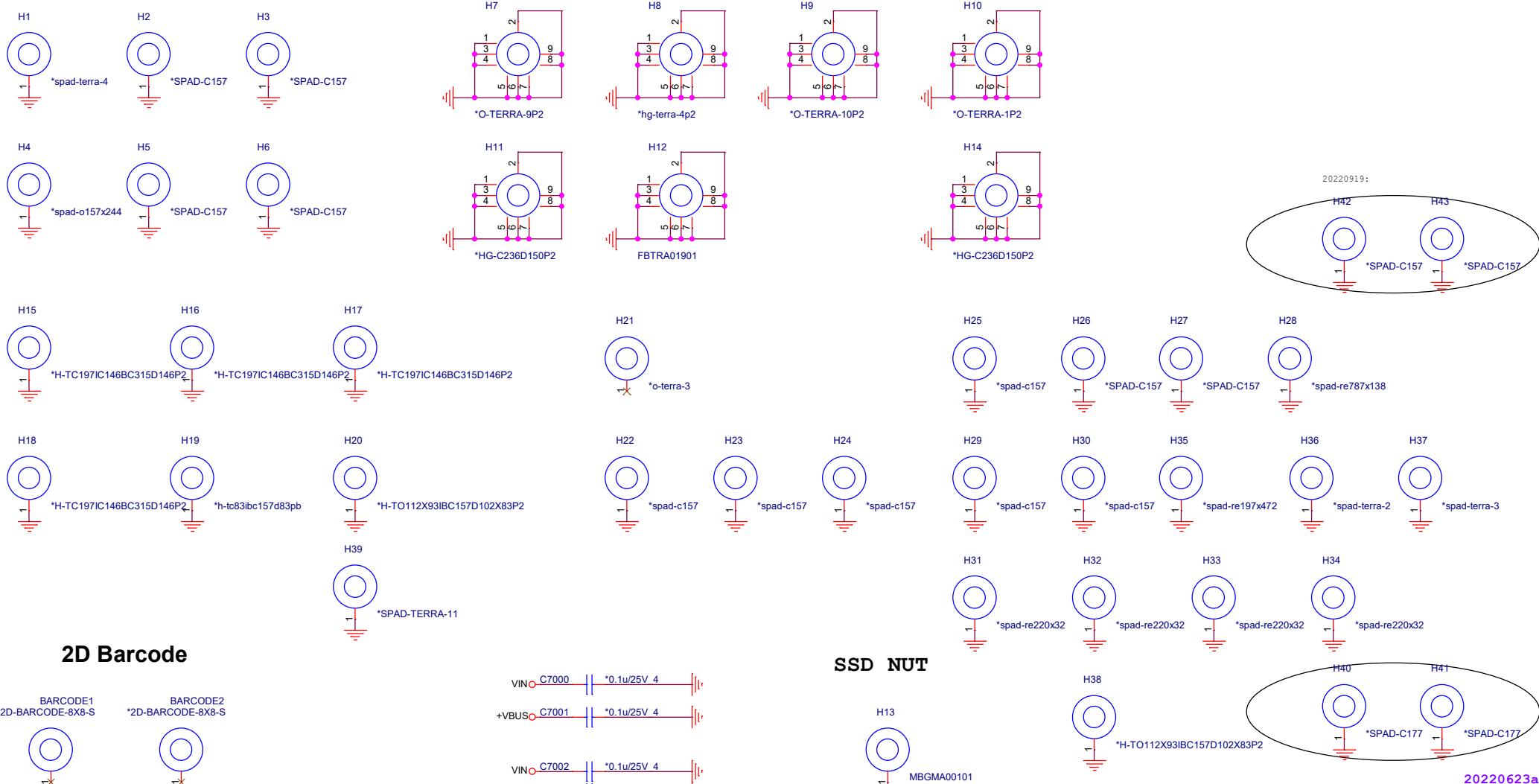


S/W Thermal Protect





Screw Hole



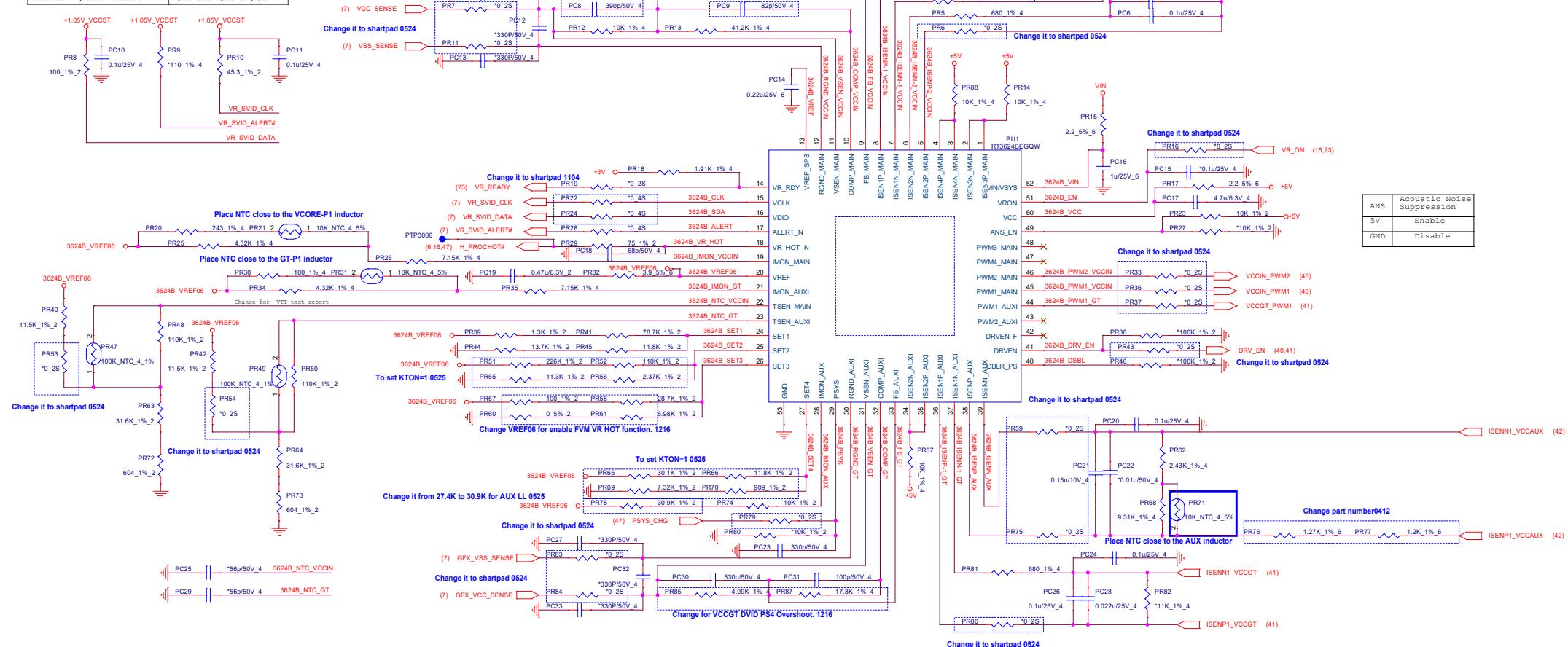
This part should not contain any substances which are specified in EM-S303.

Size	Document Number	Rev
SCREW HOLE		
Date: Wednesday, February 01, 2023	Sheet 1	38 of 50

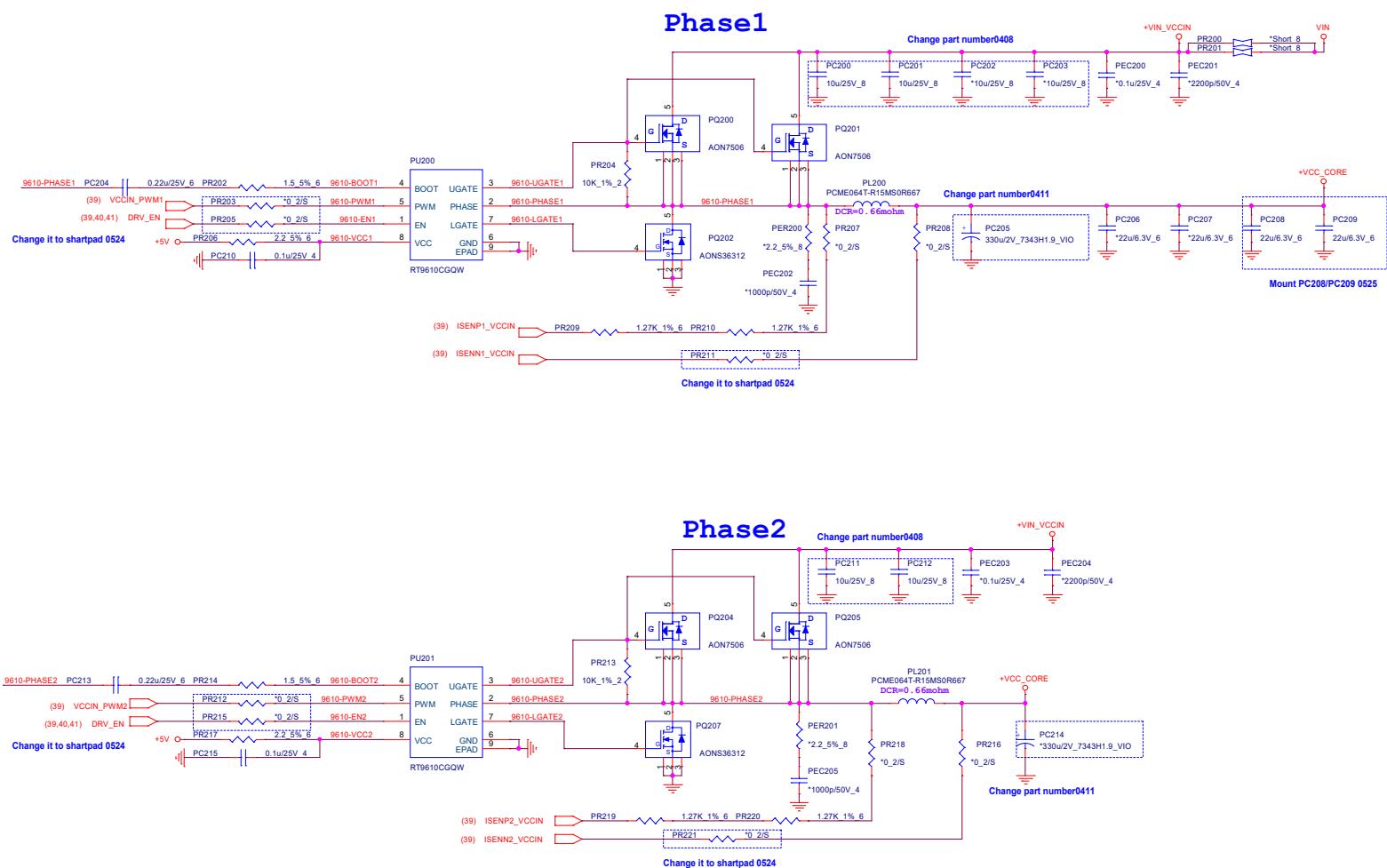
Plateform	SKU	Phase	VCC_CORE					VCC_GT				
			TDC	ICCMAX	DC_LL	AC_LL	Freq	TDC	ICCMAX	DC_LL	AC_LL	Freq
ADL	15W_Performance	2+1	43A	80A	2.8mohm	2.8mohm	421.43kHz	23A	40A	3.2mohm	3.2mohm	421.43kHz
RPL	15W_Performance	2+1	46A	81A	2.8mohm	2.8mohm	421.43kHz	23A	40A	3.2mohm	3.2mohm	421.43kHz

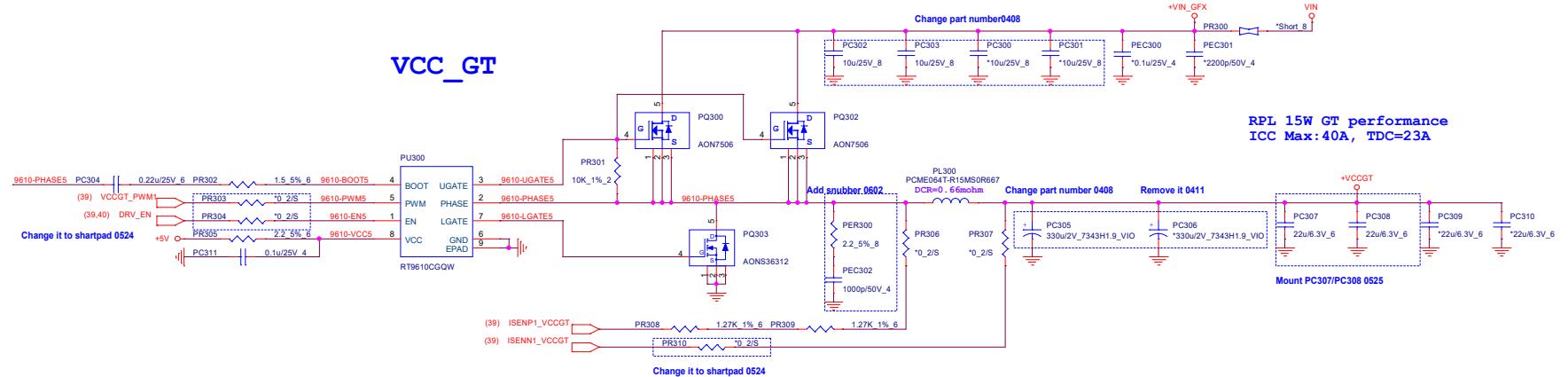
SVID Topology Notes

Note	Detail
SVID signals	VIDSOUT, VIDSK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω
VIDSK platform resistors	Rpu1=Empty, Rpu2=45Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=EmptyΩ

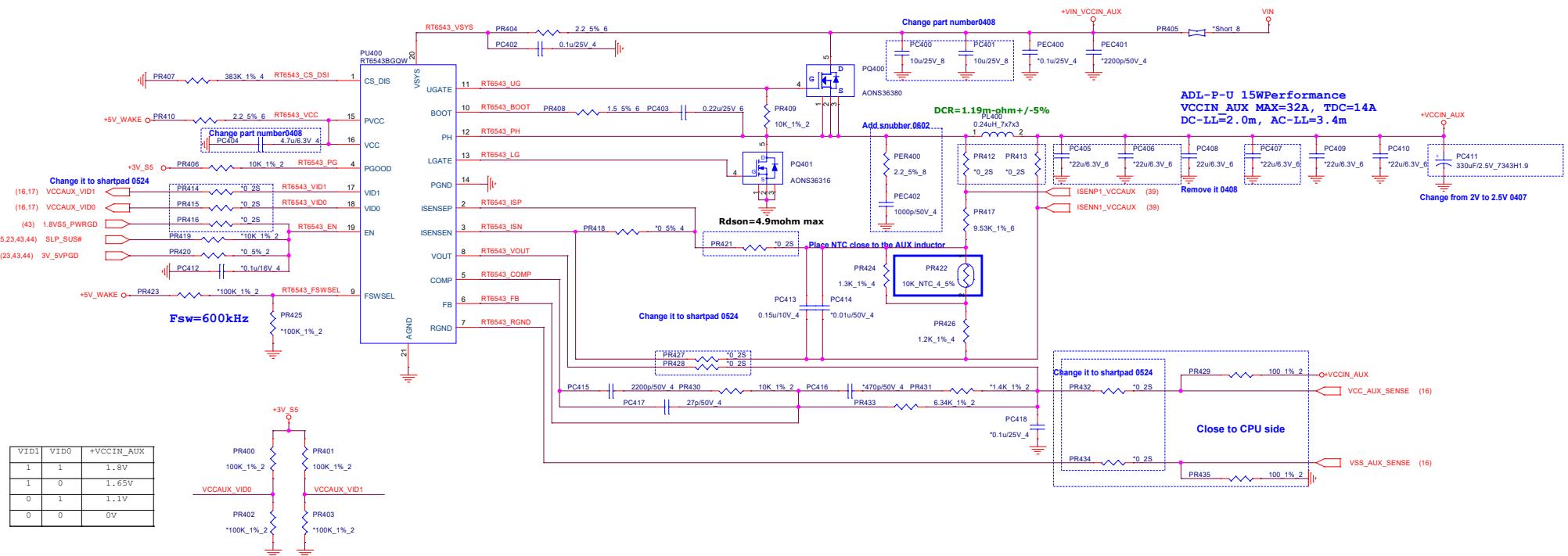


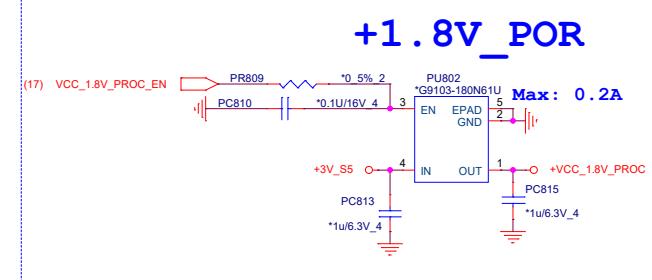
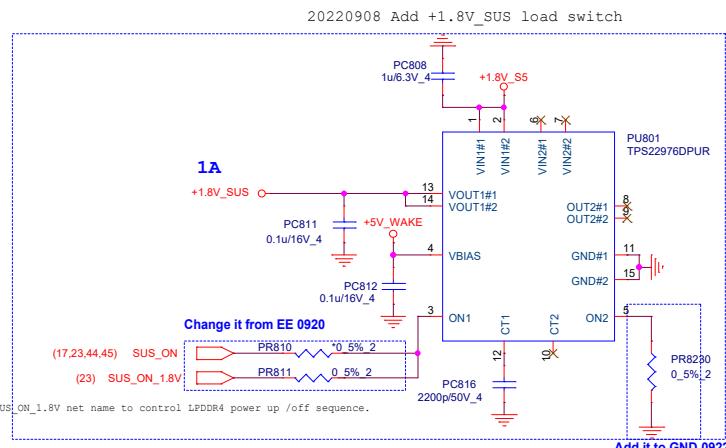
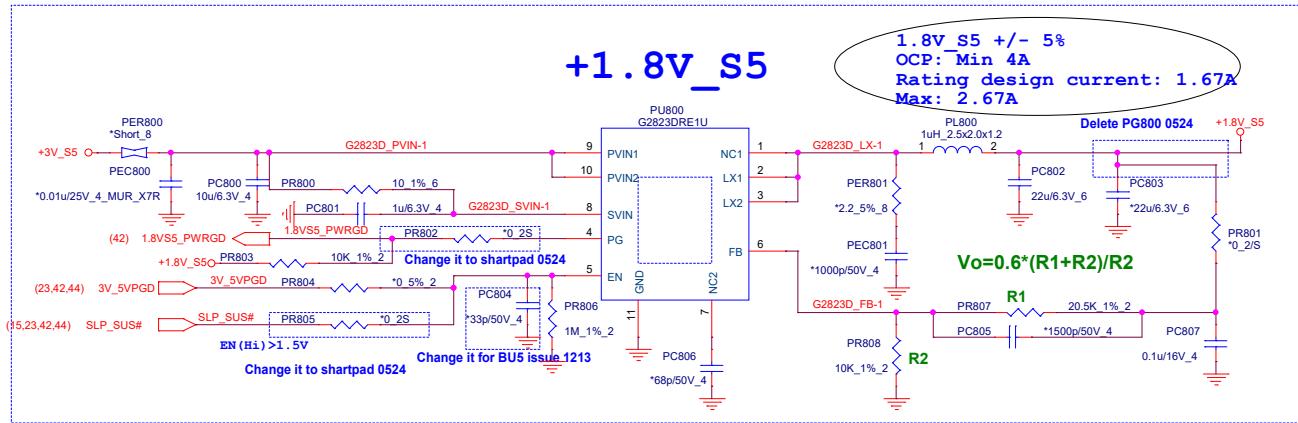
VCC_CORE

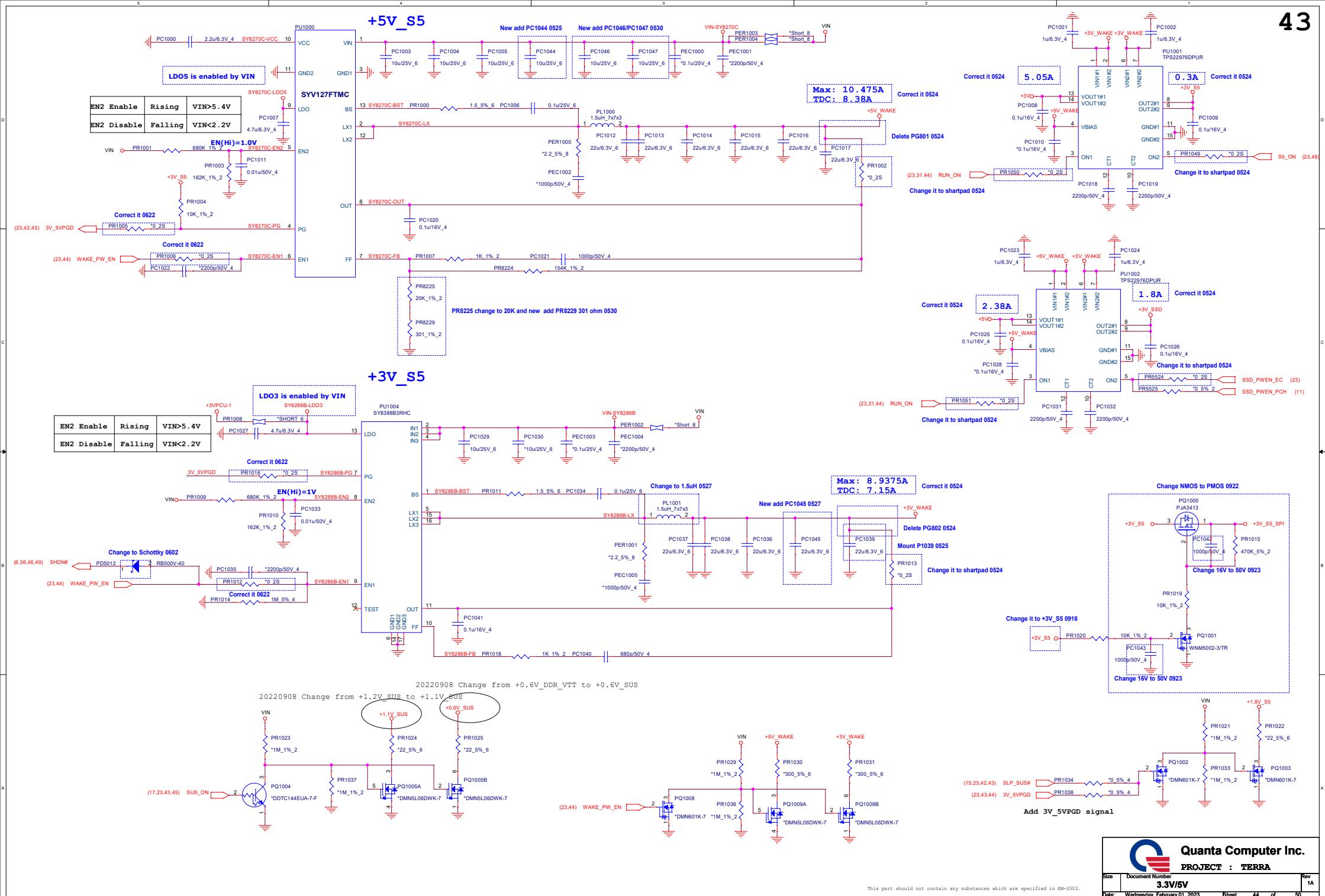


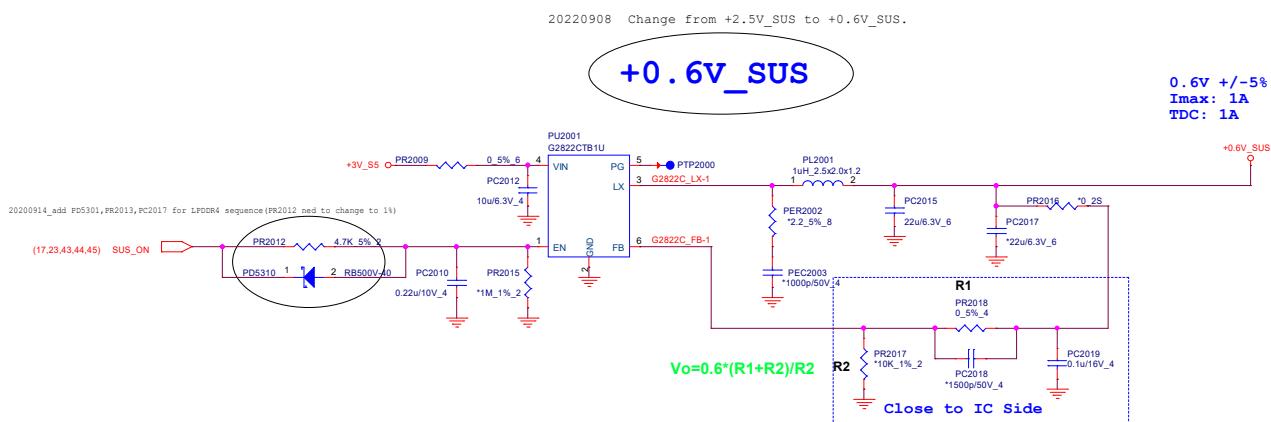
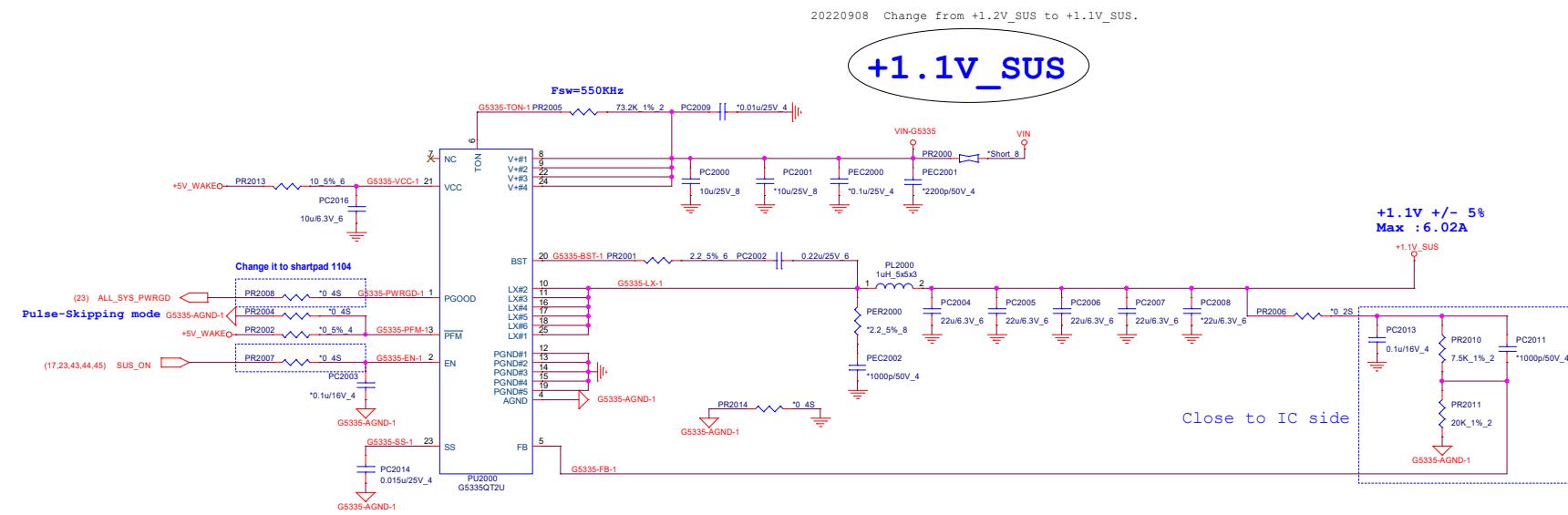


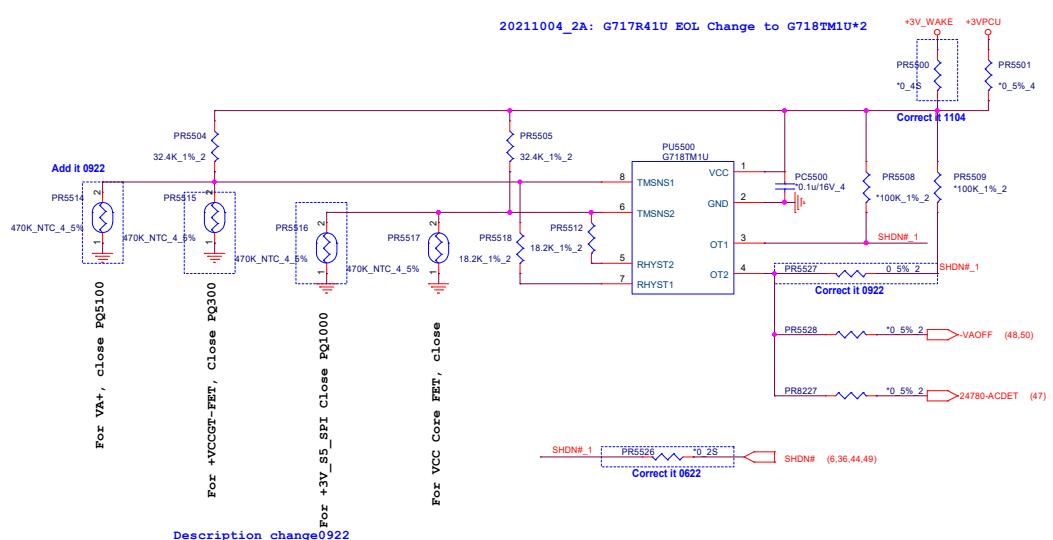
Platform	SKU	Phase	TDC	ICCMAX	DC LL	AC LL	Freq
ADL	15W-Performance	1	14A	32A	2.0mohm	3.4mohm	600kHz
RPL	15W-Performance	1	14A	32A	2.0mohm	3.4mohm	600kHz



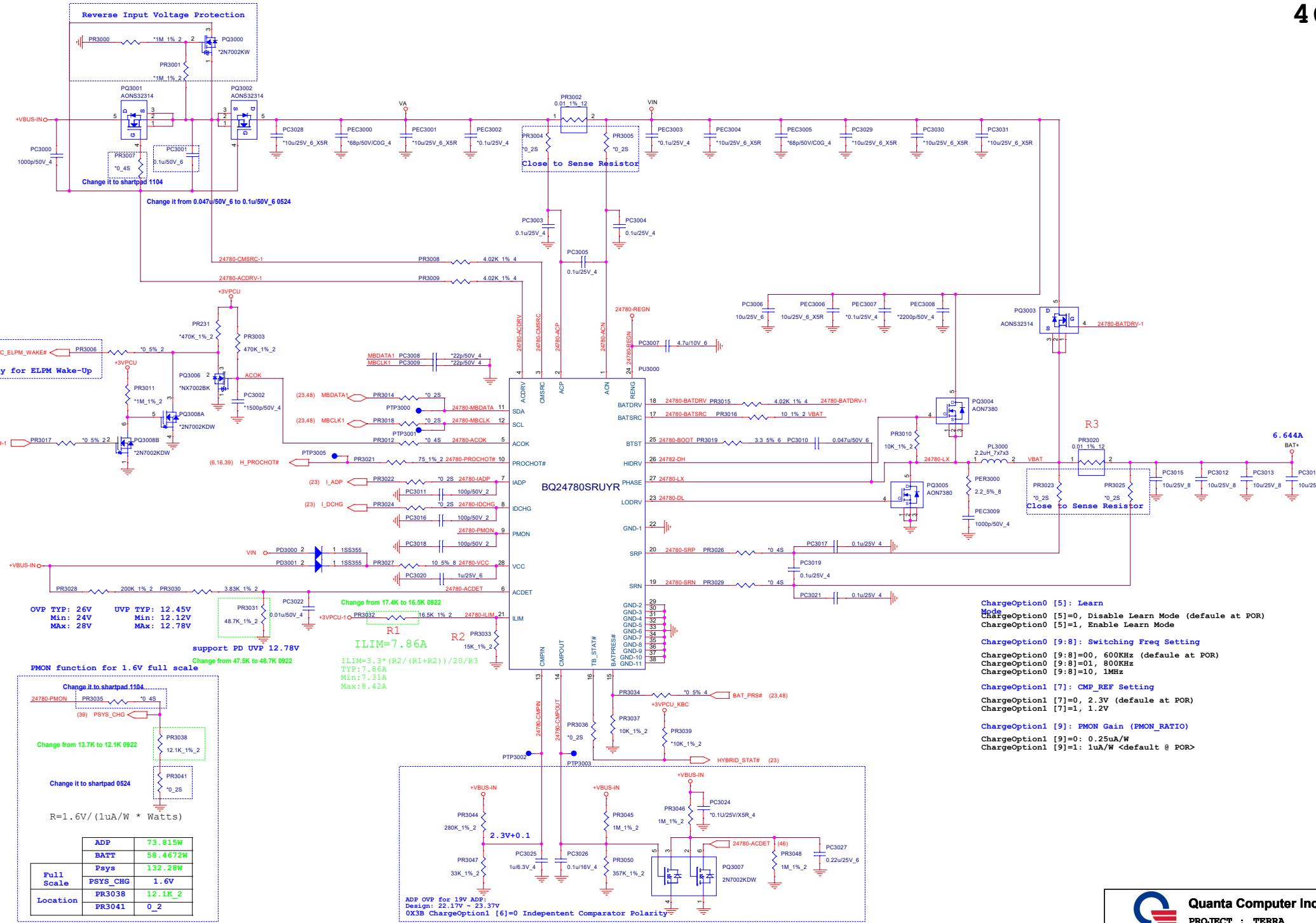


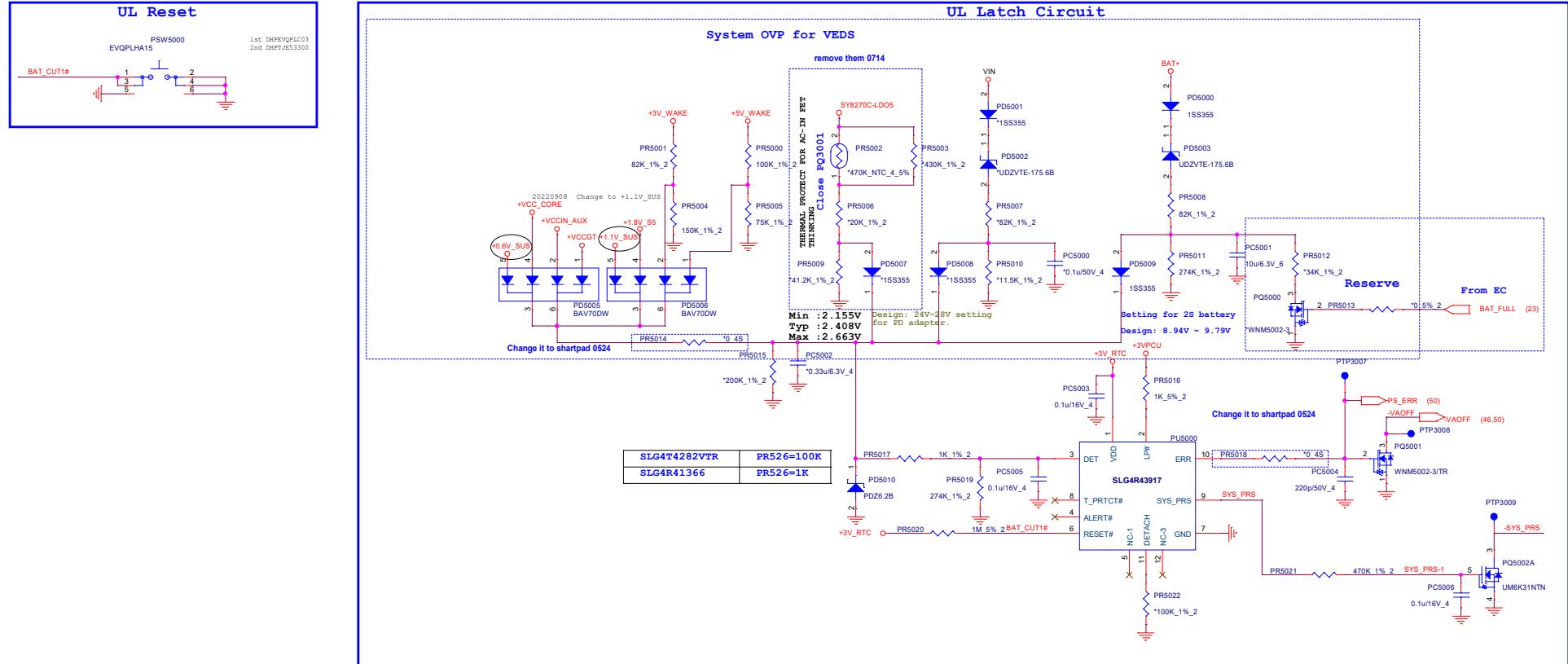






This part should not contain any substances which are specified in EN-6303.





Power for SPI ROM in Dead-Battery Condition

