ABLUE TECHNOLOGY

PTR5620

Bluetooth 5.2 ready multi-protocol Module
Embedded Cortex™ M4 32 bit processor
Support Bluetooth Direct Finding AOA/AOD,
ANT Ideal choice of IoT and Smart product

The PTR5620 ultra-low power Bluetooth 5 ready multiprotocol System on Module based on the nRF52820 from Nordic Semiconductor. The module can support Bluetooth 5.2 by upgrading the protocol stack. The module with an ARM® Cortex™ M4 32 bit processor, 256KB Flash/32KB RAM, Bluetooth 5.1 Direct Finding AOA/AOD support ,
, provide a complete solution with no additional RF design, Bluetooth 5,allowing faster time to market, while simplifying designs, reducing BOM costs, also reduce the burden of Regulatory approvals to enter the world market. Making you more quickly into the Bluetooth smart application and remove the worries.

antenna type:integral antenna
antenna factory informatioan:ABLUE TECH
antenna GAIN:2dBi

Features

- Nordic nRF52820 with ARM Cortex M4
- Multiprotocol support :
  Bluetooth 5.1,
- Bluetooth 5.1 Direction Finding AOA/AOD
- Bluetooth 5: 2 /1Mbps
- Integrated DC-DC converter.
- Serial Wire Debug (SWD)
- Nordic SoftDevice Ready
- Over-the-Air (OTA) firmware update
- Flash/RAM: 256KB/32KB.
- 18 General purpose I/O pins
- low-power comparator with wake-up from System OFF mode
- 12 bit/200KSPS ADC
- Two 2-wire Master/Slave (I2C compatible)
- 2 SPI Master/ 1 SPI Slave)
- 1 UART (with CTS/RTS and DMA)
- USB 2.0 full speed (12 Mbps) controller
- 20 channel CPU independent Programmable Peripheral Interconnect (PPI).
- Quadrature Demodulator (QDEC)
- 128-bit AES HW encryption
- 4 x 32 bits timers, 2 xReal Time Counters (RTC)
- TX power: +8dBm to-20dBm in 4 dB steps.
- PCB antenna
- Sizes: 15.4x15.4 x1.8mm
- DC/DC on board
- No external components required
- Operation voltage: 1.7V to 5.5V

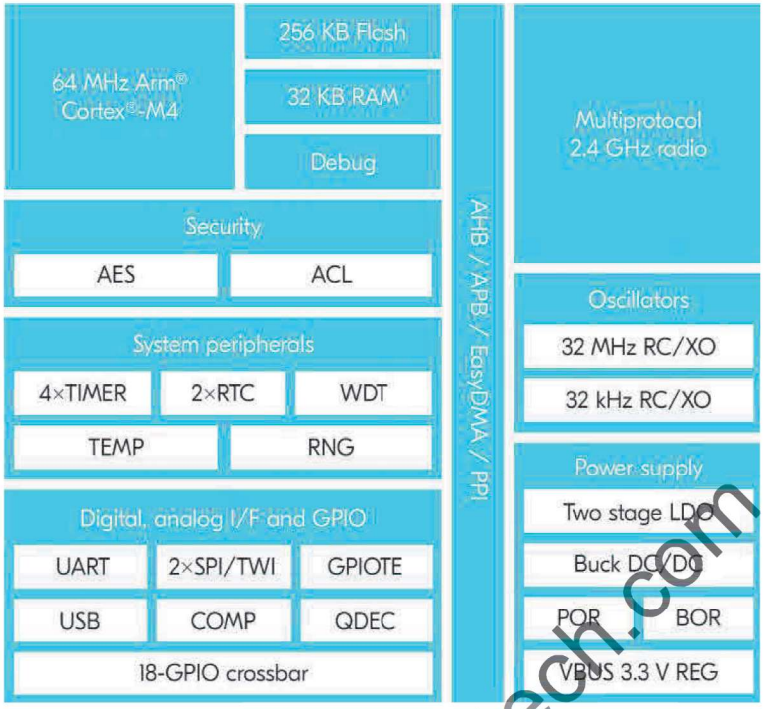
Typical Applications:

- - 2.4 GHz Bluetooth low energy systems
- - Sports and leisure equipment
- - Mobile phone accessories, Connected Appliances
- - Health Care and Medical
- - Consumer Electronics, Game pads
- - Human Interface Devices, Remote control
- - Building environment control / monitoring
- - RFID, Security Applications，Low-Power Sensors
- - Bluetooth Low Energy GateWay
- - iBeacons™, Eddystone™, Indoor navigation
- - Lighting Products
- - Fitness devices, Wearables

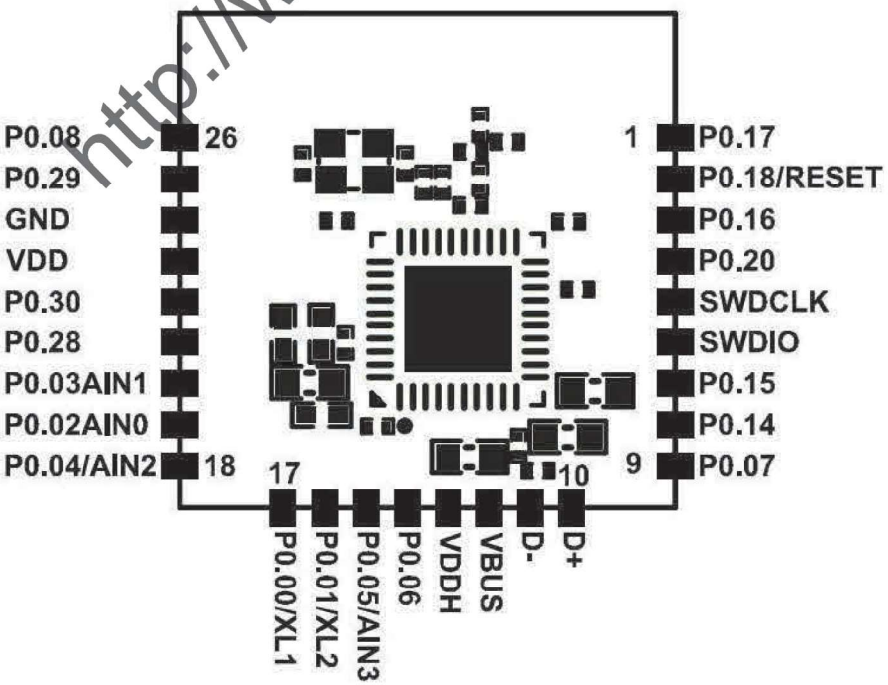
Quick Specifications:

Multi-protocol	
Version	Bluetooth 5.2
Security	AES-128
Radio	
Frequency	2.402GHz to 2.480GHz
Modulations	GFSK at 2/1 Mbps
Transmit power	+8dBm to -20dBm
Receiver sensitivity	-103dBm@BLE, -95dBm@BLE 1M
Antenna	Ext. IPX Antenna
Current Consumption	
TX only @ +8 dBm, @ 3V, DC/DC enabled	14.0 mA
TX only @ 0 dBm, @ 3V, DC/DC enabled	4.9 mA
RX only @ 1 Mbps @ 3V, DC/DC enabled	4.7 mA
CPU @ 64MHz from flash @ 3V, DC/DC	3.3 mA
System On	1.5 µA
System Off	0.6µA
Operating conditions	
Power supply	1.7~5.5V
Operating temperature	-25~+85 °C

Block diagram:



Pin Description of Module（Top View）:



Pin	Name	Description	Recommend usage
Pin1	P0.17	Digital I/O	Standard drive, low frequency I/O
Pin2	P0.18/RESET	Digital I/O/ RESET	
Pin3	P0.16	Digital I/O	Standard drive, low frequency I/O
Pin4	P0.20	Digital I/O	
Pin5	SWDCLK	HW debug and programming	
Pin6	SWDIO	HW debug and programming	
Pin7	P0.15	Digital I/O	
Pin8	P0.14	Digital I/O	
Pin9	P0.07	Digital I/O	
Pin10	D+	USB D+	USB
Pin11	D-	USB D-	USB
Pin12	VBUS	USB Power	5 V input for USB 3.3 V regulator
Pin13	VDDH	High voltage power supply	
Pin14	P0.06	Digital I/O	
Pin15	P0.05/AIN3	Digital I/O/Analog input 3	
Pin16	P0.01/XL2	Reserve for 32.768KHz use	
Pin17	P0.00/XL1	Reserve for 32.768KHz use	
Pin18	P0.04/AIN2	Digital I/O/Analog input 2	
Pin19	P0.02/AIN0	Digital I/O/Analog input 0	
Pin20	P0.03/AIN1	Digital I/O/Analog input1	Standard drive, low frequency I/O
Pin21	P0.28	Digital I/O	Standard drive, low frequency I/O
Pin22	P0.30	Digital I/O	Standard drive, low frequency I/O
Pin23	VDD	Power Supply	
Pin24	GND	Ground	
Pin25	P0.29	Digital I/O	Standard drive, low frequency I/O
Pin26	P0.08	Digital I/O	Standard drive, low frequency I/O

*Low frequency I/O is signals with a frequency up to 10 kHz

*Internal 32.768 kHz RC oscillator is used to provide low frequency clock by default. If you want to use an external crystal, you can use the reserved pins (Pin16 and Pin17) to connect the external crystal and modify the firmware configuration.

Note: An internal 4.7μF bulk capacitor has been included on the module. For those application that with heavy GPIO usage and/or current draw, it is good design practice to add additional bulk capacitance as required for your application.

General Purpose I/O:

Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be

interfaced through the PPI at the same time is limited by the number of GPIOTE channels

- All pins can be individually configured to carry serial interface or quadrature demodulator signals

Hardware RESET:

There is on-chip power-on reset circuitry, But can still be used in external reset mode, in this case, GPIO pin P0.18 as an external hardware reset pin. In order to utilize P0.18 as a hardware reset, the UICR registers PSELRESET[0] and PSELRESET[1] must be set alike, to the value of 0x7FFFFF12. When P0.18 is programmed as RESET, the internal pull-up is automatically enabled.

HW debug and flash programming of Module :

The Module support the two pin Serial Wire Debug (SWD) interface and offers flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support.

Pin	Flash Program interface
SWDIO	Debug and flash programming I/O
SWDCLK	Debug and flash programming I/O

This is the hardware debug and flash programming of module, J-Link Lite support, please refer www.segger.com.

Power and Configuration:

The module has two internal regulator stages. REG1 regulator stage has the regulator type options of Low-dropout regulator (LDO) and Buck regulator (DC/DC). REG0 regulator stage has only the option of Low-dropout regulator (LDO). The first regulator, REG0, is fed by the VDDH pin and can accept a source voltage of 2.5 V to 5.5 V. The output of REG0 is connected to the VDD pin and the input of the second regulator stage REG1. REG1 supplies power to the module core and can accept an input source voltage of 1.7V to 3.6V. Depending on how the VDD and VDDH pins are connected, the module will operate in one of two modes: Normal/Low Voltage (LV) or High Voltage (HV). The voltage present on the VDD pin is always the GPIO high logic level voltage, regardless of power mode.

To enter LV Mode, the same source voltage is applied to both the VDD and VDDH pins causing REG0 to automatically shut down leaving only the REG1 stage active. To enter HV, the source voltage is only applied to VDDH causing the VDD pin to become an output source supplied by REG0.

Mode	Pin of Module	Name	Power Connection
Normal/Low Voltage (LV)	Pin 23	VDD	1.7V to 3.6V source in
	Pin 13	VDDH	Same source as VDD
High Voltage (HV)	Pin 23	VDD	1.8V to 3.3V supply out
	Pin 13	VDDH	2.5V to 5.5V source in

Important: In both LV and HV modes, the GPIO logic level voltage is determined by the VDD pin. In HV mode, all external devices that are connected to the Module's GPIO must either be powered by

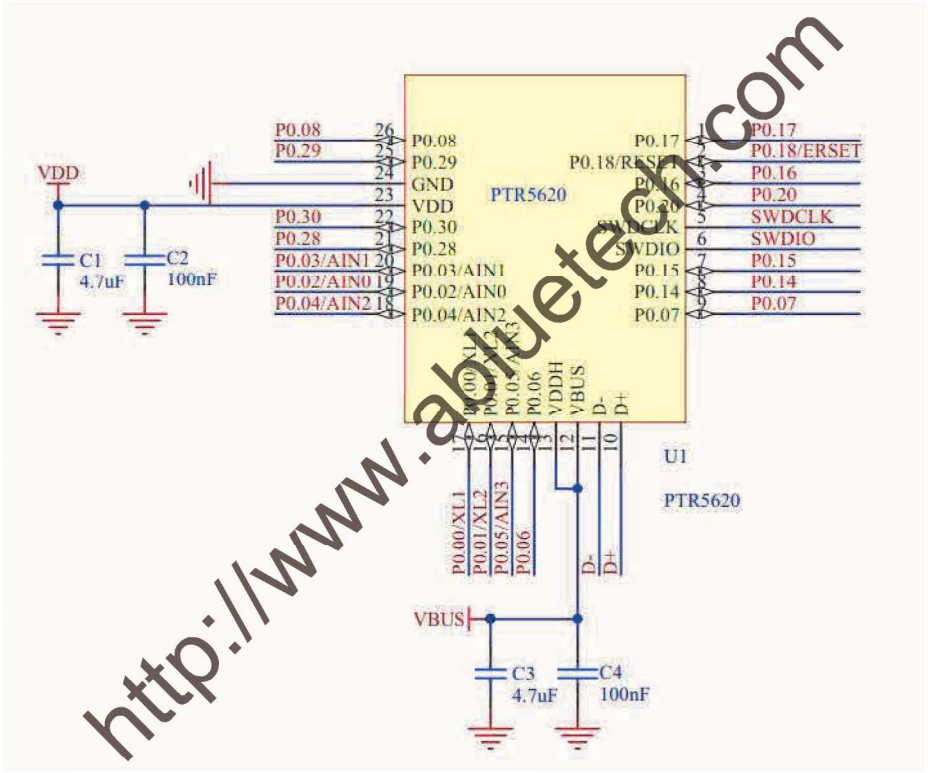
the module (from VDD) or use level translation.

USB Power: The USB interface on the Module can be used when the module is in either Normal /Low Voltage (LV) or High Voltage (HV) mode. The Module USB PHY is powered by a dedicated, internal LDO regulator that is fed by the VBUS pin (Pin43). This means that applying power to only the VBUS pin will not power the rest of the module. In order for the USB PHY to operate, VBUS must be externally powered.

Reference circuitry:

In this section there are 3 reference circuits to show how to design an application circuit with this module.

Reference Circuit configuration 1



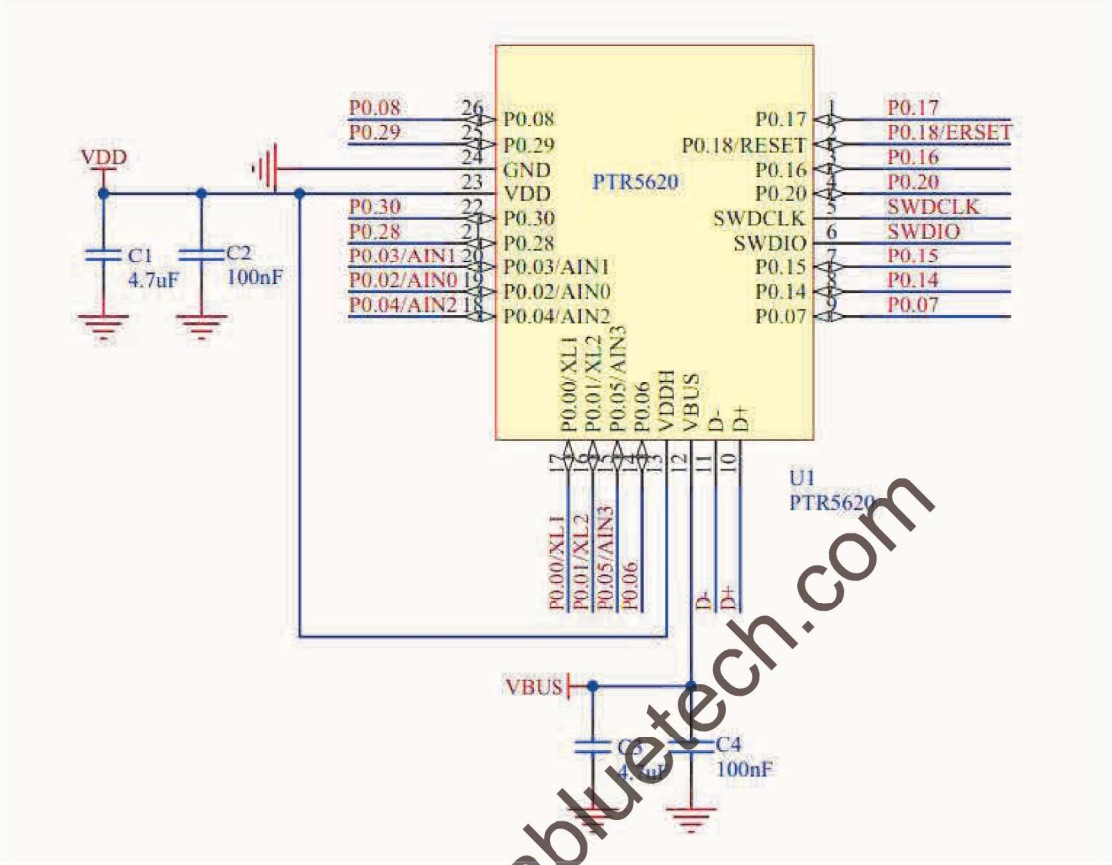
Configurations summary for reference circuit 1

Config no.	Main Supply		EXT Supply Output	USB
	VDDH	VDD		
Config.1	Battery/Ext.regulator	N/A	Yes	Yes

Explanation of symbols in reference circuit 1 schematic

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DDH}	Main supply voltage in high voltage mode	2.5	3.7	5.5	V
V_{BUS}	Supply voltage on VBUS pin	4.35	5	5.5	V
V_{EXT}	Voltage output on VDD when supplied from internal regulator (REG0). V_{DDH} is the input to REG0.	1.8		3.3	V

Reference Circuit configuration 2



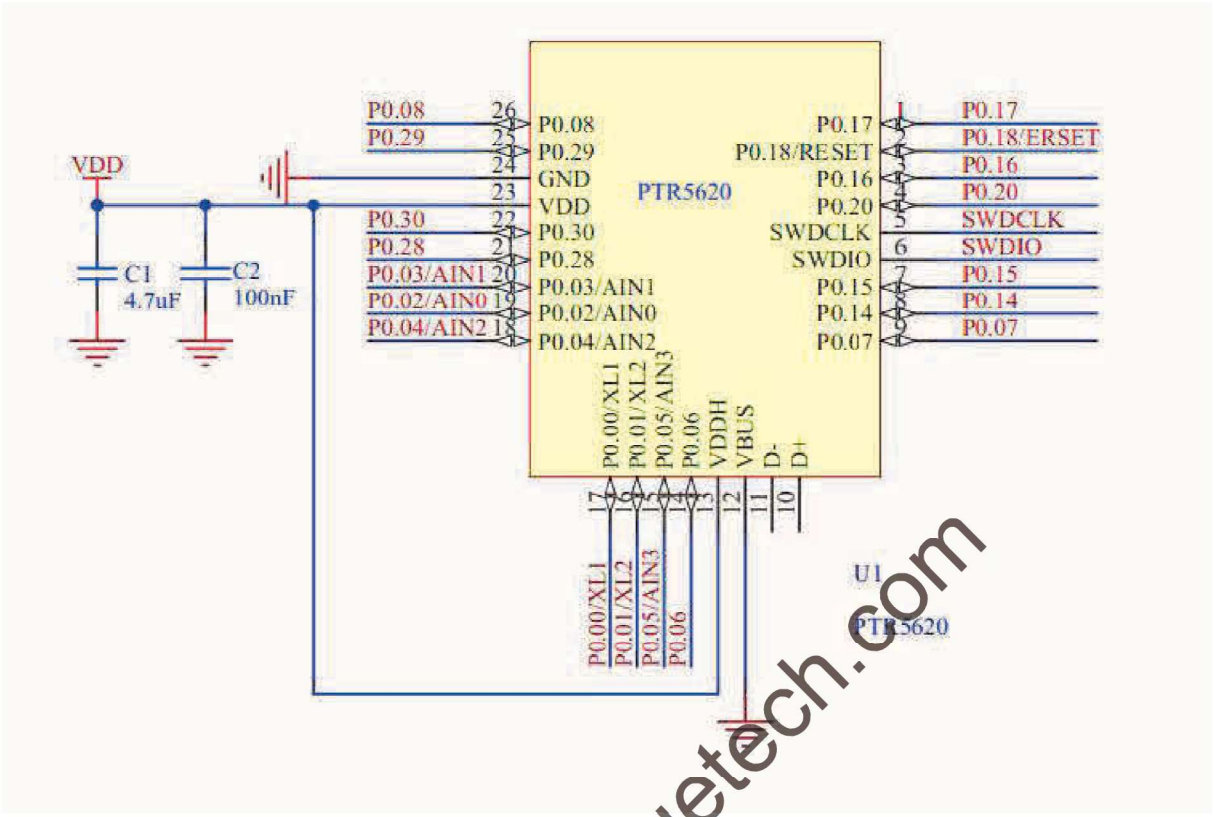
Configurations summary for reference circuit 2

Config no.	Main Supply		EXT Supply Output	USB
	VDDH	VDD		
Config.2	N/A	Battery/Ext.regulator	No	Yes

Explanation of symbols in reference circuit 2 schematic

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Main supply voltage in normal voltage mode	1.7	3	3.6	V
V_{BUS}	Supply voltage on VBUS pin	4.35	5	5.5	V

Reference Circuit configuration 3



Configurations summary for reference circuit 3

Config no.	Main Supply		EXT Supply Output	USB
	VDDH	VDD		
Config.3	N/A	Battery/Ext.regulator	No	No

Explanation of symbols in reference circuit 3 schematic

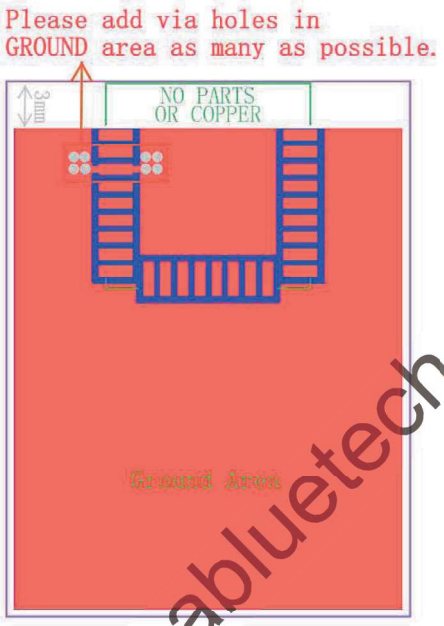
Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Main supply voltage in normal voltage mode	1.7	3	3.6	V

Some general guidance is summarized here:

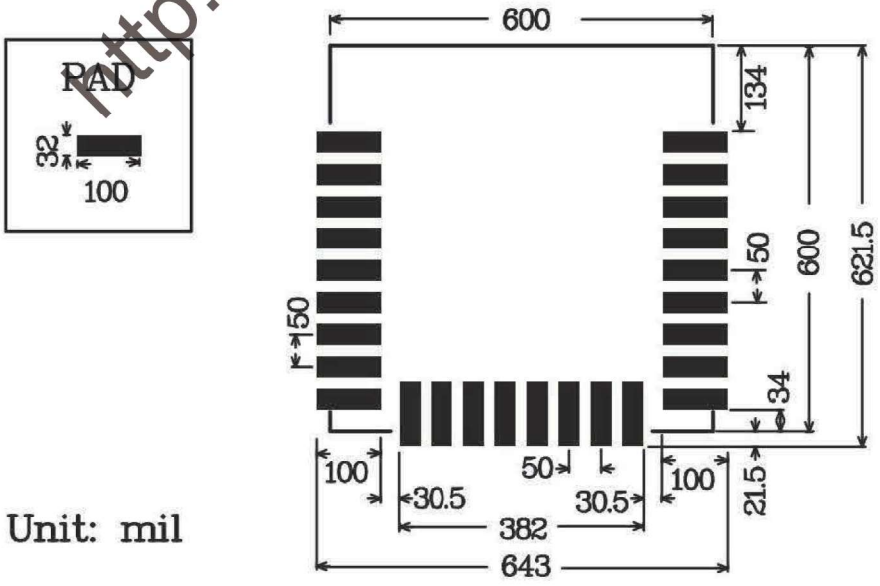
- Main supply voltage is connected to VDD/VDDH. The system will enter one of two supply voltage modes, normal or high voltage mode, depending on how the supply voltage is connected to these pins. Normal voltage mode is entered when the supply voltage is connected to both the VDD and VDDH pins (so that VDD equals VDDH).High voltage mode is entered when the supply voltage is only connected to the VDDH pin and the VDD pin is not connected to any voltage supply.
- By default, the LDO regulators in the chip are enabled and the DC/DC regulator of REG1 stage is disabled. Register DCDCEN is used to enable the DC/DC regulator for REG1 stage. External LC filters has been connected in the Module for DC/DC regulators being used.
- The GPIO high reference voltage always equals the level on the VDD pin. In normal voltage mode, the GPIO high level equals the voltage supplied to the VDD pin, and in high voltage mode it equals the level specified in the register REGOUT0 UICR registers.
- When the power is supplied to VDDH, the output from the VDD pin could be used to supply external circuitry. The feature must be configured in the EXTSUPLLY and REGOUT0 UICR registers. In the reference circuitry, External supply is annotated with the VEXT net name.
- When using the USB peripheral, a 5V USB supply needs to be provided on the VBUS pin.

Recommended RF Layout & Ground Plane:

The module integrated antenna requires a suitable ground plane to radiate effectively. The area under and extending out from the antenna portion of the module should be kept clear of copper and other metal. The module should be placed at the edge of the PCB with the antenna edge facing out. Reducing the ground plane will reduce the effective radiated power. Please add as more as possible via holes on the mother board near the GND pin of module, this will be good for the RF performance of system board.



PCB Footprint （Top View）:



Unit: mil