Blockstream Jade v1

V0.01

1.OUTLINE

Blockstream Jade v1 is ESP32 board which based on ESP32-D0WDQ6-V3 module. The board is made of PC+ABC.

1.1 Hardware Composition

The hardware of **Blockstream Jade v1**: ESP32-D0WDQ6-V3, TFT screen, camera 、Button,, TypeC-to-USB interface, Power Management chip and battery.

ESP32 is a single 2.4 GHz Wi-Fi-and-Bluetooth combo chip designed with the TSMC ultra-low-power 40 nmtechnology. It is designed to achieve the best power and RF performance, showing robustness, versatility andreliability in a wide variety of applications and power scenarios.

The **LCD** is a 1.14 inch color screen driven by st7789, with a resolution of 135 × 240. Working temperature -30-85c.

The **power management chip** is AXP192 chip of X-Powers. The operating voltage ranges from 2.9V to 6.3V. Charging current of 1.4A.

2. PIN DESCRIPTION

2.1. USB INTERFACE

Blockstream Jade v1 Configuration Type-C type USB interface, support USB2.0 standard communication protocol.

3. FUNCTIONAL DESCRIPTION

This chapter describes the ESP32-D0WDQ6-V3 various modules and functions.

3.1. CPU AND MEMORY

ESP32 contains one or two low-power Xtensa®32-bit LX6 microprocessor(s) with the following features::

- 448-KB of ROM, and the program starts for the kernel function calls
- For a 520 KB instruction and data storage chip SRAM
- RTC flash memory of 8 KB SRAM, when the RTC can be started in Deep-sleep mode, and for storing data accessed by the main CPU
- RTC slow memory, of 8 KB SRAM, can be accessed by the coprocessor in Deep-sleep mode
- Of 1 kbit of eFuse, which is a 256 bit system-specific (MAC address and a chip set); the remaining 768 bit reserved for user program, these Flash program include encryption and chip ID

3.2. STORAGE DESCRIPTION

3.2.1. External Flash and SRAM

ESP32 support multiple external QSPI flash and static random access memory (SRAM), having a hardware-based AES encryption to protect the user programs and data.

- ESP32 access external QSPI Flash and SRAM by caching. Up to 16 MB external Flash code space is mapped into the CPU, supports 8-bit, 16-bit and 32-bit access, and can execute code.
- Up to 8 MB external Flash and SRAM mapped to the CPU data space, support for 8-bit, 16-bit and 32-bit access. Flash supports only read operations, SRAM supports read and write operations.

3.3. RTC MANAGEMENT AND LOW POWER CONSUMPTION

ESP32 uses advanced power management techniques may be switched between different power saving modes. (See Table 5).

- *Power saving mode*

  - Active Mode: RF chip is operating. Chip may receive and transmit a sounding signal.

  - Modem-sleep mode: CPU can run, the clock may be configured. Wi-Fi / Bluetooth baseband and RF

  - Light-sleep mode: CPU suspended. RTC and memory and peripherals ULP coprocessor operation. Any wake-up event (MAC, host, RTC timer or external interrupt) will wake up the chip.

  - Deep-sleep mode: only the RTC memory and peripherals in a working state. Wi-Fi and Bluetooth connectivity data stored in the RTC. ULP coprocessor can work.

  - Hibernation Mode: 8 MHz oscillator and a built-in coprocessor ULP are disabled. RTC memory to restore the power supply is cut off. Only one RTC clock timer located on the slow clock and some RTC GPIO at work. RTC RTC clock or timer can wake up from the GPIO Hibernation mode.

- *Deep-sleep mode*

  - related sleep mode: power save mode switching between Active, Modem-sleep, Light-sleep mode. CPU, Wi-Fi, Bluetooth, and radio preset time interval to be awakened, to ensure connection Wi-Fi / Bluetooth.

  - Ultra Low-power sensor monitoring methods: the main system is Deep-sleep mode, ULP coprocessor is periodically opened or closed to measure sensor data. The sensor measures data, ULP coprocessor decide whether to wake up the main system.

Functions in different power consumption modes: TABLE 5

Power consumption mode	Active	Modem-sleep	Light-sleep	Deep-sleep	Hibernation
Sleep mode	Associated sleep mode			Ultra low-power Sensor measures data	-
CPU	open	open	pause	close	close
Wi-Fi/Bluetooth Radio	open	open	close	close	close
RTC memory	open	open	open	open	close
ULP coprocessor	open	open	open	open/close	close

Press and hold the side power button for two seconds to start the device. Press and hold for more than 6 seconds to turn off the device. Switch to the photo mode through the Home screen, and the avatar that can be obtained through the camera is displayed on the tft screen.The USB cable must be connected when working, and the lithium battery is used for short-term storage to prevent power failure.

FCC Statement：
Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference,and
(2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.