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SCC_20M_3634.9MHz_Q64_FULLRB_CSE0a



SCC_20M_3634.9MHz_Q64_FULLRB_CSE1



SCC_20M_3634.9MHz_Q64_FULLRB_CSE3



SCC_20M_3634.9MHz_Q64_FULLRB_CSE0b



SCC_20M_3634.9MHz_Q64_FULLRB_CSE2



SCC_20M_3634.9MHz_Q64_FULLRB_CSEpart9 6





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SCC_20M_3634.9MHz_QPSK_1RB_CSE0a



SCC_20M_3634.9MHz_QPSK_1RB_CSE1



SCC_20M_3634.9MHz_QPSK_1RB_CSE3



SCC_20M_3634.9MHz_QPSK_1RB_CSE0b



SCC_20M_3634.9MHz_QPSK_1RB_CSE2



SCC_20M_3634.9MHz_QPSK_1RB_CSEpart96





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SCC_20M_3634.9MHz_QPSK_FULLRB_CSE0a



SCC_20M_3634.9MHz_QPSK_FULLRB_CSE1



SCC_20M_3634.9MHz_QPSK_FULLRB_CSE3



SCC_20M_3634.9MHz_QPSK_FULLRB_CSE0b



SCC_20M_3634.9MHz_QPSK_FULLRB_CSE2



SCC_20M_3634.9MHz_QPSK_FULLRB_CSEpart96





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SCC_20M_3690MHz_Q16_1RB_CSE0a



SCC_20M_3690MHz_Q16_1RB_CSE1



SCC_20M_3690MHz_Q16_1RB_CSE3



SCC_20M_3690MHz_Q16_1RB_CSE0b



SCC_20M_3690MHz_Q16_1RB_CSE2



SCC_20M_3690MHz_Q16_1RB_CSEpart96





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SCC_20M_3690MHz_Q16_FULLRB_CSE0a



SCC_20M_3690MHz_Q16_FULLRB_CSE1



SCC_20M_3690MHz_Q16_FULLRB_CSE3



SCC_20M_3690MHz_Q16_FULLRB_CSE0b



SCC_20M_3690MHz_Q16_FULLRB_CSE2



SCC_20M_3690MHz_Q16_FULLRB_CSEpart96





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SCC_20M_3690MHz_Q64_1RB_CSE0a



SCC_20M_3690MHz_Q64_1RB_CSE1



SCC_20M_3690MHz_Q64_1RB_CSE3



SCC_20M_3690MHz_Q64_1RB_CSE0b



SCC_20M_3690MHz_Q64_1RB_CSE2



SCC_20M_3690MHz_Q64_1RB_CSEpart96





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SCC_20M_3690MHz_Q64_FULLRB_CSE0a



SCC_20M_3690MHz_Q64_FULLRB_CSE1



SCC_20M_3690MHz_Q64_FULLRB_CSE3



SCC_20M_3690MHz_Q64_FULLRB_CSE0b



SCC_20M_3690MHz_Q64_FULLRB_CSE2



SCC_20M_3690MHz_Q64_FULLRB_CSEpart96





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SCC_20M_3690MHz_QPSK_1RB_CSE1



SCC_20M_3690MHz_QPSK_1RB_CSE3



SCC_20M_3690MHz_QPSK_1RB_CSE0b



SCC_20M_3690MHz_QPSK_1RB_CSE2



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SCC_20M_3690MHz_QPSK_FULLRB_CSE1



SCC_20M_3690MHz_QPSK_FULLRB_CSE3



SCC_20M_3690MHz_QPSK_FULLRB_CSE0b



SCC_20M_3690MHz_QPSK_FULLRB_CSE2



SCC_20M_3690MHz_QPSK_FULLRB_CSEpart9 6



- End of the Appendix -



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