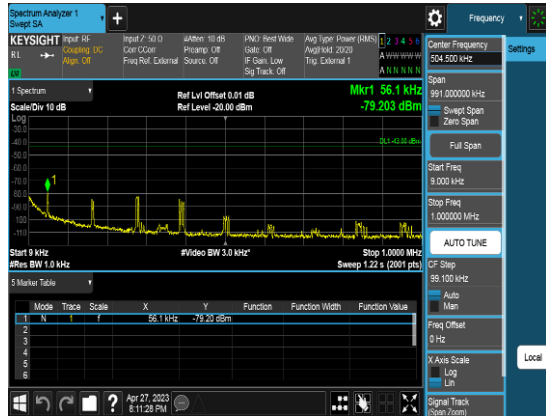


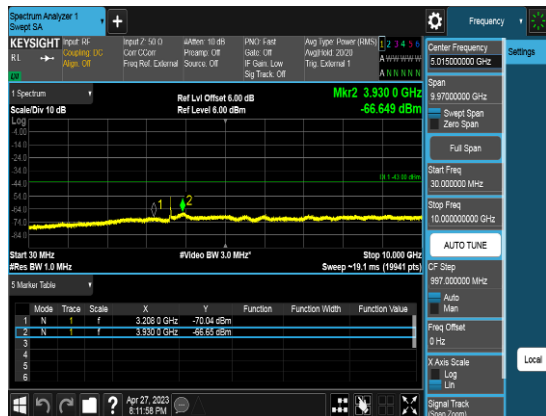
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Port2_20M_3625MHz_TM3.1_CHM_CSE0b



Port2_20M_3625MHz_TM3.1_CHM_CSE1



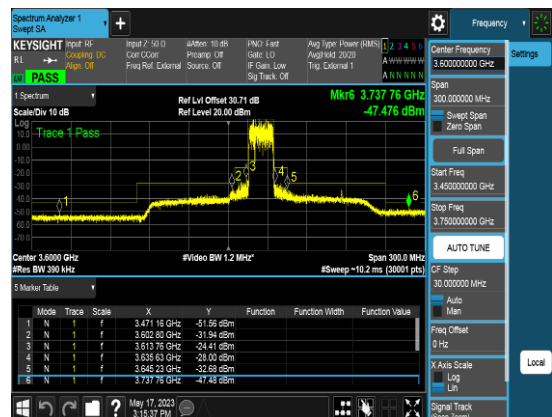
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Port2_20M_3625MHz_TM3.1_CHM_CSE3



Port2_20M_3625MHz_TM3.1_CHM_CSEpart96

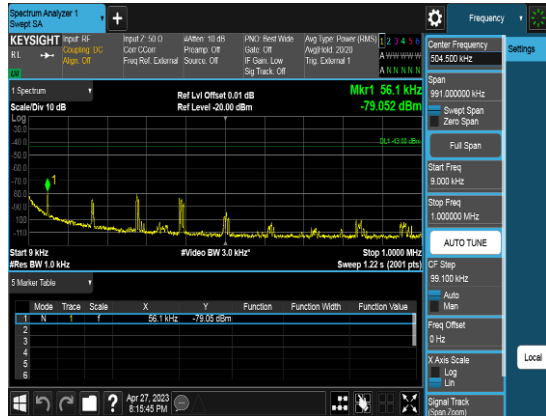


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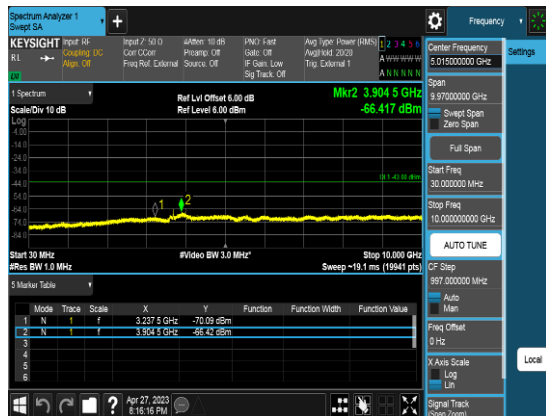
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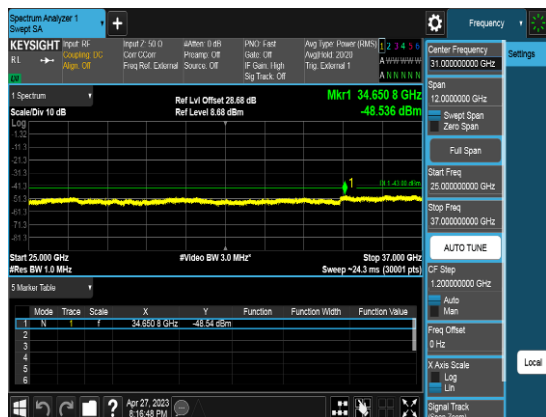
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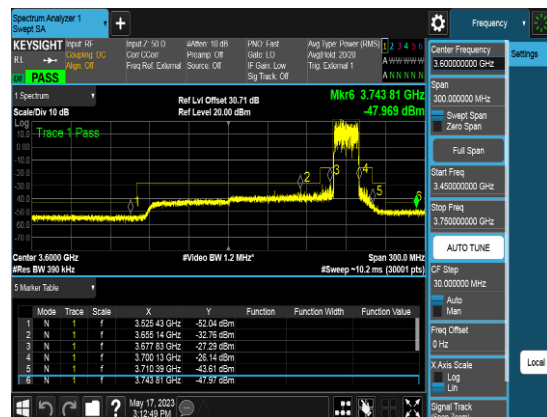
Port2_20M_3690MHz_TM3.1_CHH_CSE2



Port2_20M_3690MHz_TM3.1_CHH_CSE3



Port2_20M_3690MHz_TM3.1_CHH_CSEpart96



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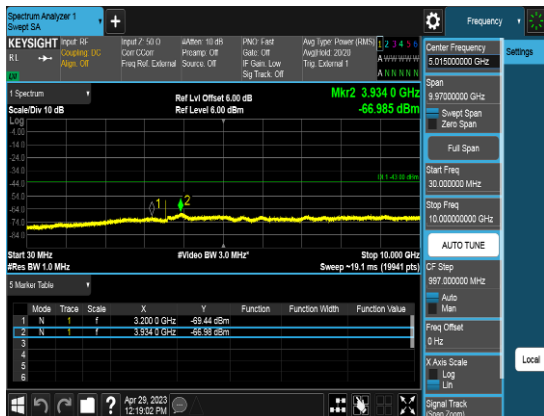
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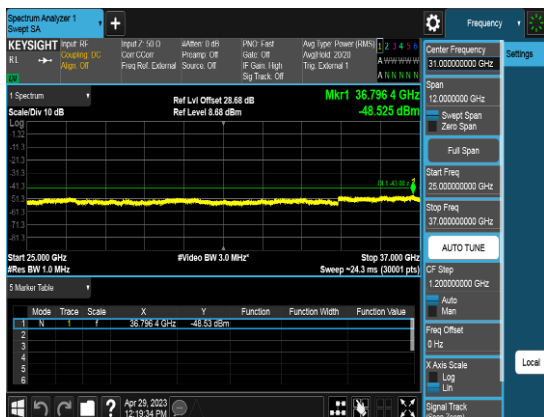
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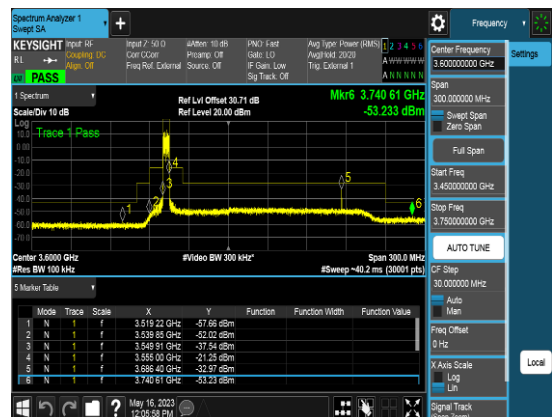
Port2_5M_3552.5MHz_TM3.1_CHL_CSE2



Port2_5M_3552.5MHz_TM3.1_CHL_CSE3



Port2_5M_3552.5MHz_TM3.1_CHL_CSEpart96



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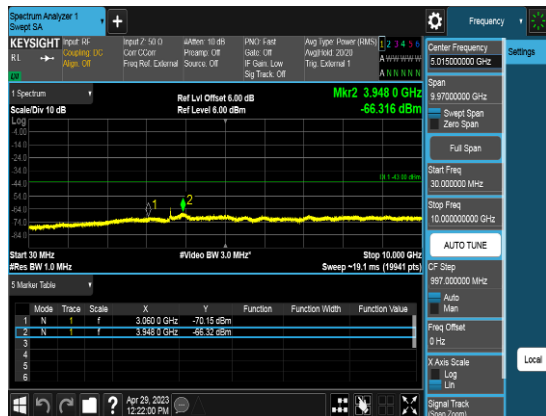
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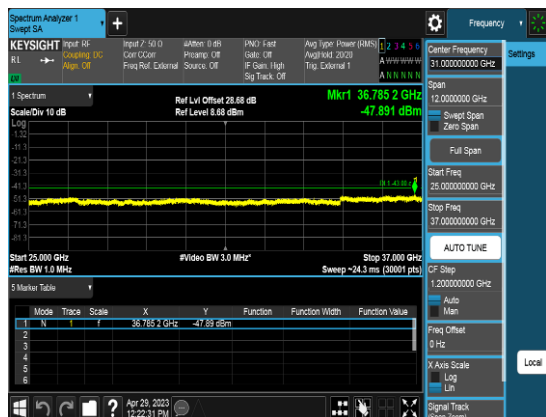
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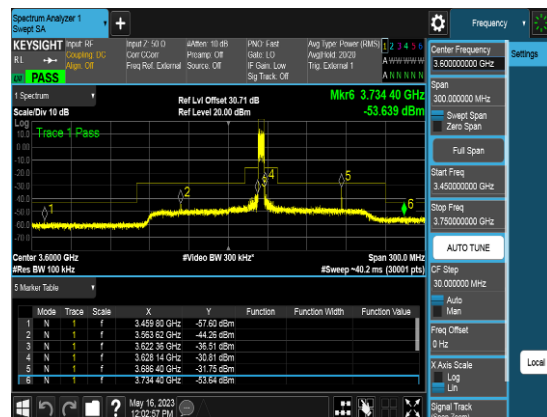
Port2_5M_3625MHz_TM3.1_CHM_CSE2



Port2_5M_3625MHz_TM3.1_CHM_CSE3



Port2_5M_3625MHz_TM3.1_CHM_CSEpart96

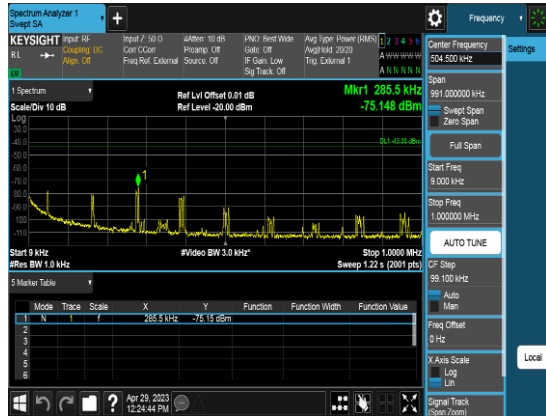


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Port2_5M_3697.5MHz_TM3.1_CHH_CSE0b



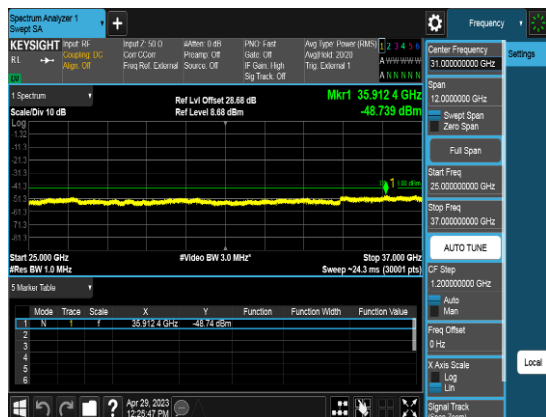
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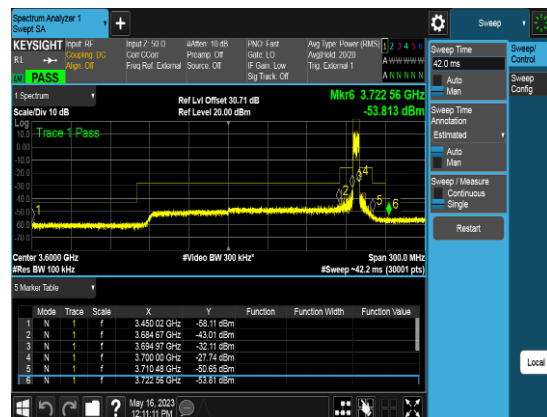
Port2_5M_3697.5MHz_TM3.1_CHH_CSE2



Port2_5M_3697.5MHz_TM3.1_CHH_CSE3



Port2_5M_3697.5MHz_TM3.1_CHH_CSEpart96



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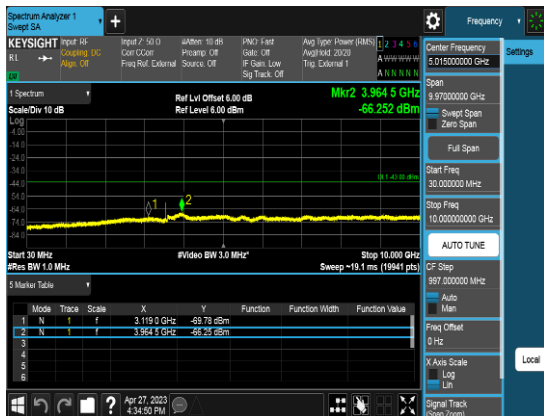
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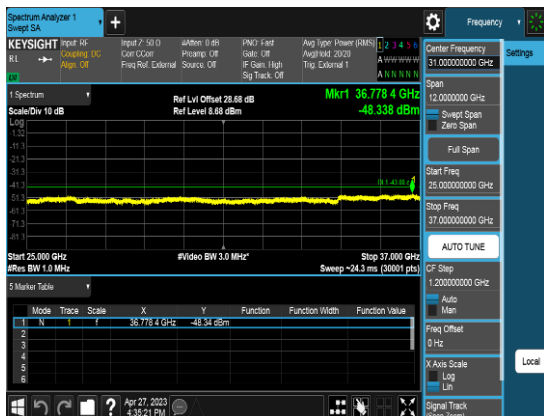
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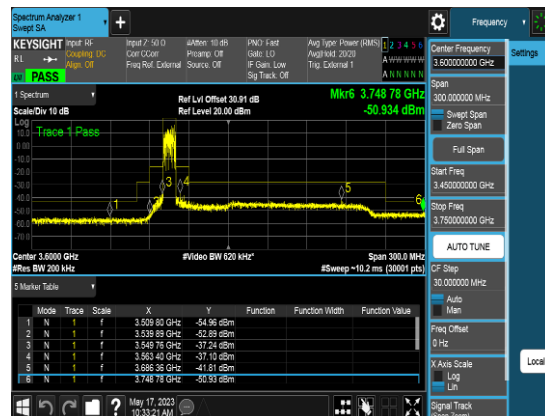
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Port1_10M_3555MHz_TM3.2_CHL_CSE3



Port1_10M_3555MHz_TM3.2_CHL_CSEpart96



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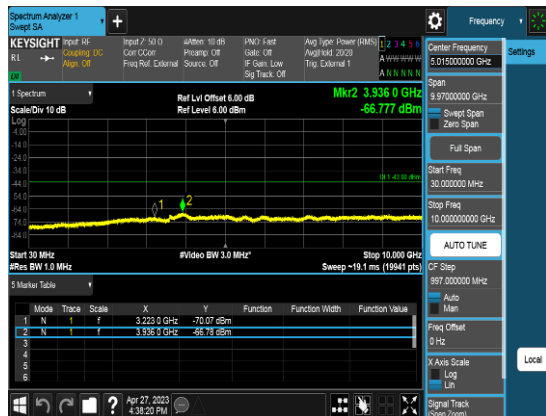
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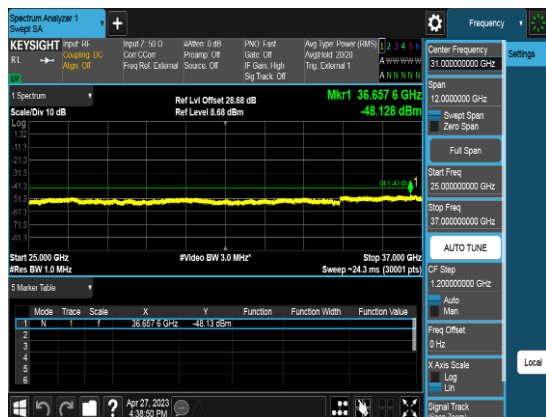
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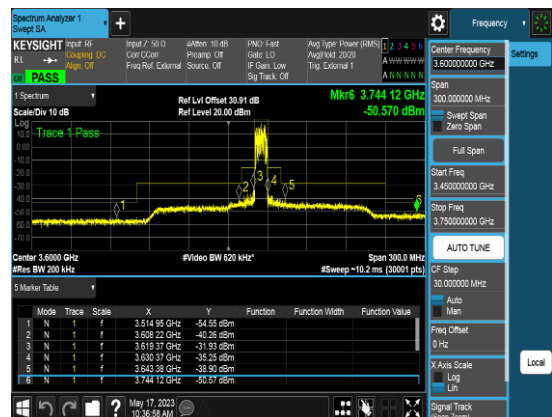
Port1_10M_3625MHz_TM3.2_CHM_CSE2



Port1_10M_3625MHz_TM3.2_CHM_CSE3



Port1_10M_3625MHz_TM3.2_CHM_CSEpart96



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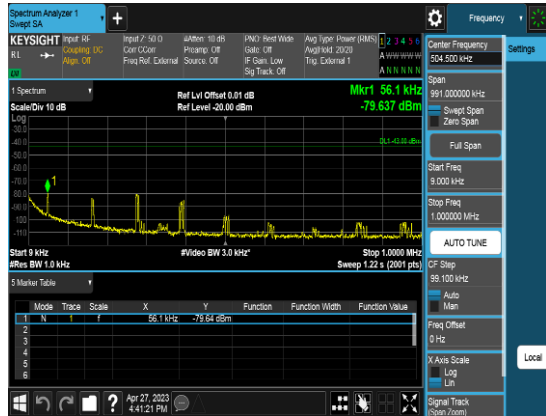
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Port1_10M_3695MHz_TM3.2_CHH_CSE0a



Port1_10M_3695MHz_TM3.2_CHH_CSE0b



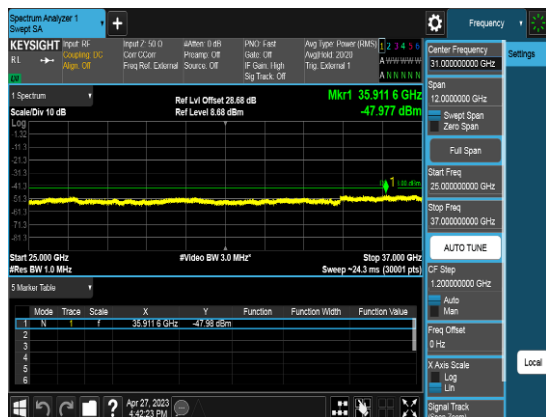
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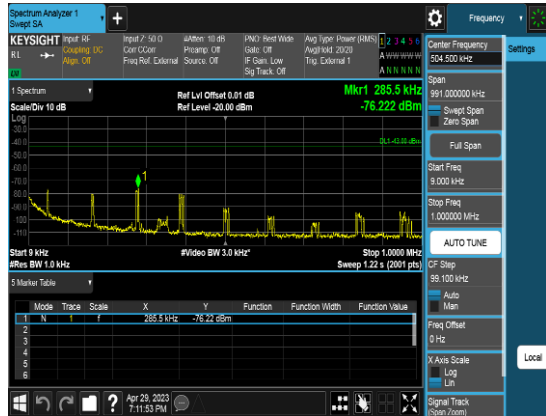
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Port1_15M_3557.5MHz_TM3.2_CHL_CSE0b



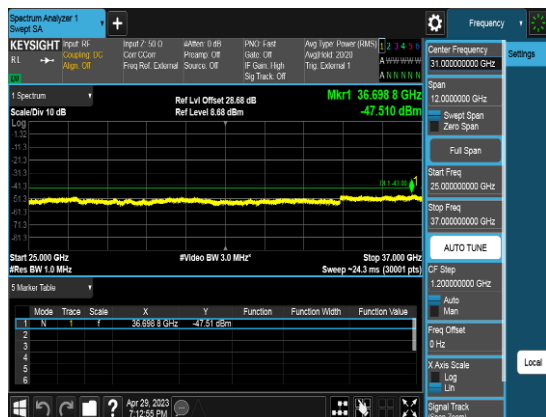
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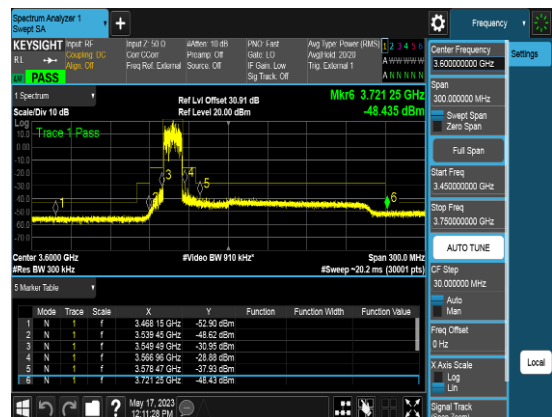
Port1_15M_3557.5MHz_TM3.2_CHL_CSE2



Port1_15M_3557.5MHz_TM3.2_CHL_CSE3



Port1_15M_3557.5MHz_TM3.2_CHL_CSEpart96



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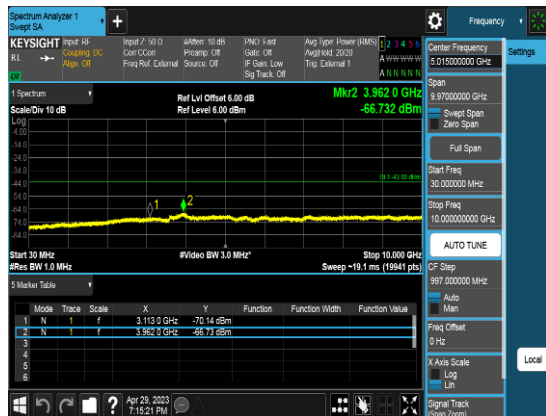
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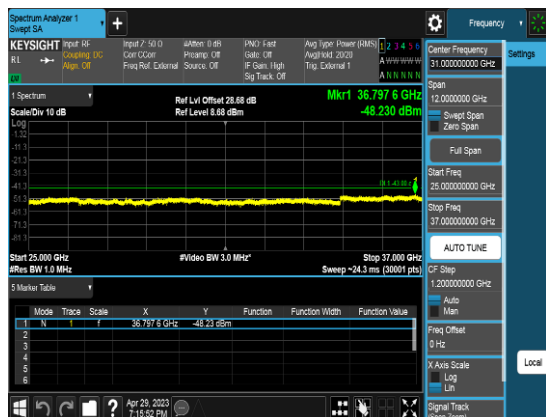
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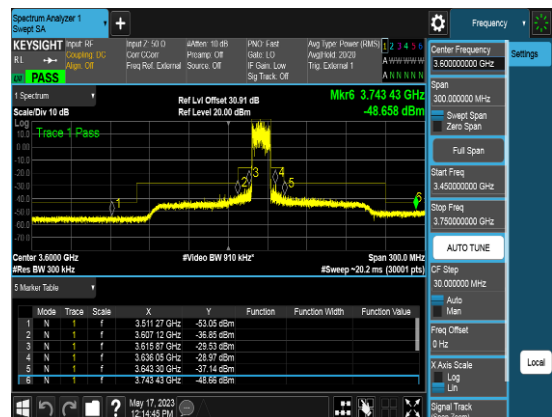
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Port1_15M_3625MHz_TM3.2_CHM_CSE3



Port1_15M_3625MHz_TM3.2_CHM_CSEpart96



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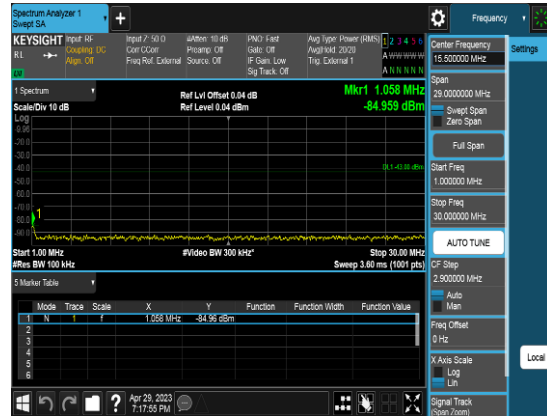
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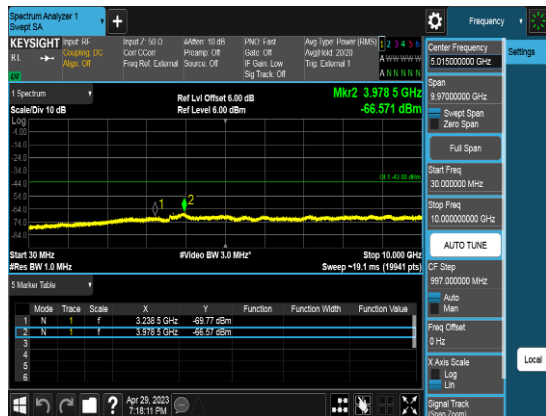
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Port1_15M_3692.5MHz_TM3.2_CHH_CSE0b



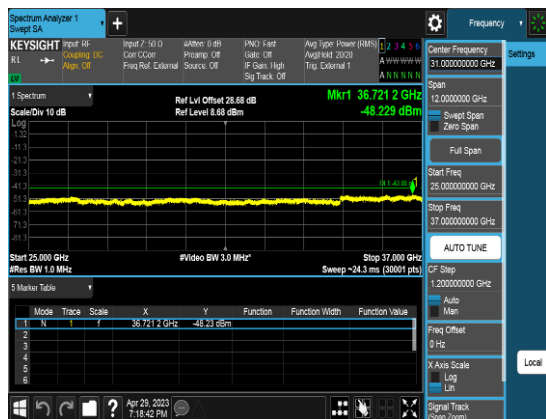
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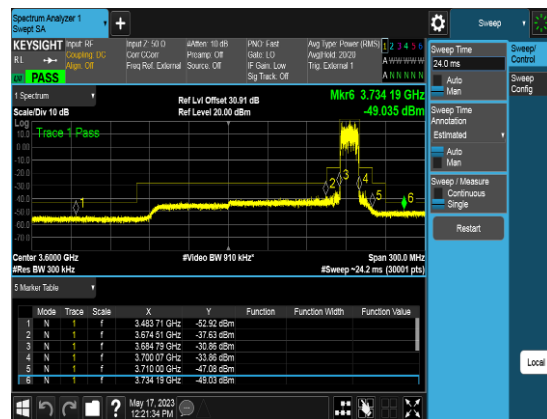
Port1_15M_3692.5MHz_TM3.2_CHH_CSE2



Port1_15M_3692.5MHz_TM3.2_CHH_CSE3



Port1_15M_3692.5MHz_TM3.2_CHH_CSEpart96



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