Operational Description

Bigfoot Unity System

Table of Contents

1. General Description …… 1
2. Principles of Operation …… 1
3. System Architecture …… 2
4. Long-Acting Pen Cap (LCAP) …… 3
5. Rapid-Acting Pen Cap (RCAP) …… 5
6. Appendix A …… 6

1. General Description

- Bigfoot Unity is an interconnected system of hardware and software for use by people with diabetes who use disposable mechanical insulin pens for self-injection.

- It comprises a pair of pen caps as shown in *Fig. 1*, designed to diminish the burden experienced by people with diabetes and their health care teams when implementing therapy regimens consisting of multiple daily injections of insulin (MDI).

2. Principles of Operation

- To generate and display glucose data;

- To capture the timing of inferred insulin doses;

- To generate glucose and system messaging, including a real-time low glucose alert; and

- To display insulin dosing recommendations from health care providers.

Fig.1: Bigfoot Unity Pen Caps; Long-Acting Pen Cap/LCAP (Black) and Rapid-Acting Pen Cap/RCAP (White)

3. System Architecture

- The Bigfoot Unity System architecture consists of networked components and connected devices and services that implement event-driven state machines.

- Events arise from user interactions, data from CGM and/or BGM, and communications which occur over standard wireless interfaces using NFC, BLE, WiFi and cellular data as shown in *Fig. 2*.

- The ecosystem includes additional applications-level features for secure, context-specific message handling between the Inject System and Web Services.

- The datasheets for the BLE and NFC chips are provided.

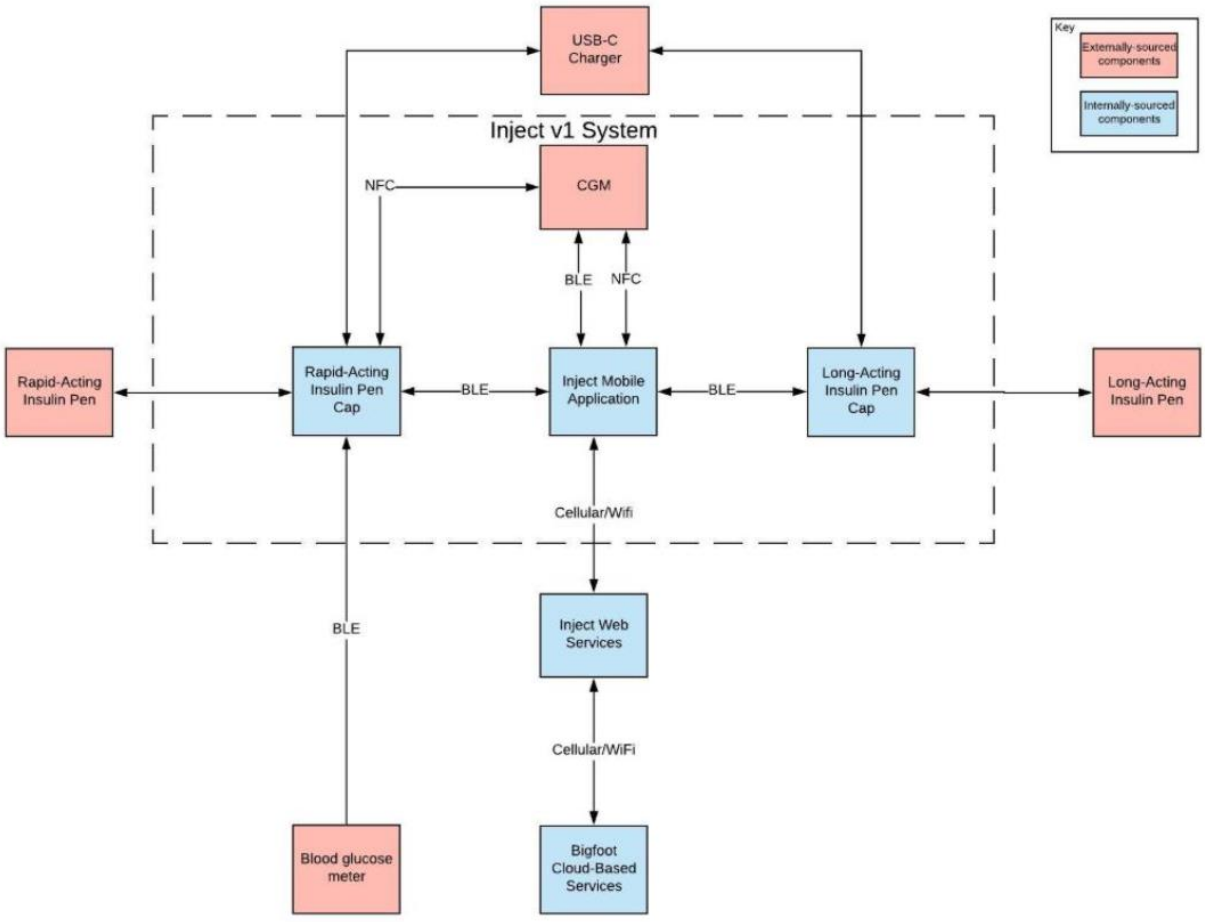

Fig.2: Bigfoot Unity System Interaction

4. Long-Acting Pen Cap (LCAP)

- The LCAP is used for tracking a patient's long-acting insulin doses which are, in most circumstances, taken once every 24 hours.

- The LCAP contains a Nordic nRF52840-QIAA-R Bluetooth Microcontroller, as shown in *Fig. 3*, that is used to communicate with the mobile application via BLE.

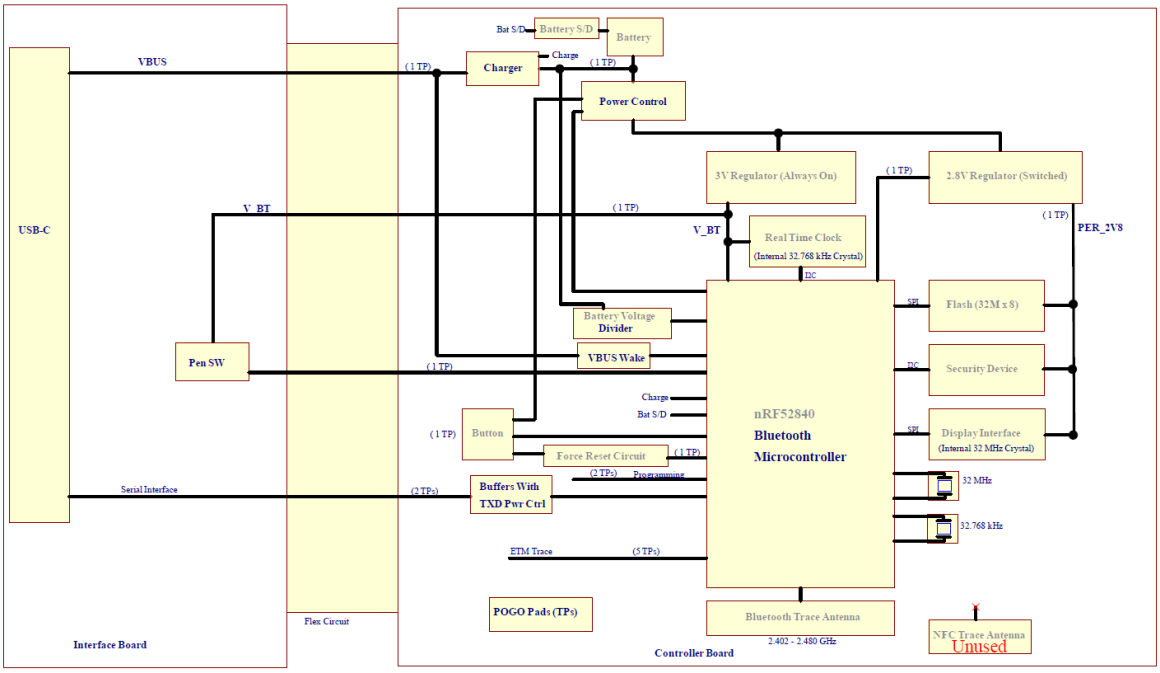

Fig. 3: LCAP Block Diagram

- The Nordic nRF52840 IC supports version 5.0 BLE central role operation and 4.2 BLE peripheral role operation (BLE 5.0 is backward compatible with BLE 4.2).

- It includes an ARM processor, 1 MB non-volatile flash memory, 256 kB RAM memory, BLE radio, functional interfaces, ADC, DC/DC converter, crystal oscillators, and general purpose I/O pins.

- A TVS diode and low pass filter at the processor's reset input mitigates against unintentional resets during ESD events.

- The functional interfaces include programming/debug, asynchronous serial communication, two SPI, two I2C, and one QSPI. The firmware stored in the flash memory determines the functionality of the LCAP.

- The internal crystal oscillators work with 32 MHZ and 32.768 kHz external crystals.
- The DC/DC converter reduces Vbt to the 1.3 V used by the BLE Processor core.

- The BLE Processor has sleep modes that minimize power consumption by internally powering down all functionality except when it is needed to wake up from an event such as RTC interrupt, button press, or power adapter connection.

- The BLE trace antenna is designed utilizing the manufacturer's recommendations and reference circuits. The design provides for tuning of the BLE antenna for best performance by adjusting antenna matching component values to be able to make the antenna impedance 50 Ohms.

- The antenna has a gain of 5.3dBi and maximum power output of 0.56mW.

- Appendix A provides a listing of the BLE Processor I/O Signals.

5. Rapid-Acting Pen Cap (RCAP)

- The RCAP is used for tracking a patient's rapid-acting insulin doses which are taken by the patient after every meal or in any situation that triggers an increase in blood sugar levels.

- The architecture of the LCAP and RCAP is the same apart from the fact that along with a Nordic nRF52840-QIAA-R Bluetooth Microcontroller for communicating with the mobile application via BLE, the RCAP also has an ST25R3911B NFC Chip that allows it to scan a CGM Sensor to read glucose values. See *Fig. 4*.

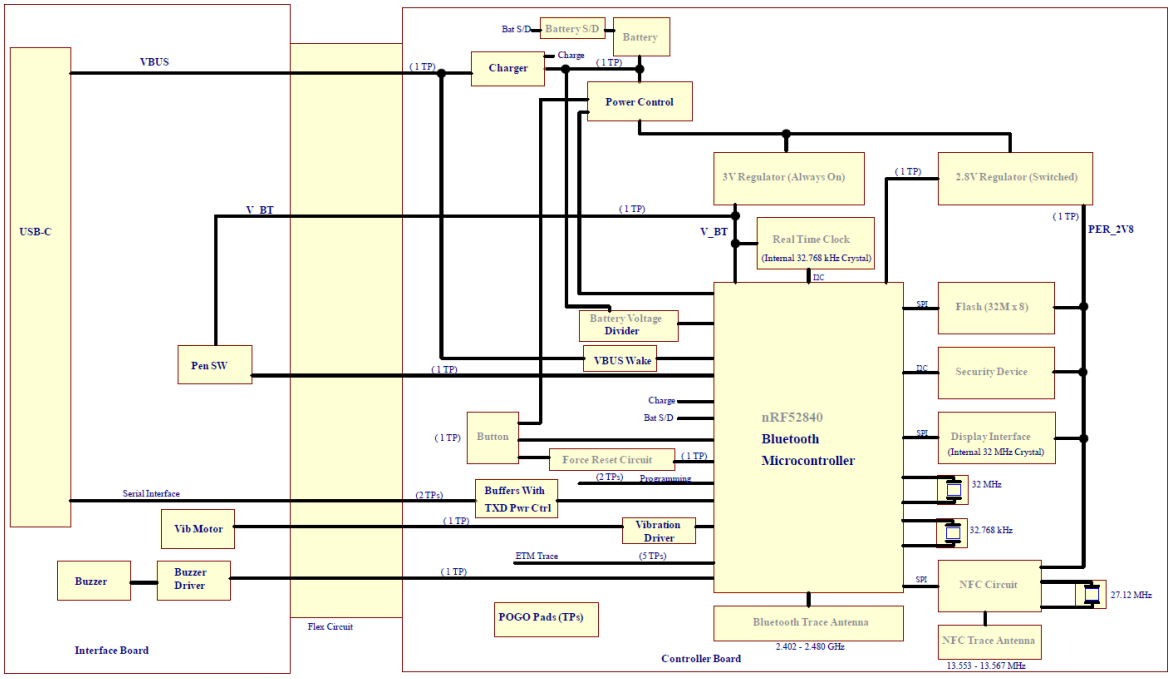

Fig. 4: RCAP Block Diagram

- The NFC antenna is designed and tuned such that the NFC radio's operating frequency is not affected by the presence of typical clothing materials and able to detect the CGM at a distance of 1cm.

- The NFC Reader is controlled by the BLE Processor using a dedicated SPI bus, is powered by peripheral power, and is configured to operate per ISO/IEC 15693.

- The NFC trace antenna is designed utilizing manufacturer's recommendations and reference circuits.

Appendix A

MAIN PROCESSOR NRF52840 I/O SIGNALS

#	Group	Pin Name	Pin #	Function	Net Name	Dir	Type	Description (application)	Sleep State	Pull
1	Annunciation	P0.10 NFC2	J24	Digital I/O NFC input	VIB_CTRL	O	Dig AH	PWM Signal to Vibration Driver	Input or low	Capacitor to Pull-Down
2	Annunciation	P0.09 NFC1	L24	Digital I/O NFC input	BUZZ_CTRL	O	Dig AH	PWM Signal to Buzzer Driver	Input or low	External Pull-Down
3	BLE ANT	ANT	H23	RF	ANT			BLE RF Out		
4	Battery Shutdown	P1.07	P23	Digital I/O	BAT_SD	I	Dig AH	High Signal causes Battery Shutdown	Input or low	
5	Battery Voltage Measure	P0.30 AIN6	B9	Digital I/O Analog input	VBAT/2	I	Anl	Analog is signal that is half of battery voltage		
6	Battery Voltage Measure	P1.04	U24	Digital I/O	VMEAS	O	Dig AH	High Signal connects battery voltage to voltage divider circuit	Input or low	External Pull-Down
7	Button	P1.03	V23	Digital I/O	BUTTON_N	I	Dig AL	Low Signal indicates button is pressed	Input	External Pull-Up to V_BT
8	Charge	P1.02	W24	Digital I/O	CHARGE	I	Dig AL	Low Signal indicates battery is charging	Input	Internal Pull-up when reading
9	Display	P0.27	H2	Digital I/O	SPI1_MOSI	O	Dig AH	SPI Interface with NFC		
10	Display	P0.06	L1	Digital I/O	SPI1_SCK	O	Dig	SPI Interface to Display	Low	
11	Display	P1.06	R24	Digital I/O	SPI1_SEL_N	O	Dig AL	SPI Interface to Display	Input or low	
12	Display	P1.05	T23	Digital I/O	DSPL_BUSY	I	Dig AH	High Signal indicates display is busy	Input	
13	Display	P1.01	Y23	Digital I/O	DSPL_RST_N	O	Dig AL	Low Signal resets display	Input	
14	Display	P0.16	AC11	Digital I/O	SPI1_MISO	I	Dig In	SPI Interface to Display		
15	Flash Memory	P0.19	AC15	Digital I/O	QSPI_SCK	O	Dig AH	Quad SPI Interface with flash memory	Input or low	
16	Flash Memory	P0.21	AC17	Digital I/O	QSPI_DIO1	I/O	Dig AH	Quad SPI Interface with flash memory	Input or low	
17	Flash Memory	P0.23	AC19	Digital I/O	QSPI_DIO3	I/O	Dig AH	Quad SPI Interface with flash memory	Input or low	
18	Flash Memory	P0.17	AD12	Digital I/O	QSPI_CSN	O	Dig AL	Quad SPI Interface with flash memory	Input or low	
19	Flash Memory	P0.20	AD16	Digital I/O	QSPI_DIO0	I/O	Dig AH	Quad SPI Interface with flash memory	Input or low	
20	Flash Memory	P0.22	AD18	Digital I/O	QSPI_DIO2	I/O	Dig AH	Quad SPI Interface with flash memory	Input or low	
21	NFC	P1.13	A16	Digital I/O	NFC_IRQ	I	Dig AL	Interrupt Signal from NFC Chip	Input	External Pull-Up to PER_2V8
22	NFC	P0.14	AC9	Digital I/O	SPI2_SCK	O	Dig AH	SPI Interface to NFC chip	Input or low	
23	NFC	P0.25	AC21	Digital I/O	SPI2_MISO	I	Dig AH	SPI Interface with NFC	Input	
24	NFC	P0.13	AD8	Digital I/O	SPI2_NFC_SEL	O	Dig AL	SPI Interface to NFC chip	Input or low	
25	NFC	P0.24	AD20	Digital I/O	SPI2_MOSI	O	Dig AH	SPI Interface with NFC	Input or low	

#	Group	Pin Name	Pin #	Function	Net Name	Dir	Type	Description (application)	Sleep State	Pull
26	Not Used	P0.31 AIN7	A8	Digital I/O Analog input		NA	ANL or Dig	Not Used	Dig In	
27	Not Used	P0.02 AIN0	A12	Digital I/O Analog input		NA	ANL or Dig	Not used	Dig In	
28	Not Used	P0.03 AIN1	B13	Digital I/O Analog input		NA	ANL or Dig	Not used	Dig In	
29	Not Used	P0.04 AIN2	J1	Digital I/O Analog input		NA	ANL or Dig	Not used	Dig In	
30	Not Used	P0.05 AIN3	K2	Digital I/O Analog input		NA	ANL or Dig	Not used	Dig In	
31	Pen Detect	P0.28 AIN4	B11	Digital I/O Analog input	PENDET	I	Dig AL	Low Signal Indicates when pen is installed	Input	External Pull-Down
32	Peripheral Power	P1.10	A20	Digital I/O	PER_2V8_EN	O	Dig Out	High signal turns ON PER_2V8 LDO	Input or low	External Pull-Down
33	Program/Debug	SWDCLK	AA24	Debug	SWDCK	I	Dig In	Serial Wire Debug (SWD) interface Clock	Float	
34	Program/Debug	SWDIO	AC24	Debug	SWDIO	I/O	Dig I/O	Serial Wire Debug (SWD) interface Data	Float	
35	Power Off	P0.29 AIN5	A10	Digital I/O Analog input	PWR_OFF	O	Dig AH	High Signal turn device power OFF	Input or low	External Pull-Down
36	Reset	P0.18 nRESET	AC13	Digital I/O	BRSTN	I	Dig AL	Processor Reset	Input	Internal Pull-up
37	Battery Charging	P1.15	A14	Digital I/O	WAKE_VBUS	I	Dig AL	Low Indicates VBUS is connected to device for charging	Input	External Pull-Up to V_BT
38	Real Time Clock	P1.14	B15	Digital I/O	I2C1_SDA	I/O	Dig I/O	I2C Interface to RTC Data	Input or low	External Pull-Up to V_BT
39	Real Time Clock	P1.12	B17	Digital I/O	WDI_INT	I	Dig AL	Signal from Real Time Clock	Input	External Pull-Up to V_BT
40	Real Time Clock	P0.26	G1	Digital I/O	I2C1_SCL	O	Dig AL	I2C interface with RTC Clock	Input or low	External Pull-Up to V_BT
41	Security Chip	P0.08	N1	Digital I/O	I2C0_SCL	O	Dig AL	I2C Interface to Security chip Clock	Input or low	External Pull-Up to PER_2V8
42	Security Chip	P1.08	P2	Digital I/O	I2C0_SDA	I/O	Dig I/O	I2C Interface to security chip Data	Input or low	External Pull-Up to PER_2V8
43	Serial Comm	P1.11	B19	Digital I/O	RXD	I	Dig AH	Serial Input to Processor	Input	
44	Serial Comm	P0.15	AD10	Digital I/O	TXD	O	Dig AH	Serial output from Processor	Input or low	
45	Trace	P0.07 TRACECLK	M2	Digital I/O Trace clock	TRACECLK	O	Dig	ETM Trace Clk	Float	
46	Trace	P1.09 TRACEDATA3	R1	Digital I/O Trace data	TRACE3	O	Dig AH	ETM Trace Output MSB	Input	
47	Trace	P0.11 TRACEDATA2	T2	Digital I/O Trace data	TRACE2	O	Dig AH	ETM Trace Output 2nd MSB	Input	

#	Group	Pin Name	Pin #	Function	Net Name	Dir	Type	Description (application)	Sleep State	Pull
48	Trace	P0.12 TRACE DATA1	U1	Digital I/O Trace data	TRACE1	O	Dig AH	ETM Trace Output 3rd MSB	Input	
49	Trace	P1.00 TRACE DATA0	AD22	Digital I/O Trace data	TRACE0	O	Dig AH	ETM Trace Output LSB	Input	
50	HF Crystal	XC2	A23	Analog input	XC2		Crystal	32 MHz crystal		
51	HF Crystal	XC1	B24	Analog input	XC1		Crystal	32 MHz crystal		
52	LF Crystal	P0.00 XL1	D2	Digital I/O Analog input	XL1		Crystal	32.768 kHz crystal		
53	LF Crystal	P0.01 XL2	F2	Digital I/O Analog input	XL2		Crystal	32.768 kHz crystal		