9. HOPPING CHANNEL SEPARATION

Test Requirement:	FCC Part15 C Section 15.247 (a)(1)
Test Method:	ANSI C63.10:2013
Receiver setup:	RBW=100KHz, VBW=300KHz, detector=Peak
Limit:	GFSK: 20dB bandwidth π/4-DQPSK & 8DSK: 0.025MHz or 2/3 of the 20dB bandwidth (whichever is greater)

9.1 Test Setup

9.2 Test procedure

1. Remove the antenna from the EUT and then connect a low RF cable from the antenna port to the spectrum.

2. Set the spectrum analyzer: RBW = 100kHz. VBW = 300kHz , Span = 3.0MHz. Sweep = auto; Detector Function = Peak. Trace = Max hold.

3. Allow the trace to stabilize. Use the marker-delta function to determine the separation between the peaks of the adjacent channels. The limit is specified in one of the subparagraphs of this Section Submit this plot.

9.3 DEVIATION FROM STANDARD

No deviation.

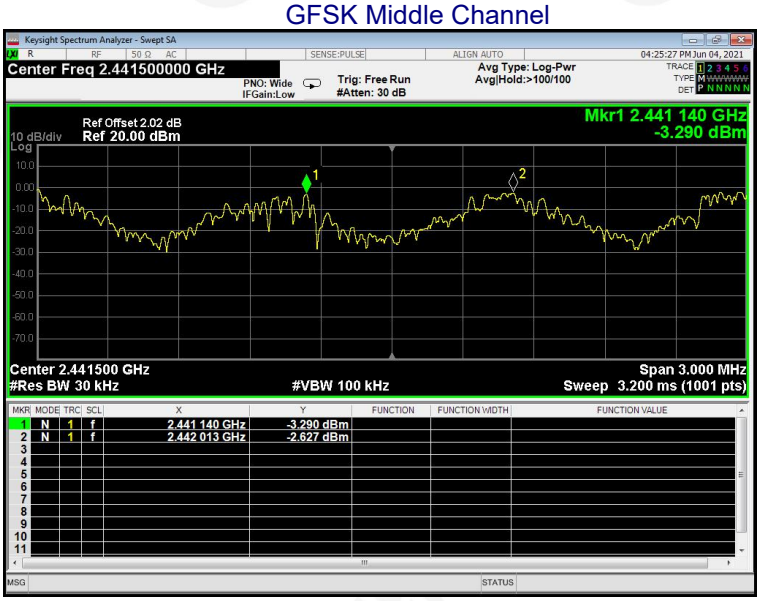
9.4 Test Result

Modulation	Test Channel	Separation (MHz)	Limit(MHz)	Result
GFSK	Low	1.005	0.594	PASS
GFSK	Middle	0.873	0.595	PASS
GFSK	High	1.089	0.637	PASS
π/4-DQPSK	Low	1.017	0.951	PASS
π/4-DQPSK	Middle	1.017	0.961	PASS
π/4-DQPSK	High	1.017	0.946	PASS
8-DPSK	Low	1.008	0.961	PASS
8-DPSK	Middle	0.993	0.979	PASS
8-DPSK	High	0.987	0.946	PASS

Test plots

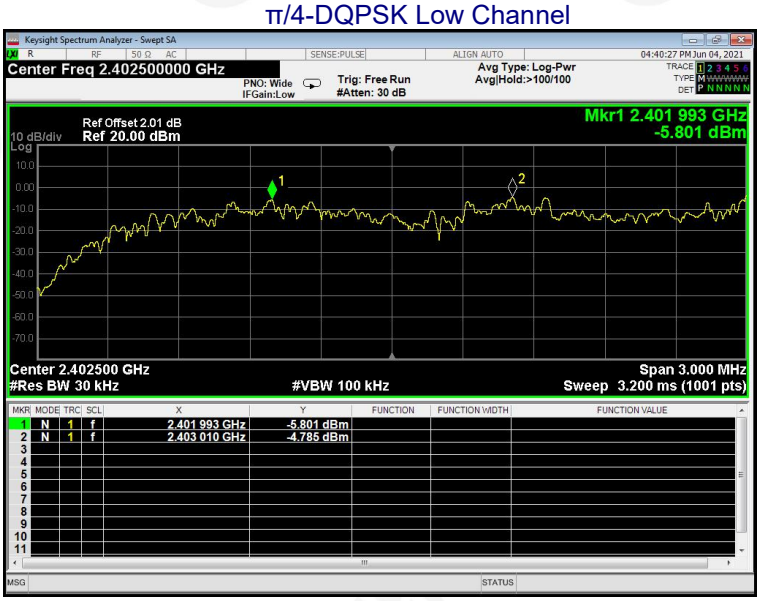
GFSK Low Channel

GFSK Middle Channel

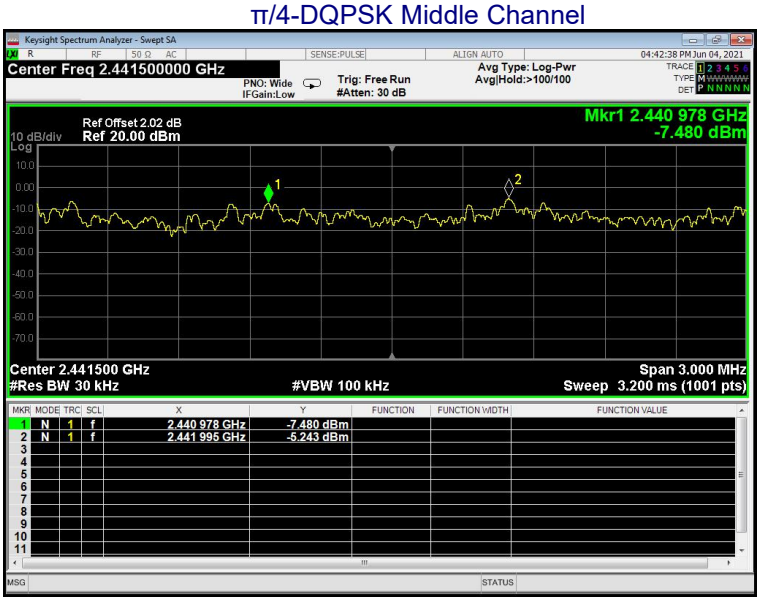


GFSK High Channel

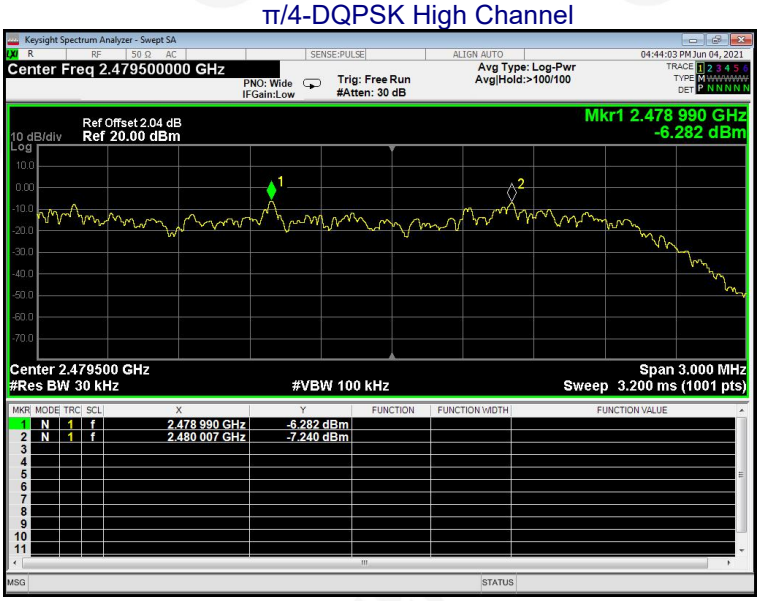
π/4-DQPSK Low Channel



π/4-DQPSK Middle Channel

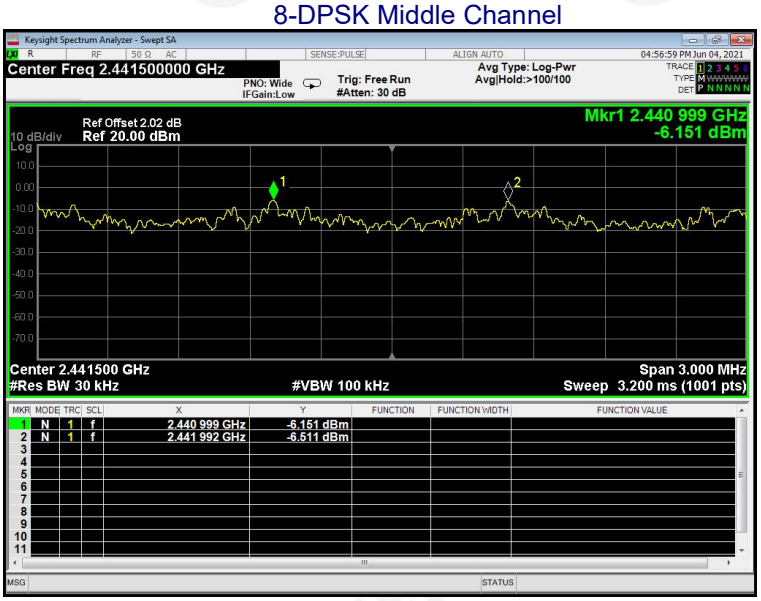


π/4-DQPSK High Channel

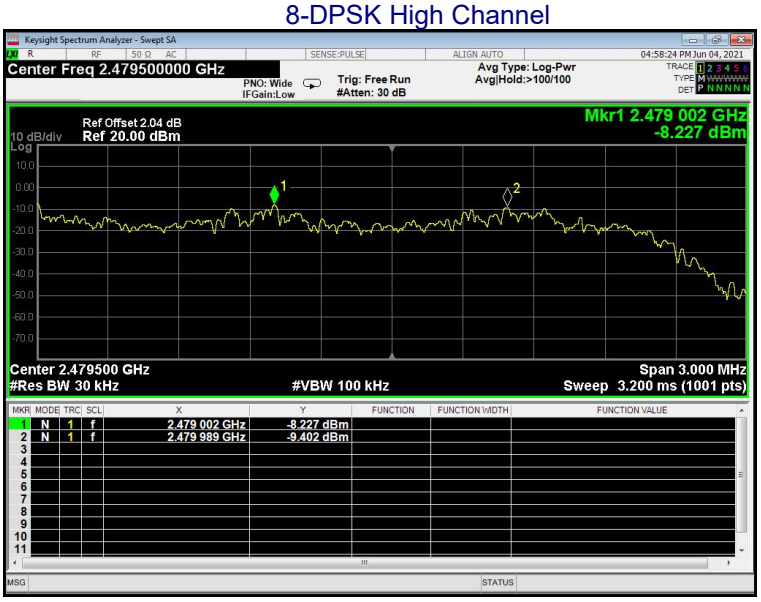


8-DPSK Low Channel

8-DPSK Middle Channel



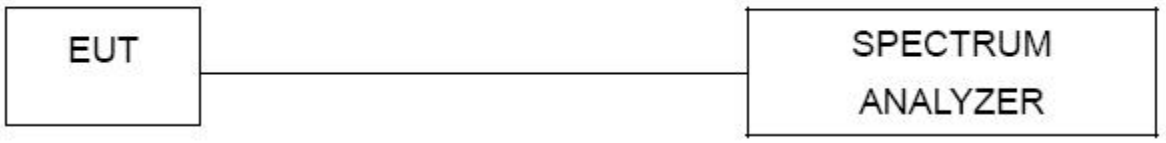
8-DPSK High Channel



10.NUMBER OF HOPPING FREQUENCY

Test Requirement:	FCC Part15 C Section 15.247 (a)(1)(iii)
Test Method:	ANSI C63.10:2013
Receiver setup:	RBW=100kHz, VBW=300kHz, Frequency range=2400MHz-2483.5MHz, Detector=Peak
Limit:	15 channels

10.1 Test Setup



10.2 Test procedure

1. Remove the antenna from the EUT and then connect a low RF cable from the antenna port to the spectrum.

2. Set the spectrum analyzer: RBW = 100kHz. VBW = 300kHz. Sweep = auto; Detector Function = Peak. Trace = Max hold.

3. Allow the trace to stabilize. It may prove necessary to break the span up to sections. in order to clearly show all of the hopping frequencies. The limit is specified in one of the subparagraphs of this Section.

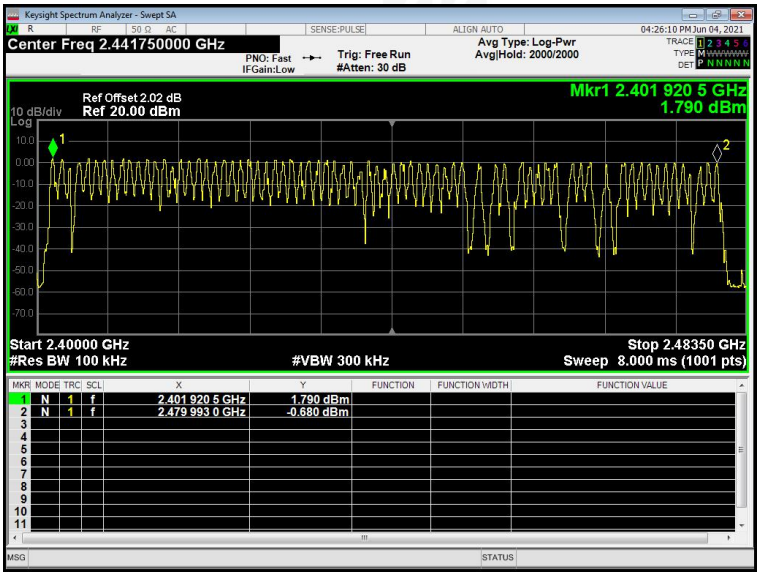
4. Set the spectrum analyzer: Start Frequency = 2.4GHz, Stop Frequency = 2.4835GHz. Sweep=auto;

10.3 DEVIATION FROM STANDARD

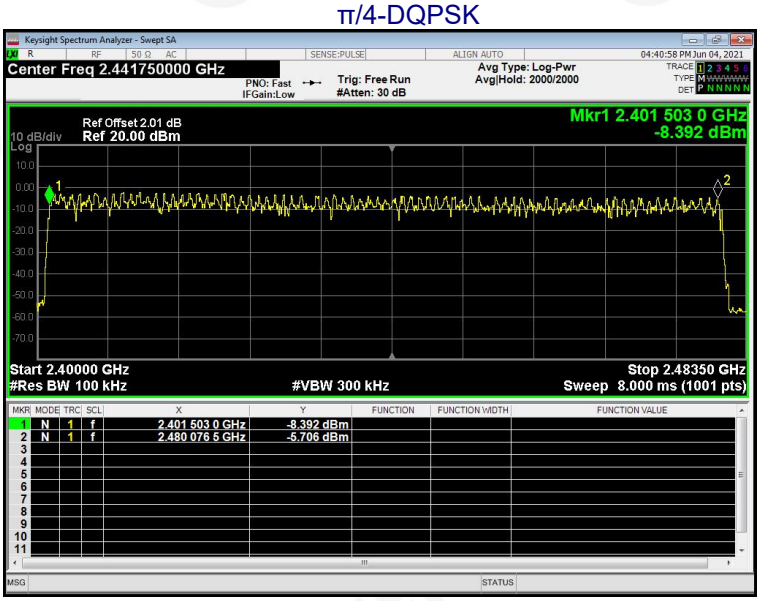
No deviation.

10.4 Test Result

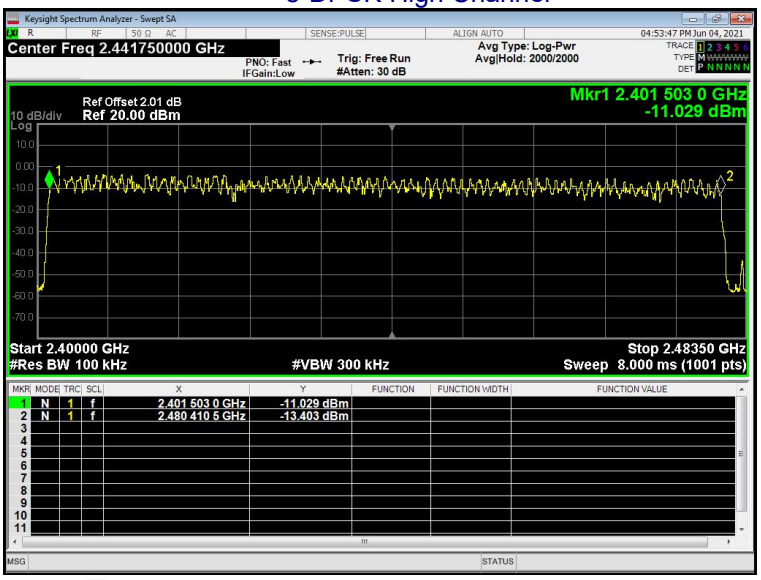
Test Plots:
79 Channels in total
GFSK



π/4-DQPSK



8-DPSK High Channel



11. DWELL TIME

Test Requirement:	FCC Part15 C Section 15.247 (a)(1)(iii)
Test Method:	ANSI C63.10:2013
Receiver setup:	RBW=1MHz, VBW=3MHz, Span=0Hz, Detector=Peak
Limit:	0.4 Second

11.1 Test Setup

11.2 Test procedure

1. Remove the antenna from the EUT and then connect a low RF cable from the antenna port to the spectrum.

2. Set spectrum analyzer span = 0Hz;

3. Set RBW = 1MHz and VBW = 3MHz.Sweep = as necessary to capture the entire dwell time per hopping channel. Set the EUT for DH5, DH3 and DH1 packet transmitting.

4. Use the marker-delta function to determine the dwell time. If this value varies with different modes of operation (e.g.. data rate. modulation format. etc.). repeat this test for each variation. The limit is specified in one of the subparagraphs of this Section. Submit this plot(s).

11.3 DEVIATION FROM STANDARD

No deviation.

11.4 Test Result

GFSK mode:

Frequency	Packet	Dwell time(ms)	Limit(ms)	Result
2441MHz	DH1	121.28	400	Pass
2441MHz	DH3	261.76	400	Pass
2441MHz	DH5	307.63	400	Pass

Remarks:

The test period: T= 0.4 Second/Channel x 79 Channel = 31.6 s
Test channel: 2441MHz as blow
DH1 time slot=0.379(ms)*(1600/ (2*79))*31.6=121.28ms
DH3 time slot=1.636(ms)*(1600/ (4*79))*31.6=261.76ms
DH5 time slot=2.884(ms)*(1600/ (6*79))*31.6=307.63ms

π/4-DQPSK mode:

Frequency	Packet	Dwell time(ms)	Limit(ms)	Result
2441MHz	2DH1	124.48	400	Pass
2441MHz	2DH3	262.56	400	Pass
2441MHz	2DH5	308.16	400	Pass

Remarks:

The test period: T= 0.4 Second/Channel x 79 Channel = 31.6 s
Test channel: 2441MHz as blow
DH1 time slot=0.389(ms)*(1600/ (2*79))*31.6=124.48ms
DH3 time slot=1.641(ms)*(1600/ (4*79))*31.6=262.56ms
DH5 time slot=2.889(ms)*(1600/ (6*79))*31.6=308.16ms

8-DPSK mode:

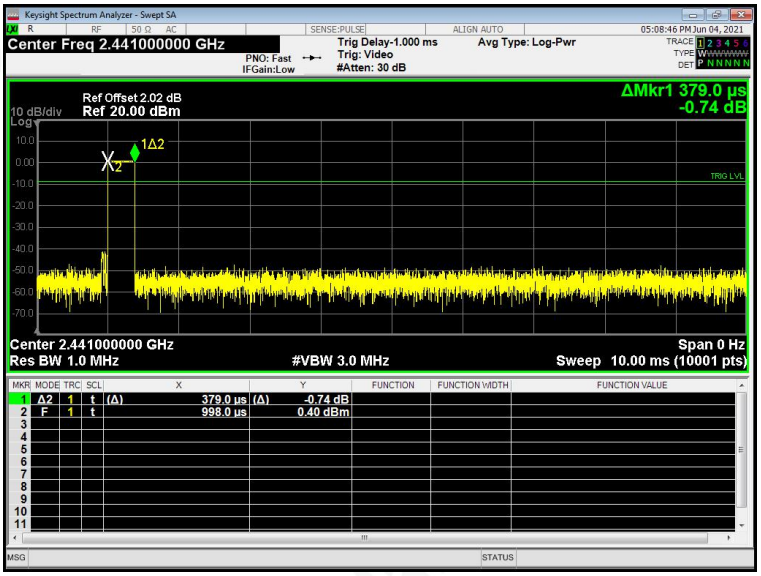
Frequency	Packet	Dwell time(ms)	Limit(ms)	Result
2441MHz	3DH1	124.48	400	Pass
2441MHz	3DH3	262.40	400	Pass
2441MHz	3DH5	308.37	400	Pass

Remarks:

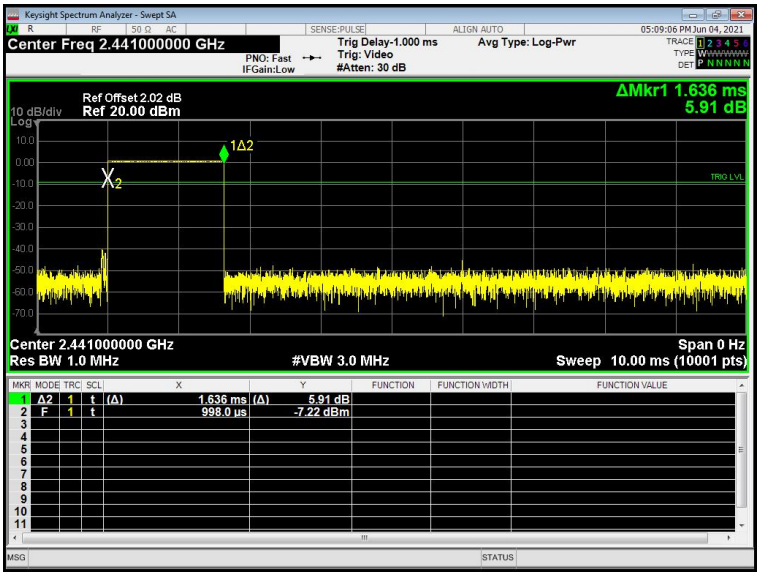
The test period: T= 0.4 Second/Channel x 79 Channel = 31.6 s
Test channel: 2441MHz as blow
DH1 time slot=0.389(ms)*(1600/ (2*79))*31.6=124.48ms
DH3 time slot=1.640(ms)*(1600/ (4*79))*31.6=262.40ms
DH5 time slot=2.891(ms)*(1600/ (6*79))*31.6=308.37ms

Test Plots

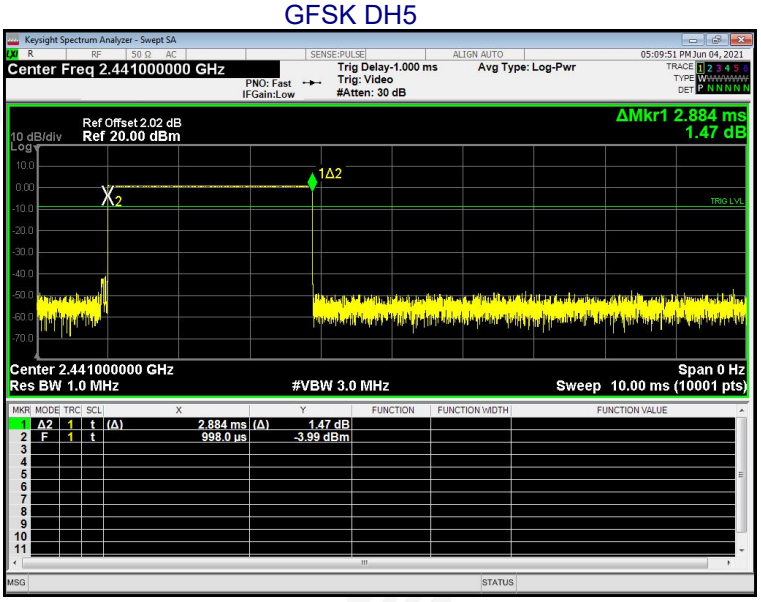
GFSK DH1



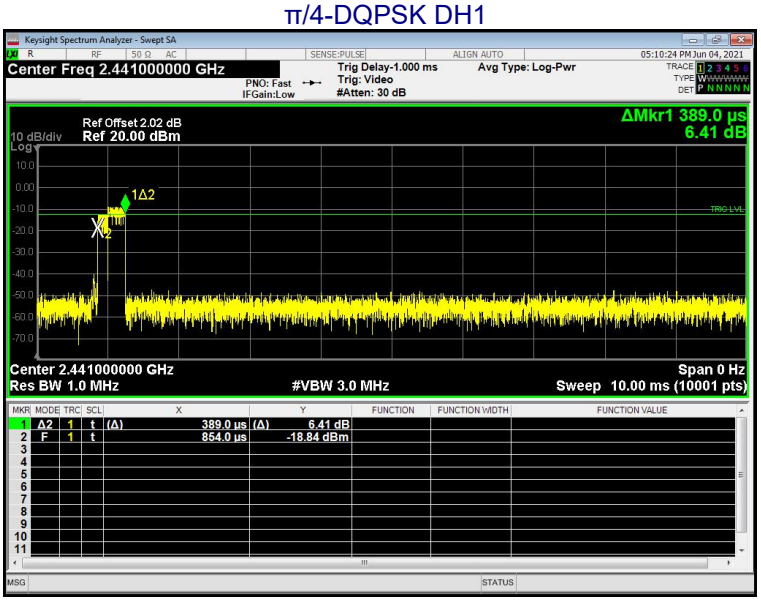
GFSK DH3



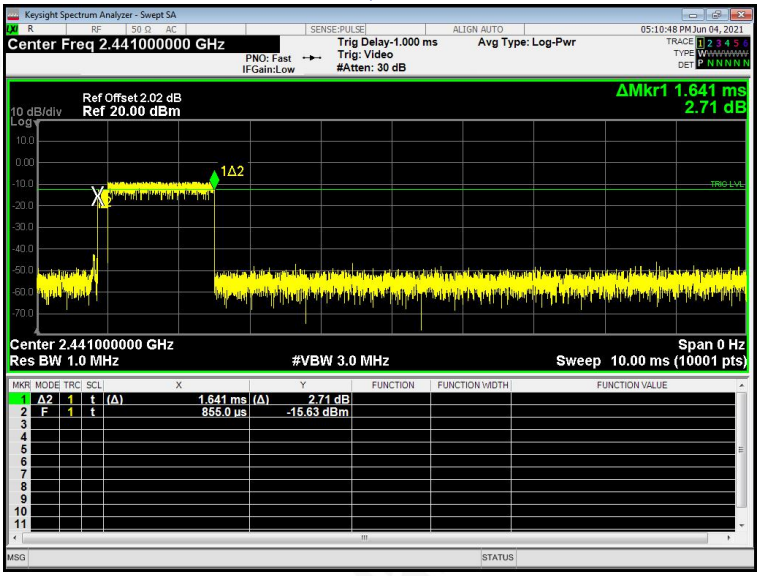
GFSK DH5



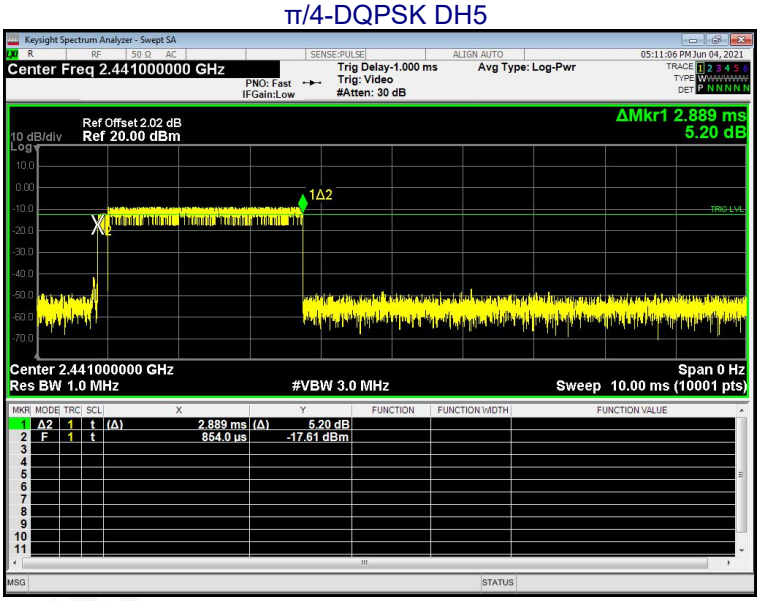
π/4-DQPSK DH1



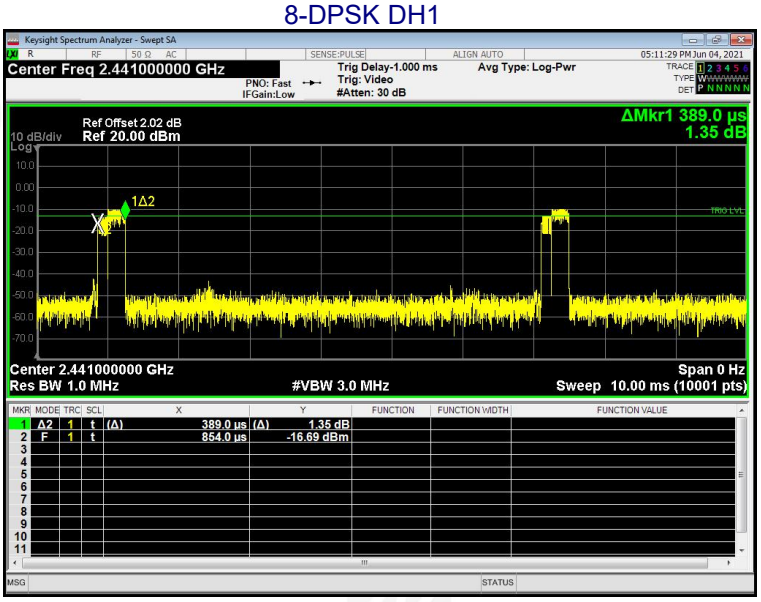
π/4-DQPSK DH3



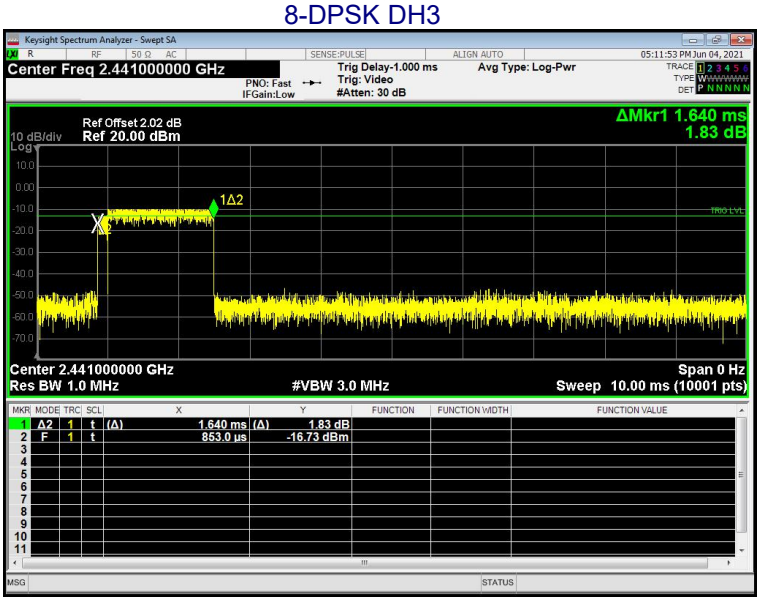
π/4-DQPSK DH5



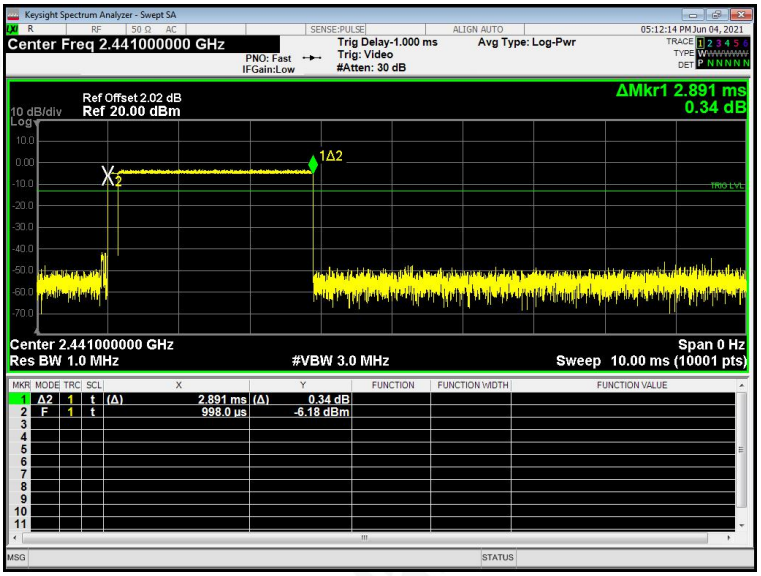
8-DPSK DH1



8-DPSK DH3



8-DPSK DH5


Keysight Spectrum Analyzer - Swept SA
Center Freq 2.441000000 GHz
PNO: Fast
IFGain:Low
Trig Delay-1.000 ms
Trig: Video
#Atten: 30 dB
Avg Type: Log-Pwr
05:12:14 PM Jun 04, 2021
Ref Offset 2.02 dB
10 dB/div
Ref 20.00 dBm
ΔMkr1 2.891 ms
0.34 dB
1Δ2
Center 2.441000000 GHz
Res BW 1.0 MHz
#VBW 3.0 MHz
Span 0 Hz
Sweep 10.00 ms (10001 pts)
1 Δ2 1 t (Δ) 2.891 ms (Δ) 0.34 dB
2 F 1 t 998.0 µs -6.18 dBm

12. Antenna Requirement

Standard requirement:	FCC Part15 C Section 15.203 /247(c)
15.203 requirement: An intentional radiator shall be designed to ensure that no antenna other than that furnished by the responsible party shall be used with the device. The use of a permanently attached antenna or of an antenna that uses a unique coupling to the intentional radiator, the manufacturer may design the unit so that a broken antenna can be replaced by the user, but the use of a standard antenna jack or electrical connector is prohibited. 15.247(c) (1)(i) requirement: (i) Systems operating in the 2400-2483.5 MHz band that is used exclusively for fixed. Point-to-point operations may employ transmitting antennas with directional gain greater than 6dBi provided the maximum conducted output power of the intentional radiator is reduced by 1 dB for every 3 dB that the directional gain of the antenna exceeds 6dBi.	
EUT Antenna:	
The antenna is PCB antenna, the best case gain of the antennas is 0dBi, reference to the appendix II for details	

13. Test Setup Photo

Reference to the appendix I for details.

14. EUT Constructional Details

Reference to the appendix II for details.

※※※※※ END OF REPORT ※※※※※