RYZ024A

LTE Category M1 Module

Description

The Renesas RYZ024A is an LTE Cat M1/NB1/NB2 module based on Renesas' second generation Sequans chip platform. RYZ024A is a total module solution, including a complete, Single-SKU™ RF front end capable of operating on every GSM band worldwide, and an integrated EAL5+ Secure Element (SE) capable of hosting the SIM inside the module with zero compromise on security while lowering cost and reducing complexity.

The LTE frequency bands supported by RYZ024A are B1 (2100), B2 (1900 PCS), B3 (1800+), B4 (AWS-1), B5 (850), B8 (900 GSM), B12 (700 a), B13 (700 c), B14 (700 PS), B17 (700 b), B18 (800 Lower), B19 (800 Upper), B20 (800 DD), B25 (1900+), B26 (850+), B28 (700 APT), B66 (AWS-3), B71 (600), B85 (700 a+).

Applications

RYZ024A is ideal for adding LTE-M and/or NB-IoT LTE connectivity to narrowband, low data rate M2M and IoT devices such as utility meters, industrial sensors, health and fitness appliances, asset trackers, and many additional devices in smart home, smart city, and wearable applications.

RYZ024A can be used by applications as slim modem controlled by an external MCU via UART.

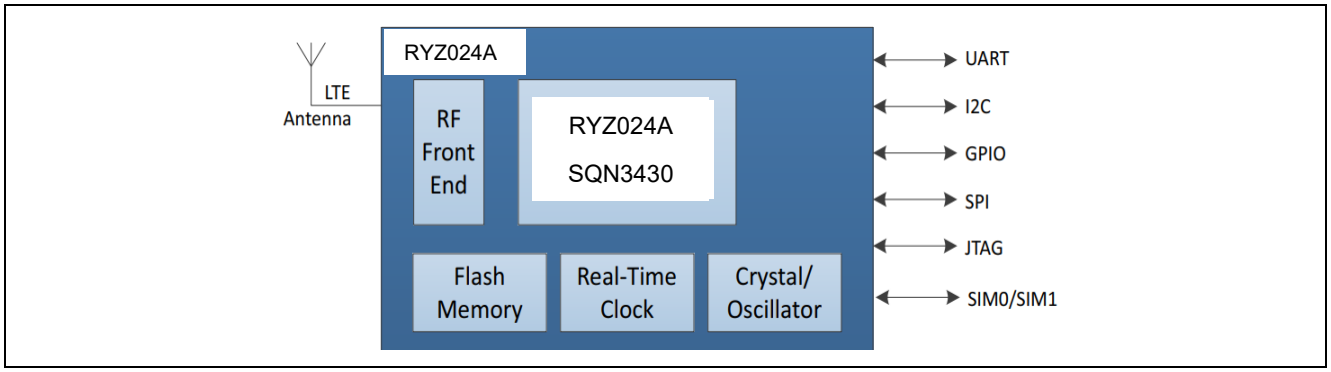


Figure 1. RYZ024A Block Diagram

Table 1. General Features

Feature	Functional description
Physical Characteristics	LGA module, 120 pads Size: 16.3 mm x 17 mm x 1.85 mm
Temperature Range	Operation temperature range: -40°C to +85 °C Storage: MSL3
Power Supply	Voltage range for RF compliance: 2.5 V to 5.5 V. Functional voltage range: 2.2 V to 5.5 V
Tx Power	+23 dBm for each band
Interfaces	Dual (U) SIM Card Interface: support for external, removable or fixed UICC. Support for integrated UICC (iUICC) with a dedicated p/n; 4x High-Speed UART Interfaces with flow control, up to 921600 bauds; GPIOs, I2C, SPI, PWM, Pulse Counter, I2S/PCM, ADC;
SMS	Text and PDU modes
Firmware Upgrade	UART interface, FOTA, support of full and differential firmware upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive, bromine-free

Feature	Functional description
LTE Features	3GPP LTE Release 13/14 Cat M1/NB1/NB2 compliant; LTE Cat M1: 1.1 Mbps / 0.3 Mbps UL/DL throughput; LTE Cat NB1: 62.5 kbps / 27.2 kbps UL/DL throughput; LTE Cat NB2: 160 kbps / 120.7 kbps UL/DL throughput. Note: Cat NB1/NB2 will be supported in future module versions via software upgrade.

Orderable Part Numbers

Orderable Part Number	Hardware Version	Software Build (ATI1)	UE Version (ATI1)	PTCRB Model Name/Model	SVN	Orderable Status
RYZ024000FZ00#HD0	HW Rev.2 FCC/IC/ RED/ UKCA/ ACMA/ JATE/ TELEC/ PTCRB/ GCF	LR 8.0.5.10	UE 8.0.5.10	See note following the table	See note following the table	See note following the table

Note: Please contact your Renesas technical representative to select the applicable part number for your project.

Pin Assignment

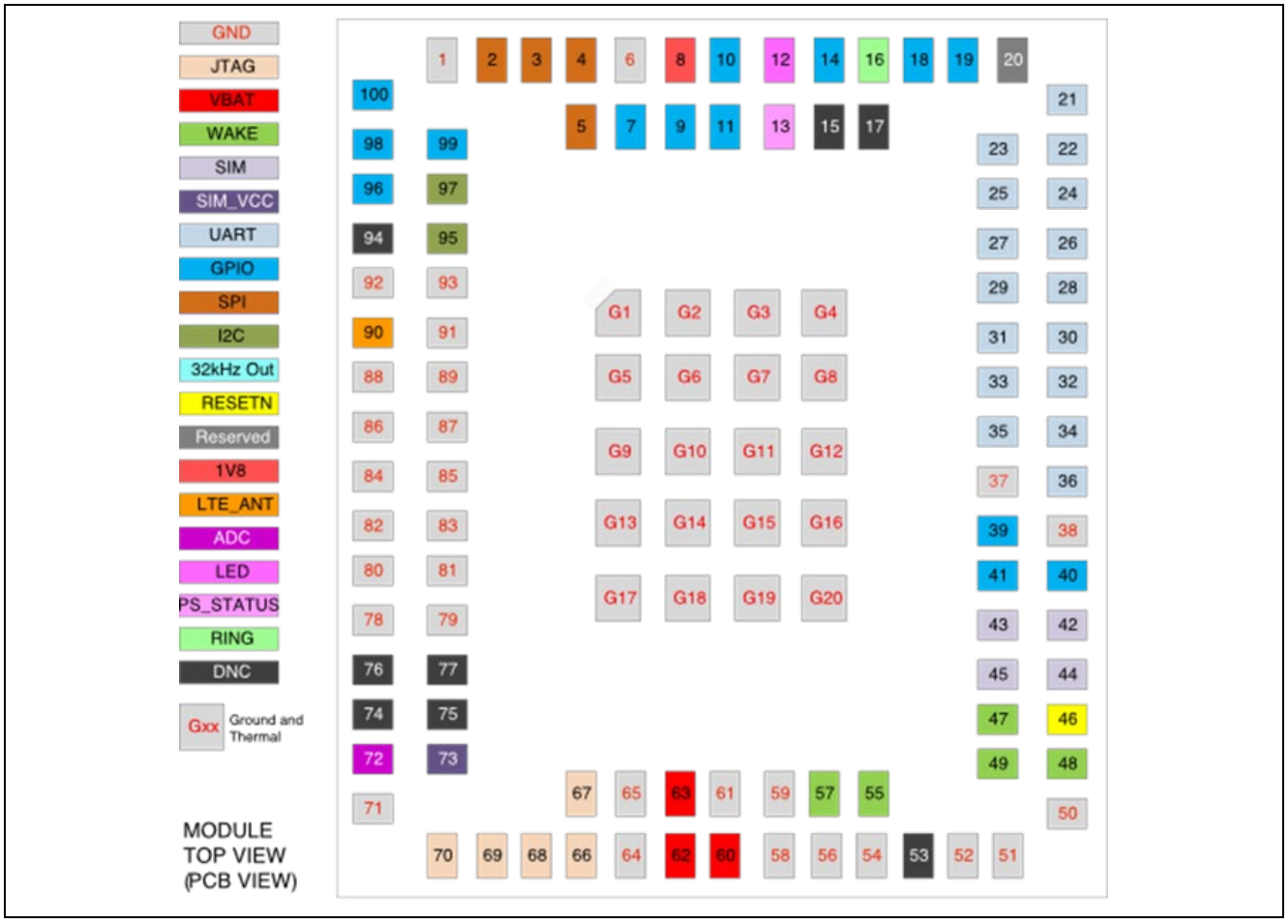


Figure 2. Module Pin Assignments

Interfaces

RYZ024A provides interfaces that connect to the external application. These interfaces include communication I/O ports, GPIO and antenna interface. This chapter provides description of all these interfaces. Power pads and details on power groups are provided in section Electrical Characteristics.

Important Notes: Please refer to this datasheet's Appendix for details on each pin's:

- Default assigned function
- State during low power modes
- Ability to be configured via AT commands
- Pull status and requirements

UART

RYZ024A, when used as a slim modem, has three UARTs available. While the function of the UARTs can be configured, the default function for each UART is as follows:

- UART0: data and control from external MCU via AT commands
- UART1: debug and upgrade
- UART2: modem console

This default configuration can be overridden. In addition, a fourth UART (UART3) is available for applications running on RYZ024A.

Note: See section Power for behavior of IOs in Deep Sleep mode.

Table 2. UART Signals

Pad #	Pad Name	Primary Function	Alternate Function[1]	Power Group	Direction	Pad Type[2]	State at reset
36	GPIO12/TXD0	TXD0	GPIO12	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		In for primary function, UART0					
34	GPIO13/RXD0	RXD0	GPIO13	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART0					
35	GPIO14/CTS0	CTS0	GPIO14	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART0					
33	RTS0	RTS0	N/A	PMU_5V	In	IN	HighZ
		Wake signal enabled by default.					
32	TXD1	TXD1	N/A	PVDD_1V8	In	BIDIR	HighZ, 2 mA
		UART1					
30	RXD1	RXD1	N/A	PVDD_1V8	Out	BIDIR	Out-1, 2 mA
		UART1					
31	CTS1	CTS1	N/A	PVDD_1V8	Out	BIDIR	Out-1, 2 mA
		UART1					
29	RTS1	RTS1	N/A	PMU_5V	In	IN	HighZ
		Wake signal enabled by default.					

Pad #	Pad Name	Primary Function	Alternate Function[1]	Power Group	Direction	Pad Type[2]	State at reset
28	GPIO15/TXD2	TXD2	GPIO15	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		In for primary function, UART2					
26	GPIO16/RXD2	RXD2	GPIO16	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART2					
27	GPIO17/CTS2/DCD0	GPIO17	CTS2/DCD0	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		UART2					
25	GPIO18/ RTS2/DSR0	GPIO18	RTS2/DSR0	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		UART2					
24	GPIO19/TXD3	GPIO19	TXD3	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		In for primary function, UART3					
22	GPIO20/RXD3	GPIO20	RXD3	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART3					
21	GPIO21/CTS3	GPIO21	CTS3	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		UART3					
23	GPIO22/RTS3	GPIO22	RTS3	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		UART3					

1. Alternate functions will be available in future versions via SW upgrade.
2. UART pad types electrical characteristics are detailed in Table 19.

High-Speed UARTs Flow Control Signals

- CTS0, CTS1, CTS2, CTS3: Clear-To-Send signals of resp. UART0, UART1, UART2, UART3 active low, of the RYZ024A. To be connected to the CTS of the remote UART device. See Table 3.
  Leave CTS unconnected if hardware flow control is not used.
- RTS0, RTS1, RTS2, RTS3: Ready-To-Send signals resp. UART0, UART1, UART2, UART3 active low, of the RYZ024A. To be connected to the RTS of the remote UART device. Tie to a 1 kOhm pull-down on RTS pin when flow control is not used. If it is connected to an external component (like a RS232 driver), the user should make sure that this component will present a low level to the RYZ024A. See Figure 3.

Figure 3 represents the typical implementation for the hardware flow control.

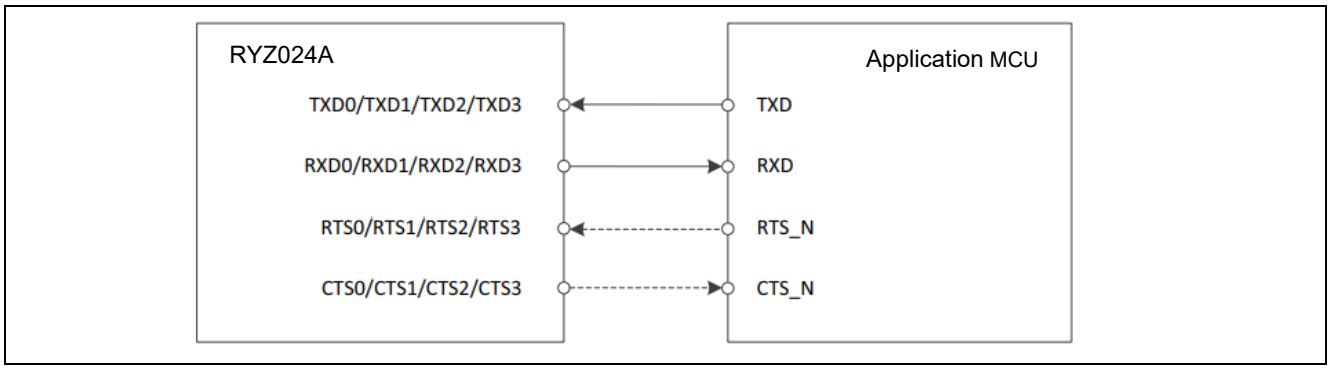


Figure 3. UART Convention and Flow Control

Note: See *Module Integration Guide* for details on UART connection.

USIM Interfaces

This section describes the SIM0 and SIM1 Interfaces.

SIM0 Interface

This is the main external SIM interface. It can be used with removable or non-removable SIM cards or with soldered SIM chips. The power supply of the SIM is managed by the modem to ensure lowest power consumption of the SIM.

Note: See section Power for behavior of IOs in Deep Sleep mode.

Table 3. SIM0 Signals

Pad #	Pad Name	Primary Function	Power Group	Direction	Pad type[1]	State at rest	Comment
42	SIM0_CLK	SIM0_CLK	PVDD_1V8	Out	BIDIR	Out-0, 2mA	Main SIM
45	SIM0_DETECT[2]	SIM0_DETECT	PMU_5V	In	IN	HighZ	Main SIM
44	SIM0_IO	SIM0_IO	PVDD_1V8	In/Out	BIDIR	HighZ, 2mA	Main SIM
43	SIM0_RSTN	SIM0_RSTN	PVDD_1V8	Out	BIDIR	Out-0, 2mA	Main SIM
73	SIM0_VCC[3]	SIM0_VCC	PVDD_1V8	Out	Supply	Out-0, 2mA	Main SIM

1. USIM pad type's electrical characteristics are detailed in Table 19.
2. SIM0_DETECT is active HIGH (HIGH when a card is present, LOW when no card is present). It can be configured as a WAKE pin via software command.
3. See range of values in Table 13.

SIM1 Interface

This interface can be used as a second SIM interface for RYZ024A, typically used for soldered SIM chips (since it lacks SIM detect and SIM VCC). If design only has one SIM, it is preferred then to use the main SIM interface (see Section SIM0 Interface above).

Note: See section Power for behavior of IOs in Deep Sleep mode.

Table 4. SIM1 Signals

Pad #	Pad Name	Primary Function	Alternate Function[1]	Power Group	Direction	Pad Type[2]	State at reset
40	GPIO26/SIM1_CLK	GPIO26	SIM1_CLK	PVDD_1V8	Out	BIDIR	Out-0, 2 mA
41	GPIO27/SIM1_RESETN	GPIO27	SIM1_RESETN	PVDD_1V8	Out	BIDIR	Out-0, 2 mA
39	GPIO25/SIM1_IO	GPIO25	SIM1_IO	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA

1. Alternate functions will be available in future versions via SW upgrade.
2. Pad types electrical characteristics are detailed in Table 19.

Important: Both SIM0 and SIM1 interfaces use 1.8 V signaling.

I2C

Note: See section Power for behavior of IOs in Deep Sleep mode.

Table 5. I2C Pad Details

Pad #	Pad Name	Primary Function	Alternate Function[1]	Power Group	Direction	Pad Type[2]	State at reset
95	GPIO23/ I2C_SDA	GPIO23	I2C_SDA	PVDD_1V8	In/Out	BIDIR	HighZ
97	GPIO24/ I2C_SCL	GPIO24	I2C_SCL	PVDD_1V8	In/Out	BIDIR	HighZ

1. Alternate functions will be available in future versions via SW upgrade.
2. I2C pad types electrical characteristics are detailed in Table 19.

PCM

Note: See section Power for behavior of IOs in Deep Sleep mode.

Table 6. PCM Pad Details

Pad #	Pad Name	Primary Function	Alternate Function[1]	Power Group	Direction	Pad Type[2]	State at reset
96	GPIO4/ PCM_CLK	GPIO4	PCM_CLK	PVDD_1V8	In/Out	BIDIR	HighZ
98	GPIO3/ PCM_RXD	GPIO3	PCM_RXD	PVDD_1V8	In/Out	BIDIR	HighZ
99	GPIO5/ PCM_FS	GPIO5	PCM_FS	PVDD_1V8	In/Out	BIDIR	HighZ
100	GPIO6/ PCM_TXD	GPIO6	PCM_TXD	PVDD_1V8	In/Out	BIDIR	HighZ

1. Alternate functions will be available in future versions via SW upgrade.
2. PCM pad type's electrical characteristics are detailed in Table 19.

SPI

Note: See section Power for behavior of IOs in Deep Sleep mode.

Table 7. SPI Pad Details

Pad #	Pad Name	Primary Function	Alternate Function[1]	Power Group	Direction	Pad Type[2]	State at reset
3	GPIO7/ SPI_SDI	GPIO7	SPI_SDI	PVDD_1V8	In/Out	BIDIR	HighZ
4	GPIO8/ SPI_SDO	GPIO8	SPI_SDO	PVDD_1V8	In/Out	BIDIR	HighZ
2	GPIO9/ SPI_CLK	GPIO9	SPI_CLK	PVDD_1V8	In/Out	BIDIR	HighZ
5	GPIO10/ SPI_CSN1	GPIO10	SPI_CSN1	PVDD_1V8	In/Out	BIDIR	HighZ
7	GPIO11/ SPI_CSN2	GPIO11	SPI_CSN2	PVDD_1V8	In/Out	BIDIR	HighZ

1. Alternate functions will be available in future versions via SW upgrade.
2. SPI pad types electrical characteristics are detailed in Table 19.

GPIO

There is a total of 33 GPIOs available on RYZ024A: 28 named GPIO1 to GPIO28 and 5 named GPIO31 to GPIO35. The GPIOs listed in Table 8 are not enabled by default. Changing their state can be done by software.

Table 8. GPIOs Disabled by Default

GPIO Range	Enable State by Default
GPIO3 to GPIO11	Disabled
GPIO17 to GPIO28	Disabled
GPIO31 to GPIO32	Disabled

The GPIOs are documented throughout this datasheet based on their shared or assigned function. In addition to the GPIO there are 5 wake signals available (documented in Section 2.8 Other Signals on page 16).

Other Signals

Note: See section Power for behavior of IOs in Deep Sleep mode.

Table 9. GND and DNC Pads

Pads Type	Pads Number
GND	1, 6, 37, 38, 50, 51, 52, 54, 56, 58, 59, 61, 64, 65, 71, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 91, 92, 93
DNC (Reserved)	15, 17, 53, 74, 75, 76, 77, 94

Table 10. Other Signals (No Interface)

Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction	Pad Type	State at reset
72	ADC1	ADC1 (See Note 1)	N/A	N/A	In	IN	N/A
		Analog Digital Converter (ADC, IN)					
12	GPIO1/ STATUS_LED	STATUS_LED	GPIO1	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		Primary Function: Status LED (STATUS_LED, OUT)					
13	GPIO2/ PS_STATUS	PS_STATUS	GPIO2	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		Primary Function: Power Saving status (PS_STATUS, OUT) enabled by default. Active high.					
14	GPIO28/ DTR0	GPIO28 (See Note 1)	DTR0	PVDD_1V8	In/Out	BIDIR	HighZ
19	GPIO31/ PWM0/ PULSE0/ 19M2_OUT	GPIO31 (See Note 1)	PWM0/ PULSE0/ 19M2_OUT	PVDD_1V8	In/Out	BIDIR	HighZ
18	GPIO32/ PWM1/ PULSE1	GPIO32 (See Note 1)	PWM1/ PULSE1	PVDD_1V8	In/Out	BIDIR	HighZ
9	GPIO33/ TX_IND	TX_IND	GPIO33	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		Primary Function: Transmission indicator (TX_IND, OUT). Active high.					
10	GPIO34/ ANT_TUNE0	ANT_TUNE0	GPIO34	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		Primary Function: Antenna tuning (ANT_TUNE0, OUT)					
11	GPIO35/ ANT_TUNE1	ANT_TUNE1	GPIO35	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		Primary Function: Antenna tuning (ANT_TUNE1, OUT)					
20	RESERVED/ FFF_FFH	RESERVED	N/A	PVDD_1V8	N/A	BIDIR	HighZ, 2 mA
		Boot mode selection (FFF_FFH, IN). This pad needs a pull-down resistor by default.					
15,	RESERVED	RESERVED	N/A	PVDD_1V8	N/A	BIDIR	N/A

Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction	Pad Type	State at reset
17, 53, 74, 75, 76, 77, 94		Do not connect					
46	RESETN	EXT_RST_N	N/A	PMU_5V	In	IN	In, Pull-up
		Module HW reset signal. Active low. The minimum duration of a reset pulse on the RESETN signal is 100 ns.					
16	RING0	RING0	N/A	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		UART0 ring line (RING0, OUT). Enabled by default with inverted polarity.					
48	WAKE0	WAKE0	N/A	PMU_5V	In	IN	HighZ
		Wake #0 input line (WAKE0, IN), disabled by default.					
47	WAKE1	WAKE1	N/A	PMU_5V	In	IN	HighZ
		Wake #1 input line (WAKE1, IN), disabled by default.					
49	WAKE2	WAKE2	N/A	PMU_5V	In	IN	HighZ
		Wake #2 input line (WAKE2, IN), disabled by default.					
55	WAKE3	WAKE3	N/A	PMU_5V	In	IN	HighZ
		Wake #3 input line (WAKE3, IN), disabled by default.					
57	WAKE4	WAKE4	N/A	PMU_5V	In	IN	HighZ
		Wake #4 input line (WAKE4, IN), disabled by default.					

1. Functions will be available in future versions via SW upgrade.
2.Pad types electrical characteristics are detailed in Table 19.

JTAG

Note: See section Power for behavior of IOs in Deep Sleep mode.

Table 11. JTAG Pad Details

Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction	Pad Type
69	JTAG_TCK	JTAG_TCK	PVDD_1V8	In	IN	In Pull-down Schmitt-trigger
67	JTAG_TDI	JTAG_TDI	PVDD_1V8	In	IN	In, Pull-up
68	JTAG_TDO	JTAG_TDO	PVDD_1V8	Out	BIDIR	Out, 0
66	JTAG_TMS	JTAG_TMS	PVDD_1V8	In	IN	In, Pull-up
70	JTAG_TRSTN	JTAG_TRSTN	PVDD_1V8	In	IN	In, Pull-down

1. JTAG pad types electrical characteristics are detailed in Table 19.

Note: The RYX024A does not support boundary scan (IEEE 1149.1) for production testing.

Antenna

Table 12. Antenna Pad Details

Pad #	Pad Name	Direction	Comments
90	LTE_ANT	In/Out	Main Antenna, for Rx and Tx

Electrical Characteristics

Power

Power pads characteristics

Note: Pad 1V8 is the reference voltage for IOs. It can be used to provide power small devices (100 mA maximum usage). This voltage is not available when the modem is in Deep Sleep. When the modem is in standby the voltage drops to 1.62 V as per Table 13.

Table 13. Power Pads

Pad #	Pad Name	Power Group	Direction	Min Operational Value	Typical Operational Value	Max Operational Value
8	1V8 See note above	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V
73	SIM_VCC[1]	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V
60, 62, 63	VBAT	N/A	In	2.2 V	5.5 V	

1. See also section USIM Interfaces.

Note: Reference VBAT voltage range is 2.5 V to 5.5 V for RF-compliant operation and 2.2 V to 5.5 V for functional behavior with possible degradation of RF performances.

Power-Up and Reset Sequences

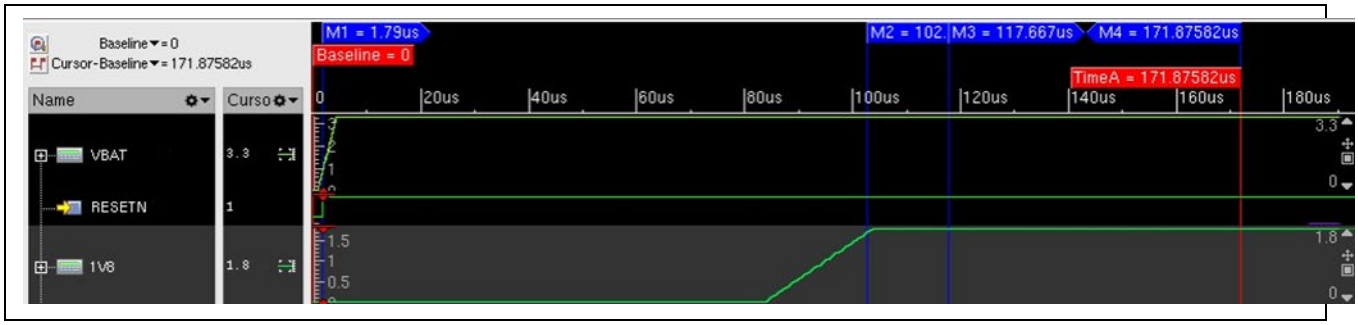


Figure 4. Timing Diagram for Power-Up Sequence

Important: The 1V8 power signal can remain low up to 370 µs after the VBAT rising edge.

Figure 5. Timing Diagram for Reset Sequence

Note: Since RESETN is pulled-up internally, RESETN does not need to be maintained low after VBAT is established. This is shown by Figure 5. There is no timing condition between RESETN and VBAT.

Note: RESETN minimum duration for reliable detection is 100 µs.

Power States

Figure 6 represents the electrical states of the module and their transitions.

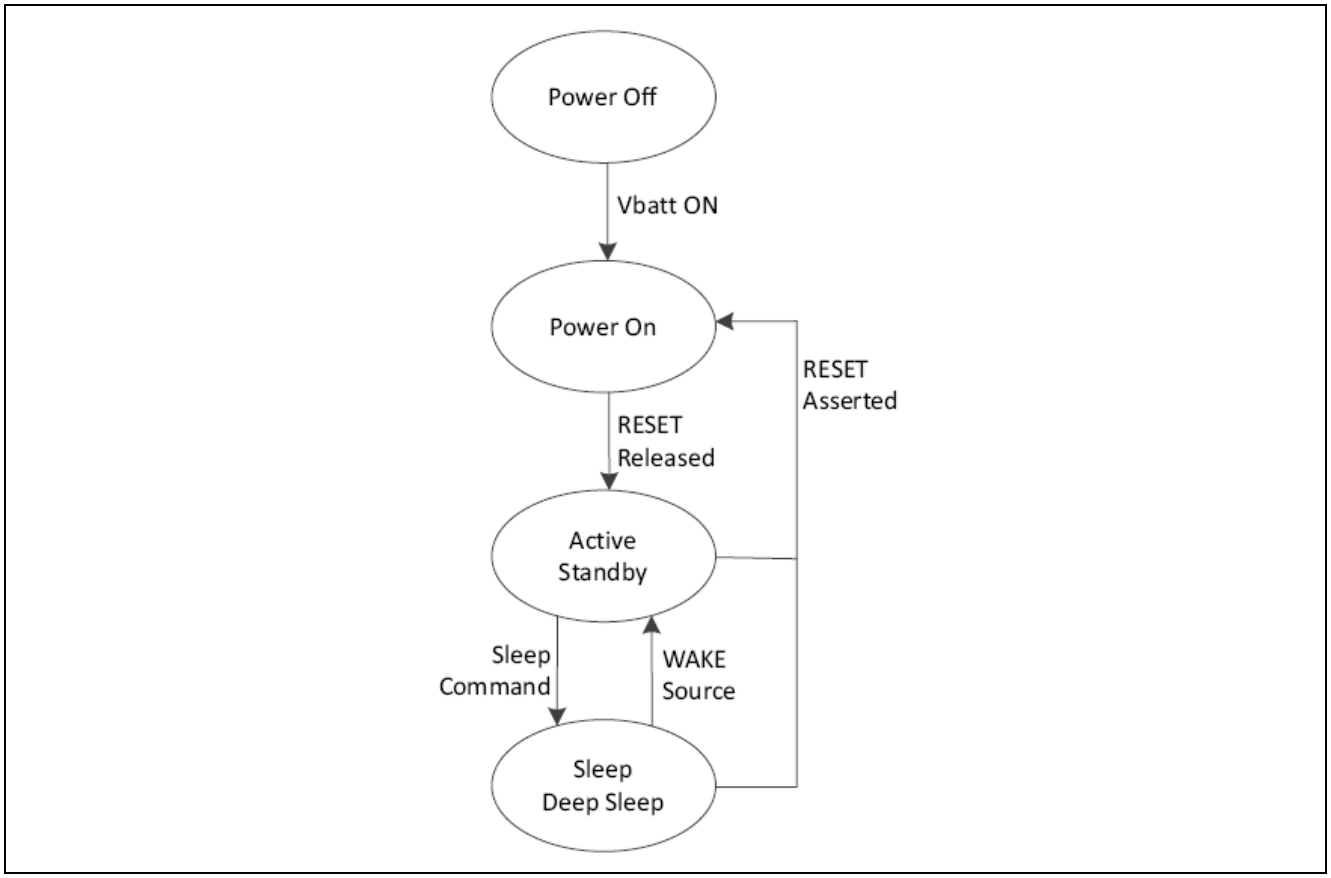


Figure 6. Electrical States and Transitions

The various power modes are described in Table 14 and illustrated on Figure 6.

Table 14. Power Modes Description

Power Mode	LTE Mode	Available Interfaces
Active	Connected (RF on)	All interfaces
Standby	Connected (RF off)	All interfaces
Sleep	Short eDRX idle duration RRC Idle	WAKE pins (including RTS0/1)
Deep Sleep	PSM idle, Long eDRX idle duration, radio-off, airplane	WAKE pins (including RTS0/1)

PVDD_1V8 BIDIR Pads State in Deep Sleep Mode

In Deep Sleep Mode the Digital PVDD_1V8 bi-directional IOs are completely powered off and can be seen as 50 MOhm high-impedance from the outside.

PMU_5V IN Pads State in Deep Sleep Mode

In Deep Sleep Mode the Digital PMU_5V inputs are completely powered off and can be seen as 180 MOhm high-impedance from the outside.

Table 15 shows the values of the measured leakage current (measurements taken on silicon) for the PMU wake inputs.

Table 15. Measured Leakage Current for the PMU Wake Inputs

Minimum	Typical	Maximum
3 nA	4 nA	12 nA

Table 16 shows values of the external pull-up/pull-down resistor to be used on the PMU wake inputs pads.

Table 16. External Pull-up/Pull-down Resistor to Be Used on the PMU Wake Input Pads

Minimum	Typical	Maximum
1 kOhm	10 kOhm	100 kOhm

Table 17 shows details about the PMU wake inputs pulses detection mechanism timings.

Table 17. Details about the PMU Wake Inputs Pulses Detection Mechanism Timings

Maximum Pulse Width that Is Guaranteed to Be Ignored	Minimum Pulse Width that Is Guaranteed to Be Seen
11. ns	100 µs

Table 18 provides the internal pull-up current range for RESETN.

Table 18. Internal Pull-Up Strength for RESETN Pad

Minimum	Typical	Maximum
73.5 nA	100 nA	160.5 nA

Digital IO Characteristics

The voltage and current characteristics of the various IO pads of the RYZ024A are described in this section.

The I/Os belong to different power groups:

- PVDD_1V8
- PMU_5V

For each I/O of these power group, the operational voltage range is described

in Table 19 and Table 20.

Caution: The PCB designer must ensure that the voltage on these pads never exceeds Vih VIH of the power group to which they belong.

See Table 19 for digital IO characteristics of the different IO pads. Refer to each interface of RYZ024A in section Interfaces to know the power group and IO pad type for each pad. Note that IN pads are inputs only whereas BIDIR can be both inputs and output.

Table 19. DC Characteristics for Digital IOs, Voltage 1.8 V, PVDD_1V8 Power Group

Symbol	Minimum	Maximum	Unit
VIH Input HIGH level	1.26	3.3	V
VIL Input LOW level	0	0.54	V
VOH Output HIGH voltage	1.44	1.8	V

Symbol	Minimum	Maximum	Unit
VOL Output LOW voltage	0	0.36	V
IRPU Input pull-up resistor current	15		µA
RRPU Input pull-up resistance	27	34	kOhm
IRPD Input pull-down resistor current	15		µA
RRPD Input pull-down resistance	27	34	kOhm
VH Input hysteresis	0.18		V
IPAD Input leakage current, non-tolerant	-1	1	µA
IOZ Off-State leakage current		1	µA

Table 20. DC Characteristics for Digital IOs, PMU_5V Power Group

Symbol	Minimum	Maximum	Unit
VIH Input HIGH level	0.8	VBAT + 0.6 (max 5.5)	V
VIL Input LOW level	0	0.2	V

RF Performance

Important: For proper operation, the VSWR at the antenna pad must be better than 2:1 in conducted mode and 3:1 in radiated mode. A higher value could result either in poor RF performance, reduced Tx power or increased sideband/harmonic emission levels. Very high VSWRs can permanently damage the power amplifier.

It is recommended to add a DC blocking capacitor in series with the module RF input/ output pad (#90).

RF Sensitivity

The GM02S exhibits the following typical RF sensitivity at 2.5 V.

Table 21. RF Sensitivity

Band	Typical Sensitivity
Low Bands: B5, B8, B12, B13, B14, B17, B18, B19, B20, B26, B28, B71, B85	-105 dBm
High bands: B1, B2, B3, B4, B25, B66	-106 dBm

RF Output Power

The GM02S maximum output power within the recommended operating range (from 2.5 to 5.5 V) is given in Table 22.

Table 22. RF Max Output Power

Bands	Output Power
All bands	23 dBm ± 1 dB

RF Performance at 2.2V

While it is not recommended to operate the GM02S in the range 2.2 to 2.5 V, the RF section will continue to work normally, albeit with reduced TX output power as shown in Table 23 below.

Table 23. RF Performance at 2.2V compared to 2.5V

Temperature	Sensitivity Loss	Output Power Loss
-30 °C	No loss	1.1 dB
25 °C	No loss	1.1 dB
85 °C	No loss	1.7 dB

Power Supply Dimensioning

This section provides guidance to device manufacturers when designing the power supply or selecting the battery that will power RYZ024A.

Overview

The current consumption of the RYZ024A peaks before every TX sub-frame as shown in Figure 7. In this figure, every time division is 50 µs. Around 150 µs from the start, two current peaks can be observed with a current peak 34% higher than the average current consumption during the 23 dBm TX tone.

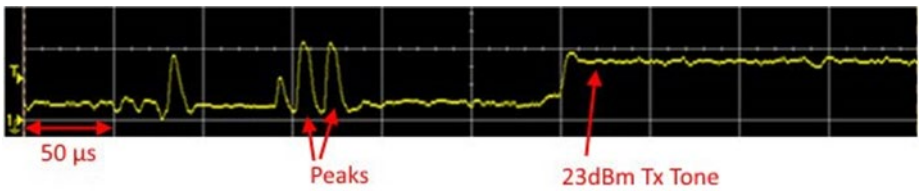


Figure 7. Current Consumption in TX Sub-Frame

Peak Current Measuring Method

Renesas recommends the setup represented in Figure 8 for peak current measurement. This setup was used to record the measurements presented in Table 24.

Notes:

1. Voltage probes are placed close to module VBAT input.
2. Voltage probes accuracy is calibrated using a current probe.
3. A large capacitance C_{batt} is placed close to the VBAT pin to simulate a battery and screen the device from the parasitic inductances of the cables and tracks.
4. 2x22 µF capacitors (C_{ext}) are placed between the voltage probes and the module VBAT input to soften the current peaks.

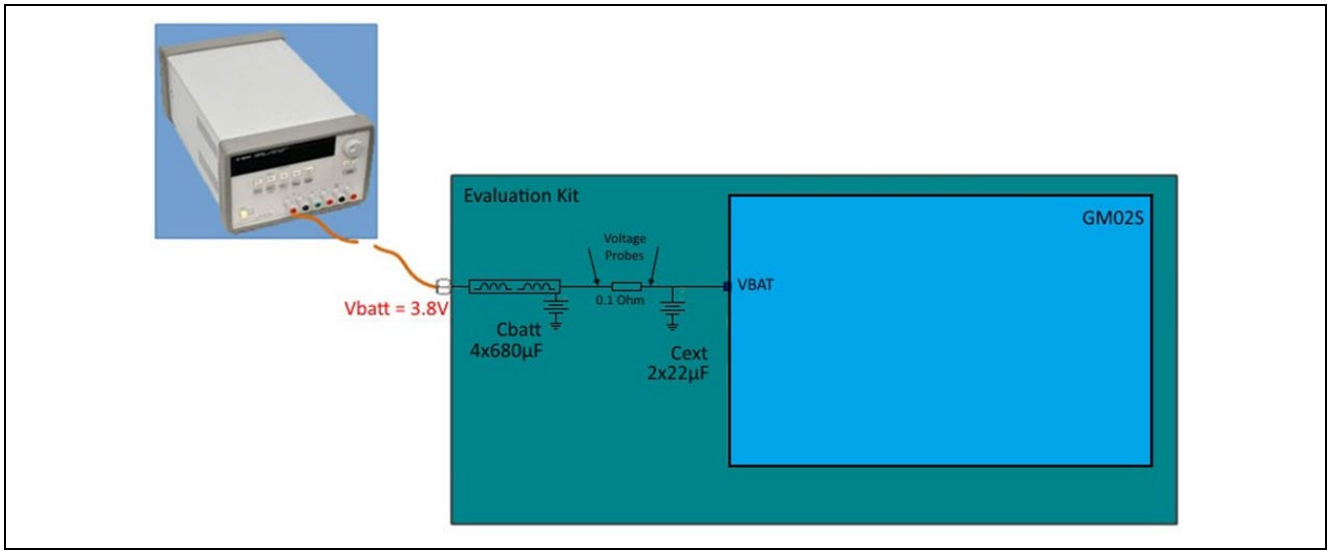


Figure 8. Setup for Current Peak Characterization

Peak Current Characterization

Table 24 represents the peak current values measured on the setup shown on Figure 8 for different voltages and temperatures within the range supported by RYZ024A.

Table 24. Peak Power Characterization

Input Voltage	Board at -40°C	Board at -30°C	Board at +25°C	Board at +85°C
5.5 V	328 mA	305 mA	263 mA	268 mA
3.8 V	475 mA	438 mA	444 mA	479 mA
2.5 V	705 mA	667 mA	679 mA	741 mA
2.2 V	676 mA	640 mA	652 mA	717 mA

Margin

Important: It is recommended that designs that could be sensitive to the peak current described in this section include the recommended C_{ext} 2x22 µF and dimension the power supply with an extra 20% margin with respect to the values provided in this section.

Electrical Maximum Ratings

Table 25. Electrical Maximum Ratings

Parameter	Minimum	Maximum
Supply Voltage VBAT	-0.2 V	5.5 V
I/Os in Power Group PVDD_1V8	-0.2 V	4.125 V
I/Os in Power Group PMU_5V	-0.2 V	6.0 V

Thermal Considerations

Special attention needs to be given to thermal dissipation.

The outer layers of the host board must be covered in as many wide copper areas as possible, and those must be stitched with evenly spaced ground vias. Care must be taken that no air gap exists along the thermal path from the RYZ024A to the dissipating copper area(s). Gaps can be filled with heat conducting materials such as GapPad™.

The Gxx pads should be tied to a large ground plane on the customer's PCB layer 1. It is also recommended to have the Gxx pads area on the PCB stitched with through ground vias to improve thermal dissipation.
If the host board is piggybacked over a larger board, the aforementioned heat dissipation considerations should be applied to both the main and the daughter board.

Mechanical Characteristics

Package Description

The package size with tolerance is:

(16.3 ± 0.15) mm x (17.0 ± 0.15) mm x (1.85 max) mm. Maximum warpage is 0.13 mm (as per JEITA ED7306). The weight of the RYZ024A is 0.85 g.

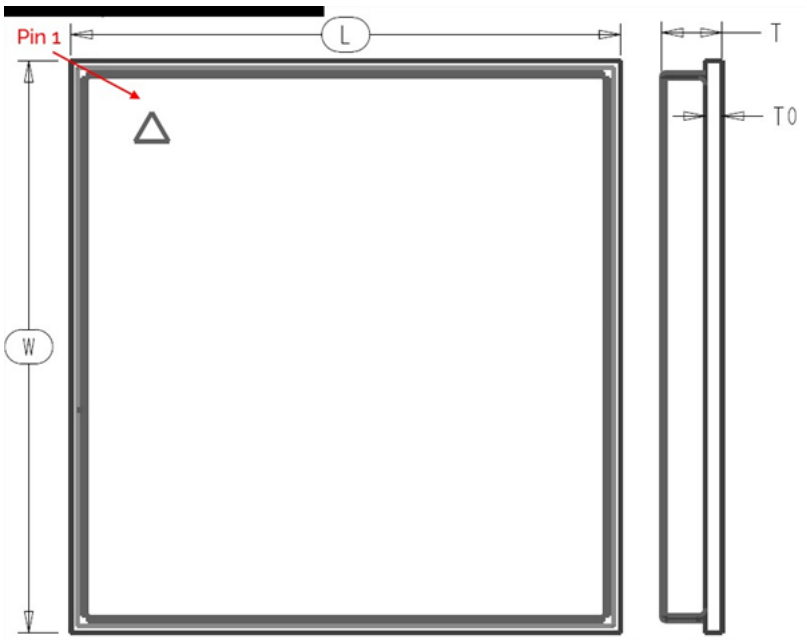


Figure 9. RYZ024A Top and Side Views

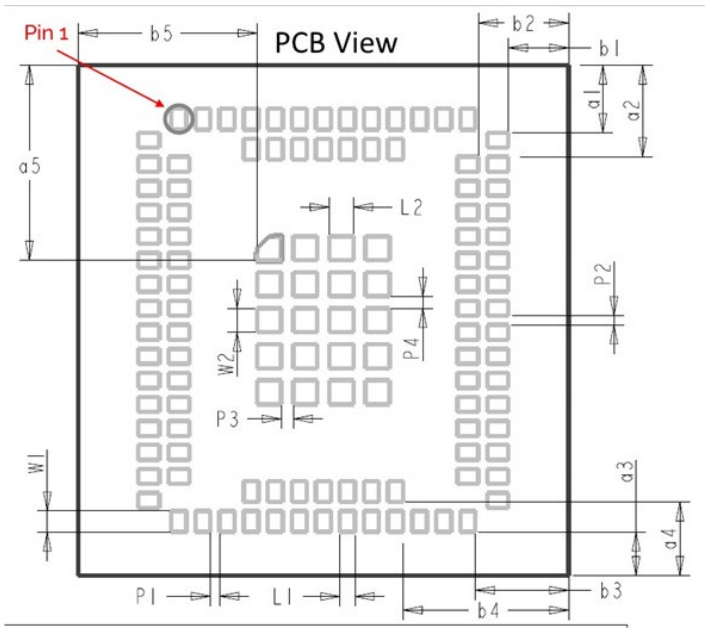


Figure 10. RYZ024A PCB View

Table 26. RYZ024A Dimensions (mm)

Dimension	Value (mm)
L	16.3 ± 0.15
W	17.0 ± 0.15
T	1.85 max

Dimension	Value (mm)
T0	0.426 max
L1	0.5 ± 0.1
W1	0.7 ± 0.1
L2	0.8 ± 0.1
W2	0.8 ± 0.1
a1	2.25 ± 0.1
a2	3.05 ± 0.1
a3	1.45 ± 0.1
a4	2.45 ± 0.1
a5	6.5 ± 0.1
b1	2.0 ± 0.1
b2	3.0 ± 0.1
b3	3.1 ± 0.1
b4	5.5 ± 0.1
b5	5.95 ± 0.1
P1	0.3 ± 0.1
P2	0.3 ± 0.1
P3	0.4 ± 0.1
P4	0.4 ± 0.1

Figure 11. RYZ024A Laser Marking (Preliminary)

Notes on Figure 11:

1. The triangle in the low-right corner provides pin#1 location.
2. FCC ID: 2AU6XRZ024A
3. IC: 20519-RZ024A
4. IMEI:*XXXXXXXXXXXXXXX*
5. S/N:G2P*YYMMDDNNNNSSS* (16 digits)
   —G2P: reserved, value subject to change at Renesas' discretion (3 digits)
   —YYMMDD: Manufacturing Date (YY:Year;MM:Month,DD:Day)
   —*NNNN*: Panel counter (from 0001~9999)
   —*SSS*: Piece location on panel (from 001~065)
6. 2D marked "a" refer to IMEI Barcode
7. 2D marked "b" refer to S/N Barcode

Environmental Conditions

The environmental operating conditions are:

- Temperature (PCB temperature as measured by on-board thermistor):
  —– Operational: -40°C, +85°C
  —– RF compliant: -30°C, +85°C
- Humidity: 10% to 85% (non-condensing)

Packing

The RYZ024A is delivered in Tape-and-Reel. Details are provided in the figures below.

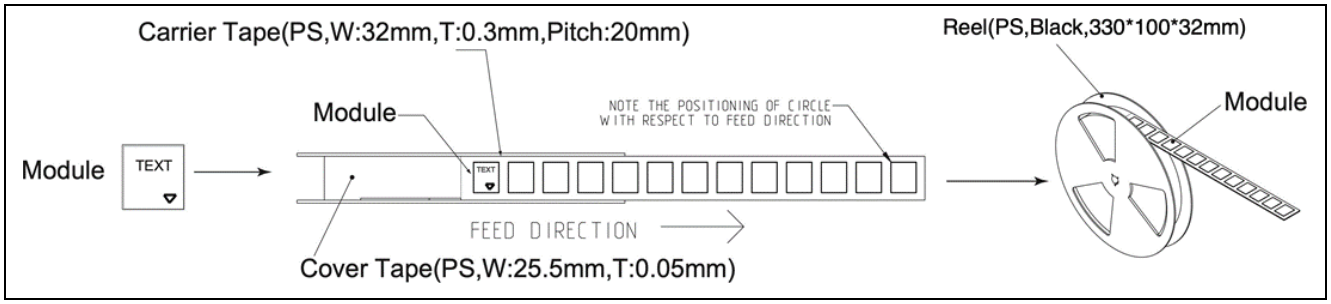


Figure 12. Packing Modules in Reels

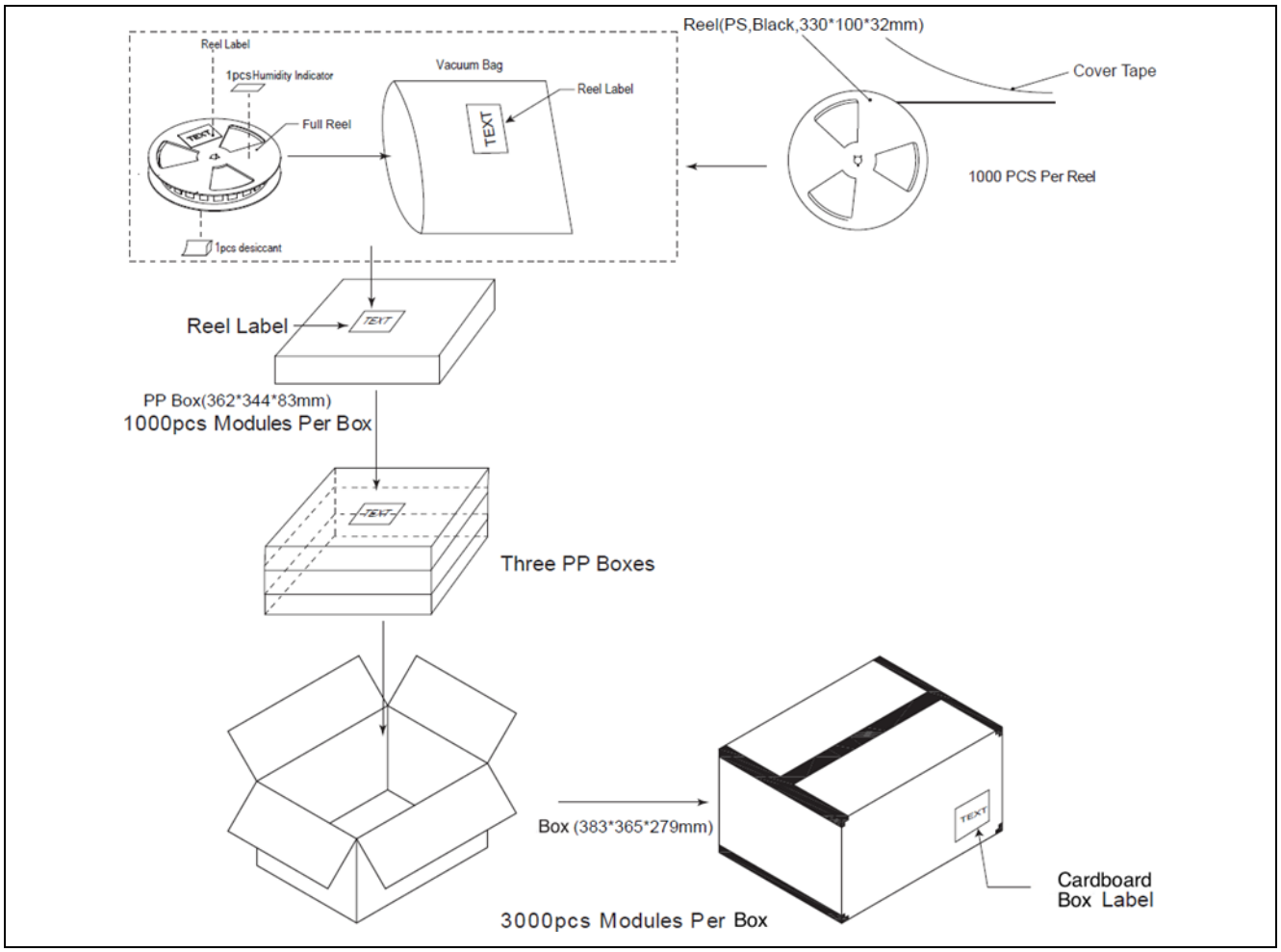


Figure 13. Packing Reels in Boxes

The full box set weights about 5.95 kg.

Storage and Mounting

The RYZ024A module is Moisture Level 3 rated as per JEDEC industrial standard: http://www.ipc.org/TOC/J-STD-033D-TOC.pdf. The RYZ024A is JEDEC J-STD-033D compliant and can be stored at T < 40 °C and relative humidity < 90%. The RYZ024A can support up to 3 reflows with 250°C maximum.

Table 27. Reflow Profile

Profile Feature	
Solder Paste Alloy	Sn 96.5/Ag 3.0/Cu 0.5 (Lead Free solder paste)
Peak Package Body Temperature	235°C to 245°C
Fusion Time	Temp: over 220°C Time: 60 seconds ~ 90 seconds
Pre-heat / Soak	Temp: 150 ~ 200°C Time: 60 seconds ~ 120 seconds
Ramp-up Rate	< 3°C/second
Ramp-down Rate	-3°C to 0°C/second
Air Composition	N2, O2 contents less than 1,500 ppm

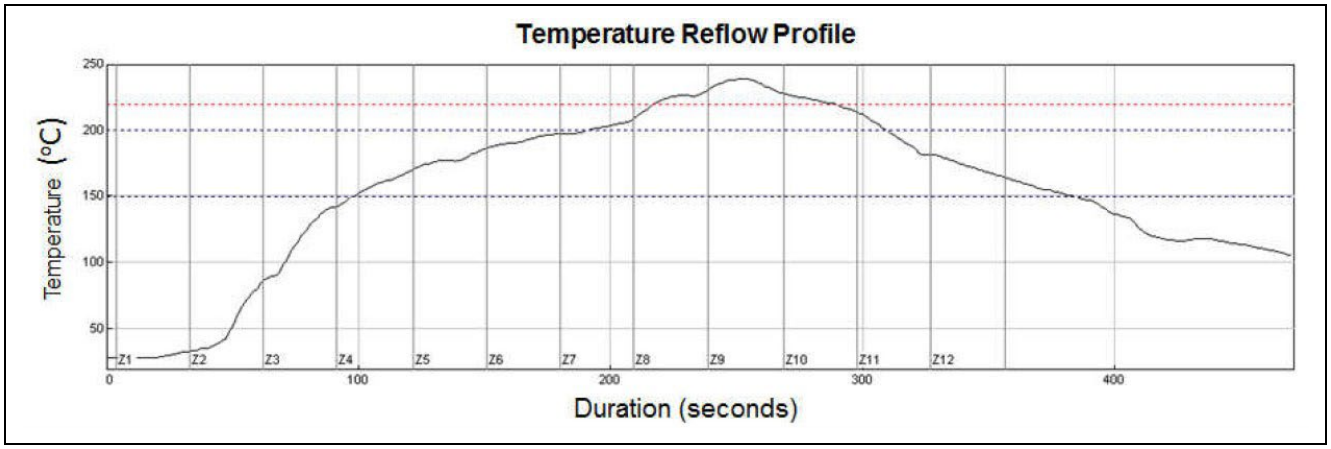


Figure 14. Reflow Profile Parameters

Recommended stencil thickness: 0.1 mm to 0.13 mm (prefer 0.1 mm). More detail on PCB land pattern will be provided in a future edition of the document.

Reliability Specification

RYZ024A has been tested against Renesas's industrial reliability specification as described in the following table.

Table 28. Reliability Test Plan

Item	Test Conditions	Standard	No. of Samples	Result
Preconditioning	• Bake: 125°C / 24 hours • MSL3: 30°C/60% RH, 192 hrs • SAT (CSAM & TSCAN) • X-ray • Reflow 3 cycles at Tp: 250 ±2°C • SAT (CSAM & TSCAN)	JESD22-A113	175	PASS

Item	Test Conditions	Standard	No. of Samples	Result
TC	Temperature Shock Cycling (TC): -40°C to +85°C air to air, 20 minutes, ramp rate 20°C/minute, 1000 cycles	JESD22-A104	25	PASS
THB	Temperature Humidity Bias Test +85°C, 85 % RH, Vcc Max, Read Point at 168 hrs	JESD22-A101	25	168 hrs: PASS
Environmental Testing - A Cold	Environmental Testing Test A Cold. -40°C, 500 hrs	IEC60068-2-1 JESD22-A119	25	PASS
Environmental Testing - B Dry Heat	Environmental Testing Test B Dry Heat. +85°C, 500 hrs	IEC60068-2-2 JESD22-A103	25	PASS
HTOL	High Temperature Operating Test 75°C, Vcc max, Tx: 50% / Rx: 50%. Read Point at 283/500/1,000 hours	N/A	50	PASS
Shock	Mechanical Shock (MS) (Half Sine, 500G, 1.0 ms, 1 shock for	DIN IEC 68-2-27	15	PASS
Drop	Drop Test 1. Height: 80 cm; 2. Concrete or steel; 3. All surfaces and edges.	DIN IEC 68-2-31 ETS 300019-2-7	15	PASS
Vibration	Vibration Test (Vib) Sweep-Sine Vibration. Sinusoidal, 10 ~ 500 Hz, 1.0 octave/ min, 10 sweep cycles for 2 hr for each axis.	DIN IEC 68-2-6 EIA/TIA 571 §4.1.1.2	15	PASS
ESD	HBM Start: ±1000V, Stop:± 1500V	JS-001JESD22-A114	12	PASS
	CDM Start: ±250V, Stop: ±500V	JS-002STM5.3.1	12	PASS
TCT	Temperature Change Test 10 cycles; 1 cycle has the following steps (roughly 7+ hrs): • Ramp from ambient (23°C) to -40°C at 3°C/min. • 3 hrs at - 40°C • Ramp to 85°C at 3°C/min • 3 hrs at 85°C • Ramp from 85°C to 23°C at 3°C/ min	IEC60068-2-14	25	PASS

Regulatory Information

This section contains general regulatory information.

FCC Regulatory Approval

FCC-ID: 2AU6XRZ024A (single modular approval)

This above identified LTE radio module is not intended to be provided to end-users but is for installation by OEM integrators only.

Installation/Integration

OEM integrators must follow Renesas installation instructions to provide for and benefit from FCC compliant module integrations and must abide especially by the following provisions:

The maximum antenna gain values (accounting for cable attenuation) to comply with the FCC maximum ERP/EIRP limits and with RF Exposure rules:

- LTE band 2 (1900 PCS): 8.0 dBi
- LTE band 4 (AWS-1): 5.0 dBi
- LTE band 5 (850): 9.4 dBi
- LTE band 12 (700a): 8.6 dBi
- LTE band 13 (700c): 9.1 dBi
- LTE band 17 (700b): 8.7 dBi
- LTE band 25 (1900+): 8.0 dBi
- LTE band 66 (AWS-3): 5.0 dBi

The Renesas' module integration guidelines must be closely followed.

Compliance of host integrations of the module is limited to hosts adaptation designs which are identical to Renesas' reference design.

Host integrations with adaption designs deviating from Renesas' reference design require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID;

Host integrations with co-located (simultaneously operating) radio transmitters must be evaluated in accordance with FCC multi-transmitter rules and may require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID, dependent on the result of the evaluation; Inquiry at FCC or a TCB is urgently recommended.

Integrations of the module into host products which are intended for portable use, i.e. less than 20cm distance between its radiating structures (antenna) and the body of nearby persons, or which otherwise put additional technical requirements like Hearing Aid compatibility require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID;

Compliance with Unwanted Emission Limits for Digital Device

If the OEM host integration fully complies with the above described reference design and can completely inherit and rest on compliance of the existing modular approval the OEM remains still responsible to show compliance of the overall end-product with the FCC limits for unwanted conducted and radiated emissions from the digital device.

End-product Labelling

- FCC-ID

The module's FCC-ID must either be visible from the exterior of the host product (e.g. per window) or per electronic display, or shall be displayed on an additional exterior label per the following or similar string: contains FCC-ID: 2AU6XRZ024A

- Digital Device - Unwanted Emissions Notice

If the end-product falls under part 15 of the FCC rules (it shall display the following user notice on its exterior acc. to part 15.19 (the notice may be printed in the manual in case the host is too small):

```
This device complies with Part 15 of the FCC Rules. Operation is subject to the
following two conditions:

1. This device may not cause harmful interference, and
```

2. This device must accept any interference received, including interference that may cause undesired operation.

- Further Labelling Requirements may apply dependent on the FCC rule parts relevant to the host product.
- End-product User Instructions / Notices in the Manual

At a minimum, end-product users must be provided with the following notices at a prominent location of the product literature furnished with the product:

— Product Modifications

Modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

— RF Exposure Compliance

This equipment complies with FCC radio frequency radiation exposure rules and limits set forth for an uncontrolled environment, when installed and operated with minimum distance of 20cm between its radiating structures (antenna) and the body of nearby persons and when not operated simultaneously with other nearby radio-transmitters.

- Maximum Antenna Gain

The user instructions of end-products equipped with standard external antenna connectors for the modular radio transmitter providing the option to connect other antennae than those which may or may not be bundled with the end-product must list the maximum allowed antenna gain values as derived from those given above, accounting for the cable attenuations of the actual installation.

- Digital Device - Unwanted Emissions Notice

If the end-product is or contains a digital device (unintentional radio portions) and is not exempted by its use case (like vehicular use) the following part 15.105 (b) user notice shall be provided at prominent location of the product literature:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: o Reorient or relocate the receiving antenna. o Increase the separation between the equipment and receiver. o Connect the equipment into an outlet on a circuit different from that to which the receiver is connected. o Consult the dealer or an experienced radio/TV technician for help

- Further User Notices

  May be required dependent on the FCC rule parts relevant to the host product.
- Non-allowed User Instructions

  The end-product user guidance may NOT include instructions about how to install or de-install the module.

ISED Regulatory Approval

This device complies with ISED's licence exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR de l'ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit supporter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1. The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2. The transmitter module may not be co located with an y other transmitter or antenna.

As long as the two conditions above are met , further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1. L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2. Le module émetteur peut ne pas être coïmp lanté av ec un autre émetteur ou antenne.

Tant que les duex conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

- LTE band 2 (1900 PCS): 8.0 dBi
- LTE band 4 (AWS-1): 5.0 dBi
- LTE band 5 (850): 6.1 dBi
- LTE band 12 (700a): 5.6 dBi
- LTE band 13 (700c): 5.9 dBi
- LTE band 17 (700b): 5.6 dBi
- LTE band 25 (1900+): 8.0 dBi
- LTE band 66 (AWS-3): 5.0 dBi

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorisation is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re evaluating the end product (including the transmitter) and obtaining a separate Canada authorisation.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labelling

This transmitter module is authorised only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: 20519-RZ024A".

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:

"Contient des IC: 20519-RZ024A".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

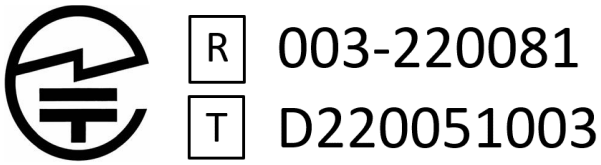
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

ACMA Regulatory Marking

Japan radio/terminal equipment based on type certification Regulatory Marking

RYZ024A has obtained certified construction type certification (certification number: 003-220081). Manufacturers of terminal equipment that incorporates the RYZ014A module must display the technical suitability mark on the embedded terminal equipment. For the antenna used for certification, refer to RYZ024A Antenna List for Type Certification in Japan.

In addition, RYZ024A has certified the Telecommunications Business Law (certification number: D220051003).



RE Directive Regulatory Safety Notice

Hereby, Renesas Electronics America Inc. declares that the radio equipment type RYZ024A is in compliance with Directive 2014/53/EU.

Caution: Equipment must be supplied by ES1, PS1 circuits according to the standard EN 62368-1.

UKCA Regulatory Marking

Acronyms

Acronym	Definition
ADC	Analog to Digital Converter
CPU	Central Processing Unit
DL	Downlink
ESD	Electro-static discharge
ETSI	European Telecommunications Standard Institute
GND	Ground
GPIO	General Purpose Input Output
I/O	Input/Output
I^2C	Inter-Integrated Circuit interface
IMEI	International Mobile Equipment Identity
IP	Internet Protocol
JTAG	Joint Test Action Group
LGA	Large Grid Array
LNA	Low-Noise Amplifier
LTE	Long Term Evolution, or 4G. Standard is developed by the 3GPP www.3gpp.org.
MIMO	Multiple In Multiple Out
NAS	Network Access Server
OMADM	Open Mobile Alliance Device Management
PCM	Pulse-Code Modulation
PHY	Physical Layer
RED	European Radio Equipment Directive
SAW	Surface Acoustic Wave (filter)
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
Rx	Reception
S/N	or SN: Serial Number
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
Tx	Transmission
UART	Universal Asynchronous Receiver Transmitter
UE	User Equipment
UL	Uplink
USB	Universal Serial Bus

Appendix 1. Related Documents

Component	Document Type	Description
Microcontrollers	Datasheet	Features, overview, and electrical characteristics of the MCU
	User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
	Application Notes	Technical notes, board design guidelines, and software migration information
	Technical Update (TU)	Preliminary reports on product specifications such as restrictions and errata
Software	User's Manual: Software	Command set, API reference, and programming information
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications
Tools & Kits, Solutions	User's Manual: Development Tools	User's manuals and quick start guides for developing embedded software applications with Software Packages, Development Kits, Starter Kits, Promotion Kits, Product Examples, and Application Examples
	Quick Start Guide	
	Application Notes	Project files, guidelines for software programming, and application examples for developing embedded software applications

Appendix 2. Pin Descriptions

	Pad #	Pad Name	Power Group	Direction	Min Operational Value	Typical Operational Value	Max Operational Value	State @ PSP-M (Deep Sleep)	State @ PSP	State @ PSPA / PSPO (Standby / Active)
Power	8	1V8	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V	Not available	Min value	Typical value
	73	SIM_ VCC1	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V	Not available	Typical value	Typical value
	60, 62, 63	VBAT	N/A	in	2.2 V	5.5 V				

Function Enabled	**Function Disabled**

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur -able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
UART	36	GPIO 12/TX D0	TXD0 In for primary function, UART0	GPIO12	PVDD _1V8	In/Out	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz		Yes	pull-up
	34	GPIO 13/RX D0	RXD0 Out for primary function, UART0	GPIO13	PVDD _1V8	In/Out	Out	BIDIR	Out-1, 2mA	Highz	Highz	Driven by GM02S	Driven by GM02S		Yes	
	35	GPIO 14/CT S0	CTS0 Out for primary function, UART0	GPIO14	PVDD _1V8	In/Out	Out	BIDIR	Out-1, 2mA	Highz	High	Driven by GM02S	Driven by GM02S	Low	Yes	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur-able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
	33	RTS0	RTS0 Wake signal enabled by default.	N/A	PMU_5V	In	In	IN	HighZ	Highz	Highz	Highz	Highz	Low	Yes	pull-up
	32	TXD1	TXD1, UART1	N/A	PVDD_1V8	In	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz	High	Yes	pull-up
	30	RXD1	RXD1, UART1	N/A	PVDD_1V8	Out	Out	BIDIR	Out-1, 2mA	Highz	Highz	Driven by GM02S	Driven by GM02S	High	Yes	
	31	CTS1	CTS1, UART1	N/A	PVDD_1V8	Out	Out	BIDIR	Out-1, 2mA	Highz	High	Driven by GM02S	Driven by GM02S	Low	Yes	
	29	RTS1	RTS1,Wake signal enabled by default.	N/A	PMU_5V	In	In	IN	HighZ	Highz	Highz	Highz	Highz	Low	Yes	pull-up
	28	GPIO 15/TXD2	TXD2, UART2	GPIO15	PVDD_1V8	In/Out	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz	High	Yes	pull-up
	26	GPIO 16/RXD2	RXD2, UART2	GPIO16	PVDD_1V8	In/Out	Out	BIDIR	Out-1, 2mA	Highz	Highz	Driven by GM02S	Driven by GM02S	High	Yes	
	27	GPIO 17/ CTS2 /DCD 0	GPIO17 , UART2	CTS2/DCD0	PVDD_1V8	In/Out	In	BIDIR	Out-1, 2mA	Highz	Highz	Highz	Highz		No	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur-able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
	25	GPIO 18/ RTS2 /DSR 0	GPIO18 , UART2	RTS2/DS R0	PVDD _1V8	In/Out	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz		No	pull-up
	24	GPIO 19/TX D3	GPIO19 , UART3	TXD3	PVDD _1V8	In/Out	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz	High	Yes	pull-up
	22	GPIO 20/RX D3	GPIO20, UART3	RXD3	PVDD _1V8	In/Out	In	BIDIR	Out-1, 2mA	Highz	Highz	Highz	Highz	High	Yes	pull-up
	21	GPIO 21/CT S3	GPIO21, UART3	CTS3	PVDD _1V8	In/Out	In	BIDIR	Out-1, 2mA	Highz	Highz	Highz	Highz	High	Yes	
	23	GPIO 22/RT S3	GPIO22, UART3	RTS3	PVDD _1V8	In/Out	In	BIDIR	Out-1, 2mA	Highz	Highz	Highz	Highz	High	Yes	pull-up
USIM0	42	SIM0 _CLK	SIM0_CL K	N/A	PVDD _1V8	Out	Out	BIDIR	Out-0, 2mA	Highz	Driven by GM02S	Driven by GM02S	Driven by GM02S		Yes	
	45	SIM0 _DET ECT	SIM0_DE TECT	N/A	PMU_ 5V	In	In	IN	HighZ	Highz	Highz	Highz	Highz	High	No	
	44	SIM0 _IO	SIM0_IO	N/A	PVDD _1V8	In/Out	In/Out	BIDIR	HighZ, 2mA	Highz	Driven by GM02S	Driven by GM02S	Driven by GM02S		Yes	
	43	SIM0 _RST N	SIM0_RS TN	N/A	PVDD _1V8	Out	Out	BIDIR	Out-0, 2mA	Highz	Driven by GM02S	Driven by GM02S	Driven by GM02S	Low	Yes	
	73	SIM0 _VCC	SIM0_VC C	N/A	PVDD _1V8	Out	Out	Supply	Out-0, 2mA	Highz	Power enabled	Power enabled	Power enabled		Yes	
USIM1	40	GPIO 26/SI	GPIO26	SIM1_CL K	PVDD _1V8	Out	In	BIDIR	Out-0, 2mA	Highz	Highz	Highz	Highz	High	Yes	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur-able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
		M1_CLK														
	41	GPIO27/SIM1_RESETN	GPIO27	SIM1_RESETN	PVDD_1V8	Out	In	BIDIR	Out-0, 2mA	Highz	Highz	Highz	Highz	High	Yes	
	39	GPIO25/SIM1_IO	GPIO25	SIM1_IO	PVDD_1V8	In/Out	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz	High	Yes	
I2C	95	GPIO23/I2C_SDA	GPIO23	I2C_SDA	PVDD_1V8	In/Out	In	BIDIR	HiZ	Highz	Highz	Highz	Highz	High	Yes	pull-up
	97	GPIO24/I2C_SCL	GPIO24	I2C_SCL	PVDD_1V8	In/Out	In	BIDIR	HiZ	Highz	Highz	Highz	Highz	High	Yes	pull-up
PCM	96	GPIO4/PCM_CLK	GPIO4	PCM_CLK	PVDD_1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	98	GPIO3/PCM_RXD	GPIO3	PCM_RXD	PVDD_1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	99	GPIO5/PCM_FS	GPIO5	PCM_FS	PVDD_1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	100	GPIO6/PCM_TXD	GPIO6	PCM_TXD	PVDD_1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur-able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
SPI	3	GPIO 7/ SPI_ SDI	GPIO7	SPI_SDI	PVDD _1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	4	GPIO 8/ SPI_ SDO	GPIO8	SPI_SDO	PVDD _1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	2	GPIO 9/ SPI_ CLK	GPIO9	SPI_CLK	PVDD _1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	5	GPIO 10/ SPI_ CSN1	GPIO10	SPI_CSN 1	PVDD _1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	7	GPIO 11/ SPI_ CSN2	GPIO11	SPI_CSN 2	PVDD _1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
Other	72	ADC1	ADC1 Analog Digital Converte r (ADC, IN)	N/A	N/A	In		IN	N/A	Highz	Highz	Highz	Highz			
	12	GPIO 1/ STAT US_L ED	STATUS _LED Primary Function: Status LED (STATUS _LED, OUT)	GPIO1	PVDD _1V8	In/Out	Out	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz	High	Yes	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur -able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
	13	GPIO 2/ PS_S TATU S	PS_STA TUS Primary Function: Power Saving status (PS_STA TUS, OUT) enabled by default. Active high.	GPIO2	PVDD _1V8	In/Out	Out	BIDIR	HighZ, 2mA	Highz	Low	Driven by GM02S	Driven by GM02S	High	Yes	
	14	GPIO 28/ DTR0	GPIO28 (See Note 1)	DTR0	PVDD _1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz		No	
	19	GPIO 31/ PWM 0/ PULS E0/ 19M2 _OUT	GPIO31 (See Note 1)	PWM0/ PULSE0/ 19M2_O UT	PVDD _1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	18	GPIO 32/ PWM 1/ PULS E1	GPIO32 (See Note 1)	PWM1/ PULSE1	PVDD _1V8	In/Out	In	BIDIR	HighZ	Highz	Highz	Highz	Highz	High	Yes	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur-able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
	9	GPIO 33/ TX_I ND	TX_IND Primary Function: Transmis sion indicator (TX_IND, OUT). Active high.	GPIO33	PVDD _1V8	In/Out	Out	BIDIR	HighZ, 2mA	Highz	Highz	Low	Low	High	Yes	
	10	GPIO 34/ ANT_ TUNE 0	ANT_TU NE0 Primary Function: Antenna tunning (ANT_TU NE0, OUT)	GPIO34	PVDD _1V8	In/Out	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz		Yes	
	11	GPIO 35/ ANT_ TUNE 1	ANT_TU NE1 Primary Function: Antenna tunning (ANT_TU NE1, OUT)	GPIO35	PVDD _1V8	In/Out	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz		Yes	
	20	RESE RVED / FFF_ FFH	RESERV ED Boot mode selection (FFF_FF H, IN).	N/A	PVDD _1V8	N/A	In	BIDIR	HighZ, 2mA	Highz	Highz	Highz	Highz		Yes	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur-able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
			This pad needs a pull-down resistor by default.													
	15, 17, 53, 74, 75, 76, 77, 94	RESERVED	RESERVED Do not connect	N/A	PVDD_1V8	N/A		BIDIR								
	46	RESETN	EXT_RST_N Module HW reset signal. Active low. This pin has an internal pull-up.	N/A	PMU_5V	In	In	IN	In, Pull-up	Highz	Highz	Highz	Highz	Low	No	pull-up
	16	RING0	RING0 UART0 ring line (RING0, OUT). Enabled by	N/A	PVDD_1V8	In/Out	Out	BIDIR	HighZ, 2mA	Highz	High	Driven by GM02S	Driven by GM02S	Low	Yes	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur -able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
			default with inversed polarity.													
	48	WAKE0	WAKE0 Wake #0 input line (WAKE0, IN), disabled by default	N/A	PMU_5V	In	In	IN	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	47	WAKE1	WAKE1, Wake #1 input line (WAKE1, IN), disabled by default.	N/A	PMU_5V	In	In	IN	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	49	WAKE2	WAKE2, Wake #2 input line (WAKE2, IN), diabled by default.	N/A	PMU_5V	In	In	IN	HighZ	Highz	Highz	Highz	Highz	High	Yes	
	55	WAKE3	WAKE3, Wake #3 input line (WAKE3, IN), diabled	N/A	PMU_5V	In	In	IN	HighZ	Highz	Highz	Highz	Highz	High	Yes	

Function Enabled	Function Disabled

	Pad #	Pad Name	Primary Function	Alternate Function	Power Group	Direction capability	Direction set after boot up	Pad type	State @reset	State @ deep-sleep	State @sleep	State @standby	State @active	Active Logical Level	Configur-able by AT+SQN HWCFG	Is internal Pull-up or Pull-down set ?
			by default.													
	57	WAKE4	WAKE4, Wake #4 input line (WAKE4, IN), diabled by default.	N/A	PMU_5V	In	In	IN	HighZ	Highz	Highz	Highz	Highz	High	Yes	
JTAG	69	JTAG_TCK	JTAG_TCK	N/A	PVDD_1V8	In	In	IN	In Pull-down Schmitt-trigger	Highz	Highz	Highz	Highz		No	pull-down
	67	JTAG_TDI	JTAG_TDI	N/A	PVDD_1V8	In	In	IN	In, Pull-up	Highz	Highz	Highz	Highz		No	pull-up
	68	JTAG_TDO	JTAG_TDO	N/A	PVDD_1V8	Out	Out	BIDIR	Out, 0	Highz	Highz	Highz	Highz		No	
	66	JTAG_TMS	JTAG_TMS	N/A	PVDD_1V8	In	In	IN	In, Pull-up	Highz	Highz	Highz	Highz		No	pull-up
	70	JTAG_TRSTN	JTAG_TRSTN	N/A	PVDD_1V8	In	In	IN	In, Pull-down	Highz	Highz	Highz	Highz		No	pull-down

Revision History

Rev.	Date	Description	
		Page	Summary
0.90	Aug.9.21	—	Initial version
0.95	May.25.22	—	Updated
0.96	Sep.20.22	—	Updated

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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