General Description

The DA16600 series is a highly integrated ultra-low power Wi-Fi +BLE Combo Module solution. This module includes the DA16200 which contains an 802.11b/g/n radio (PHY), a baseband processor, a media access controller (MAC), on-chip memory, and a host networking application processor. It also has a DA14531 which contains a 2.4 GHz transceiver and an Arm® Cortex-M0+® microcontroller with a RAM of 48 kB and a One-Time Programmable (OTP) memory of 32 kB.
The radio transceiver, the baseband processor, and the qualified Bluetooth® low energy stack is fully compliant with the Bluetooth® Low Energy 5.1 standard.

The DA16600 is a synthesis of breakthrough ultra-low power technologies, which enables extremely low power operation in the module. The DA16200 and DA14531 shut down every micro element of the chip that is not in use, which allows a near zero level of power consumption when not actively transmitting or receiving data. Such low power operation can extend the battery life up to a year or more depending on the application. The DA16600 also enables ultra-low power transmission and reception modes when the SoC needs to be awake to exchange information with other devices. Advanced algorithms enable sleep mode until the exact moment when wake up is required to transmit or receive data.

Module Features

- Module Variants
  - DA16600MOD-AAC4WA32 (Chip Antenna)
  - DA16600MOD-AAE4WA32 (u.FL Connector)
- Dimensions
  - 14.3 mm × 24.3 mm × 3.0 mm, 51-Pins
- Operating temperature range
  - -40 °C to 85 °C

Wi-Fi Features

- Highly integrated ultra-low power Wi-Fi® system on chip
  - Sleep current: 3.5 uA, VBAT=3.3 V
- Best RF Performance
  - Tx Power: +18 dBm, 1 Mbps DSSS
  - Rx Sensitivity: -97.5 dBm, 1 Mbps DSSS
- Full offload: SoC runs full networking OS and TCP/IP stack
- Hardware accelerators
  - General HW CRC engine
  - HW zeroing function for fast booting
  - Pseudo random number generator (PRNG)
- Complete software stack
  - Comprehensive networking software stack
  - Provides TCP/IP stack: in the form of network socket APIs
- Built-in 4-channel auxiliary ADC for sensor interfaces
  - 12-bit SAR ADC: single-ended four channels
  - Provides dynamic auto switching function
- Wi-Fi processor
  - IEEE 802.11b/g/n, 20 MHz channel bandwidth, 2.4 GHz
  - IEEE 802.11s Wi-Fi mesh
  - Wi-Fi security: WPA/WPA2-Enterprise/Personal, WPA2 SI, WPA3 SAE, and OWE
  - Vendor EAP types: EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1, EAP-FAST, and EAP-TLS
  - Operating modes: Station, SoftAP, and Wi-Fi Direct® Modes (GO, GC, GO fixed)
  - WPS-PIN/PBC for easy Wi-Fi provisioning
  - Connection manager for autonomous and fast Wi-Fi connections

- CPU core subsystem
  - Arm® Cortex®-M4F core w/ clock frequency of 30~160 MHz
  - ROM: 256 KB, SRAM: 512 KB, OTP: 8 KB, Retention Memory: 48 KB
- Advanced security
  - Secure booting
  - Secure debugging using JTAG/SWD and UART ports
  - Secure asset storage
- Built-in hardware crypto engines for advanced security
  - TLS/DTLS security protocol functions
  - Crypto engine for key deliberate generic security functions: AES (128,192,256), DES/3DES, SHA1/224/256, RSA, DH, ECC, CHACHA, and TRNG
- Power management unit
  - On-Chip RTC
  - Wake-up control of fast booting or full booting with minimal initialization time
  - Supports three ultra-low power sleep modes
- Supports various interfaces
  - QSPI for external flash control
  - Three UARTs
  - SPI Master/Slave interface
  - I2C Master/Slave interface
  - I2S for digital audio streaming
  - 4-channel PWM
  - Individually programmable, multiplexed GPIO pins
  - JTAG and SWD
- SPI flash Memory
  - 32 M-bit / 4 M-byte
- Regulatory certifications: *(will be progress)*
  - FCC
  - IC
  - CE
- Supply
  - Operating voltage: 2.1 V to 3.6 V (typical: 3.3 V)
  - 2 Digital I/O Supply Voltage: 1.8 V / 3.3 V
  - Black-out and brown-out detector

Bluetooth Features

- Compatible with Bluetooth V5.1, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
- Supports up to three BLE connections
- Typical cold boot to radio active 35 ms
- Processing power
  - 16 MHz 32-bit Cortex-M0+ with SWD interface
  - Dedicated Link Layer Processor
  - AES-128 encryption Processor
  - Software based certified True Random Number Generator (TRNG)
- Memories
  - 32 kB One-Time-Programmable (OTP)
  - 48 kB Retainable System RAM
  - 144 kB ROM
- Power management
  - Integrated Buck/Boost DCDC converter
  - Buck: 1.8 V $\leq V_{BAT\_HIGH} \leq$ 3.3 V if OTP read needed
  - Buck: 1.1 V $\leq V_{BAT\_HIGH} \leq$ 3.3 V if RAM retained
  - Clock-less Hibernation mode of 270 nA
  - 10-bit ADC for battery voltage monitoring
  - Built-in temperature sensor for die temperature monitoring
- Digital controlled oscillators
  - 32 MHz crystal and 32 MHz RC oscillator
  - 32 kHz crystal and 32/512 kHz RC oscillator
- 15 kHz RCX as 32 kHz crystal replacement
- Programmable Reset Circuitry
- 2 x General purpose Timers with capture and PWM capabilities

- Digital interfaces
  - UART
  - SPI Master/Slave up to 32 MHz (Master)
  - I2C bus at 100 kHz, 400 kHz
  - 3-axis capable Quadrature Decoder
  - Keyboard controller
- Analog interfaces
  - 4-channel 10-bit ADC
- Radio transceiver
  - Fully integrated 2.4 GHz CMOS
  - transceiver
  - Single wire antenna
  - TX: 3.5 mA, RX: 2.2 mA (system currents with DC-Dc, V_{BAT_HGH} = 3V and 0 dBm)
  - Programmable transmit output power from
  - -20 dBm to +2.0 dBm
  - -93.5 dBm receiver sensitivity

Contents

Figures

Tables

1 References

DA16600MOD consist of DA16200 and DA14531 chipset, please refer to the chipset datasheet for details.

[1] DA16200_Datasheet

[2] DA14531_Datasheet

3 Pinout

3.1 Pin-out Description (51-pins)

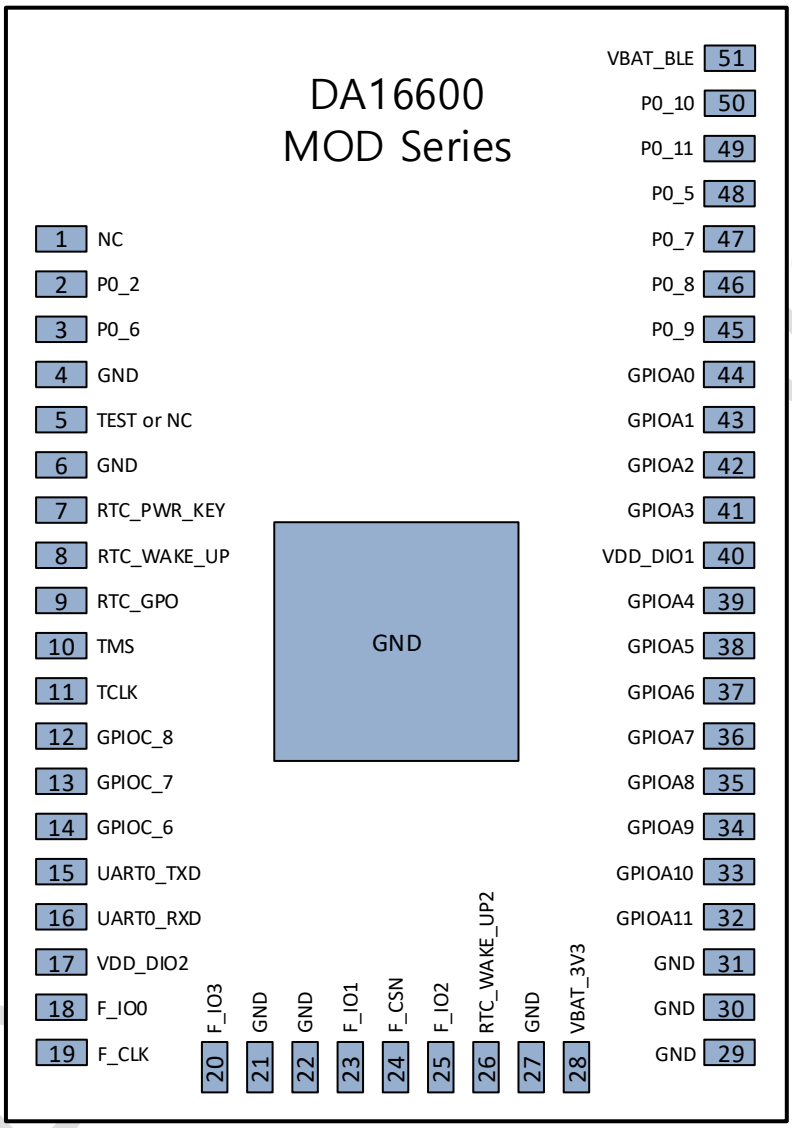


Figure 2: DA16600MOD 51-pins Pin-out Diagram (Top View)

Table 1: Pin Description

#Pin	Pin Name	Type	Drive(mA)	Reset State	Related chipset	Description
1	NC	AI			DA14531	Not Connect
2	P0_2	DIO			DA14531	
3	P0_6	DIO			DA14531	Internally connected to RF switch
4	GND	GND			Common	Ground
5	TEST or NC	AI			Common	Chip antenna type : RF_Test u.FL connector type : NC
6	GND	GND			Common	Ground
7	RTC_PWR_KEY	DI			DA16200	RTC block enable signal
8	RTC_WAKE_UP	DI			DA16200	RTC block wake-up signal
9	RTC_GPO	DO			DA16200	Sensor control signal
10	TMS	DIO	2/4/8/12	I-PU	DA16200	JTAG I/F , SWDIO
11	TCLK	DIO	2/4/8/12	I-PD	DA16200	JTAG I/F , SWCLK ,General Purpose I/O
12	GPIOC_8	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
13	GPIOC_7	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
14	GPIOC_6	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
15	UART0_TXD	DO	2/4/8/12	O	DA16200	UART Transmit data
16	UART0_RXD	DI	2/4/8/12	I	DA16200	UART Receive data
17	VDD_DIO2	VDD			DA16200	Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
18	F_IO0	DIO			DA16200	Internally connected to Flash Memory
19	F_CLK	DIO			DA16200	Internally connected to Flash Memory
20	F_IO3	DIO			DA16200	Internally connected to Flash Memory
21	GND	GND			Common	
22	GND	GND			Common	
23	F_IO1	DIO			DA16200	Internally connected to Flash Memory
24	F_CSN	DIO			DA16200	Internally connected to Flash Memory
25	F_IO2	DIO			DA16200	Internally connected to Flash Memory
26	RTC_WAKE_UP2	DI			DA16200	RTC block wake-up signal
27	GND	GND			Common	
28	VBAT_3V3	VDD			DA16200	Supply power for internal DC-DC, DIO_LDO,and analog IP of DA16200
29	GND	GND			Common	
30	GND	GND			Common	
31	GND	GND			Common	
32	GPIOA11	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
33	GPIOA10	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
34	GPIOA9	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
35	GPIOA8	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
36	GPIOA7	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O

#Pin	Pin Name	Type	Drive(mA)	Reset State	Related chipset	Description
37	GPIOA6	DIO	2/4/8/12	I-PD	DA16200	General Purpose I/O
38	GPIOA5	DIO	2/4/8/12	I-PD	DA16200	Internally connected to P0_3 of DA14531
39	GPIOA4	DIO	2/4/8/12	I-PD	DA16200	Internally connected to P0_4 of DA14531
40	VDD_DIO1	VDD			DA16200	Supply power for digital I/O GPIOA0~GPIOA11
41	GPIOA3	AI/DIO	2/4/8/12	I-PD	DA16200	Aux.ADC input/General Purpose I/O
42	GPIOA2	AI/DIO	2/4/8/12	I-PD	DA16200	Aux.ADC input/General Purpose I/O
43	GPIOA1	AI/DIO	2/4/8/12	I-PD	DA16200	Internally connected to P0_0 of DA14531
44	GPIOA0	AI/DIO	2/4/8/12	I-PD	DA16200	Internally connected to P0_1 of DA14531
45	P0_9	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
46	P0_8	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
47	P0_7	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
48	P0_5	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
49	P0_11	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
50	P0_10	DIO	3.5 / 0.3	I-PD	DA14531	General Purpose I/O
51	VBAT_BLE	VDD			DA14531	Supply power for DA14531

Note 1 Pin 38,Pin 39 , Pin 43 , and Pin 44 are connected internally so it is not possible to use GPIO in application system

4 Electrical Specification

4.1 Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Parameter	#Pins	Min	Max	Units
VBAT_3V3	28	VSS	3.9	V
VDD_DIO1	40	VSS	3.9	V
VDD_DIO2	17	VSS	3.9	V
VBAT_BLE	51	-0.2	3.6	V
Operating temperature range (TA)		-40	+85	°C

4.2 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	#Pins	Min	Typ	Max	Units
VBAT_3V3	28	2.1		3.6	V
VDD_DIO1	40	1.62		3.6	V
VDD_DIO2	17	1.62		3.6	V
VBAT_BLE	51	1.1		3.3	V
Operating temperature range (TA)		-40		+85	°C

4.3 Electrical Characteristics

4.3.1 DC Parameters, 1.8V IO

Table 4: DC Parameters, 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3 × DVDD	V
Input High Voltage	V_{IH}	Guaranteed logic High level	0.7 × DVDD		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.2 × DVDD	V
Output High Voltage	V_{OH}	DVDD=Min.	0.8 × DVDD		DVDD	V
Pull-up Resistor	R_{PU}	V_{PAD}=V_{IH}, DIO=Min.			32.4	kΩ
Pull-down Resistor	R_{PD}	V_{PAD}=VIL, DIO=Min.			32.4	

Note 1 DVDD = 1.8V, VDD_DIO1, VDD_DIO2 Logic Level

4.3.2 DC Parameters, 3.3V IO

Table 5: DC Parameters, 3.3V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.8	V
Input High Voltage	V_{IH}	Guaranteed logic High level	2.0		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.4	V
Output High Voltage	V_{OH}	DVDD=Min.	2.4		DVDD	V
Pull-up Resistor	R_{PU}	VPAD=VIH, DIO=Min.			19.4	kΩ
Pull-down Resistor	R_{PD}	V_{PAD}=V_{IL}, DIO=Min.			16.0	

Note 1 DVDD= 3.3 V, VDD_DIO1, VDD_DIO2 Logic Level

4.4 Radio Characteristics

4.4.1 WLAN Characteristics

TA = +25 °C, VBAT = 3.3 V , CH1 (2412MHz)

Table 6: WLAN Receiver Characteristics

Parameter	Condition	Min	Typ	Max	Units
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)	1 Mbps DSSS	-98.5	-97.5	-95.5	dBm
	2 Mbps DSSS	-94	-93	-91	
	11 Mbps CCK	-89	-88	86	
	6 Mbps OFDM	-90	-89	-87	
	9 Mbps OFDM	-90	-89	-87	
	18 Mbps OFDM	-88	-87	-85	
	36 Mbps OFDM	-81	-80	-78	
	54 Mbps OFDM	-75	-74	-72	
	MCS0(GF)	-90	-89	-87	
	MCS7(GF)	-72	-71	-69	
Maximum input level (8% PER for 11b rates, 10% PER for 11g/11n rates)	802.11b	-4	0	0	
	802.11g	-10	-4	-3	

Table 7: WLAN Transmitter Characteristics

Parameter	Condition	Min	Typ	Max	Units
Maximum Output Power measured form IEEE spectral mask and EVM	1 Mbps DSSS	15.5	18	19	dBm
	2 Mbps DSSS	15.5	18	19	
	5.5 Mbps CCK	15.5	18	19	
	11 Mbps CCK	15.5	18	19	
	6 Mbps OFDM	14.5	17	18	
	9 Mbps OFDM	14.5	17	18	
	12 Mbps OFDM	14.5	17	18	
	18 Mbps OFDM	14.5	17	18	
	24 Mbps OFDM	13.5	16	17	
	36 Mbps OFDM	13.5	16	17	
	48 Mbps OFDM	12	14.5	15.5	
	54 Mbps OFDM	11	13.5	14.5	
	MCS0 OFDM	14.5	17	18	
	MCS7 OFDM	11	13.5	14.5	
Transmit center frequency accuracy		-25		+25	ppm

4.4.2 BLE Characteristics

Table 8: BLE 1Mb/s specifications – AC Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
P_{SENS_CLEAN}	sensitivity level	Dirty Transmitter disabled; DC-DC converter disabled; PER = 30.8 %; Note 1		-93		dBm
P_{SENS_EPKT}	sensitivity level	Extended packet size (255 octets) Note 1		-89.5		dBm
P_{SENS}	sensitivity level	Normal Operating Conditions; DC-DC converter disabled; PER = 30.8 %; Note 1		-92		dBm
P_{SENS_EOC}	sensitivity level	Extreme Operating Conditions; DC-DC converter enabled; PER = 30.8 %; -40 °C ≤ T_A ≤ +85 °C Note 1			-89	dBm
$P_{SENS\_EPK\_TCLEAN}$	sensitivity level	Dirty Transmitter disabled; DC-DC converter disabled; Extended packet size (255 octets) Note 1		-90.5		dBm
P_{I_MAX}	maximum input power level	DC-DC converter disabled; PER = 30.8 %; Note 1	0			dBm
P_{INT_IMD}	intermodulation distortion interferer power level	worst-case interferer level @ f_1, f_2 with $2*f_1 - f_2 = f_0$, $\|f_1 - f_2\|$ = n MHz and n = 3, 4, 5; P_{WANTED} = -64 dBm @ f_0; PER = 30.8 %; Note 1	-35	-20.5		dBm
CIR_0	carrier to interferer ratio	n = 0; interferer @ $f_1 = f_0 + n*1$ MHz; Note 1		7.5	21	dB
CIR_1	carrier to interferer ratio	n = ±1; interferer @ $f_1 = f_0 + n*1$ MHz; Note 1		-1.5	15	dB
CIR_{P2}	carrier to interferer ratio	n = +2 (image frequency); interferer @ f_1 = f0 + n*1 MHz; Note 1		-27	-9	dB
CIR_{M2}	carrier to interferer ratio	n = -2; interferer @ $f_1 = f_0 + n*1$ MHz; Note 1		-31	-17	dB

Parameter	Description	Condition	Min	Typ	Max	Unit
CIR_{P3}	carrier to interferer ratio	n = +3 (image frequency + 1 MHz); interferer @ $f_1 = f_0 + n*1$ MHz; Note 1		-37.5	-15	dB
CIR_{M3}	carrier to interferer ratio	n = -3; interferer @ $f_1 = f_0 + n*1$ MHz; Note 1		-43	-27	dB
CIR_4	carrier to interferer ratio	|n| ≥ 4 (any other B channel); interferer @ $f_1 = f_0 + n*1$ MHz; Note 1		-41.5	-27	dB
P_{BL_I}	blocker power level	30 MHz ≤ f_{BL} ≤ 2000 MHz; P_{WANTED} = -67 dBm; Note 1	-17	5		dBm
P_{BL_II}	blocker power level Note 2	2003 MHz ≤ f_{BL} ≤ 2399 MHz; P_{WANTED} = -67 dBm; Note 1	-17	0		dBm
P_{BL_III}	blocker power level	2484 MHz ≤ f_{BL} ≤ 2997 MHz; P_{WANTED} = -67 dBm; Note 1	-17	0		dBm
P_{BL_IV}	blocker power level	3000 MHz ≤ f_{BL} ≤ 12.75 GHz; P_{WANTED} = -67 dBm; Note 1	-17	5		dBm
L_{ACC_RSSI}	level accuracy	tolerance at 5 % to 95 % confidence interval of P_{RF}: when RXRSSI[7:0] = X, 50 < X < 175; burst mode, 1500 packets;		0	3	dB
L_{RES_RSSI}	level resolution	gradient of monotonous range for RXRSSI[7:0] = X, 50 < X < 175; burst mode, 1500 packets;		0.5		dB/LSB
ACP_{2M}	adjacent channel power level	f_{OFS} = 2 MHz; Note 1		-53		dBm
ACP_{2M_EOC}	adjacent channel power level	Extreme Operating Conditions; f_{OFS} = 2 MHz; -40 °C ≤ TA ≤ +85 °C Note 1		-53	-47	dBm
ACP_{3M}	adjacent channel power level	f_{OFS} ≥ 3 M ; Note 1		-57		dBm
ACP_{3M_EOC}	adjacent channel power level	Extreme Operating Conditions; f_{OFS} ≥ 3 M ; -40 °C ≤ TA ≤ +85 °C Note 1		-57	-47	dBm

Parameter	Description	Condition	Min	Typ	Max	Unit
P_{O_12}	output power level	RF_ATTR_REG [PA_POWE _SETTING]= 12		2.5		dBm
P_{O_11}	output power level	RF_ATTR_REG [PA_POWE _SETTING]= 11		1.5		dBm
P_{O_10}	output power level	RF_ATTR_REG [PA_POWE _SETTING]= 10		1		dBm
P_{O_09}	output power level	RF_ATTR_REG [PA_POWE _SETTING]= 9		0		dBm
P_{O_08}	output power level	RF_ATTR_REG [PA_POWE _SETTING]= 8		-1		dBm
P_{O_07}	output power level	RF_ATTR_REG [PA_POWE _SETTING]= 7		-2		dBm
P_{O_06}	output power level	RF_ATTR_REG [PA_POWER_SETTING]= 6		-3.5		dBm
P_{O_05}	output power level	RF_ATTR_REG [PA_POWER _SETTING]= 5		-5		dBm
P_{O_04}	output power level	RF_ATTR_REG [PA_POWER _SETTING]= 4		-7		dBm
P_{O_03}	output power level	RF_ATTR_REG [PA_POWER _SETTING]= 3		-10		dBm
P_{O_02}	output power level	RF_ATTR_REG [PA_POWER_SETTING]= 2		-13.5		dBm
P_{O_01}	output power level	RF_ATTR_REG [PA_POWER_SETTING]= 1		-19.5		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/5.1.0

Note 2 Frequencies close to the ISM band can show slightly worse performance

4.5 Current Consumption

4.5.1 WLNA Characteristics

TA = +25 °C, VBAT = 3.3 V, w/ CPU clock is 80 MHz.

Table 9: Current Consumption in Active State

Parameter	Condition			Min	Typ	Max	Units
ACTIVE	TX	1 Mbps DSSS	@ 18.0 dBm	260	280	320	mA
		6 Mbps OFDM	@ 17.0 dBm	240	260	300	
		54 Mbps OFDM	@ 13.5 dBm	180	200	240	
		MCS7	@ 13.5 dBm	180	200	240	
	RX	No signal Note		25	29	51	
		1 Mbps DSSS Note 1		26.5	30.5	53	
		1 Mbps DSSS		27	37.5	54	
		54 Mbps OFDM		29	38.5	54	
		MCS7		29	38.5	54	

Note 1 Low Power Mode& CPU clock 30 MHz

TA = +25 °C, VBAT = 3.3 V

Table 10: Current Consumption in Low Power Operation

Parameter	Condition	Min	Typ	Max	Units
Low Power Operation	Sleep 1		0.2		µA
	Sleep 2		1.8		
	Sleep 3		3.5		

4.5.2 BLE characteristics

Table 11: BLE 1Mb/s specifications - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
$I_{BAT\_RF\_RX}$	Current at V_{BAT_LOW} = 1.1 V	radio receiver and synthesizer active; T_A = 25 °C		4.3		mA
$I_{BAT\_RF\_TX\_12}$	Current at V_{BAT_LOW} = 1.1 V	radio transmitter and synthesizer active; power setting = 12; P_{OUT}= 2.5dBm; T_A = 25 °C		7.9		mA
$I_{BAT\_RF\_TX\_9}$	Current at V_{BAT_LOW} = 1.1 V	radio transmitter and synthesizer active; power setting = 9; P_{OUT} = 0 dBm; T_A = 25 °C		6.9		mA
$I_{BAT\_RF\_TX\_6}$	Current at V_{BAT_LOW} = 1.1 V	radio transmitter and synthesizer active; power setting = 6; P_{OUT} = -3.5dBm; T_A = 25 °C		5.7		mA

4.6 Radiation Performance

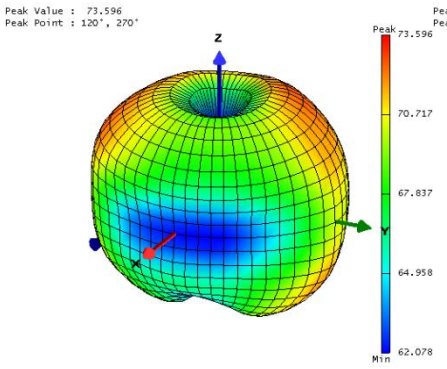


Figure 3: TIS 3D

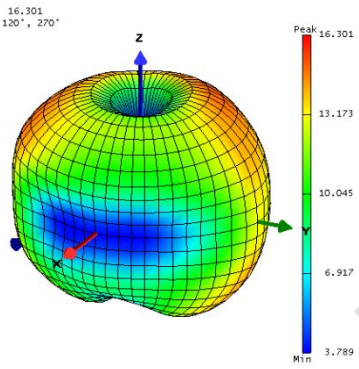


Figure 4: TRP 3D

4.7 ESD Ratings

Table 12: ESD performance

Reliability Test	Standards	Test Conditions	Result
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001-2017	± 2,000 V	Pass
Charge Device Mode (CDM)	ANSI/ESDA/JEDEC JS-002-2018	± 500 V	Pass

6 Package Information

6.1 Dimension: DA16600MOD-AAC

Unit: millimeters (mm)

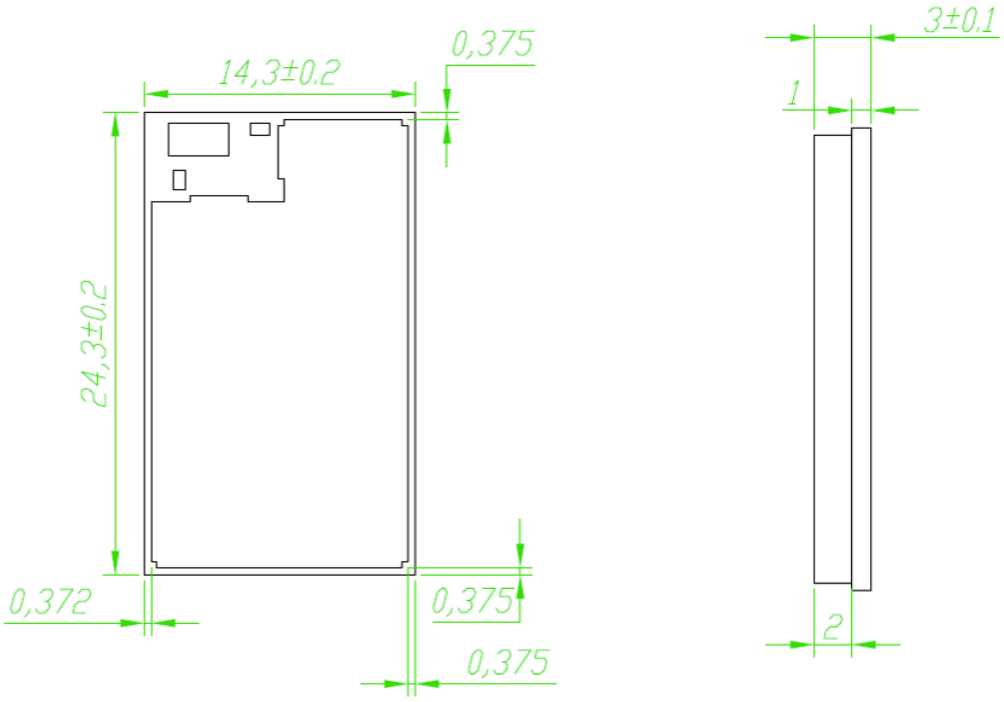


Figure 6: Module Top

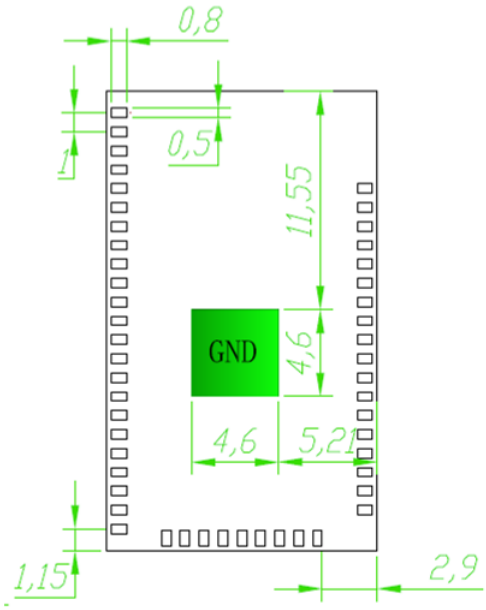


Figure 7: Module Bottom Top-View

6.2 Dimension: DA16600MOD-AAE

Unit: millimeters (mm)

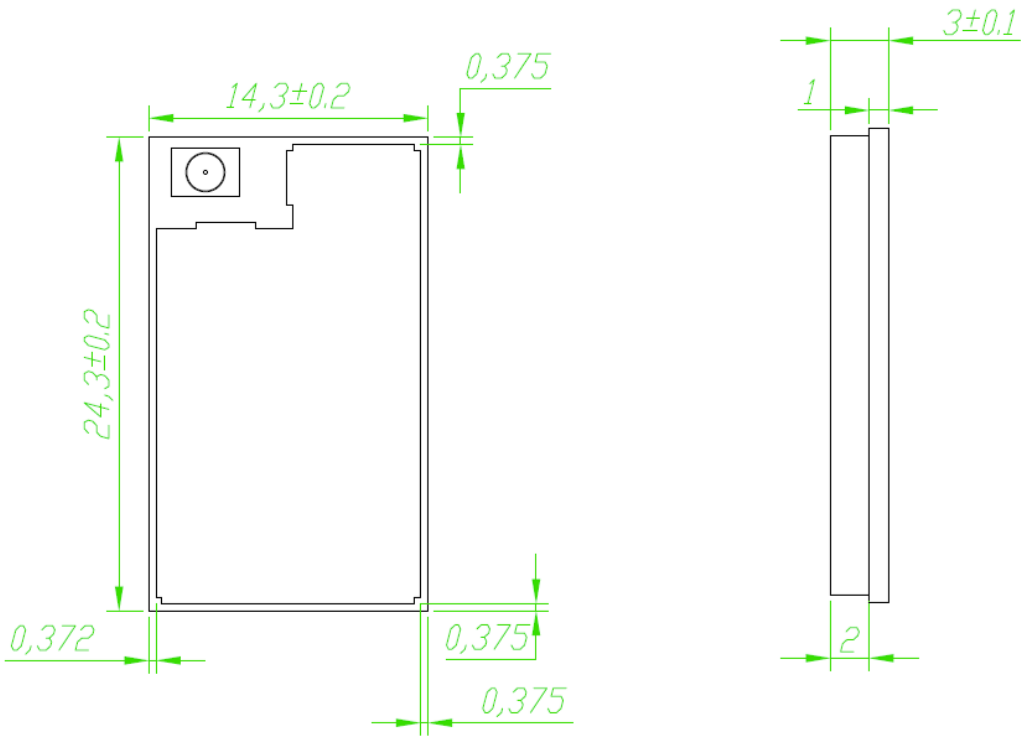


Figure 8: Module Top

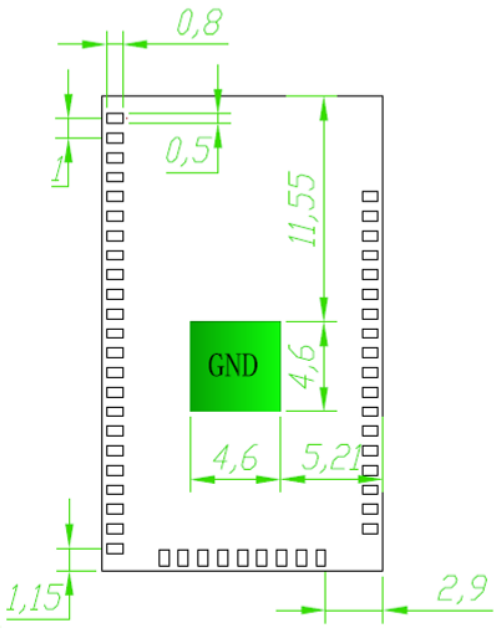
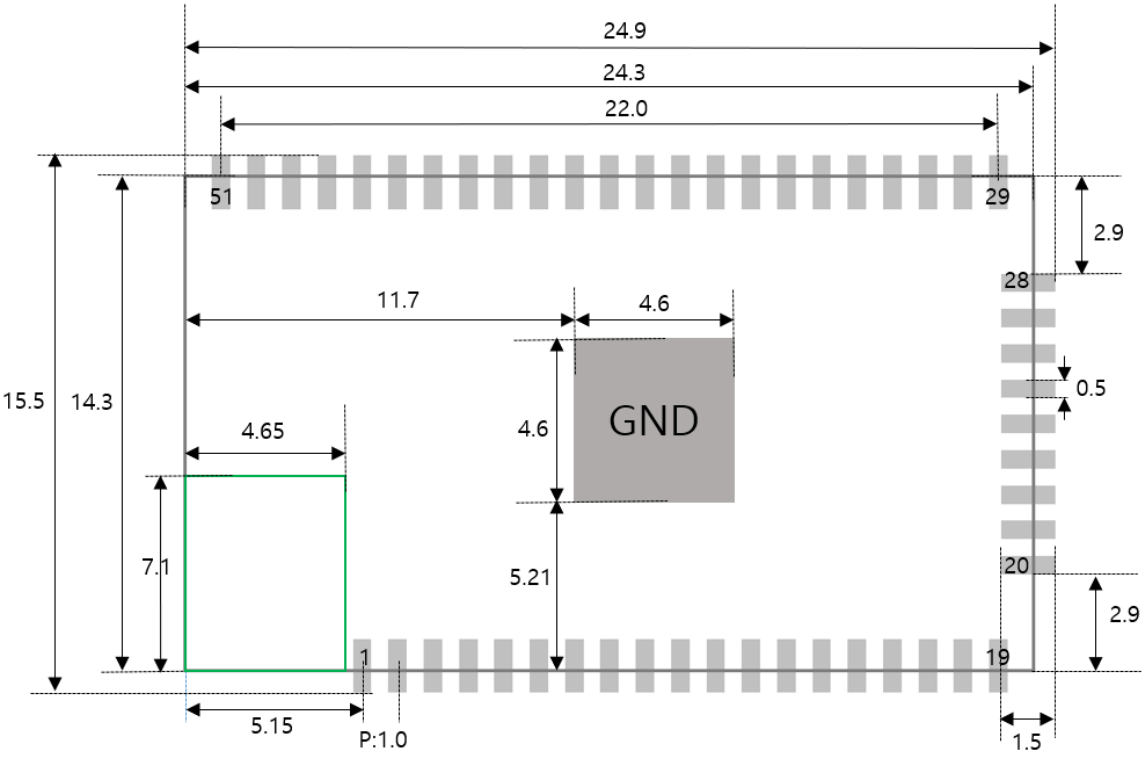


Figure 9: Module Bottom Top-View

6.3 PCB Land Pattern

Unit: millimeters (mm)



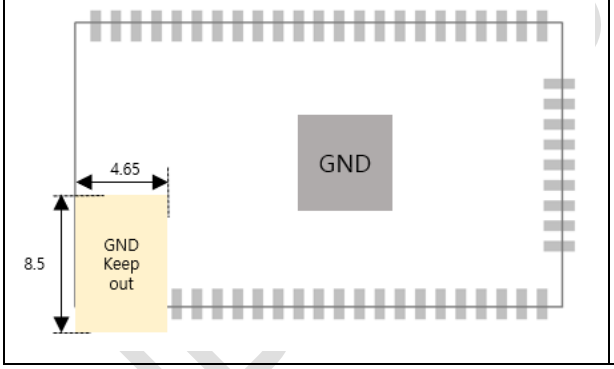
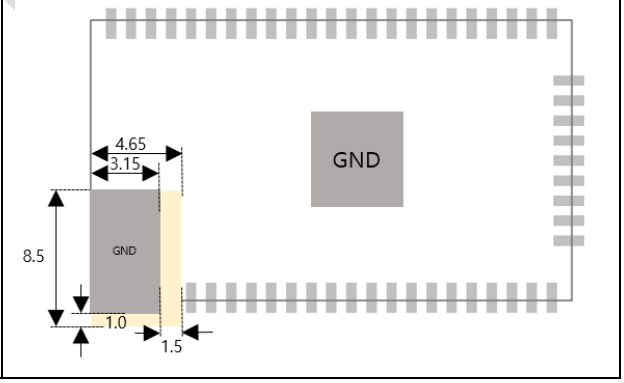
Top and Inner layer keep out area	Bottom layer keep out area
	

Figure 10: PCB Land Pattern (Top View)

6.4 Soldering Information

6.4.1 Recommended Condition for Reflow Soldering

Figure 11 shows the typical process flow for mounting surface mount packages to PCB.

The reflow profile depends on the solder paste being used and the recommendations from the paste manufacture should be followed to determine the proper reflow profile. Figure 11 shows a typical reflow profile when a no-clean paste is used. Oven time above liquidus (260 °C for lead-free solder) is 20 to 40 seconds.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste application
4. Component placement
5. Component attachment

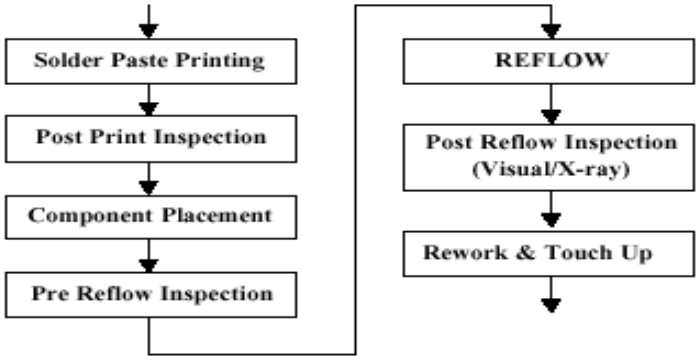


Figure 11: Typical PCB Mounting Process Flow

Table 14: Typical Reflow Profile (Lead Free): J-STD-020C

Profile Feature	Lead Free SMD
Average ramp up rate (Ts_{max} to T_p)	3 °C/s Max.
Preheat	
• Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (Ts_{max} to Ts_{min})	• 150 °C • 200 °C • 60 to 180 seconds
Time maintained above	
• Temperature (T_L) • Time (t_L)	• 217 °C • 60 to 150 seconds
Peak/Classification temperature (T_p)	260 °C
Time within 5 °C of peak temperature (tp)	20 to 40 seconds
Ramp down rate	6 °C/s Max.
Time from 25 °C to peak temperature	8 minutes Max.

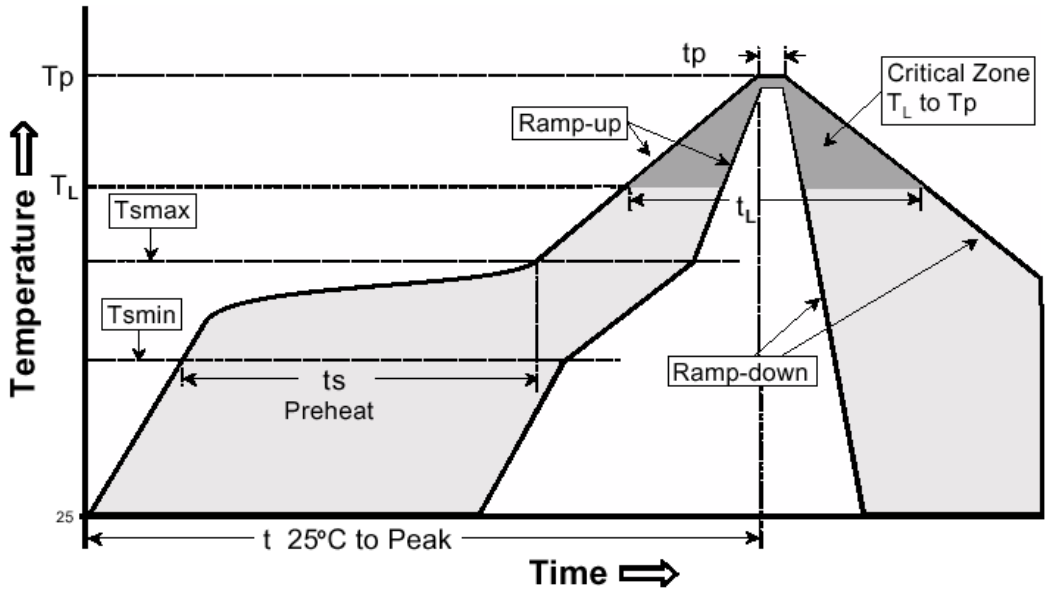


Figure 12: Reflow Condition

7 Ordering Information

The order number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer support portal or your local sales representative.

Table 15: Ordering Information (Samples)

Part Number	Pins	Size (mm)	Shipment Form	Pack Quantity
DA16600MOD-AAC	51	14.2 x 24.6 x 3.0	Reel	
DA16600MOD-AAE	51	14.2 x 24.6 x 3.0	Reel	

Table 16: Ordering Information (Production)

Part Number	Pins	Size (mm)	Shipment Form	Pack Quantity
DA16600MOD-AAC	51	14.2 x 24.6 x 3.0	Reel	500
DA16600MOD-AAE	51	14.2 x 24.6 x 3.0	Reel	500

Part Number Legend:

DA16600MOD-AAC4WA32

AA: Module revision number

C: Select module type

[C] Chip antenna, [E] u.FL connector

4: Flash memory

[4] 4Mbyte, [2] 2Mbyte

W: Voltage range

[W] 3.3 V, [L] 1.8 V

A3: Package No.

2: T&R packing

Revision History

Revision	Date	Description
1.3	15-July-2020	Modified application schematic
1.2	22-May-2020	Added ESD performance, Table 122
1.1	29-April-2020	Preliminary datasheet

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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2.2 List of applicable FCC rules
CFR 47 FCC PART 15 SUBPART C has been investigated. It is applicable to the modular Transmitter

2.3 Specific operational use conditions
This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module man

2.4 Limited module procedures
Single modular Approval.

2.5 Trace antenna designs
Not applicable

2.6 RF exposure considerations
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

2.7 Antennas
This radio transmitter 2AU49-DA16600ME has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Operating frequency band	Antenna type	Maximum Antenna gain
2000-2500Mhz	ExternalAntenna	2dbi

2.8 Label and compliance information
The final end product must be labeled in a visible area with the following" Contains FCC ID: 2AU49-DA16600ME.

2.9 Information on test modes and additional testing requirements
Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

2.10 Additional testing, Part 15 Subpart B disclaimer
Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B.

FCC Warning

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any inte rference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interferenceto radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

ISED Statement

- English: This device complies with Industry Canada license‑exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause interference, and (2) This device must accept any interference, including interference that may cause undesired operation of the device. The digital apparatus complies with Canadian CAN ICES‑3 (B)/NMB‑3(B).
- French: Le présentappareilestconforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitationestautorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareildoit accepter tout brouillageradioélec triquesubi, mêmesi le brouillageest susceptible d'encompromettre le fonctionnement.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.