General Description

The DA16200MOD-AA series is a fully integrated Wi-Fi® module with ultra-low power consumption, best RF performance and easy development environment. Such low power operation can extend the battery life as long as a year or more depending on the application.

This series included DA16200 SoC, 40MHz crystal oscillator, 32.768KHz RTC clock, RF Lumped RF filter, flash memory and chip antenna or u.FL connector. The DA16200MOD-AA series has chip antenna type (DA16200MOD-AAC4WA32) and u.FL connector type (DA16200MOD-AAE4WA32) for external antenna.

The DA16200 SoC is a highly integrated ultra-low power Wi-Fi system on a chip (SoC), which contains an 802.11b/g/n radio (PHY), a baseband processor, a media access controller (MAC), on-chip memory, and a host networking application processor, all on a single silicon die.

The SoC is built from the ground up for the “Internet of Things” and is ideal for wearables, door locks, home appliances, sprinkler systems, thermostats, connected lighting, drop-in video cameras, and other devices that comprise the "Connected Home".

The modules certified Wi-Fi alliance for IEEE802.11b/g/n, Wi-Fi Direct, WPS functionalities and also received regulatory approval in the United States (FCC) and Canada (IC). Using the Wi-Fi Alliance transfer policy, the Wi-Fi Certifications can be transferred without being tested again.

Key Features

- Module variants
  - DA16200MOD-AAC (chip Antenna)
  - DA16200MOD-AAE (u.FL connector)
- Highly integrated ultra-low power Wi-Fi® system on chip
  - Sleep current: 2.9uA, VBAT=3.3V
- Best RF Performance
  - Tx Power: +19dBm, 1Mbps DSSS
  - Rx Sensitivity: -98.5dBm, 1Mbps DSSS
- Full offload: SoC runs full networking OS and TCP/IP stack
- Wi-Fi processor
  - IEEE 802.11b/g/n, 1×1 MIMO, 20MHz channel bandwidth, 2.4GHz
  - IEEE 802.11s Wi-Fi mesh
  - Wi-Fi security: WPA/WPA2-Enterprise/Personal, WPA2 SI, WPA3 SAE, and OWE
  - Vendor EAP types: EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1, EAP-FAST, and EAP-TLS
  - Operating modes: Station, SoftAP, and Wi-Fi Direct® Modes (GO, GC, GO fixed)
  - WPS-PIN/PBC for easy Wi-Fi provisioning
  - Bluetooth coexistence
  - Antenna switching diversity
- CPU core subsystem
  - ARM Cortex-M4F core w/ clock frequency of 30~160 MHz
  - Embedded Memory
  - ROM: 256KB
  - SRAM: 512KB
  - OTP: 8KB
- Hardware accelerators
  - General HW CRC engine
  - HW zeroing function for fast booting
  - Pseudo random number generator (PRNG)
- Complete software stack
  - Comprehensive networking software stack
  - Provides TCP/IP stack: in the form of network socket APIs
- Advanced security
  - Secure booting
  - Secure debugging about JTAG/SWD and UART ports
  - Secure asset storage
- Built-in hardware crypto engines for advanced security
  - TLS/DTLS security protocol functions
  - Crypto engine for key deliberate generic security functions: AES (128,192,256), DES/3DES, SHA1/224/256, RSA, DH, ECC, CHACHA, and TRNG

- Built-in 4-channel auxiliary ADC for sensor interfaces
  - 12-bit SAR ADC: single-ended four channels
  - Provides dynamic auto switching function
- Supports various interfaces
  - eMMC/SD expanded memory
  - SDIO Host/Slave function
  - QSPI for external flash control
  - Three UARTs
  - SPI Master/Slave interface
  - I2C Master/Slave interface
  - I2S for digital audio streaming
  - 4-channel PWM
  - Individually programmable, multiplexed GPIO pins
  - JTAG and SWD
- Power management unit
  - On-Chip RTC
  - Wake-up control of fast booting or full booting with minimal initialization time
  - Supports three ultra-low power sleep modes
- Regulatory certifications: (in progress)
  - FCC
  - IC
  - CE
  - KC
  - TELEC
  - SRRC
- Supply
  - Operating voltage: 2.1Vto 3.6V (typical: 3.3V)
  - 2 Digital I/O Supply Voltage: 1.8V / 3.3V
  - Black-out and brown-out detector
- Dimensions
  - 13.5mm × 21.5mm x 3.2mm, 37-Pins,
- Operating temperature range
  - -40°C to 85°C

Applications

DA16200MOD is a full offload SoC for IoT Applications, such as:

- Security systems
- Door locks
- Thermostats
- Garage door openers
- Blinds
- Lighting control
- Sprinkler systems
- Video camera security systems
- Smart appliances
- Video door bell

System Diagram

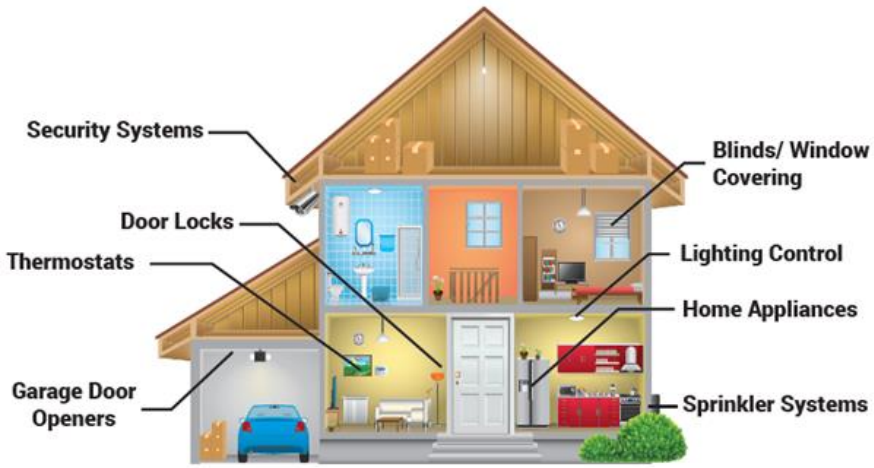

Figure 1: System Diagram

Contents

Figures

Tables

1 Terms and Definitions

API	Application Programming Interface
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
HW	Hardware
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IoT	Internet of Things
JTAG	Joint Test Action Group
LDO	Low-dropout Regulator
LLI	Linked-List Item
NVIC	Nested Vectored Interrupt Contoller
NVRAM	Non-Volatile RAM
PLL	Phase-locked Loop
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
QSPI	Quad-lane SPI
RTC	Real-time Clock
SAR ADC	Successive Approximation Analog-to-Digital Converter
SPI	Serial Peripheral Interface
SW	Software
SWD	Serial Wire Debug
UART	Universal Asynchronous Receivers and Transmitter
XIP	eXecutein Place
TAP	Test Access Port

2 References

[1] ARM Cortex-M4F r0p1 technical reference manual:arm_cortexm4_processor_trm_100166_0001_00_en.pdf

[2] ITU-T O.150, General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment, 1996

[3] Arm® TrustZone® CryptoCell-312, Revision r1p1, Software Integrators Manual

[4] IEEE Standard 1149.1, Test Access Port and Boundary-Scan Architecture

[5] DA16200_SDK_Programmer_Guide.pdf

[6] AMBA AHB bus specification, Rev 3.0

[7] https://static.docs.arm.com/ihi0033/a/IHI0033A_new_eula.pdf?_ga=2.168295970.2050075868.1561605067-2006940633.1551143688

3 Block Diagram

Figure 2 shows the DA16200MOD hardware (HW) block diagram.

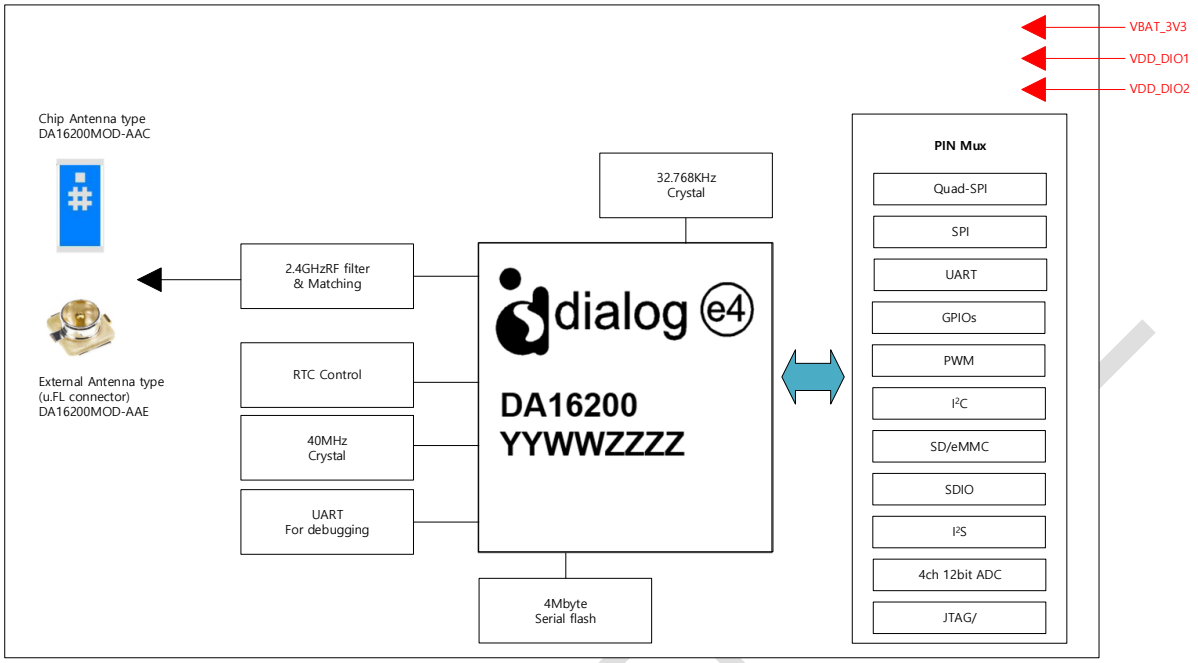

Figure 2: Hardware Block Diagram

Figure 3 shows the DA16200 SoC software (SW) block diagram.

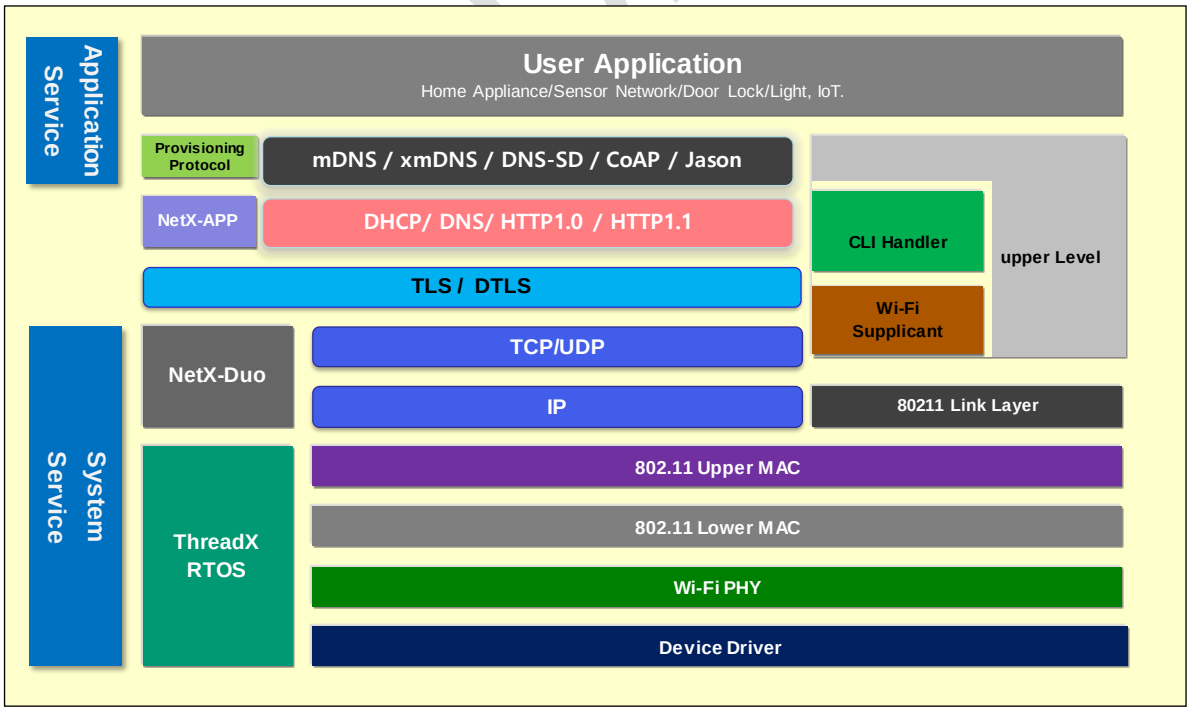

Figure 3: Software Block Diagram

The following descriptions are about the SW block diagrams.

- Kernel layer
  - Real Time Operating System
- The Wi-Fi layer is divided into four layers:
  - Lower MAC
    - SW module to control/handle HW Wi-Fi MAC/PHY and interfaces with Upper MAC layer
  - Upper MAC
    - SW module to control/handle Wi-Fi control/handle to interface with supplicant
    - Wi-Fi Link Layer: Interface layer between Upper MAC and supplicant
    - Supplicant: SW module to control/management to operate Wi-Fi operation
  - Network stack layer
    - Used to control/handle network operation
    - Main protocols are IP, TCP, and UDP
    - Other necessary protocols are supported
  - Security Layer
    - Crypto operation engine is ported to use crypto HW engine
- TLS/TCP and DTLS/UDP APIs are supported to handle security operation:
  - User application layer
    - Variable sample codes are supported in SDK – sample codes use supported APIs
    - TCP Client/Server, UDP Client/Server, TLS Client/Server
    - HTTP/HTTPs download, OTA Update usage, and MQTT usage
    - Applications from other customers can be implemented easily in SDK

4 Pinout

4.1 Pin-out Description (37-pins)

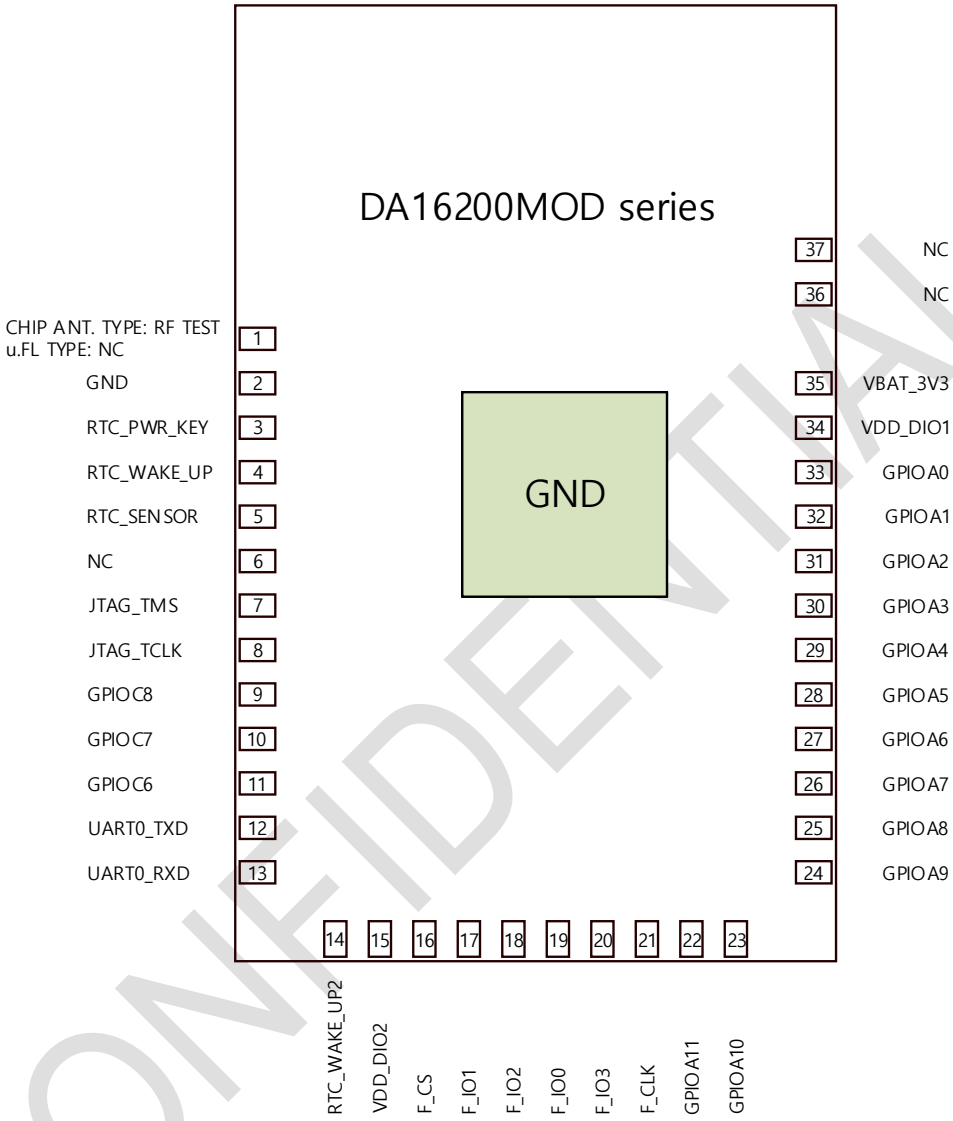

Figure 4: DA16200MOD 37-pins Pin-out Diagram (TopView)

Table 1: Pin Description

#Pin	Pin Name	Type	Drive(mA)	Reset State	Description
1	RT_TEST or NC	AI			Chip antenna type: RF_TEST u.FL connector type: NC
2	GND	GND			RF VDD
3	RTC_PWR_KEY	DI			RTC block enable signal
4	RTC_WAKE_UP	DI			RTC block wake-up signal
5	RTC_SENSOR	DO			Sensor control signal
6	NC	NC			NOT CONNECT
7	JTAG_TMS	DIO	2/4/8/12	I-PU	JTAG I/F, SWDIO
8	JTAG_TCLK	DIO	2/4/8/12	I-PD	JTAG I/F, SWCLK, General Purpose I/O
9	GPIOC8	DIO	2/4/8/12	I-PD	General Purpose I/O
10	GPIOC7	DIO	2/4/8/12	I-PD	General Purpose I/O
11	GPIOC6	DIO	2/4/8/12	I-PD	General Purpose I/O
12	UART_TXD	DO	2/4/8/12	O	UART transmit data
13	UART_RXD	DI	2/4/8/12	I	UART receive data
14	RTC_WAKE_UP2	DI			RTC block wake-up signal
15	VDD_DIO2	VDD			Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
16	F_CSN	DIO			External Flash Memory I/F
17	F_IO1	DIO			External Flash Memory I/F (F_SI)
18	F_IO2	DIO			External Flash Memory I/F (F_WP)
19	F_IO0	DIO			External Flash Memory I/F (F_SO)
20	F_IO4	DIO			External Flash Memory I/F (F_HOLD)
21	F_CLK	DIO			External Flash Memory I/F
22	GPIOA11	DIO	2/4/8/12	I-PD	General Purpose I/O
23	GPIOA10	DIO	2/4/8/12	I-PD	General Purpose I/O
24	GPIOA9	DIO	2/4/8/12	I-PD	General Purpose I/O
25	GPIOA8	DIO	2/4/8/12	I-PD	General Purpose I/O
26	GPIOA7	DIO	2/4/8/12	I-PD	General Purpose I/O
27	GPIOA6	DIO	2/4/8/12	I-PD	General Purpose I/O
28	GPIOA5	DIO	2/4/8/12	I-PD	General Purpose I/O
29	GPIOA4	DIO	2/4/8/12	I-PD	General Purpose I/O
30	GPIOA3	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
31	GPIOA2	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
32	GPIOA1	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
33	GPIOA0	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
34	VDD_DIO1	VDD			Supply power for digital I/O
35	VBAT_3V3	VDD			Supply power for integrated power amplifier
36	NC	NC			NOT CONNECT
37	NC	NC			NOT CONNECT

4.2 Pin Multiplexing

This device provides various interfaces to support many kinds of applications. It is possible to control each pin according to the required application in reference to the pin multiplexing illustrated in Table 2. Pin control can be realized through register setting. This device can use a maximum of 16 GPIO pins and each of the GPIO pins multiplexes signals of various functions. In particular, four pins from GPIOA0 to GPIOA3 multiplex analog signals, which also can be realized through register setting.

Table 2: DA16200MOD Pin Multiplexing

Pin	JTAG	Analog	SPI slave	SPI Master	I2C master	I2C slave	SDIO slave	SDeMMC	BT coex	I2S	I2S_Clock	UART0	UART1	UART2	Muxed w/Analog	Pin State (nRESET=0)	Driving Strength
GPIOA0		channel0	SPI_MISO		I2C_SDA	I2C_SDA				BCLK			TXD		O	I-PD	2/4/8/12mA
GPIOA1		channel1	SPI_MOSI		I2C_CLK	I2C_CLK		WRP		MCLK			RXD		O	I-PD	2/4/8/12mA
GPIOA2		channel2	SPI_CSB			I2C_SDA				SDO		RTS	TXD		O	I-PD	2/4/8/12mA
GPIOA3		channel3	SPI_CLK			I2C_CLK				LRCK	Clock_In	CTS	RXD		O	I-PD	2/4/8/12mA
GPIOA4					I2C_SDA	I2C_SDA	cmd	cmd		BCLK		RTC	TXD/RTS		X	I-PD	2/4/8/12mA
GPIOA5					I2C_CLK	I2C_CLK	CLK	CLK		MCLK		CTS	RXD/CTS		X	I-PD	2/4/8/12mA
GPIOA6			SPI_CSB	SPI_CSB		I2C_SDA	D3	D3		SDO		RTS	TXD		X	I-PD	2/4/8/12mA
GPIOA7			SPI_CLK	SPI_CLK		I2C_CLK	D2	D2		LRCK		CTS	RXD		X	I-PD	2/4/8/12mA
GPIOA8			SPI_MISO	SPI_DIO0 (MOSI)	I2C_SDA		D1	D1	BT_sig0	BCLK					X	I-PD	2/4/8/12mA
GPIOA9			SPI_MOSI	SPI_DIO1 (MISO)	I2C_CLK		D0	D0	BT_sig1	MCLK					X	I-PD	2/4/8/12mA
GPIOA10			SPI_MISO	SPI_DIO2				WRP	BT_sig2		Clock_In			TXD	X	I-PD	2/4/8/12mA
GPIOA11			SPI_MOSI	SPI_DIO3										RXD	X	I-PD	2/4/8/12mA
TCLK/ GPIOA15	TCLK														X	I-PD	2/4/8/12mA
TMS	TMS														X	I-PU	2/4/8/12mA
UART_TXD															X	O	2/4/8/12mA
UART_RXD															X	I	2/4/8/12mA
GPIOC6	TDI														X	I-PD	2/4/8/12mA
GPIOC7	TDO													RXD	X	I-PD	2/4/8/12mA
GPIOC8	NTRST													TXD	X	I-PD	2/4/8/12mA
F_IO1			SPI_MOSI				D0			LRCK					X		2/4/8/12mA
F_IO2			SPI_MISO				D1			SDO				RXD	X		2/4/8/12mA
F_IO3							D2							TXD	X		2/4/8/12mA
F_IO4							D3								X		2/4/8/12mA
F_CSN			SPI_CSB				cmd			BCLK					X		2/4/8/12mA
F_CLK			SPI_CLK				CLK			MCLK					X		2/4/8/12mA

5 Electrical Specification

5.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	#Pins	Min	Max	Units
VBAT_3V3	35	VSS	3.9	V
VDD_DIO1	34	VSS	3.9	V
VDD_DIO2	15	VSS	3.9	V
Operating temperature range (TA)		-40	+85	°C

5.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	QFN Pins	Min	Typ	Max	Units
VBAT_3V3	35	2.1		3.6	V
VDD_DIO1	34	1.62		3.6	V
VDD_DIO2	15	1.62		3.6	V
Operating temperature range (TA)		-40		+85	°C

5.3 Electrical Characteristics

5.3.1 DC Parameters, 1.8V IO

Table 5: DC Parameters, 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3 × DVDD	V
Input High Voltage	V_{IH}	Guaranteed logic High level	0.7 × DVDD		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.2 × DVDD	V
Output High Voltage	V_{OH}	DVDD=Min.	0.8 × DVDD		DVDD	V
Pull-up Resistor	R_{PU}	V_{PAD}=V_{IH}, DIO=Min.			32.4	kΩ
Pull-down Resistor	R_{PD}	V_{PAD}=VIL, DIO=Min.			32.4	

Note 1 DVDD = 1.8V, VDD_DIO1, VDD_DIO2 Logic Level

5.3.2 DC Parameters, 3.3V IO

Table 6: DC Parameters, 3.3V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.8	V
Input High Voltage	V_{IH}	Guaranteed logic High level	2.0		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.4	V
Output High Voltage	V_{OH}	DVDD=Min.	2.4		DVDD	V
Pull-up Resistor	R_{PU}	VPAD=VIH, DIO=Min.			19.4	kΩ
Pull-down Resistor	R_{PD}	$V_{PAD}=V_{IL}$, DIO=Min.			16.0	

Note 1 DVDD= 3.3V, VDD_DIO1, VDD_DIO2 Logic Level

5.4 Radio Characteristics

5.4.1 WLAN Receiver Characteristics

TA = +25°C, VBAT = 3.3V. Parameters are measured at #1 pin [RF_TEST]

Table 7: WLAN Receiver Characteristics

Parameter	Condition	Min	Typ	Max	Units
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)	1Mbps DSSS		-98.5		dBm
	2Mbps DSSS		-94		
	11Mbps CCK		-89		
	6Mbps OFDM		-90		
	9Mbps OFDM		-90		
	18Mbps OFDM		-88		
	36Mbps OFDM		-81		
	54Mbps OFDM		-75		
	MCS0(GF)		-90		
	MCS7(GF)		-72		
Maximum input level (8% PER for 11b rates, 10% PER for 11g/11n rates)	802.11b		-4		
	802.11g		-4		

Table 8: WLAN Transmitter Characteristics

Parameter	Condition	Min	Typ	Max	Units
Maximum Output Power measured form IEEE spectral mask and EVM	1Mbps DSSS		19.0		dBm
	2Mbps DSSS		19.0		
	5.5Mbps CCK		19.0		
	11Mbps CCK		19.0		
	6Mbps OFDM		18.0		
	9Mbps OFDM		18.0		
	12Mbps OFDM		18.0		
	18Mbps OFDM		18.0		
	24Mbps OFDM		17.0		
	36Mbps OFDM		17.0		
	48Mbps OFDM		15.5		
	54Mbps OFDM		15.5		
	MCS0 OFDM		18.0		
	MCS7 OFDM		14.5		
Transmit center frequency accuracy		-25		+25	ppm

5.5 Current Consumption

TA = +25°C, VBAT = 3.3V, w/ CPU clock is 80MHz.

Table 9: Current Consumption in Active State

Parameter	Condition			Min	Typ	Max	Units
ACTIVE	TX	1 Mbps DSSS	@ 19.0 dBm		280		mA
		6 Mbps OFDM	@ 17.0 dBm		260		
		54 Mbps OFDM	@ 14.5 dBm		200		
		MCS7	@ 14.5 dBm		200		
	RX	No signal (Note 1)			28.1		
		1 Mbps DSSS (Note 1)			29.6		
		1 Mbps DSSS			36.0		
		54 Mbps OFDM			37.4		
		MCS7			37.4		

Note 1 Low Power Mode& CPU clock 30MHz

TA = +25°C, VBAT = 3.3V

Table 10: Current Consumption in Low Power Operation

Parameter	Condition	Min	Typ	Max	Units
Low Power Operation	Sleep 1		0.2		µA
	Sleep 2		1.8		
	Sleep 3		2.9		

5.6 Radiation Performance

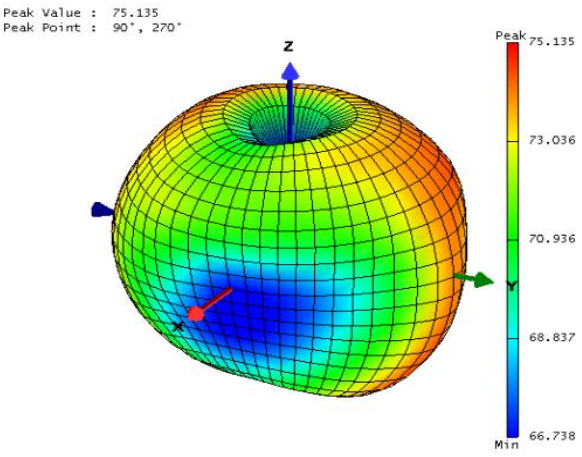

Figure 5: TIS 3D

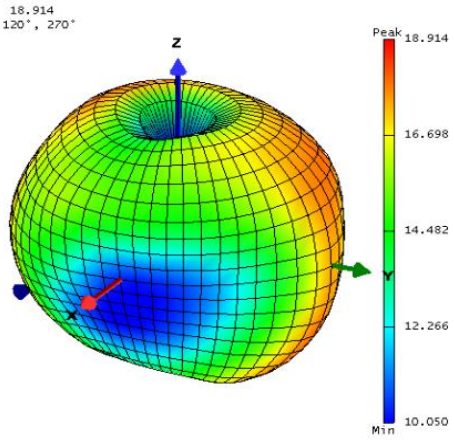

Figure 6: TRP 3D

5.7 Brown-Out and Black-Out

The device enters a brown-out condition whenever the input voltage dips below V_{BROWN} (see Table 11). This condition must be considered during design of the power supply routing, especially if the SoC is operated from a battery. High-current operations, like TX operation, cause a dip in the supply voltage, potentially triggering a brown-Out. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (for example, four contacts for two AA batteries), wiring resistance, and PCB routing resistance.

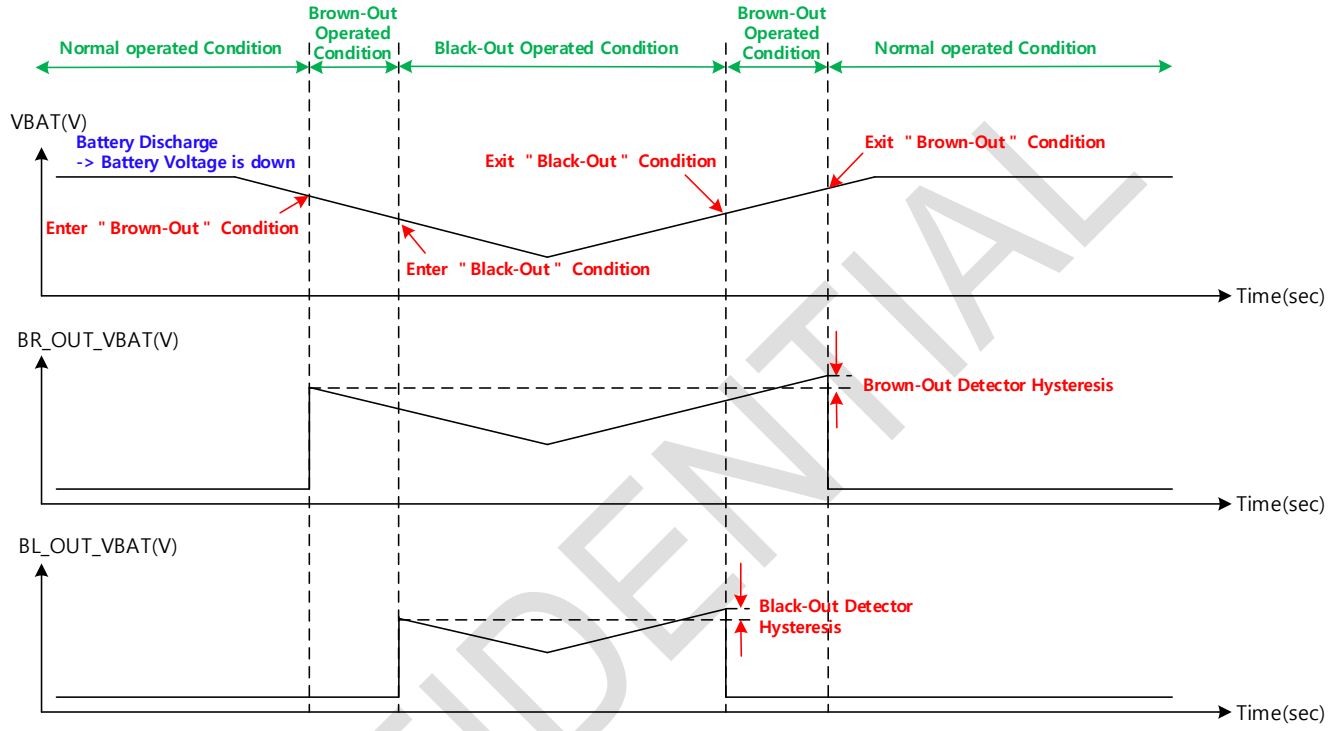

Figure 7: Brown-Out and Black-Out Levels

Brown-out and black-out conditions only operate in normal mode. The black-out condition is equivalent to a hardware reset event in which all states within the device are lost. Table 11 lists the brown-out and black-out voltage levels.

Table 11: Brown-Out and Black-Out Voltage Levels

Condition	Voltage	Hysteresis	Operation
$V_{brown-out}$	2.10 V (Note 1)	90 mV	S/W Control
$V_{black-out}$	1.75 V (Note 1)	90 mV	Full boot

Note 1 Recommended voltage level. Adjustable depending on the application condition.

6 Power Management

DA16200MOD has an RTC block which provides power management and function control for low power operation. In normal operation, the RTC block is always powered on when RTC_PWR_KEY is enabled..

6.1 Power On Sequence

The sequence after the initial switching from power-off to power-on is shown in Figure 8. The RTC_PWR_KEY of DA16200MOD is a pin that enables the RTC block. Once RTC_PWR_KEY is enabled after VBAT power is supplied, all the internal regulators are turned on automatically in the sequence pre-defined by the RTC block.

Once RTC_PWR_KEY is turned on, LDOs for both XTAL and digital I/O are turned on shortly and then the DC-DC regulator is turned on according to the pre-defined interval. The enabling intervals are also modifiable by register setting after initial power-up.

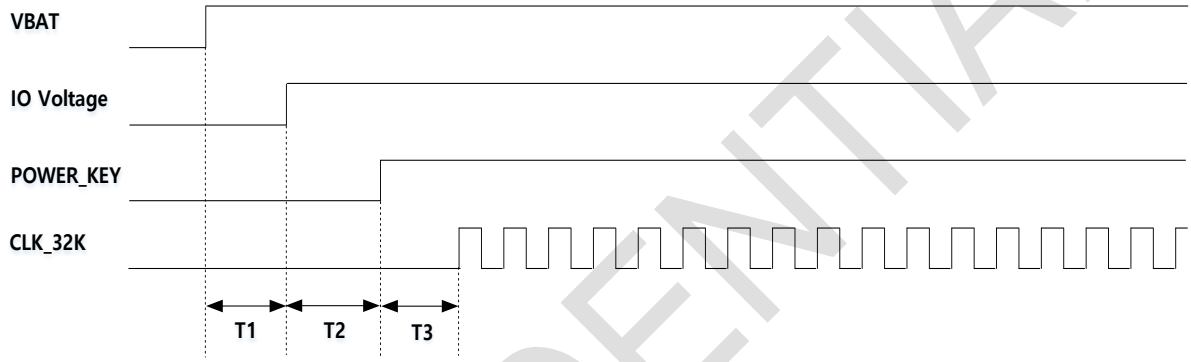

Figure 8: Power on Sequence

Table 12: Power on Sequence Timing Requirements

Name	Description	Min	Typ	Max	Unit
T1	IO voltage and VCC supply		0		µs
T2	RTC_PWR_KEY turn-on time after VBAT supply		100		µs
T3	Internal RC oscillator wake-up time		217		µs

6.2 Low Power Operation Mode

DA16200MOD provides three sleep modes as low power operation modes.

6.2.1 Sleep Mode 1

Sleep mode 1 is an operation mode in which RTC_PWR_KEY is not enabled yet. In other words, RTC_PWR_KEY is in the disabled (zero) state and DA16200MOD is only supplied with external VBAT. With all the internal blocks off, only the leakage current from minimal number of internal blocks connected to VBAT remains.

6.2.2 Sleep Mode 2

Sleep mode 2 is an operation mode in which RTC_PWR_KEY is enabled and only the RTC block is running. Only the 32-kHz clock is active. Sleep mode 2 can be activated by a command from the CPU. In other words, by setting the registers of the RTC block, power management unit can be controlled and DA16200MOD can enter sleep mode 2.

Since only the RTC block operates in sleep mode 2, minimal power consumption can be realized in this mode.

To turn sleep mode 2 back to the idle state, the count value that has been set by the CPU prior to entering the sleep mode should be reached or an external wake-up event should occur via the RTC_WAKE_UP pin.

6.2.3 Sleep Mode 3

Compared to sleep mode 2, sleep mode 3 is an operation mode where the retention memory is also alive. DA16200MOD can enter either of the sleep modes, sleep mode 2 or sleep mode 3, by application's selection which is activated by a CPU command.

To supply power to the retention memory, a specially separated uLDO is required. To put information into the retention memory and enter sleep mode 3, uLDO in the RTC block should be turned on.

7 Core System

7.1 ARM Cortex-M4F Processor

The Cortex-M4F processor is a low-power processor that features low gate count, low interrupt latency, low-cost debug, and includes floating point arithmetic functionality. The processor is intended for deeply embedded applications that require fast interrupt response features.

The features of the Cortex-M4F processor in DA16200 SoC are summarized below:

- Operation clock frequency is up to 160 MHz
- 32-bit ARM Cortex-M4F architecture optimized for embedded applications
- Thumb-2 mixed 16/32-bit instruction set
- Hardware division and fast multiplication
- Includes Nested Vectored Interrupt Contoller (NVIC)
- SysTick timer provided by Cortex-M4F processor
- Supports both standard JTAG (5-wire) and the low-pin-count ARM SWD (2-wire, TCLK/TMS) debug interfaces
- Cortex-M4F is binary compatible with Cortex-M3

For more information on the ARM Cortex-M4F, see the *ARM Cortex-M4F r0p1 technical reference manual* [1].

7.2 Wi-Fi Processor

DA16200 SoC includes an internal MCU (ARM Cortex-M4F) to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast and secure WLAN and Internet connections with 256-bit encryption. It supports the station, SoftAP, and Wi-Fi Direct modes. It also supports WPA/WPA2 personal and enterprise security, WPA2 SI, WPA3 SAE, OWE, and WPS 2.0. It includes an embedded IPv4 and IPv6 TCP/IP stack.

7.3 RTC

Among the pins in DA16200MOD, four special pins are directly connected to the RTC block, which are RTC_PWR_KEY, RTC_GPO, RTC_WAKE_UP, and RTC_WAKE_UP2.

Table 13:RTC Pin Description

Pin Name	Pin Number	Description
RTC_PWR_KEY	3	RTC_PWR_KEY represents a power key for the RTC block. When this pin is enabled, the RTC starts to work by following a pre-defined power-up sequence and eventually all the necessary power is supplied to all the sub-blocks including the main digital block in DA16200 SoC. When disabled, all blocks are powered off and this mode is defined as sleep mode 1. DA16200MOD consumes minimum leakage current in sleep mode 1. This pin also operates as a RESET pin of the whole chip.
RTC_SENSOR	5	This pin is an output pin. It has three different functions. ● GPO function: output value can be set as 1 or 0 via register setting. It can keep the value even in sleep mode ● Flash control function: when in sleep mode, it becomes 0; when in active mode, it is 1 ● Sensor wakeup function: when used in sensor wake-up function (section 8.8.4), it provides a programmable periodic signal for an external device. Inside the RTC, there are registers for setting count values

Pin Name	Pin Number	Description
RTC_WAKE_UP	4	This pin is an input pin for receiving an external event signal from an external device like a sensor. The RTC block detects an external event signal via this pin and wakes up DA16200 from sleep mode 2 or sleep mode 3.
RTC_WAKE_UP2	14	

RTC block has a 36-bit real time counter. Its resolution is equal to one clock period of 32.768 kHz. The count value can be read via the register read command.

7.3.1 Wake-up Controller

The wake-up controller is designed to wake up DA16200MOD from a sleep mode by an external signal. It detects an edge trigger of the wake-up signal and selects either the rising edge or the falling edge. Also, the wake-up signal must be maintained for at least 200 µs upon occurrence of transition on one side.

When it comes to the source of wake-up, 11 digital I/Os in addition to the two pins directly connected to the RTC block can be used. Although up to 11 digital I/Os are available for use, the maximum number of digital I/Os that are simultaneously available is eight. Table 14 describes the digital I/Os that are available for simultaneous use.

Table 14: Wake-up Sources

Input Selection = 0	Input Selection = 1
GPIOA4	X
GPIOA5	X
GPIOA6	X
GPIOA7	X
GPIOA8	X
GPIOA9	GPIOC6
GPIOA10	GPIOC7
GPIOA11	GPIOC8

The wake-up controller is located in the RTC block. Several parameters can be set by RTC registers and they identify which pin is used to wake up the SoC by checking the status register after wake-up.

DA16200MOD has another wake-up function using analog sources, which is described in section 8.8.4. Using the Aux-ADC, DA16200 detects whether it exceeds the pre-defined threshold value. If it detects the wanted condition, it will wake up from a sleep mode. Four ports (GPIOA[3:0]) are used for this function.

8 Peripherals

This section describes the peripherals that are supported by the DA16200 device.

8.1 QSPI: Master with XIP Feature

QSPI master supports 4-line SPI communication with commercial flash memory devices and uses Motorola SPI-compatible interface among SPI communication modes. The highest communication speed is the same as the AMBA bus clock, and the speed is adjustable in integer multiples. The designed QSPI supports 4-/2-/1-line types depending on the purpose. These types should be combined. Especially when the 1-line communication mode is used, it can be used as the SPI master.

QSPI master is an IP for communication between the flash memory and AMBA AHB bus and is designed to support XIP. The features of the QSPI master are summarized as follows:

Serial flash interface:

- SPI compatible serial bus interface
  - Configurable SPI I/O modes:
    - Single I/O mode
    - Dual I/O mode
    - Quad I/O mode
  - JEDEC Standard: JESD216B
  - 24-bit and 32-bit addressing
  - Supports to access flash with XIP mode
    - Read access without command
    - Read access without address and command
  - Programmable SPI clock phase and polarity
  - Maximum number of SPI CS is four that can be operated
- Compatible with serial NOR flash devices, such as Macronix, Micron, Spansion, ESMT, and ISSI

AMBA slave interface

- Compliance to the *AMBA AHB bus specification*, *Rev 3.0* [6]
- Direct code execution: directly addressable access without additional driver software
- Supports single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Supports byte, half-word, and word transaction
- AMBA slave interface is optional to access configuration and status registers
- Simple timer is used to check the completion time of flash operation
- XIP path of QSPI master supports HW remapping function to execute selected boot image for over-the-air programming (OTA)

AMBA master interface

- Compliance to the *AMBA AHB bus specification*, *Rev 3.0* [6]
- Supports DMA operation to access serial flash devices
  - Automatic copy of code image from serial flash to system RAM
  - Automatic programming of code image from system RAM to serial flash
- Performs a mem-to-mem copy in units of 32 bits, regardless of the address and length
- Supports single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Supports byte, half-word, and word transaction

Figure 9 shows the QSPI Master Block Diagram.

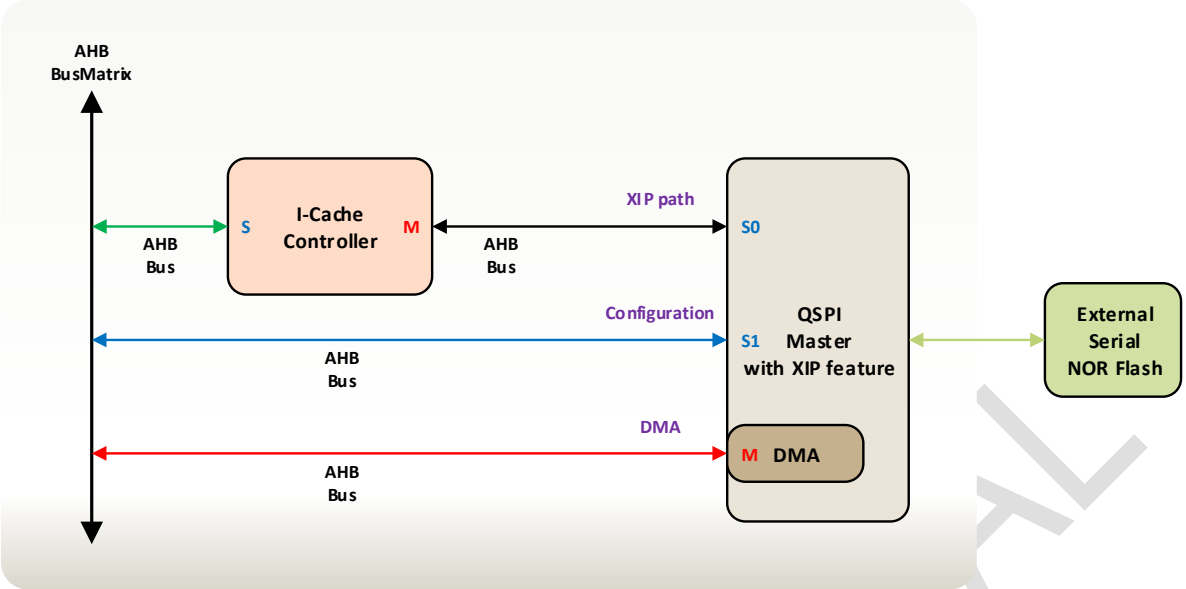

Figure 9: QSPI Master Block Diagram

Table 15 shows the pin definition of the external QSPI master interface.

Table 15: External QSPI Master Pin Configuration

Pin Name	Pin Number	I/O	Function Name
F_CSN	16	O	QSPI_CSB1
F_CLK	21	O	QSPI_CLK
F_IO0	19	I/O	QSPI_SO (TXD0)
F_IO1	17	I/O	QSPI_SI (TXD1)
F_IO2	18	I/O	QSPI_WP (TXD2)
F_IO3	20	I/O	QSPI_HOLD (TXD3)

Figure 10 shows the timing diagram for the QSPI master.

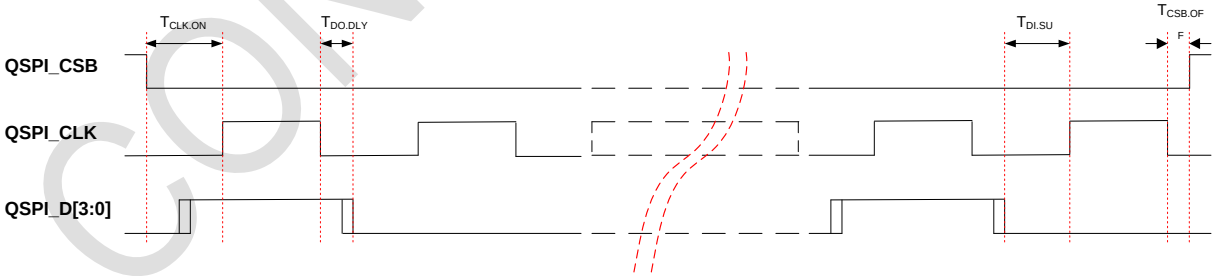

Figure 10: QSPI Master Timing Diagram (Mode 0)

Table 16 lists the timing parameters for the QSPI master.

Table 16: QSPI Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	10		120	MHz
QSPI_CLK clock duty			50		%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 ×T_{CLK}		T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0		TCLK	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6			ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$			2	ns

Note 1 $T_{CLK} = (F_{CLK} \times 10^6)^{-1}$ seconds

8.2 SPI Master

QSPI can use SPI master using single line interface. Table 17 shows the pin definition of the SPI master interface. SPI signal timing is the same as QSPI.

To use DA16200 as an SPI master, the CSB signal can be used with any of the GPIO pins. CSB [3:1] can be selected from GPIO special function by setting the registers in the GPIO.

Table 17: SPI Master Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOx		O	E_SPI_CSB[3:1]
GPIOA6		O	E_SPI_CSB[0]
GPIOA7		O	E_SPI_CLK
GPIOA8		I/O	E_SPI_MOSI or E_SPI_D[0]
GPIOA9		I/O	E_SPI_MISO or E_SPI_D[1]
GPIOA10		I/O	E_SPI_D[2]
GPIOA11		I/O	E_SPI_D[3]

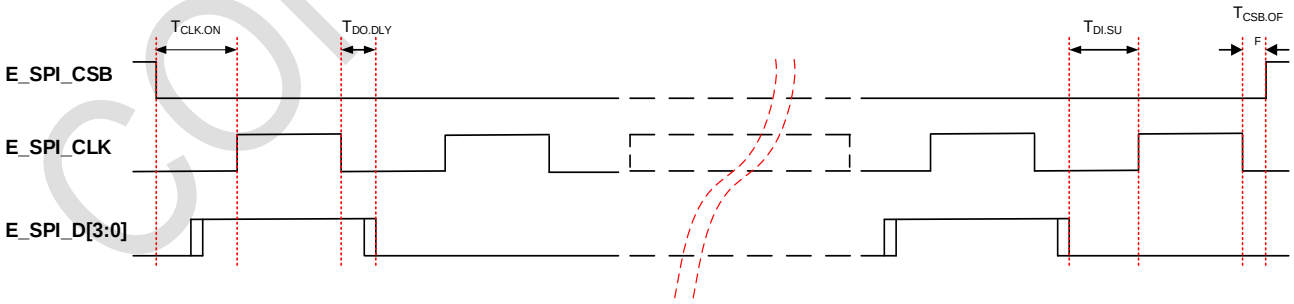

Figure 11: SPI Master Timing Diagram (Mode 0)

Table 18: SPI Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	5		60	MHz
QSPI_CLK clock duty			50		%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 × T_{CLK}		T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0		T_{CLK}	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6			ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$			2	ns

Note 1 $T_{CLK} = (F_{CLK} \times 10^6)^{-1}$ seconds

8.3 SPI Slave

SPI slave interface supports the control of DA16200 by an external host. The range of SPI clock speed is the same as that of internal bus clock speed. The SPI slave supports both the burst mode and non-burst mode. In the burst mode, SPI_CSB remains active from the start to the end of communication. In the non-burst mode, SPI_CLK remains active at every eight bits.

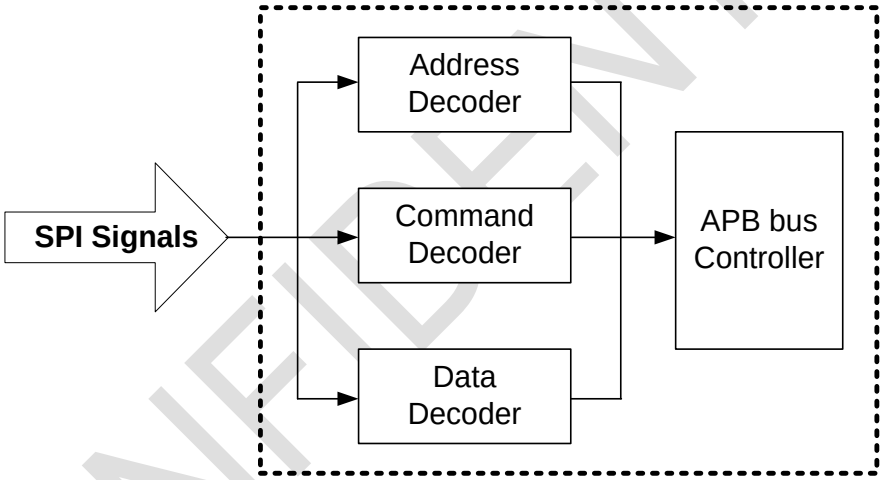

Figure 12: SPI Slave Block Diagram

Communication protocols of the SPI slave interface use either 4-byte or 8-byte control signals. Between the two available communication protocols, the CPU chooses one before initiating the control.

Figure 13 and Figure 14 shows the 8-byte and 4-byte control types.

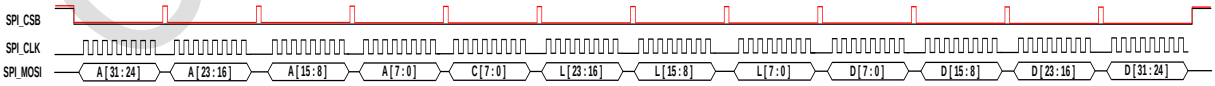

Figure 13: 8-byte Control Type

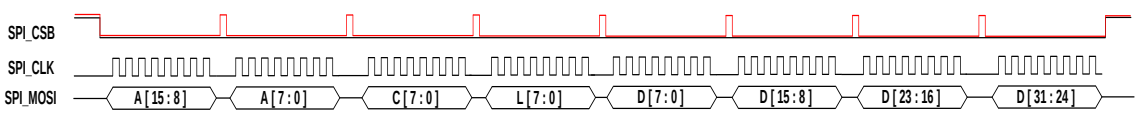

Figure 14: 4-byte Control Type

The 8-byte control type uses 4-byte address, 1-byte control, and 3-byte length. The 4-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 3-byte length shows the length of data subject to continuous access in bytes. Hence, when the 8-byte control type is applied, the maximal length of data subject to continuous access is 16 MB.

The 4-byte control type uses 2-byte address, 1-byte control, and 1-byte length. The 2-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 1-byte length shows the length of data subject to continuous access in bytes. Since the 32-bit address map is used internally, the 2-byte address is not enough to express everything. Thus, the upper 2-byte base address is designated, and then the lower 2-byte address is used.

Table 19 and Table 20 shows the meaning of each bit in the 1-byte control in the 8-byte control type and the 4-byte control type, respectively.

Table 19: Control Field of the 8-byte Control Type

Control Bit	Abr.	Description	
7	Auto Inc.	1 = Internal Address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5:0		Not used. Set all bits to ‘0’	

Table 20: Control Field of the 4-byte Control Type

Control Bit	Abr.	Description	
7	Auto Inc.	1 = Internal address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5	Common	1 = Refer base address as common area	0 = Refer base address
4	Length section	1 = Refer to register value	0 = Refer to length field
3:0	Length[12:8]	Length field upper	

Table 21 shows the pin definition of the SPI slave interface.

Table 21: SPI Slave Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA2	31	I	SPI_CSB
GPIOA6	27	I	
F_CSN	16	I	
GPIOA3	30	I	SPI_CLK
GPIOA7	26	I	
F_CLK	21	I	
GPIOA1	32	I	SPI_MOSI
GPIOA9	24	I	
GPIOA11	22	I	
F_IO0	19	I	
GPIOA0	33	O	SPI_MISO
GPIOA8	25	O	
GPIOA10	23	O	
F_IO1	17	O	

Figure 15 shows the timing diagram for the SPI slave.

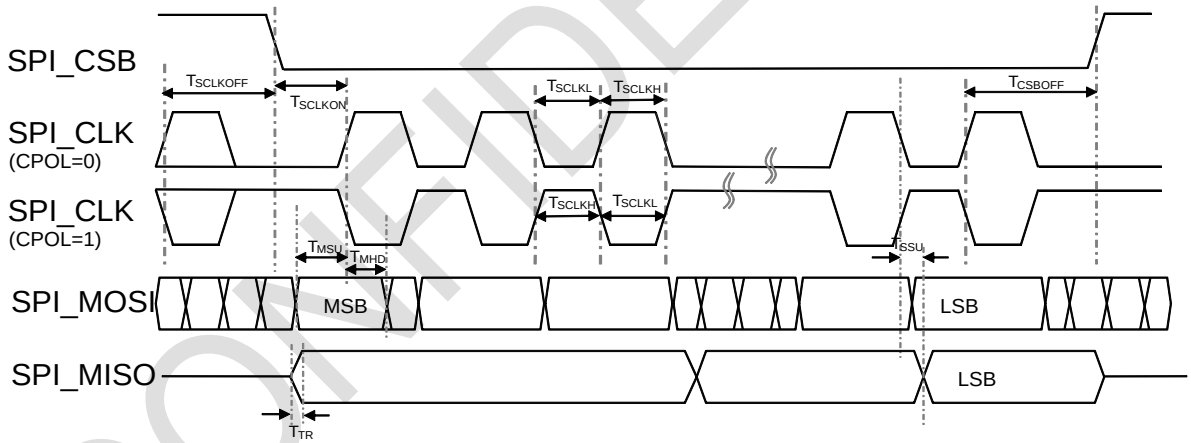

Figure 15: SPI Slave Timing Diagram

Table 22 lists the timing parameters for the SPI slave.

Table 22: SPI Slave Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	F_{SCLK}	-	-	50	MHz
SCLK clock duty		40			%
Non active duration	$T_{SCLKOFF}$	400	-	-	ns
1st CLK active rising transition time	T_{SCLKON}	T_{SCLKL}(CPOL=0) T_{SCLKH} (CPOL=1)	-	-	ns
CSB non active rising transition time	T_{CSBOFF}	T_{SCLKH} (CPOL=0) T_{SCLKL} (CPOL=1)	-	-	ns
MOSI setup time	T_{MSU}	8	-	T_{SCLK} (Note 1)	ns
MOSI hold time	T_{MHD}	8	-	T_{SCLK}	ns
MISO delay time	T_{SSU}	-	-	8	ns
MISO transition time(10% to 90% transition)	T_{TR}	-	4	5	ns

Note 1 $T_{SCLK} = 0.5 \times (F_{SCLK} \times 10^{6})^{-1}$ second

8.4 SDIO

SDIO is a full/high speed card suitable for memory card and I/O card applications with low power consumption. The full/high speed card supports SPI, 1-bit SD, and 4-bit SD transfer modes at the full clock range of 0 to 50 MHz. To be compatible with the serviceable SDIO clock, the internal BUS clock needs to be set to minimum 50 MHz. The CIS and CSA area is located inside the internal memory and the SDIO registers(CCCR and FBR) are programmed by the SD host.

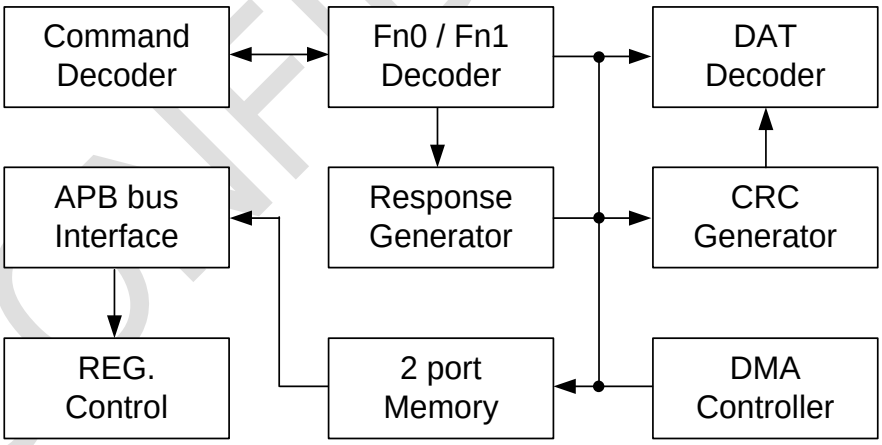

Figure 16: SDIO Slave Block Diagram

Table 23 shows the pin definition of the SDIO interface.

The GPIOA4 and GPIOA5 pins are set to SDIO CMD and CLK by default. If SDIO initialization is performed and SDIO communication is enabled, SDIO data pin setting is performed automatically. In other words, when the SDIO communication is detected, the pin used as the SDIO data among the GPIO pins is automatically activated in the SDIO use mode. However, the auto setting function is not supported for the F_xxx pin used as the flash function.

Table 23: SDIO Slave Pin Configuration

Pin Name	Pin Number		I/O	Function Name
GPIOA4	34	F4	I/O	SDIO_CMD
F_CSN	18	J5	I/O	
GPIOA5	33	D2	I	SDIO_CLK
F_CLK	19	K4	I	
GPIOA9	29	H2	I/O	SDIO_D0
F_IO0	14	K8	I/O	
GPIOA8	30	G3	I/O	SDIO_D1
F_IO1	15	L7	I/O	
GPIOA7	31	E1	I/O	SDIO_D2
F_IO2	16	J7	I/O	
GPIOA6	32	E3	I/O	SDIO_D3
F_IO3	17	K6	I/O	

Figure 17 shows the timing diagram for the SDIO slave.

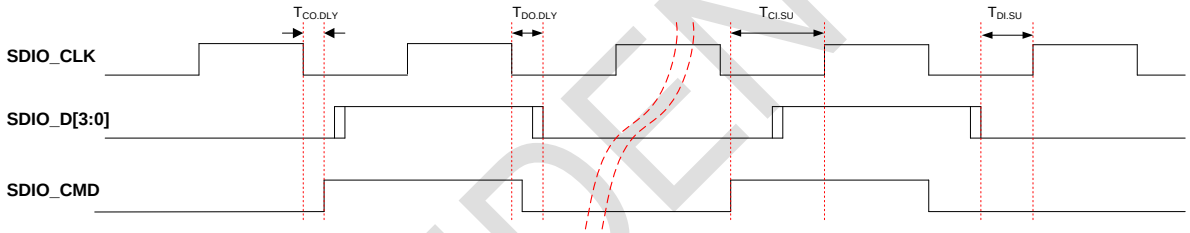

Figure 17: SDIO Slave Timing Diagram

Table 24 lists the timing parameters for the SDIO slave.

Table 24: SDIO Slave Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SDIO_CLK frequency	F_{SCLK}	-	-	50	MHz
SDIO_CLK clock duty			50		%
SDIO_CMD input setup time	$T_{CI.SU}$	3			ns
SDIO_CMD output delay time	$T_{CO.DLY}$			11 (Note 1)	ns
SDIO_D[3:0] input setup time	$T_{DI.SU}$	3			ns
SDIO_D[3:0] output delay time	$T_{DO.DLY}$			11 (Note 1)	ns

Note 1 SDIO signals can set previous output from half cycle.

8.5 I2C Interface

8.5.1 I2C Master

DA16200 includes an I2C master module. Three ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), and high (3.4 MHz) speed mode. Table 25 shows the pin definition of the I2C master interface.

Table 25: I2C Master Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA1	32	O	I2C_CLK
GPIOA5	28	O	
GPIOA9	24	O	
GPIOA0	33	I/O	I2C_SDA
GPIOA4	29	I/O	
GPIOA8	25	I/O	

Figure 18 shows the I2C timing diagram. The timing diagram is the same as that of I2C slave timing diagram.

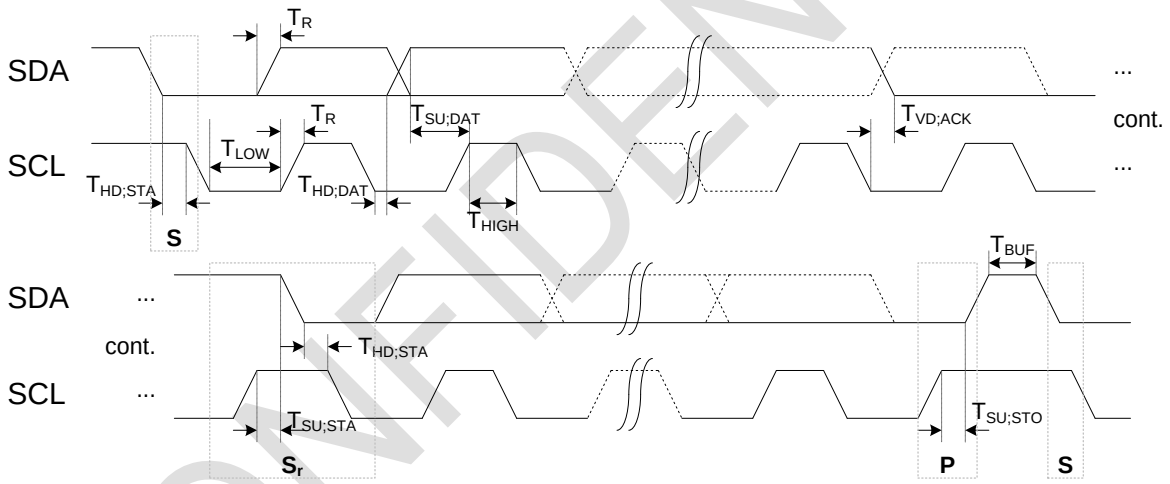

Figure 18: I2C Master Timing Diagram

Table 26 lists the I2C master timing parameters.

Table 26: I2C Master Timing Parameters

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	FSCLK	100	400	100	3400 (Note 2)	kHz
Hold time of START	THD; STA	0.2	-	0.2	-	µs
Low period of the SCL clock	TLOW	1.27	-	0.15	-	µs
High period of the SCL clock	THIGH	1.23	-	0.14	-	µs
Setup time for START condition	TSU; STA	1.1	-	0.37	-	µs
Data hold time	THD; DAT	0.07	-	0.07	-	µs
Data setup time	TSU; DAT	0.08	-	0.08	-	µs
Rise time of both SDAand SCL	TR (Note 3)	0.02	0.3	-	0.05	µs
Setup time for STOP condition	TSU; STO	0.36	-	0.36	-	µs
Data valid acknowledge time	TVD; ACK	0.04	-	0.04	-	µs
Buffer free time between START and STOP condition	TBUF	0.5	-	0.5	-	µs

Note 1 Clock duty ratio = (THIGH /TSCLK) × 100[%], TSCLK = 1/FSCLK

Note 2 Max. clock = 3.4MHz (clock period = 295ns)

Note 3 TR depends on a pull-up resistor value.

8.5.2 I2C Slave

I2C slave interface supports the control of DA16200 by an external host. Pin mux condition is defined in Table 27. Three ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), and high (1.0 MHz) speed mode.

Table 27: I2C Slave Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA1	32	I	I2C_CLK
GPIOA3	30	I	
GPIOA5	28	I	
GPIOA7	26	I	
GPIOA0	33	I/O	I2C_SDA
GPIOA2	31	I/O	
GPIOA4	29	I/O	
GPIOA6	27	I/O	

Figure 19 shows the I2C slave timing diagram.

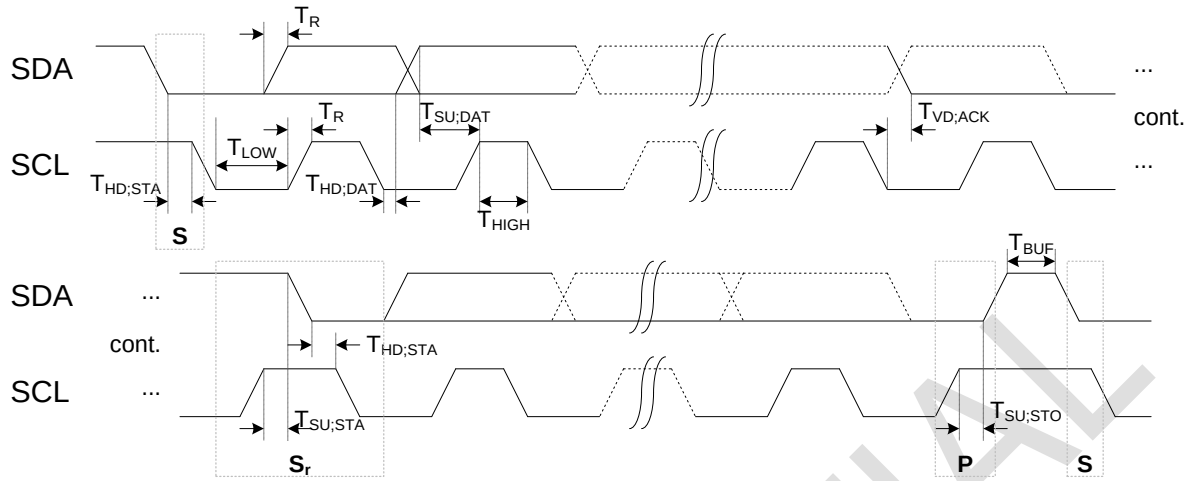

Figure 19: I2C Slave Timing Diagram

Table 28 lists the I2C slave timing parameters.

Table 28: I2C Slave Timing Parameters

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	F_{SCLK}	0	400	0	1000 (Note 2)	kHz
Hold time of START	$T_{HD;STA}$	0.6	-	0.26	-	µs
Low period of the SCL clock	T_{LOW}	1.3	-	0.5	-	µs
High period of the SCL clock	T_{HIGH}	0.6	-	0.26	-	µs
Setup time for START condition	$T_{SU;STA}$	0.6	-	0.26	-	µs
Data hold time	$T_{HD;DAT}$	0	-	0	-	µs
Data setup time	$T_{SU;DAT}$	100	-	50	-	ns
Rise time of both SDA and SCL	T_R	20	300	-	120	ns
Setup time for STOP condition	$T_{SU;STO}$	0.6	-	0.26	-	µs
Data valid acknowledge time	$T_{VD;ACK}$	-	-	-	-	µs
Buffer free time between START and STOP condition	T_{BUF}	1.3	-	0.5	-	µs

Note 1 Clock duty ratio = (THIGH/TSCLK) × 100[%], TSCLK = 1/FSCLK

Note 2 Max. clock = 1.0 MHz (clock period = 1000 ns)

8.6 SD/SDeMMC

The SD/eMMC host IP provides the function for DA16200 to access SD or eMMC cards. This SD/eMMC host IP only supports a 4-bit data bus and the maximum clock rate is 50 MHz. The maximum data rate is 25 MB/s (200 Mbps) under the 4-bit data bus and 50 MHz clock.

SD/eMMC pin mux condition is defined in Table 29.

Table 29: SD/eMMC Master Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA4	34	F4	I/O	SD/eMMC_CMD
GPIOA5	33	D2	O	SD/eMMC_CLK
GPIOA9	29	H2	I/O	SD/eMMC_D0
GPIOA8	30	G3	I/O	SD/eMMC_D1
GPIOA7	31	E1	I/O	SD/eMMC_D2
GPIOA6	32	E3	I/O	SD/eMMC_D3
GPIOA10	28	F2	I	SD/eMMC_WRP
GPIOA1	38	C3	I	

8.6.1 Block Diagram

Figure 20 shows the block diagram of SD/eMMC host IP and it includes the control register, clock control, command/response pipe, data pipe, and AHB master interface blocks.

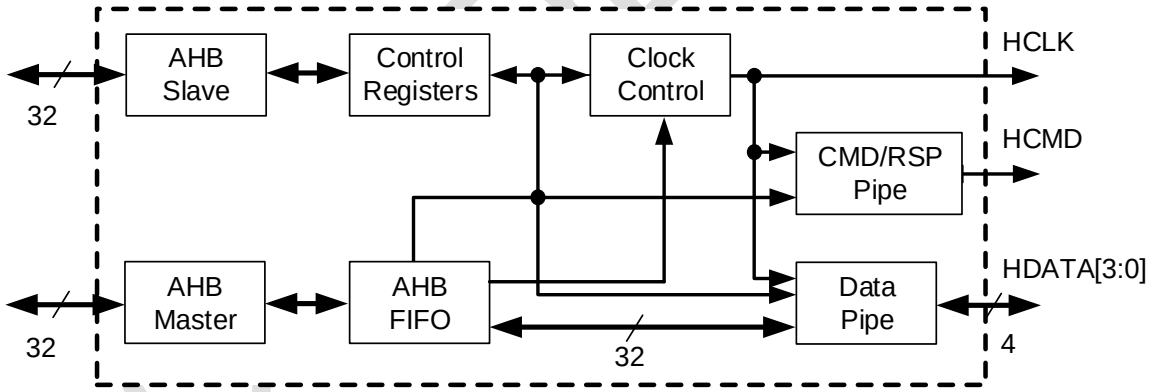

Figure 20: SD/eMMC Block Diagram

Figure 21 shows the timing diagram for the SD/eMMC master.

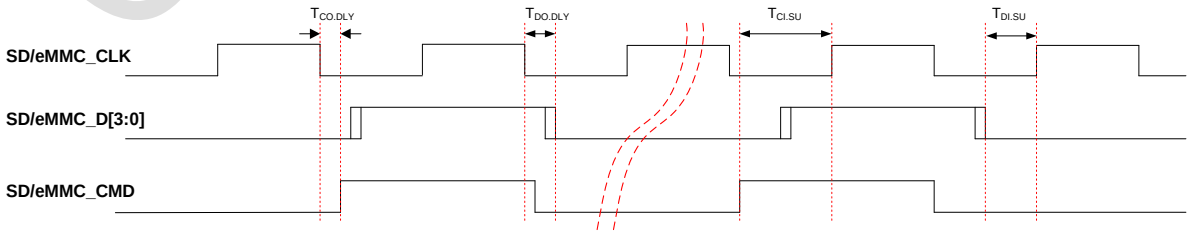

Figure 21: SD/eMMC Master Timing Diagram

Table 30 lists the timing parameters for the SD/eMMC master.

Table 30: SD/eMMC Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SD/eMMC_CLK frequency	F_{SCLK}	-	-	50	MHz
SD/eMMC_CLK clock duty			50		%
SD/eMMC_CMD input setup time	$T_{CI.SU}$	8			ns
SD/eMMC_CMD output delay time	$T_{CO.DLY}$			3	ns
SD/eMMC_D[3:0] input setup time	$T_{DI.SU}$	8			ns
SD/eMMC_D[3:0] output delay time	$T_{DO.DLY}$			8	ns

8.7 I2S

DA16200 provides an I2S interface. Once an I2S block receives audio data through the DMA, it sends audio data to the external port according to the I2S standard. To use the external DAC, output through the GPIO port is possible through the register setting according to the pin configuration (Table 31).

The I2S also provides a receive function. However, I2S transmission and reception functions cannot be used at the same time. The transmit and receive functions can be selected by register setting. If the I2S signal is input from outside after the reception function is set, the audio signal can be decoded, stored in the FIFO, and read out through the DMA. The decodable reception function provides 8/16/24/32-bit modes and can receive either mono or stereo.

Using the I2S clock divider register, the internal PLL clock can be variably applied to the I2S clock source. The available I2S clock source is 24/48 MHz. There is also a way to apply the I2S clock source directly from outside using the GPIO pin. For accurate I2S audio sampling, I2S clock source can be input to external GPIO pins. It needs to select the GPIO pin setting as the I2S clock input and apply appropriate clock source. The available I2S clock pins are shown in Table 31.

Table 31: I2S Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA1	32	O	I2S_MCLK
GPIOA5	28	O	
GPIOA9	24	O	
F_CLK	21	O	
GPIOA0	33	O	I2S_BCLK
GPIOA4	29	O	
GPIOA8	25	O	
F_CSN	16	O	
GPIOA3	30	O	I2S_LRCK
GPIOA7	26	O	
F_IO0	19	O	
GPIOA2	31	I/O	I2S_SDO
GPIOA6	27	I/O	
F_IO1	17	I/O	
GPIOA3	30	I	I2S_CLK_IN
GPIOA10	23	I	

8.7.1 I2S Transmit and Receive Timing Diagram

I2S output is possible in the following three modes. The main clock (MCLK) always outputs in 512×fs.

- I2C Mode

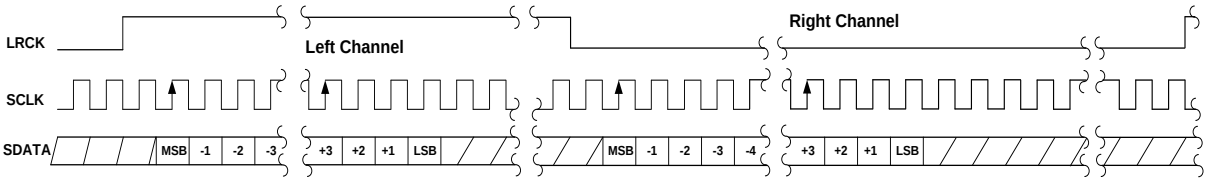

Figure 22: I2S Timing Diagram

- Left Justified Mode

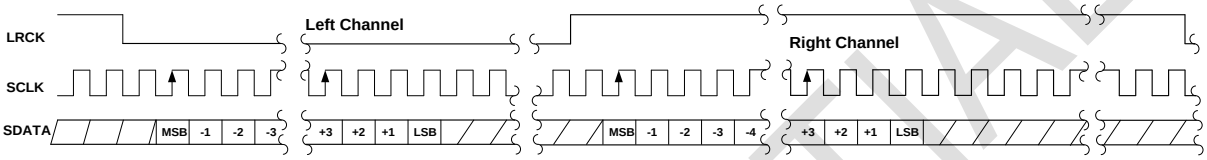

Figure 23: Left Justified Mode Timing Diagram

- Right Justified Mode

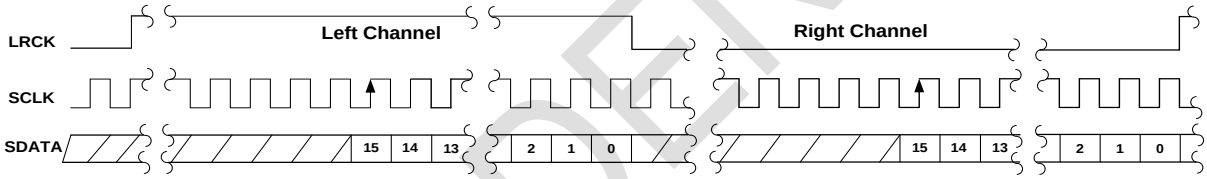

Figure 24: Right Justified Mode Timing Diagram

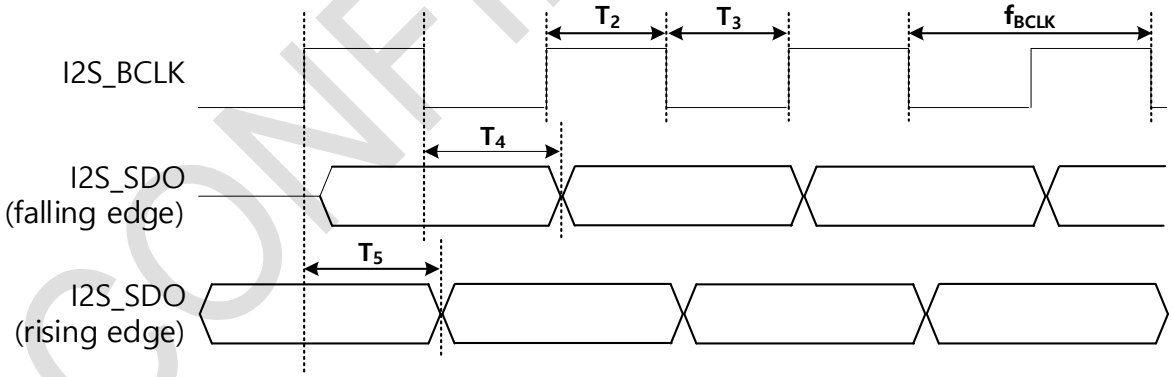

Figure 25: I2S Transmit Timing Diagram

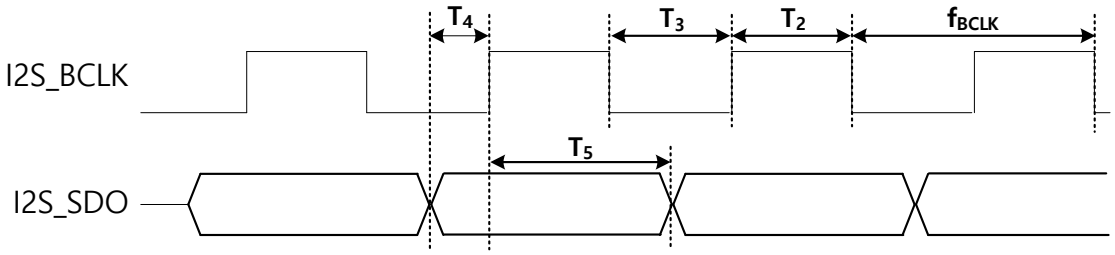

Figure 26: I2S Receive Timing Diagram

Table 32: I2S Transmit Timing Parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-		3.072	MHz
High period of the BCLK clock	T_2	-		½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-		½ f_{BCLK}	ns
I2S_SDO output hold (falling edge)	T_4	160		-	ns
I2S_SDO output hold (rising edge)	T_5	160		-	ns

Table 33: I2S Receive Timing Parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-		3.072	MHz
High period of the BCLK clock	T_2	-		½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-		½ f_{BCLK}	ns
I2S_SDO input setup time	T_4	15		-	ns
I2S_SDO input hold time	T_5	60		-	ns

8.8 ADC (Aux 12-bit)

8.8.1 Overview

DA16200 includes a high precision, ultra-low power, and wide dynamic range SAR ADC with a 12-bit resolution. It has a 4-channel single-end ADC.

Analog input is measured by four pins from GPIOA0 to GPIOA3, and pin selection is changed through the register setting.

Figure 27 shows the control block diagram.

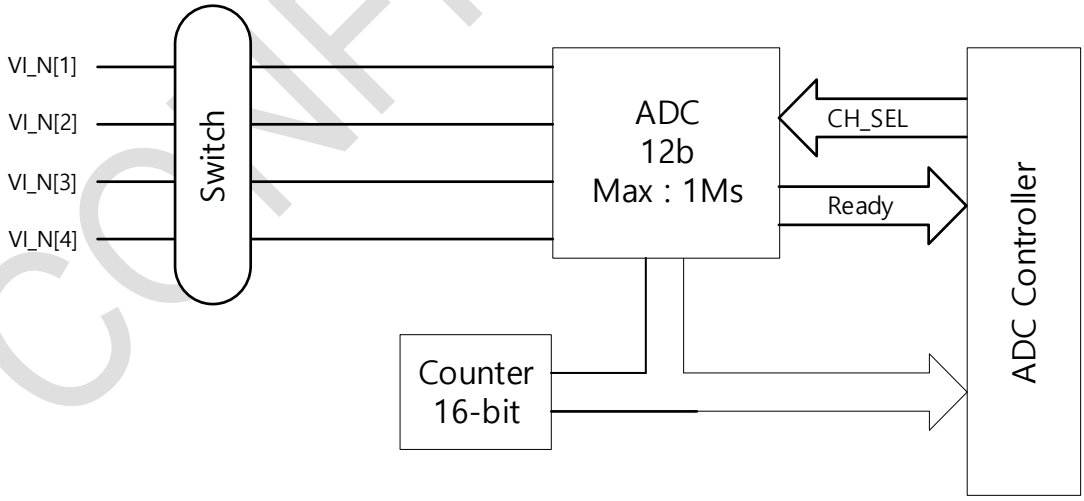

Figure 27: ADC Control Block Diagram

8.8.2 Timing Diagram

The input is digitized at a maximum of 1.0Msps throughput rate. And maximum input clock rate is 15MHz.

Figure 28 shows the conversion timing, and Table 34 describes DC specifications.

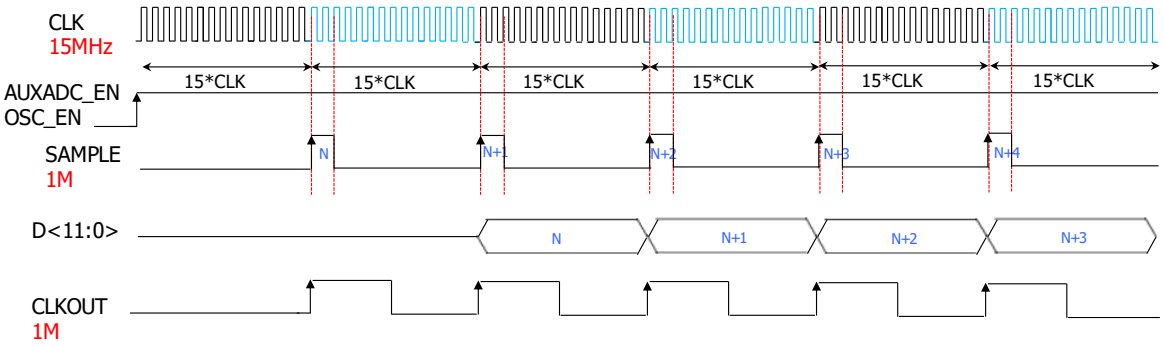

Figure 28: 12-bit ADC Timing Diagram

Table 34: DC Specification

Description	Min	Typ	Max	Unit
Resolution	4	12	12	Bits
Max clock input			15	MHz
Conversion frequency			1	MHz
Accuracy:				
• SNR • SNDR		• 61.7 • 67.2		• dB • dB
Analog input range	0		1.4	V

8.8.3 DMA Transfer

There are four ADC channel settings available. Once the input data of each channel reaches the FIFO level, it is possible to read the data through the DMA path.

8.8.4 Sensor Wake-up

DA16200MOD provides an external sensor wake-up function using the analog input signal through this Aux ADC. Even in sleep modes, it detects the change of external analog signal, wakes up from a sleep mode, and converts DA16200MOD into a normal operation. This function can be used in up to four channels. Also, when multiple external sensors are used, it detects analog signals while changing the channel automatically. For example, if it sets all four channels as input sources, it measures the channels sequentially from 0 to 3. If one of the four values exceeds the allowed range of values set by the threshold register, DA16200MOD is awaken from sleep modes. The setting value of input change can be of two types, over threshold and under threshold.

8.8.5 ADC Ports

Table 35 shows the pin definition of the ADC.

Table 35: ADC Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA3	30	A	Analog signal
GPIOA2	31	A	Analog signal
GPIOA1	32	A	Analog signal
GPIOA0	33	A	Analog signal

8.9 GPIO

All digital pads can be used as GPIO, and each GPIO port is muxed with a multi-functional interface. The GPIO features of DA16200MOD are listed below:

- Input or output lines in a programmable direction
- Word and half word read/write access
- Address-masked byte writes to facilitate quick bit set and clear operations
- Address-based byte reads to facilitate quick bit test operations
- Maskable interrupt generation based on input value change
- Possible to be output signal of PWM[3:0], external interrupt, QSPI_CSB[3:1], RF_SW[1:0], and UART_TXDOE[2:0] on the GPIO pins:
  - It provides special functions for GPIO pin use. PWM [3:0], external interrupt, QSPI_CSB [3:1], RF_SW [1:0], and UART_TXDOE [2:0] signals can be output by selecting unused pins among the GPIO pins. It is possible to select the function to be output from the GPIO register setting and select the remaining GPIO pin without using it to output the specific function to the desired GPIO pins

8.9.1 Antenna Switching Diversity

DA16200MOD provides the antenna switching diversity function for performance improvement in multi-path environment. Phy block measures the RSSI of each antenna and selects the antenna with the largest RSSI. The selected antenna is also used for transmission. To use this function, an external switching element is required, and switching control is performed through the GPIO. Two GPIOs can be used for switching control, and any unused pins among the GPIO pins can be selected for this purpose. The control signal can be changed by register setting to suit the external switching device.

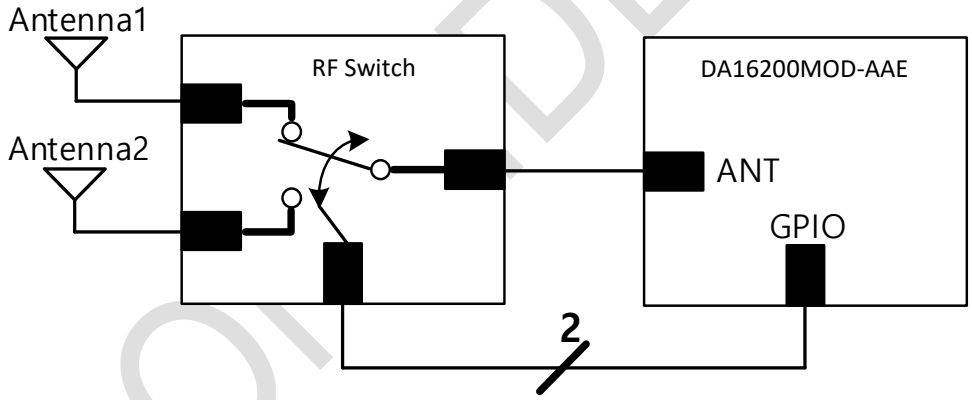

Figure 29: Antenna Switching Internal Block Diagram

8.10 UART

DA16200 provides 3 UARTs, features of which are described below:

- Programmable use of UART
- Compliance to the *AMBA AHB bus specification* [6] for easy integration into SoC implementation
- Supports both byte and word access for reduction of bus burden
- Supports both RS-232 and RS-485
- Separate 32×8 bit transmit and 32×12 bit receive FIFO memory buffers to reduce CPU interrupts
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Standard asynchronous communication bits (start, stop and parity), which are added prior to transmission and removed on reception
- Independent masking of transmit FIFO, receive FIFO, and receive timeout
- Supports for DMA
- False start bit detection
- Programmable flow control (only supported in UART1 and UART2)
- Fully programmable serial interface characteristics:
  - Data can be of 5,6,7, or 8 bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1- or 2- stop bit generation
  - Baud rate generation

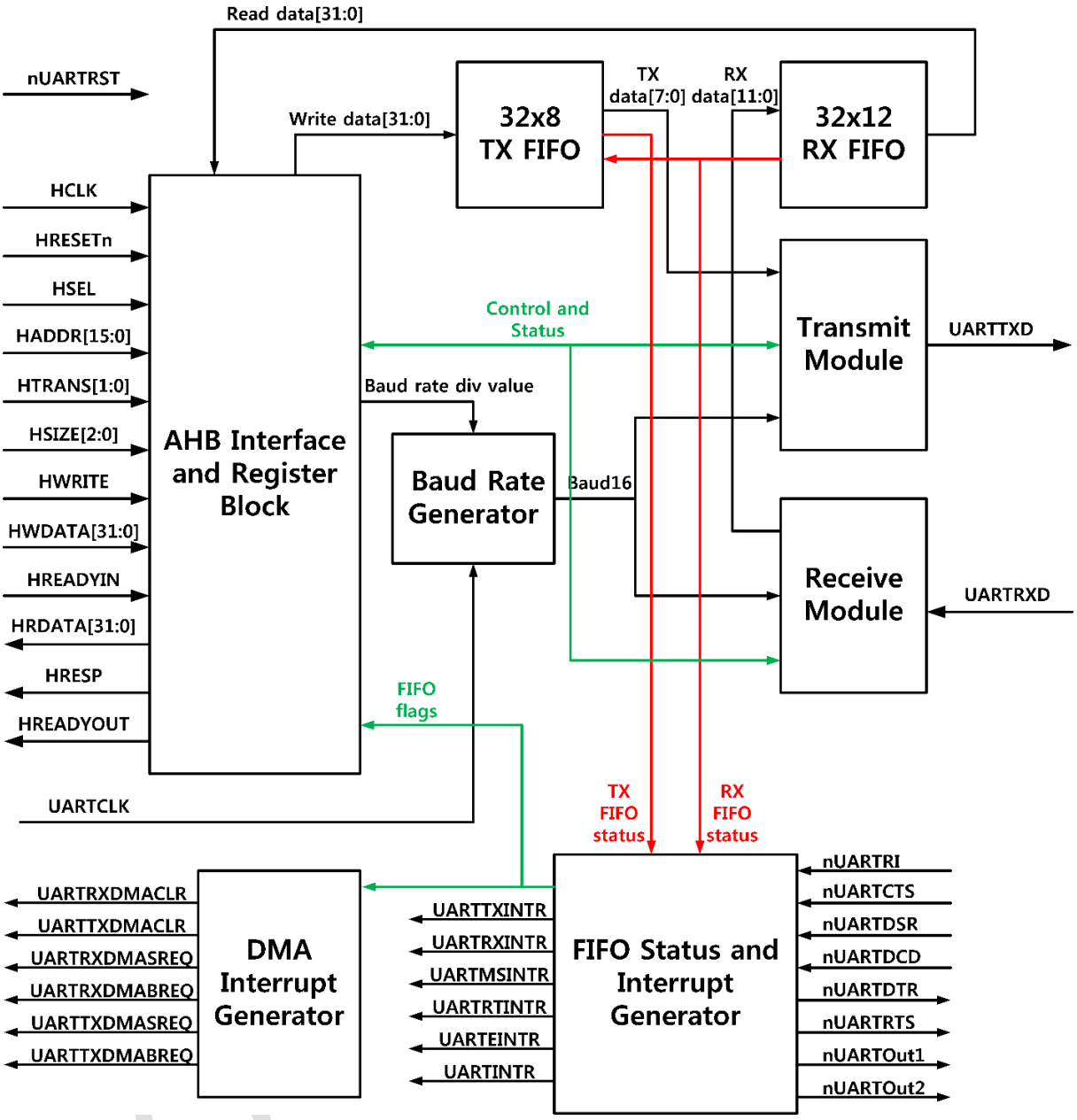

Figure 30: DA16200 UART Block Diagram

8.10.1 RS-485

DA16200 UART supports RS-485. UART485EN register (0x054) is required to be assigned to one to enable the RS-485. In order to use RS-485, additional signal (UARTTXDOE) is required to notice TXD intervals. This signal can be an output by selecting any unused pins among the GPIO pins.

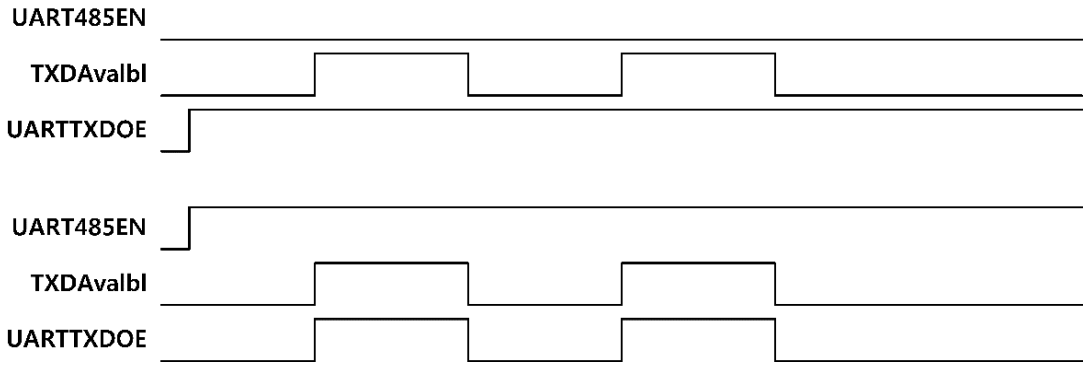

Figure 31: UARTTXDOE Output Signal for UART RS-485

Table 36 shows the pin definition of the UART interface.

Table 36: UART Pin Configuration

Pin Name	Pin Number	I/O	Function Name
UART0_RXD	13	I	UART0_RXD
UART0_TXD	12	O	UART0_TXD
GPIOA7	26	I	UART1_RXD
GPIOA5	28	I	
GPIOA3	30	I	
GPIOA1	32	I	
GPIOA6	27	O	UART1_TXD
GPIOA4	29	O	
GPIOA2	31	O	
GPIOA0	33	O	
GPIOA5	28	I	UART1_CTS
GPIOA4	29	O	UART1_RTS
GPIOA11	22	I	UART2_RXD
GPIOC7	10	I	
F_IO2	18	I	
GPIOA10	23	O	UART2_TXD
GPIOC6	11	O	
F_IO3	20	O	

8.11 PWM

Pulse width modulation (PWM) is a modulation technique used to encode a message into a pulse signal. The blocks are designed to adjust output pulse duration by the CPU bus clock (HCLK).

Figure 32 shows the structure of the PWM block.

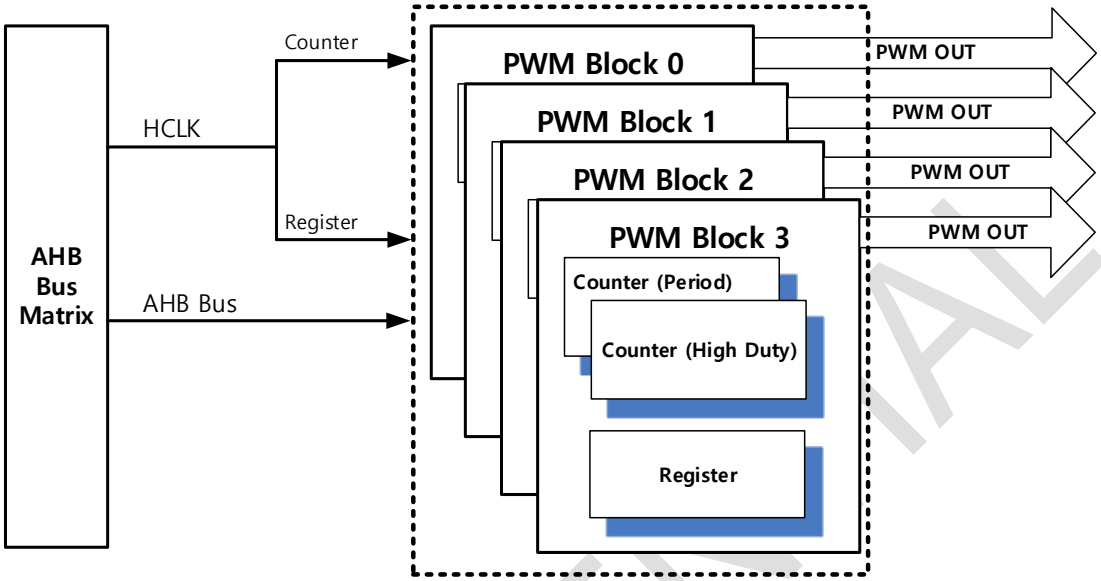

Figure 32: PWM Block Diagram

Table 37 shows the pin definition of the PWM interface. GPIOx means that PWM signals can go out through any GPIO pins via register setting.

Table 37: PWM Pin Configuration

Pin Name	Pin Number		I/O	Function Name
GPIOx				PWM[3:0] output

8.11.1 Timing Diagram

Table 38 shows the relation between the internal bus clock and PWM output wave patterns. Figure 33 show the conversion timing diagram. '**a**' and '**b**' can be adjusted through the register setting, and PWM wave patterns vary depending on the ratio. '**a**' controls the high width of pulses (nCycle High), while '**b**' controls the general cycle (nCycle Period).

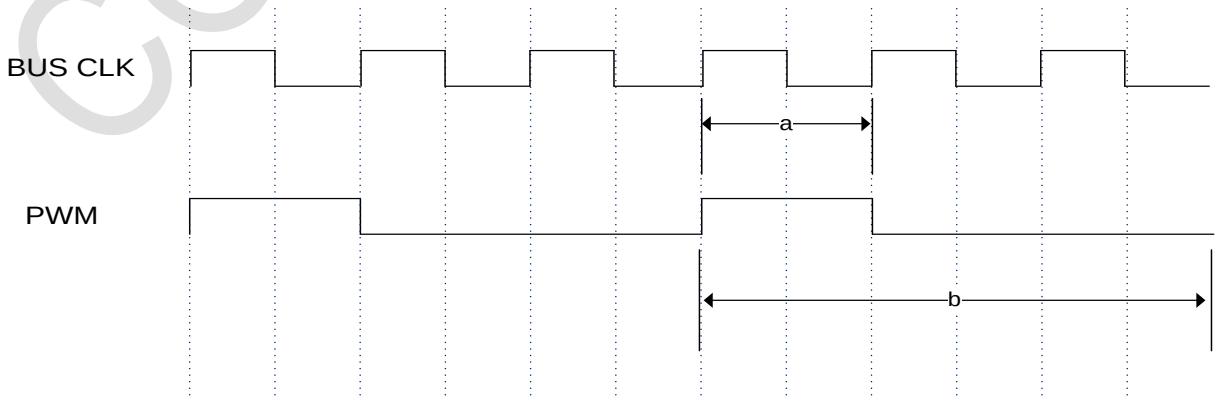

Figure 33: PWM Timing Diagram

Table 38: PWM Timing Diagram Description

Time	Description
a	Bus Clock Period × (nCycle High + 1)
b	Bus Clock Period × (nCycle Period + 1)

8.12 Debug Interface

DA16200 supports both IEEE Standard 1149.1 JTAG (5-wire) and the low-pin-count ARM SWD (2-wire, TCLK/TMS) debug interfaces. The SWD protocol can handle the same debug features as the JTAG.

The JTAG port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see [4].

Figure 34 shows the JTAG timing diagram.

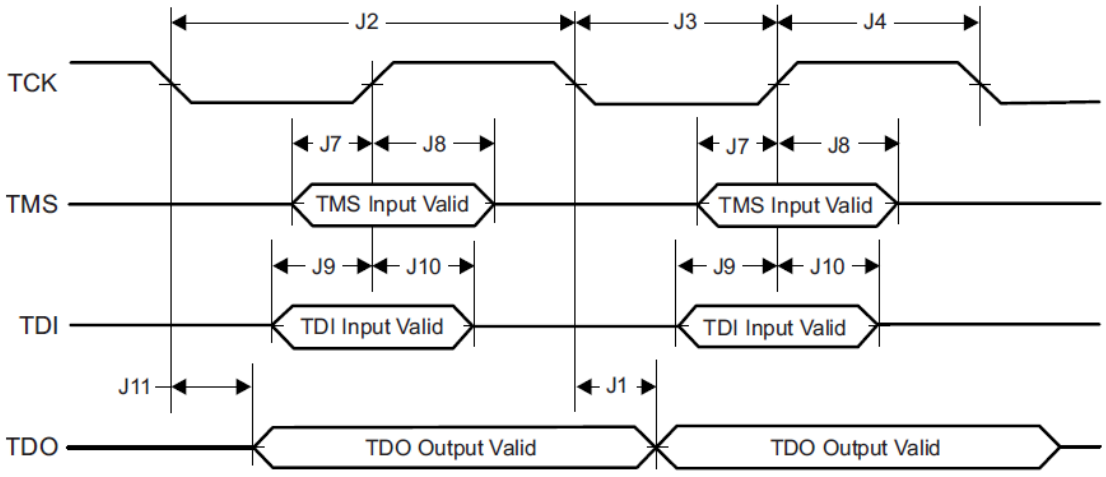

Figure 34: JTAG Timing Diagram

Table 39 shows the JTAG timing parameters.

Table 39: JTAG Timing Parameters

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
J1	f_{TCK}	Clock Frequency		15	MHz
J2	t_{TCK}	Clock Period		$1/f_{TCK}$	ns
J3	t_{CL}	Clock Low Period		$t_{TCK}/2$	ns
J4	t_{CH}	Clock High Period		$t_{TCK}/2$	ns
J7	t_{TMS_SU}	TMS Setup Time	1		
J8	t_{TMS_HO}	TMS Hold Time	16		
J9	t_{TDI_SU}	TDI Setup Time	1		
J10	t_{TDI_HO}	TDI Hold Time	16		
J11	t_{TDO_HO}	TDO Hold Time		15	

Table 40 shows the pin definition of the JTAG interface.

Table 40: JTAG Pin Configuration

Pin Name	Pin Number	I/O	Function Name
TMS	7	I/O	Data
TCLK	8	I	Clock
GPIOC8	9	I	TDI: Data Input
GPIOC7	10	O	TDO: Data Output
GPIOC6	11	I	nTRST: Reset

8.13 Bluetooth Coexistence

DA16200MOD provides the Bluetooth coexistence function to be properly aligned with external devices activated at 2.4 GHz.

8.13.1 Interface Configuration

The following three pins can be set in pin multiplexing:

- BT_sig0 (oWlanAct)
  - It indicates that Output, WLAN is currently active
- BT_sig1 (iBtAct)
  - It indicates that Input, BT/BLE is currently active
- BT_sig2 (iBTPri)
  - It indicates that Input (Optional), BT/BLE has a higher priority

A variety of configurable settings are available, including active high/low, manual force mode, use status of the optional iBTPri function, and whether or not to switch oWlanAct to active in the event of TX/RX/TRX.

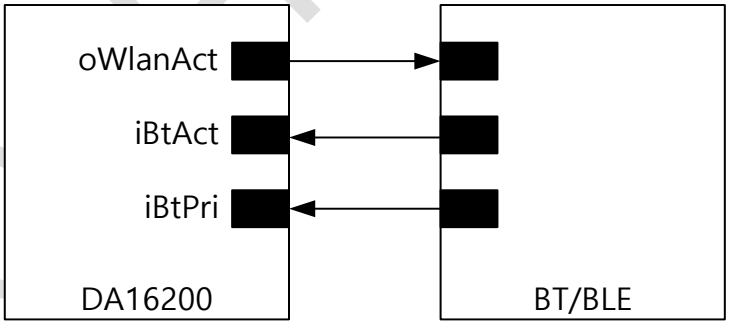

Figure 35: Bluetooth Coexistence Interface

8.13.2 Operation Scenario

The Bluetooth coexistence can be turned on/off by the configurable register, and the activation scenarios based on the status of each pin are described below:

- BT_sig0 (oWlanAct)
  - When asserted, external BT/BLE is expected to stop occupying RF
- BT_sig1 (iBtAct)
  - When asserted, DA16200 stops occupying RF
- BT_sig2 (iBTPri)
  - It is optional and thus may not be used

- If it is used and DA16200's iBtAct = Active while iBTPri = Non-Active, DA16200 may ignore iBtAct

9 Applications Schematic

9.1 Typical Application

Figure 36 shows the schematics for an application.

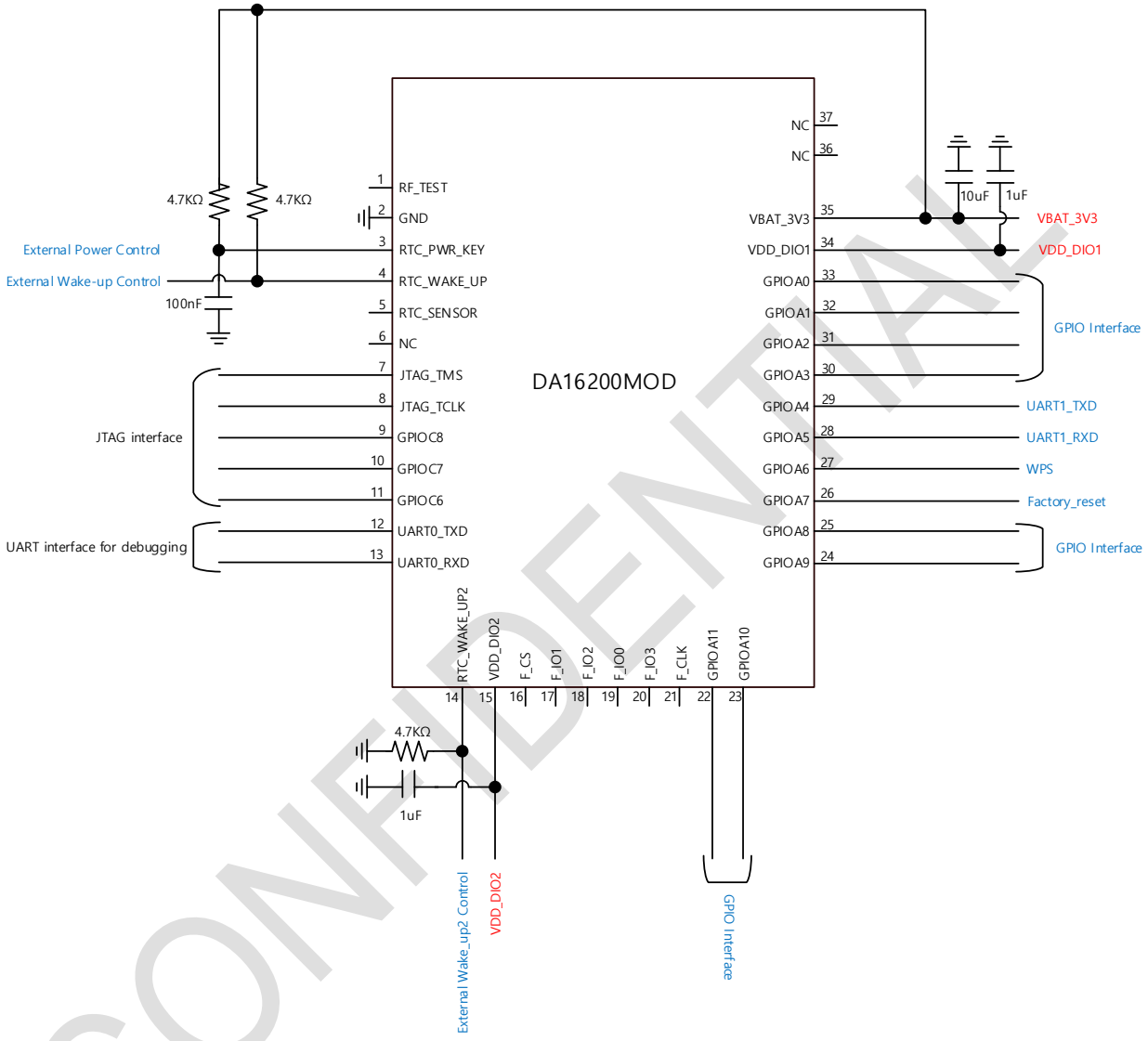

Figure 36: Typical Application

10 Package Information

10.1 Dimension: DA16200MOD-AAC

Unit: mm

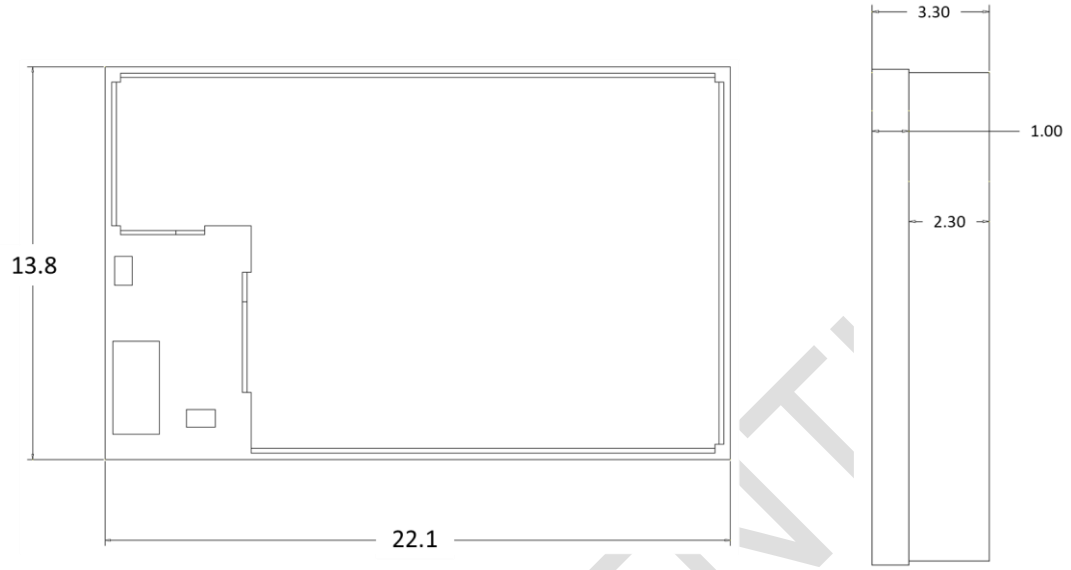

Figure 37: Module Top

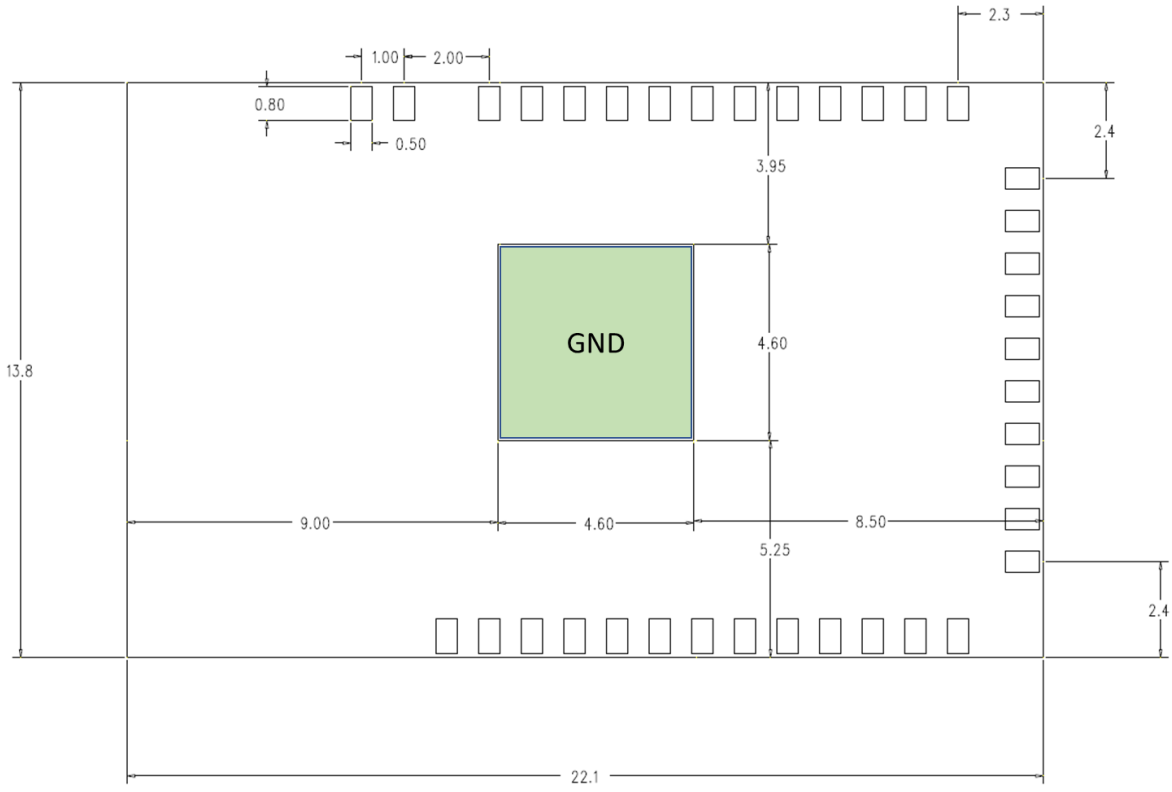

Figure 38: Module Bottom Top-View

10.2 Dimension: DA16200MOD-AAE

Unit: mm

Figure 39: Module Top

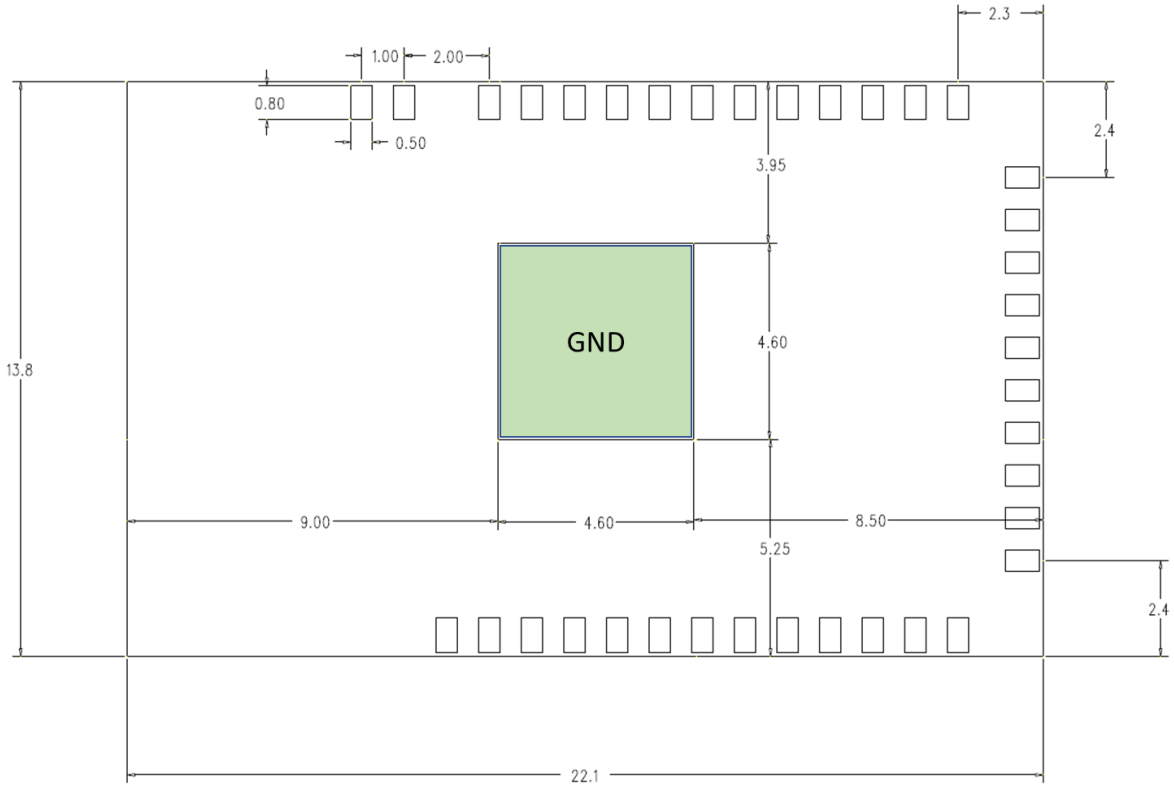

Figure 40: Module Bottom Top-View

10.3 PCB Land Pattern

Unit: mm

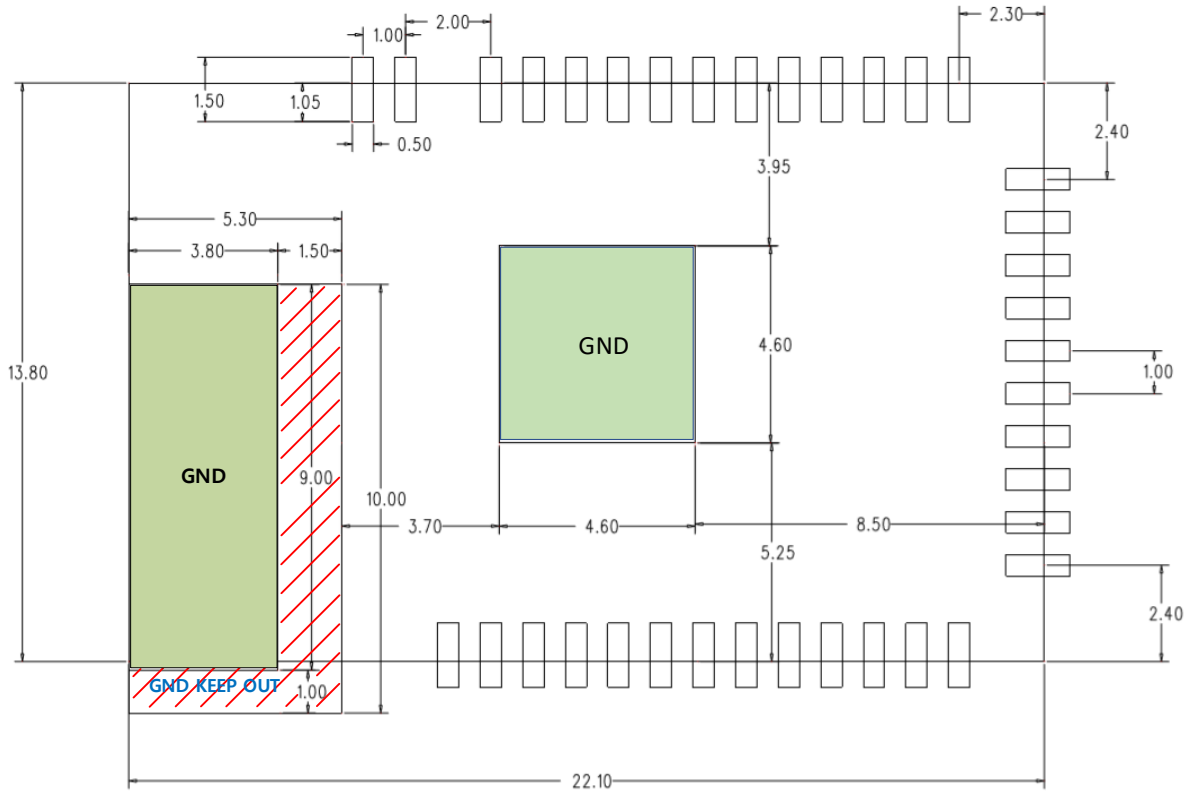

Figure 41: PCB Land Pattern (Top View)

10.4 Soldering Information

10.4.1 Recommended Condition for Reflow Soldering

Figure 42 shows the typical process flow for mounting surface mount packages to PCB.

The reflow profile depends on the solder paste being used and the recommendations from the paste manufacture should be followed to determine the proper reflow profile. Figure 42 shows a typical reflow profile when a no-clean paste is used. Oven time above liquidus (260°C for lead-free solder) is 20 to 40 seconds.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste application
4. Component placement
5. Component attachment

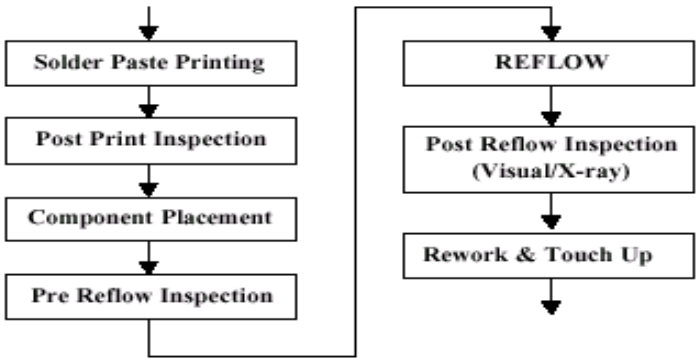

Figure 42: Typical PCB Mounting Process Flow

Table 41: Typical Reflow Profile (Lead Free): J-STD-020C

Profile Feature	Lead Free SMD
Average ramp up rate (Ts_{max} to T_p)	3°C/s Max.
Preheat	
• Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (Ts_{max} to Ts_{min})	• 150°C • 200°C • 60 to 180 seconds
Time maintained above	
• Temperature (T_L) • Time (t_L)	• 217°C • 60 to 150 seconds
Peak/Classification temperature (T_p)	260°C
Time within 5°C of peak temperature (tp)	20 to 40 seconds
Ramp down rate	6°C/s Max.
Time from 25°C to peak temperature	8 minutes Max.

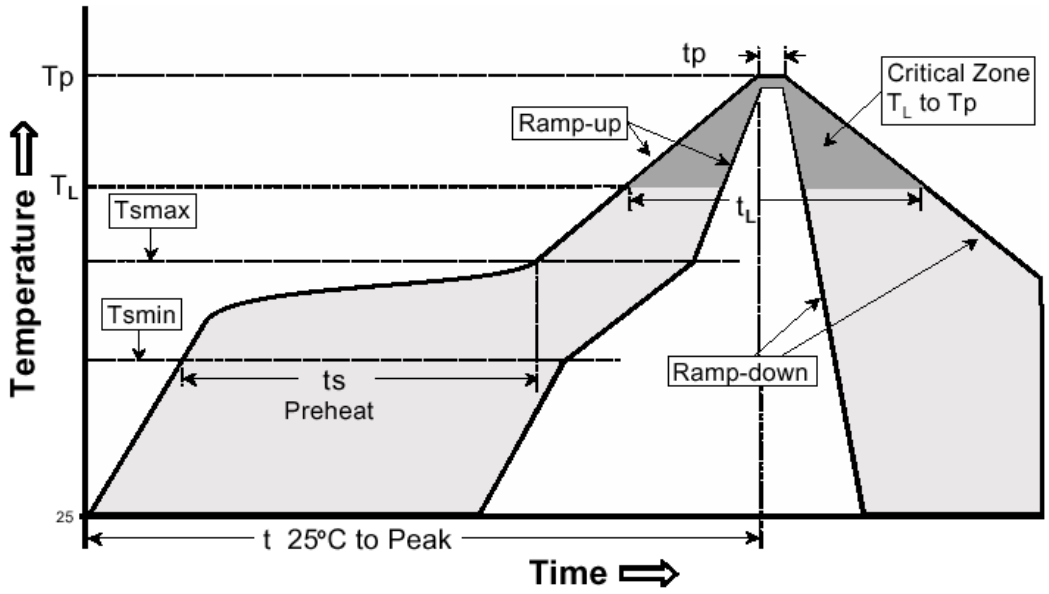

Figure 43: Reflow Condition

11 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer support portal or your local sales representative.

Table 42: Ordering Information (Samples)

Part Number	Pins	Size (mm)	Shipment Form	Pack Quantity
DA16200MOD-AAC4WA32	37	13.8 x 22.1 x 3.3	Reel	
DA16200MOD-AAE4WA32	37	13.8 x 22.1 x 3.3	Reel	

Table 43: Ordering Information (Production)

Part Number	Pins	Size (mm)	Shipment Form	Pack Quantity
DA16200MOD-AAC4WA32	37	13.8 x 22.1 x 3.3	Reel	
DA16200MOD-AAE4WA32	37	13.8 x 22.1 x 3.3	Reel	

Part Number Legend:

DA16200MOD-AAC4WA32

AA: Module revision number

C: Antenna

[C] Chip antenna, [E] u.FL connector

4: Flash memory

[4] 4Mbyte, [2] 2Mbyte

W: Voltage range

[W] 3.3V, [L] 1.8V

A3: Package No.

2: T&R packing

12 Regulatory Approval

12.1 Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

12.1.1 FCC Caution:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

12.1.2 FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.
The module must be installed in WiFi Module.
This End equipment should be installed and operated with a minimum distance of 20cm between the radiator and your body.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

12.1.3 End Product Labeling

The final end product must be labeled in a visible area with the following:
“Contains FCC ID: 2AU49-DA16200MC”.

12.1.4 Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.

12.2 Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

12.2.1 Caution Exposure:

This device meets the exemption from the routine evaluation limits in section 2.5 of RSS102 and users can obtain Canadian information on RF exposure and compliance.
Le dispositif répond à l'exemption des limites d'évaluation de routine dans la section 2.5 de RSS102 et les utilisateurs peuvent obtenir des renseignements canadiens sur l'exposition aux RF et le respect.

12.2.2 The final end product must be labelled in a visible area with the following:

The Industry Canada certification label of a module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the Industry Canada certification number of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:
Contains transmitter module IC: 25650-DA16200MC

The module must be installed in WiFi Module.

This End equipment should be installed and operated with a minimum distance of 20cm between the radiator and your body.

Cet équipement devrait être installé et actionné avec une distance minimum de 20cm entre le radiateur et votre corps.

The end user manual shall include all required regulatory information/warning as show in this manual.

Revision History

Revision	Date	Description
1.0	03-Oct-2019	Preliminary datasheet
1.1	22-Oct-2019	Modified module size
1.2	12-Dec-2019	Add Regulatory Approval

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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