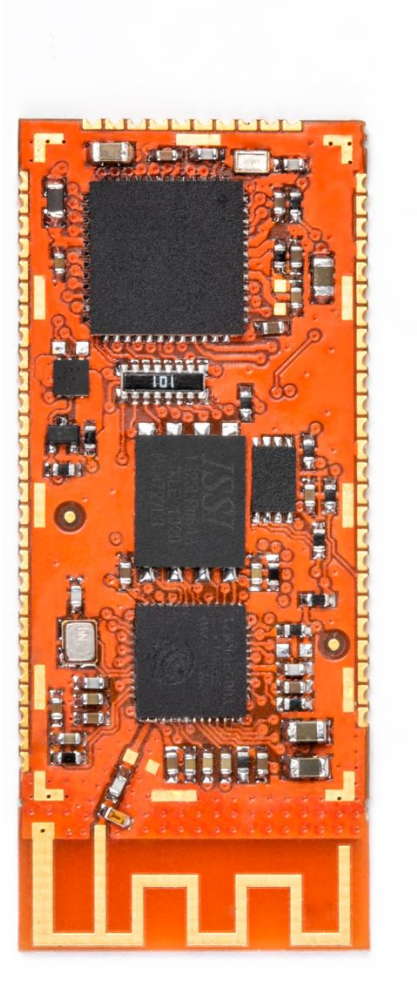
MBC-WB01
Modular Brick Concept

Combo Wi-Fi/BT-SoM
Product Specifications



1. Revision History

Revision number	Revision date	Summary of changes	Authors
1.0	05/11/2018	Initial version	D. Trimarchi

2. Index

3. Introduction

The MBC-WB01 SoM is part of Meteca's MBC family of devices. It follows the MBC standard specification that allows users to switch from one module to another (also with different MCU and/or functionalities) in a seamless fashion, since all modules share same pinout and dimensions.

This compact and certified SoM is the ideal solution for designers that want a unique device with Wi-Fi & BT/BLE connectivity plus a dedicated control MCU.

It features:

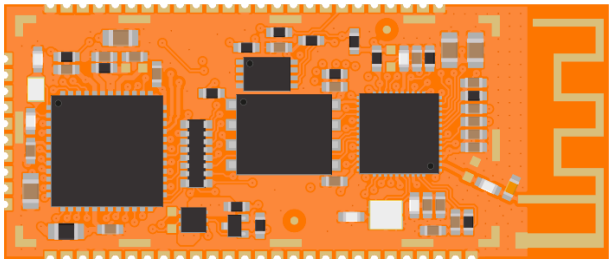
- One ATSAMD21G18A ARM® Cortex®-M0+ MCU - best for control purposes (like motor and actuator control, sensor acquisition, SERCOM interface etc.);
- one ESP32-D0WD dual-core Tensilica Xtensa LX6 running @ 240MHz with integrated Wi-Fi and dual-mode Bluetooth, perfect for connectivity and heavy computational tasks;
- One CryptoAuth ECC608A chip - for securing cloud connections and the OTA/boot procedure;
- One QSPI 64-Mbit or 128-Mbit flash - for storing both ESP32 firmware and user data.

Both the MCU's are fully user accessible (both in programming and debugging) to allow a perfect configuration/customization for each design. This feature gives the user the power to decide which of the two MCUs should act as a master or a slave (or have a more "liquid" configuration) and what features each chip should implement in order to achieve a perfect balance between power consumption, functionalities implemented and overall performance.

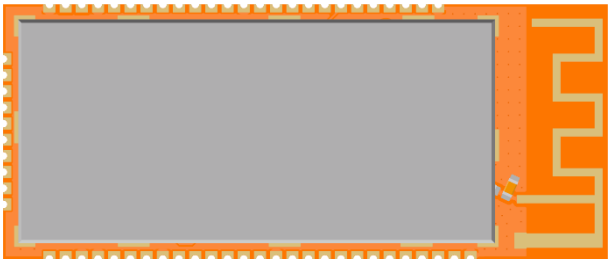
The two MCUs share two high-speed communication interfaces (plus some synchronizing signals): one SPI and one UART suitable for data exchange and firmware update.

Each chip has the capability of its own auto-update - or counterpart's firmware, allowing both in-board (through serial or USB interfaces) and over-the-air (through Wi-Fi or BT interfaces) firmware upgrade mechanisms in a secured environment thanks to the CyptoAuth chip supplied with the board.

Every MBC features a specific ID line that allows a carrier board to recognize the SoM characteristics (MCUs mounted on the SoM, operating voltages, power consumptions, features enabled, etc.)



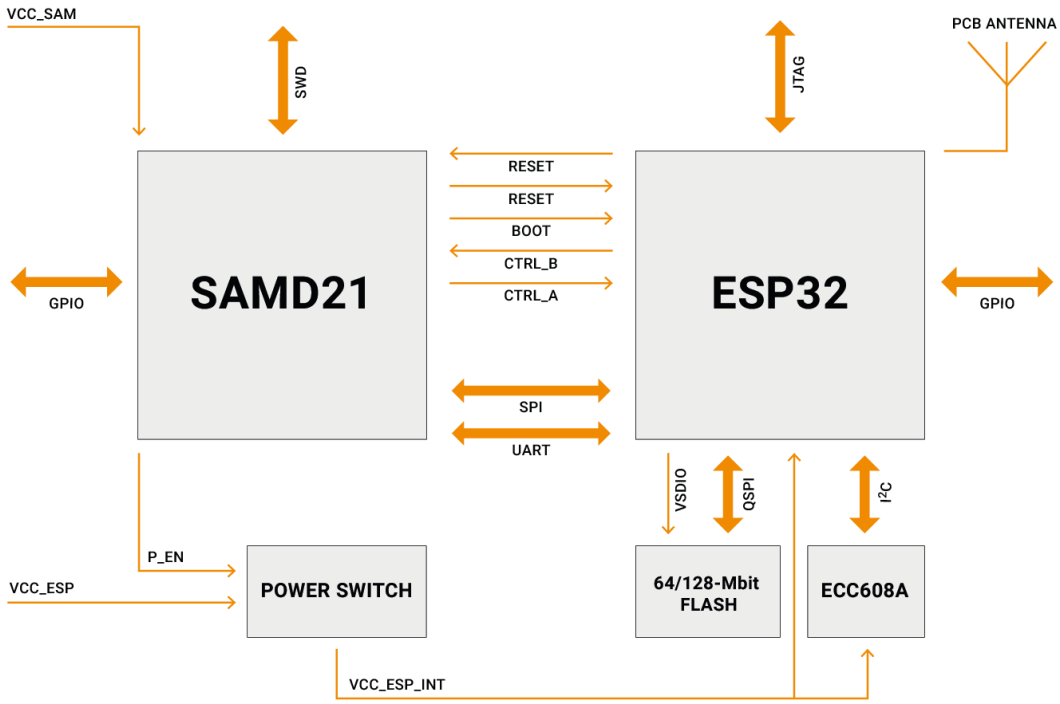
MBC-WB01 top



MBC-WB01 top with shielding can

4. Block Diagram

The following image shows the functional block diagram of the MBC-WB01 module.



5. Key features

Features of the ESP32:

- Processors
  - CPU: Xtensa dual-core (or single-core) 32-bit LX6 microprocessor, operating at 240 MHz and performing at up to 600 DMIPS
  - Ultra low power (ULP) co-processor
  - Memory: 520 KiB SRAM
- Wireless connectivity
  - Wi-Fi: 802.11 b/g/n
  - Bluetooth: v4.2 BR/EDR and BLE
- Peripherals
  - 12-bit SAR ADC up to 18 channels
  - 2 × 8-bit DACs
  - 10 × touch sensors (capacitive sensing GPIOs)
  - Temperature sensor
  - 4 × SPI
  - 2 × I²S interfaces
  - 2 × I²C interfaces
  - 3 × UART
  - SD/SDIO/CE-ATA/MMC/eMMC host controller
  - SDIO/SPI slave controller
  - Ethernet MAC interface with dedicated DMA and IEEE 1588 Precision Time Protocol support
  - CAN bus 2.0
  - Infrared remote controller (TX/RX, up to 8 channels)
  - Motor PWM
  - LED PWM (up to 16 channels)
  - Hall effect sensor
  - Ultra low power analog pre-amplifier
- Security
  - IEEE 802.11 standard security features all supported, including WFA, WPA/WPA2 and WAPI
  - Secure boot
  - Flash encryption
  - 1024-bit OTP, up to 768-bit for customers
  - Cryptographic hardware acceleration: AES, SHA-2, RSA, elliptic curve cryptography (ECC), random number generator (RNG)
- Power management
  - Internal low-dropout regulator
  - Individual power domain for RTC
  - 5uA deep sleep current
  - Wake up from GPIO interrupt, timer, ADC measurements, capacitive touch sensor interrupt

Features of the ATSAMD21:

- Processor
  - ARM©, Cortex-M0+ CPU running at up to 48MHz
  - Single-cycle hardware multiplier
  - Micro Trace Buffer
- Memories
  - 256KB in-system self-programmable Flash
  - 32KB SRAM Memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M) and 48MHz to 96MHz fractional
  - External Interrupt Controller (EIC), 16 external interrupts, one non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
  - Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Peripherals
  - 12-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Up to five 16-bit Timer/Counters (TC), configurable as either:
  - One 16-bit TC with compare/capture channels
  - One 8-bit TC with compare/capture channels
  - One 32-bit TC with compare/capture channels, by using two TCs
  - Three 24-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins,
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface with Device and embedded Host and 8 endpoints
  - Six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I2C Bus up to 3.4MHz
    - SMBUS/PMBUS
    - SPI
    - LIN slave
  - 12-bit, 350 ksps Analog-to-Digital Converter (ADC) with up to 14 channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC) with 256-channel capacitive touch and proximity sensing I/O
  - 38 GPIO pins

Features of the ATECC608A:

- Cloud authentication for AWS IoT
- Cloud authentication for Google Cloud IoT Core
- Secure Boot implementation with an ATSAMD21 Cortex-M0+
- Cryptographic coprocessor with secure hardware-based key storage
  - Protected storage for up to 16 Keys, certificates or data
- Hardware support for asymmetric sign, verify, key agreement – ECDSA: FIPS186-3 Elliptic Curve Digital Signature
- ECDH: FIPS SP800-56A Elliptic Curve Diffie-Hellman
- NIST standard P256 elliptic curve support
- Hardware support for symmetric algorithms
  - SHA-256 & HMAC hash including off-chip context save/restore
  - AES-128: encrypt/decrypt, galois field multiply for GCM
- Networking key management support
  - Turnkey PRF/HKDF calculation for TLS 1.2 & 1.3
  - Ephemeral key generation and key agreement in SRAM – Small message encryption with keys entirely protected
- Secure boot support
  - Full ECDSA code signature validation, optional stored digest/signature – optional communication key disablement prior to secure boot
  - Encryption/Authentication for messages to prevent on-board attacks
- Internal high-quality FIPS 800-90 A/B/C Random Number Generator (RNG)
- Two high-endurance monotonic counters
- Guaranteed unique 72-bit serial number
- Two interface options available
  - High-speed single pin interface with One GPIO pin
  - 1MHz Standard I2C interface
- 1.8V to 5.5V IO levels, 2.0V to 5.5V supply voltage
- <150nA Sleep current

6. Security

A key point of IoT and IIoT is security. Since many industrial companies are extensively implementing the Internet of Things at the edge of their networks and increasing the capabilities of the network itself, connecting many devices presents a huge security threat. This big number of connected devices offers a much larger surface prone to cyber-attack than the IT space where, by comparison, the volumes of data are lower and its exchanging can be more precisely controlled.

In the industrial sector, huge amounts of data are being processed by physical devices at the edge (through their firmware), sent back to the cloud for further analysis and used by different applications or, after processing, by the devices themselves to control the processes or the plant environment. Attackers can exploit these devices and their software to subvert and compromise the hardware itself. Significant numbers of IoT devices are not being used with security in mind, so every single device and sensor in the IoT represent a potential risk and an easy entry point to the network.

The MBC-WB01 features a double security layer.

The first directly inside the ESP32, that, along with TLS v1.2, implements secure boot, flash content encryption and cryptographic hardware acceleration (with AES, SHA-2, RSA, elliptic curve cryptography (ECC) and random number generator (RNG) support).

The secure boot support ensures that when the ESP32 executes any software from flash, that software is trusted and signed by a known entity. If even a single bit in the software bootloader and application firmware is modified, the firmware is not trusted, and the device will refuse to execute this untrusted code. This is achieved by building a chain of trust from the hardware, to the software bootloader, to the application firmware.

The flash encryption support ensures that any application firmware, that is stored in the flash of the ESP32, stays encrypted. This allows manufacturers to ship encrypted firmware in their devices.

The second is the Microchip ATECC608A that integrates ECDH (Elliptic Curve Diffie Hellman) security protocol - an ultra-secure method to provide key agreement for encryption/decryption - along with ECDSA (Elliptic Curve Digital Signature Algorithm) sign-verify authentication.

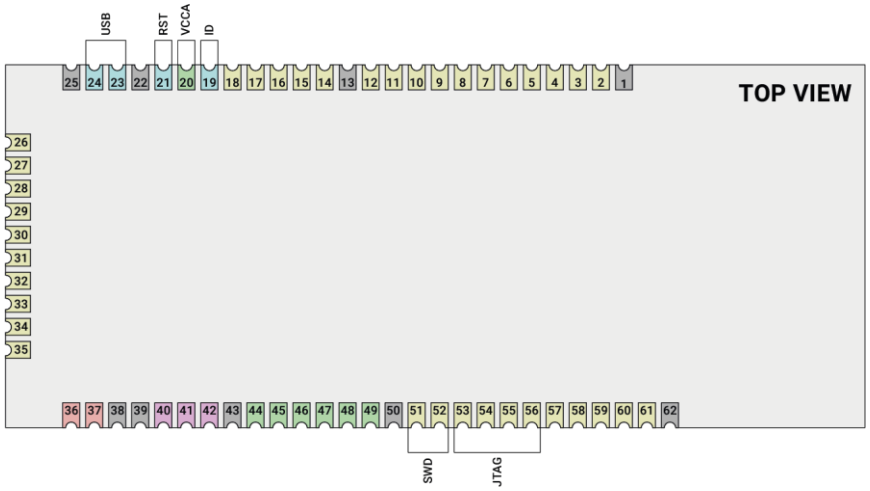
It also offers an integrated AES hardware accelerator extending the secure boot features to both the MBC’s MCU and supplying the full range of security such as confidentiality, data integrity, and authentication to MBC’s system. The ATECC608A employs ultra-secure hardware-based cryptographic key storage and cryptographic countermeasures which eliminate potential backdoors linked to software weaknesses.

It can also perform Elliptic Curve Diffie Hellman Key Exchange which means that the part can securely store the asymmetric keys (private key) for a TLS (v. 1.3) exchange and deliver the master secret to the microcontroller for the symmetric portions of the protocol, simplifying the connection and the authentication to Azure, AWS, and Google cloud platforms.

7. Pinout

The following images show the pinout of the MBC-WB01 module.

The MBC standard has up to 62 pins, 14 of them are dedicated for power supply, 2 are dedicated for the USB 2.0 interface, 1 for main board reset, 1 for the ID, 1 for the analog power supply reference, 6 can be analog or digital GPIOs and the remaining 37 pins can be used as digital GPIOs.



- SAMD21 power supply pin
- ESP32 power supply pin
- Ground pin
- Analog Input pin (can also be used as digital GPIO)
- Digital GPIO pin
- Special function pin – USB, SAMD21/ESP reset and ID

pin #	Connected to	Main Function	Voltage	Direction	Note / Alt. Functions
1	-	Ground pin	0	P	-
2	ESP32	GPIO 25	3.3	I/O	DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
3	ESP32	GPIO 27	3.3	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
4	ESP32	GPIO 32	3.3	I/O	32K_XP (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
5	ESP32	GPIO 26	3.3	I/O	DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
6	ESP32	GPIO 33	3.3	I/O	32K_XN (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
7	ESP32	TXD	3.3	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
8	ESP32	RXD	3.3	I/O	GPIO3, U0RXD, CLK_OUT2
9	ESP32	GPIO 35	3.3	I	ADC1_CH7, RTC_GPIO5
10	ESP32	GPIO 34	3.3	I	ADC1_CH6, RTC_GPIO4
11	ESP32	GPIO 4	3.3	I/O	ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
12	ESP32	GPIO 2	3.3	I/O	ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
13	-	Ground pin		P	-
14	SAMD21	PA27	3.3	I/O	EXTINT[15], GCLK_IO[0]
15	SAMD21	PA14	3.3	I/O	EXTINT[14], SERCOM2/PAD[2], SERCOM4/PAD[2], TC3/WO[0], TCC0/WO[4], GCLK_IO[0]
16	SAMD21	PA10	3.3	I/O	EXTINT[10], AIN[18], PTC_X[2], SERCOM0/PAD[2], SERCOM2/PAD[2], TCC1/WO[0], TCC0/WO[2], I2S/SCK[0], GCLK_IO[4]
17	SAMD21	PA09	3.3	I/O	EXTINT[9], AIN[17], PTC_X[1], SERCOM0/PAD[1], SERCOM2/PAD[1], TCC0/WO[1], TCC1/WO[3], I2S/MCK[0]
18	SAMD21	PA08	3.3	I/O	NMI, AIN[16], PTC_X[0], SERCOM0/PAD[0], SERCOM2/PAD[0], TCC0/WO[0], TCC1/WO[2], I2S/SD[1]
19	-	MBC's device ID	3.3	O	Connect to a Serial RX pin to read out the SoM ID and features
20	SAMD21	VCCA	3.3	P	Analog voltage reference for ADC/DAC
21	SAMD21	Reset	3.3	I	SAMD21 reset source: leave unconnected or connect to a weak pull-up (100k); drive low to reset the board.
22	-	Ground pin	0	P	-

23	SAMD21	USB D-		I/O	EXTINT[12], SERCOM3/PAD[2], SERCOM5/PAD[2], TC5/WO[0], TCC1/WO[2]
pin #	**Connected to**	**Main Function**	**Voltage**	**Direction**	**Note / Alt. Functions**
24	SAMD21	USB D+		I/O	EXTINT[13], SERCOM3/PAD[3], SERCOM5/PAD[3], TC5/WO[1], TCC1/WO[3]
25	-	Ground pin	0	P	
26	SAMD21	PA23	3.3	I/O	EXTINT[7], PTC_X[11], SERCOM3/PAD[1], SERCOM5/PAD[1], TC4/WO[1], TCC0/WO[5], USB/SOF 1kHz, GCLK_IO(7)
27	SAMD21	PB02	3.3	I/O	EXTINT[2], AIN[10], PTC_Y[8], SERCOM5/PAD[0], TC6/WO[0]
28	SAMD21	PB03	3.3	I/O	EXTINT[3], AIN[11], PTC_Y[9], SERCOM5/PAD[1], TC6/WO[1]
29	SAMD21	PB08	3.3	I/O	EXTINT[8], AIN[2], PTC_Y[14], SERCOM4/PAD[0], TC4/WO[0]
30	SAMD21	PB09	3.3	I/O	EXTINT[9], AIN[3], PTC_Y[15], SERCOM4/PAD[1], TC4/WO[1]
31	SAMD21	PB11	3.3	I/O	EXTINT[11], SERCOM4/PAD[3], TC5/WO[1], TCC0/WO[5], I2S/SCK[1], GCLK_IO[5]
32	SAMD21	PB10	3.3	I/O	EXTINT[10], SERCOM4/PAD[2], TC5/WO[0], TCC0/WO[4], I2S/MCK[1], GCLK_IO[4]
33	SAMD21	PA12	3.3	I/O	EXTINT[12], SERCOM2/PAD[0], SERCOM4/PAD[0], TCC2/WO[0], TCC0/WO[6], AC/CMP[0]
34	SAMD21	PA13	3.3	I/O	EXTINT[13], SERCOM2/PAD[1], SERCOM4/PAD[1], TCC2/WO[1], TCC0/WO[7], AC/CMP[1]
35	SAMD21	PA11	3.3	I/O	EXTINT[11], AIN[19], PTC_X[3], SERCOM0/PAD[3], SERCOM2/PAD[3], TCC1/WO[1], TCC0/WO[3], I2S/FS[0], GCLK_IO[5]
36 37	SAMD21	Core/logic power supply	3.3	P	-
38 39	-	Ground pin	0	P	-
40 41 42	ESP32	Core/logic power supply	3.3	P	-
43	-	Ground pin		P	-
44	SAMD21	AIN5	3.3	I/O	PA07, EXTINT[7], AIN[7], AC_AIN[3], PTC_Y[5], SERCOM0/PAD[3], TCC1/WO[1], I2S/SD[0]

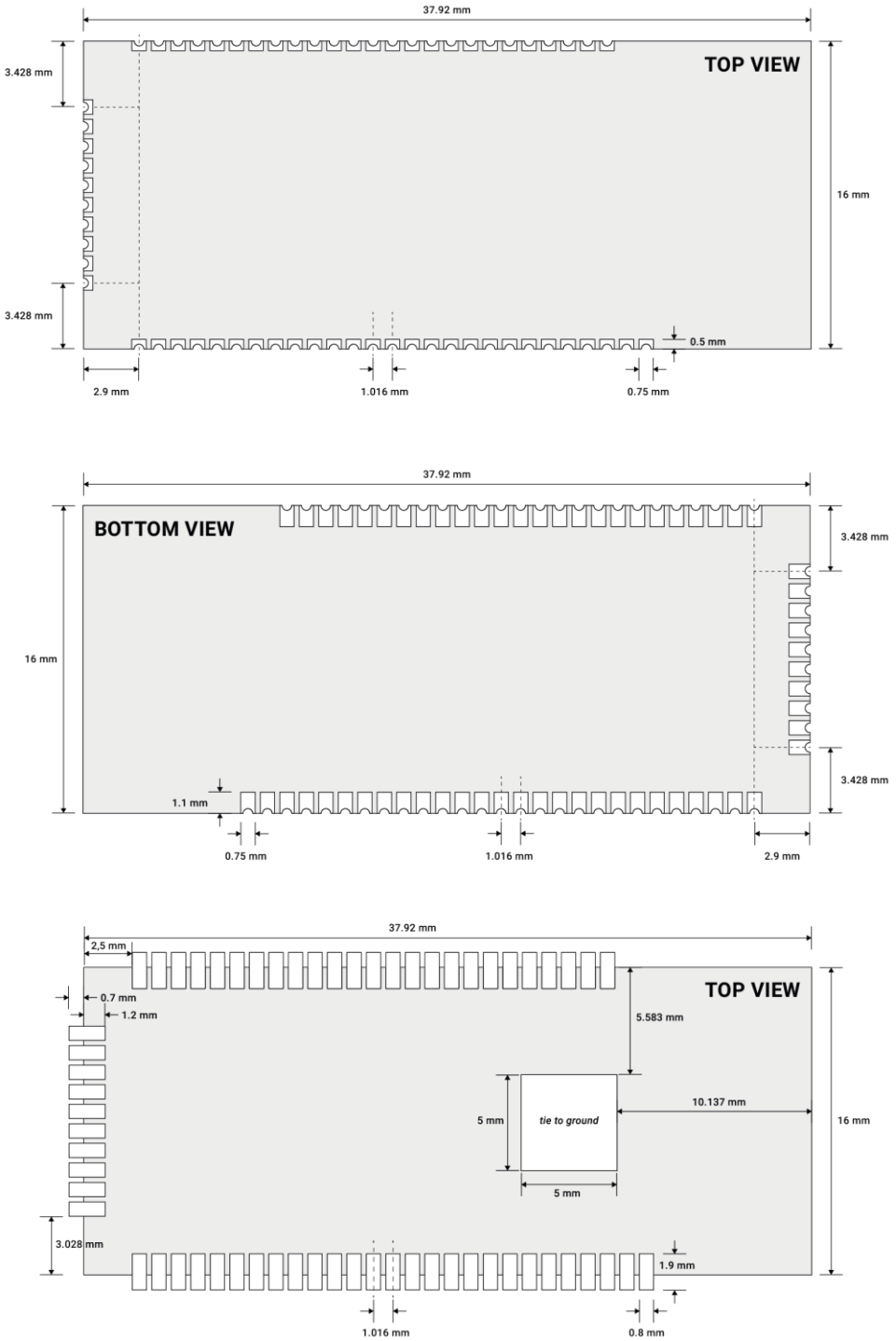
45	SAMD21	AIN4	3.3	I/O	PA06, EXTINT[6], AIN[6], AC_AIN[2], PTC_Y[4], SERCOM0/PAD[2], TCC1/WO[0]
46	SAMD21	AIN3	3.3	I/O	PA05, EXTINT[5], AIN[5], AC_AIN[1], PTC_Y[3], SERCOM0/PAD[1], TCC0/WO[1]
pin #	**Connected to**	**Main Function**	**Voltage**	**Direction**	**Note / Alt. Functions**
47	SAMD21	AIN2	3.3	I/O	PA04, EXTINT[4], ADC/VREFB, AIN[4], AC_AIN[0], PTC_Y[2], SERCOM0/PAD[0], TCC0/WO[0]
48	SAMD21	AIN1	3.3	I/O	PA03, EXTINT[3], ADC/VREFA, DAC/VREFA, AIN[1], PTC_Y[1]
49	SAMD21	AIN0	3.3	I/O	PA02, EXTINT[2], AIN[0], PTC_Y[0], DAC_VOUT
50	-	Ground pin	0	P	-
51	SAMD21	SWDIO	3.3	I/O	PA31, EXTINT[11], SERCOM1/PAD[3], TCC1/WO[1]
52	SAMD21	SWDCLK	3.3	I/O	PA30, EXTINT[10], SERCOM1/PAD[2], TCC1/WO[0], GCLK_IO[0]
53	ESP32	MTDO	3.3	I/O	GPIO15, ADC2_CH3, TOUCH3, RTC_GPIO13, MTDO, HSPICS0, HS2_CMD, SD_CMD, EMAC_RXD3
54	ESP32	MTCK	3.3	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
55	ESP32	MTDI	3.3	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
56	ESP32	MTMS	3.3	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
57	ESP32	GPIO 16	3.3	I/O	HS1_DATA4, U2RXD, EMAC_CLK_OUT
58	ESP32	GPIO 17	3.3	I/O	HS1_DATA5, U2TXD, EMAC_CLK_OUT_180
59	ESP32	Power ON	3.3	I	Disable the control of this pin from the MBC's SAMD21 before driving externally; LOW level enables the ESP, HIGH level disables.
60	ESP32	Reset	3.3	I	Disable the control of this pin from the MBC's SAMD21 before driving externally
61	ESP32	Boot enable	3.3	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
62	-	Ground pin	0	P	-

Pin description

Note: P for power pin, I/O for input/output, I for Input and O for Output

8. Module geometry and PCB land pattern

The image below shows the MBC's physical dimensions, the pitch and pad's dimensions. A tolerance of about ±0.1mm should be considered.



9. Programming and languages support

The MBC-WB01 is fully Arduino® IDE compliant.

Both the MCUs are supplied with a customized Arduino® Core in a master (SAMD21) – slave (ESP32) configuration, the typical and easiest configuration to use. Other kind of implementations/configurations are also possible; for example, the user can decide to use the ESP32 as a master and the SAMD21 as slave or use both chips in a multi-master configuration delegating specific tasks to one or the other MCU to provide more efficient and professional code.

A custom Arduino® IDE Platform has been specifically designed to allow the user to program both the MCUs directly through the USB device interface, in accordance with the SAMD21 bootloader implementation, simplifying the in-system firmware update procedure and avoiding the use of external tools.

An OTA interface has also been implemented into the ESP32 chip to ensure the same firmware update functionalities also with wireless connections.

For those who want to design robust professional C/C++ firmware, two debug interfaces are available on the board pinout (SWD for SAMD21 and JTAG for ESP32) allowing the user to gain full control over the code generated.

Languages supported are:

- C
- C++
- Python

10. Electrical characteristics

All typical values are measured at T = 25°C unless otherwise specified. All minimum and maximum values are valid across all operating temperatures and voltages unless otherwise specified.

Symbol	Description	Min.	Typ.	Max.	Unit
VCC_SAM	Input supply voltage for SAMD21	2.3	3.3	3.6	V
VCC_ESP	Input supply voltage for ESP32	2.3	3.3	3.6	V
ICC_SAM	Current absorption from SAMD21				
ICC_ESP	Current absorption from ESP32				
OPE_T	Operating temperature				

11. Ordering information

Example: MBC-WB01-E0APN

MBC	WB	01	E	0	A	P	N
Device family: Modular Brick Concept	**Features:** W: Wi-Fi B: BT/BLE	**HW revision**	**First MCU:** E: ESP32 0: No chip	**Second MCU:** 0: Cortex-M0+ 4: Cortex-M4	**Flash Size:** A: 2MB B: 8MB C: 16MB	**Ant. Option:** 0: I-PEX P: PCB Antenna	**Enhanced Security:** N: no S: yes

Federal Communication Commission Statement

• This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules see Ref. 4. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

– Reorient or relocate the receiving antenna

– Increase the separation between the equipment and receiver

– Connect the equipment into an outlet on a circuit different from that to which the receiver is connected

– Consult the dealer or an experienced radio/TV technician for help

• OEM integrators instructions

– The OEM integrators are responsible for ensuring that the end-user has no manual instructions to remove or install module

– The module is limited to installation in mobile or fixed applications, according to CFR 47 Part 2.1091(b)

– Separate approval is required for all other operating configurations, including portable configurations with respect to CFR 47 Part 2.1093 and different antenna configurations

• User guide mandatory statements

– User's instructions of the host device must contain the following statements in addition to operation instructions:

* “This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation”

* “Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment”

• FCC RF Exposure requirements

– User's instructions of the host device must contain the following instructions in addition to operation instructions:

Avoid direct contact to the antenna, or keep it to a 20 cm minimum distance while using this equipment. This device must not be collocated or operating in conjunction with another antenna or transmitter.

This module has been designed to operate with antennas having a maximum gain of 1 dBi. Antennas having a gain greater than 1 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

Test Board: Model: MBC-WB

FCC end product labelling

The final ‘end product’ should be labelled in a visible area with the following:
Contains TX FCC ID: 2ATX7-MBC-WB01 to reflect the version of
the module being used inside the product.
Applicable Standard: 15.247 and 15.249.
Test mode: Bluetooth LE GFSK, Bluetooth EDR GFSK, Pi/4 DQPSK, 8DPSK
The modular transmitter is only FCC authorized for the specific rule parts
(i.e., FCC transmitter rules) listed on the grant, and that the host product
manufacturer is responsible for compliance to any other FCC rules that apply
to the host not covered by the modular transmitter grant of certification.