FSC-BT906

4.2 Dual Mode Bluetooth Module Data Sheet

Document Type: FSC-BT906

Document Version: V1.8

Release Date: April.30. 2019

Release Record

Version Number	Release Date	Comments
Revision 1.0	2016-08-27	First Release
Revision 1.1	2016-09-21	Update the circuit diagram
Revision 1.2	2016-12-08	1, modify the pin definition and application circuit diagram 2, increase the electric performance parameters
Revision 1.3	2018-02-26	Modify the 9,10,14,27,28,31 pin description
Revision 1.4	2018-05-05	Modify Bluetooth Version: Upgrade from BT4.0 to BT4.2
Revision 1.5	2019-02-22	Clarify HID/SPP profiles.
Revision 1.6	2019-08-29	Add certificate picture
Revision 1.7	2019-10-18	Feature update
Revision 1.8	2020-04-30	Increase power consumption parameters

1. INTRODUCTION

FSC-BT906 is a bluetooth 4.2 Smart Ready device (with BR/EDR & LE support simultaneou sly) . It is a small form factor, highly power and highly economic Bluetooth radio module that allows OEM to add wireless capability to their products. The module supports multiple interfaces that make it simple to integrate into fully certified embedded Bluetooth solutions.

With AT programming interfaces, designers can easily customize their applications to support different Bluetooth profiles, such HS/HF, A2DP, AVRCP, OPP, DUN, SPP, and etc. The module supports Bluetooth® Enhanced Data Rate (EDR) and delivers up to 3 Mbps data rate for distances to 10M.

The module is an appropriate product for designers who want to add wireless capability to their products. The supported remote devices' OS are iOS, Android, and Windows.

1.1 Block Diagram

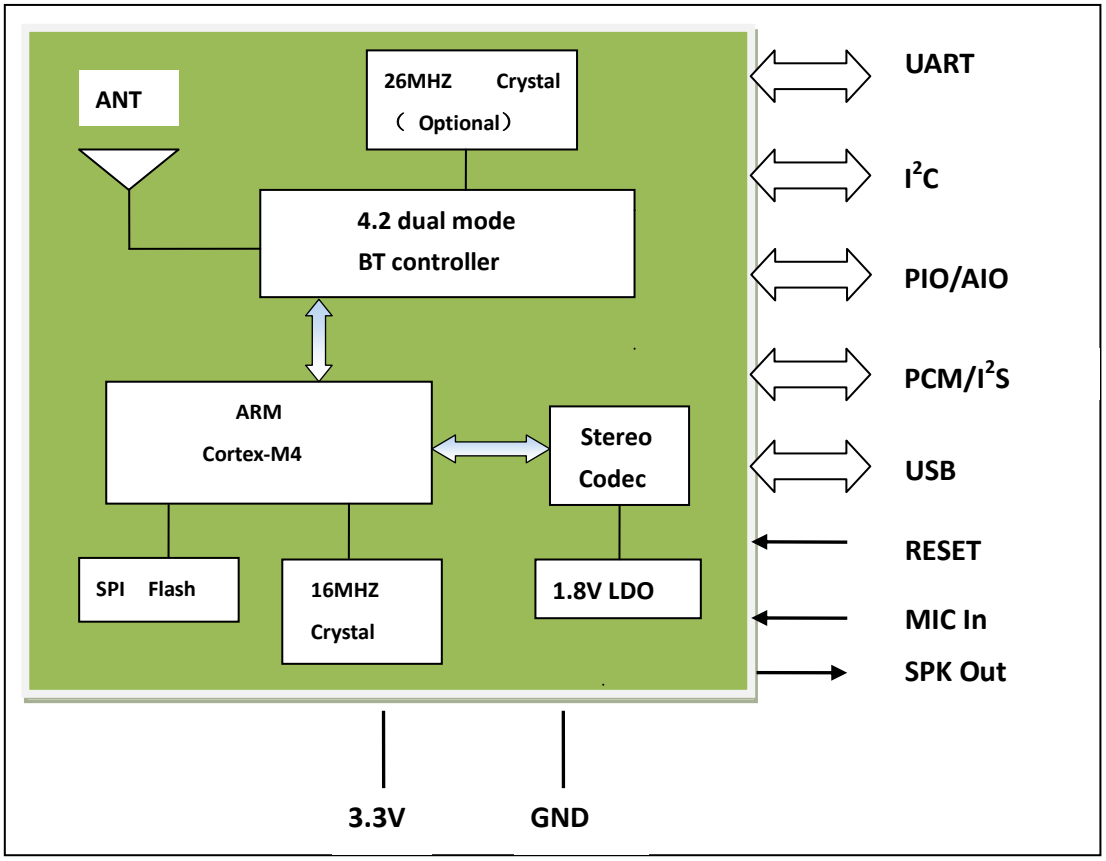


Figure 1

1.2 Feature

- Fully qualified Bluetooth 4.2/3.0/2.1/2.0/1.2/1.1
- Postage stamp sized form factor,
- Low power
- Class 1.5 support(high output power)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921Kbps,.
- UART, I^2C, PCM/I^2S data connection interfaces.
- Profiles including HS/HF, A2DP, AVRCP, OPP, DUN, SPP, HID,BLE
- USB 2.0 full-speed device/host/OTG controller
- RoHS compliant
- KC Certified
- Power Consumption In Sleep Mode (VDD_3V3 at 3.3 V)
  - Discoverable：1.73mA

- BR/EDR Connection：11.12mA
- LE Connection：2.46mA

◆ Power Consumption In Working Mode (VDD_3V3 at 3.3 V)

- Discoverable：11.56mA
- BR/EDR Connection：20.95mA
- LE Connection：12.08mA

1.3 Application

◆ Portable Multimedia players

◆ High quality stereo headsets

◆ High quality mono headsets

◆ Hands-free car kits

◆ Wireless speakers

◆ Bluetooth-Enable Automotive Dashboards

◆ VOIP handsets

◆ Analogue and USB Multimedia Dongles

◆ Medical devices

◆ Barcode and RFID scanners

2. GENERAL SPECIFICATION

General Specification	
ChipSet	BT4.2 Dual Mode
Product ID	FSC-BT906
Dimension	13mm(W) x 26.9mm(L) x 2.4mm(H) (Tolerance: ±0.1mm)
Bluetooth Specification	Bluetooth V4.2 (Dual Mode)
Power Supply	3.3 Volt DC
Output Power	8.5 dBm (Class 1.5)
Sensitivity	-88dBm@0.1%BER
Frequency Band	2.402GHz -2.480GHz ISM band

Modulation	8DPSK,DQPSK,GFSK
Baseband Crystal OSC	16MHz
Hopping & channels	1600hops/sec, 1MHz channel space,79 Channels(BT 4.2 to 2MHz channel space)
RF Input Impedance	50 ohms
Antenna	FPC Antenna
Interface	Data: UART (Standard), I^2C Audio: MIC In/SPK Out (Standard), PCM/I^2S Others: PIO, AIO, Touch sensor, PWM. USB 2.0
Profile	SPP, GATT(BLE Standard) MFI, Airsync, ANCS, iBeacon, HID HS/HF, A2DP, AVRCP
Temperature	-40ºC to +85ºC
Humidity	10%~95% Non-Condensing
Environmental	RoHS Compliant
MSL grade:	MSL 3
ESD grade	Human Body Model: Class-2 Machine Model: Class-B

Table 1

3. PHYSICAL CHARACTERISTIC

- Dimension： 13mm(W) x 26.9mm(L) x 2.4mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

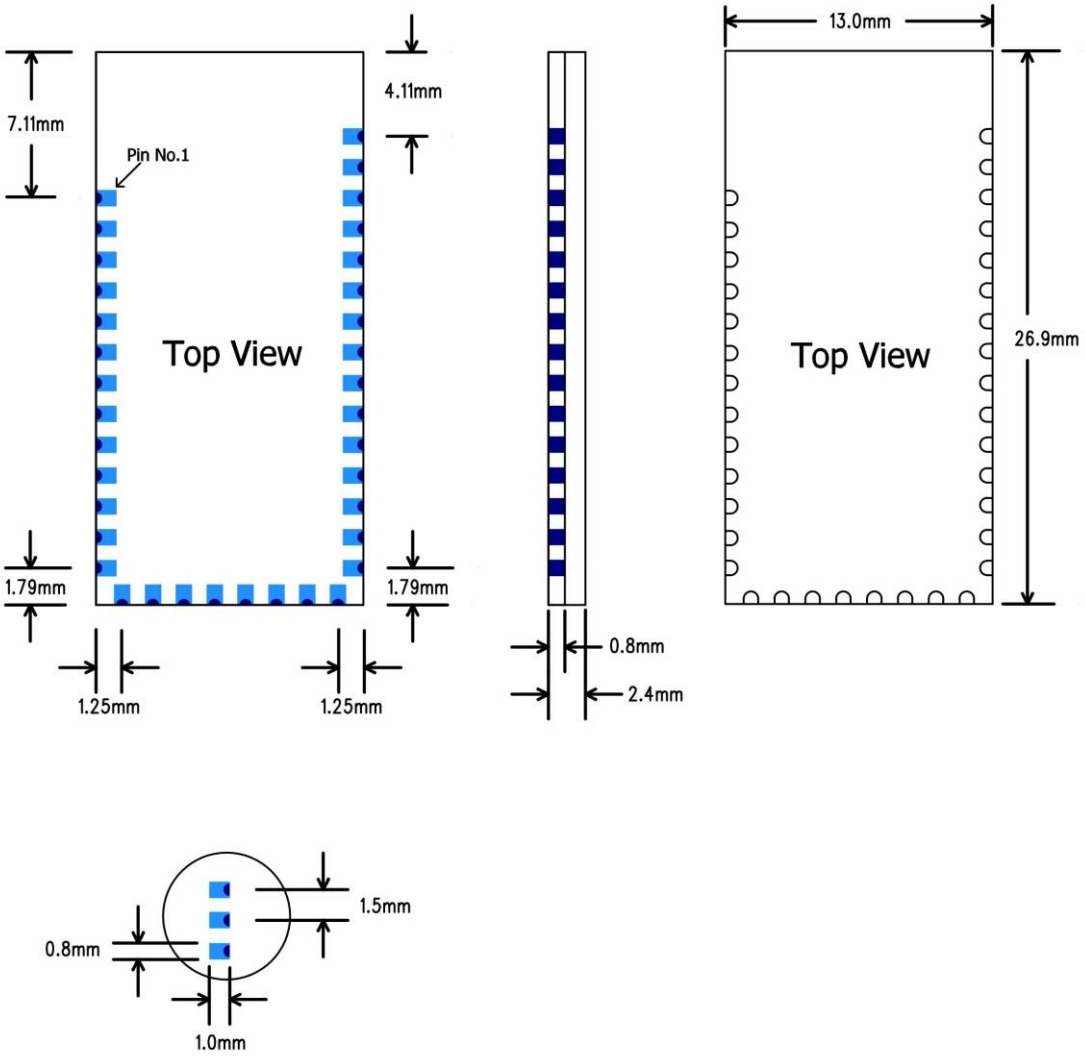

7.11mm
4.11mm
Pin No.1
Top View
1.79mm
1.79mm
1.25mm
1.25mm
0.8mm
2.4mm
13.0mm
Top View
26.9mm
1.5mm
0.8mm
1.0mm

Figure 2

4. PIN DEFINITION DESCRIPTIONS

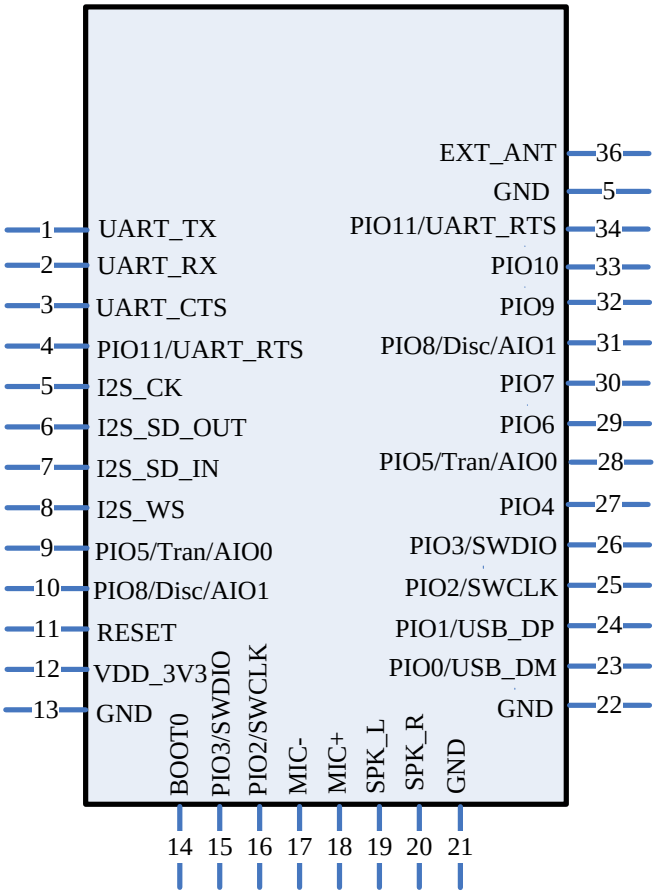


Figure 3: FSC-BT906 PIN Diagram

Pin NO.	Pin Name	Type	Pin Descriptions
1	UART_TX	CMOS output	UART data output
2	UART_RX	CMOS input	UART data input
3	UART_CTS	CMOS input	UART clear to send active low Alternative Function: Programmable input/output line
4	PIO11/UART_RTS	CMOS output/ Bi-directional	UART request to send active low Alternative Function: Programmable input/output line
5	I2S_CK	Bi-directional	I^2S CLK (BCLK)
6	I2S_SD_OUT	Bi-directional	I^2S Data Output
7	I2S_SD_IN	Bi-directional	I^2S Data Input
8	I2S_WS	Bi-directional	I^2S Chip Select For Synchronous Serial Interface

9	PIO5/Tran/AIO 0	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU change UART transmission mode.
10	PIO8/Disc/AIO 1	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU disconnect bluetooth.
11	RESET	CMOS input	Reset if low. Input debounced so must be low for >5ms to cause a reset.
12	VDD_3V3	VDD	Power supply voltage 3.3V
13	GND	VSS	Power Ground
14	BOOT0	CMOS input	The default is low. (internal 10K resistance drop) UART DFU Mode, Enabled at startup when set to high level, Disabled by default
15	PIO3/SWDIO	Bi-directional	Debugging through the data line(Default) Alternative Function: Programmable input/output line
16	PIO2/SWCLK	Bi-directional	Debugging through the clk line(Default) Alternative Function: Programmable input/output line
17	MIC-	Analogue Input	MIC- Input
18	MIC+	Analogue Input	MIC+ Input
19	SPK_L	Analogue Output	Right Output (Line or Headphone)
20	SPK_R	Analogue Output	Left Output (Line or Headphone)
21	GND	VSS	Power Ground
22	GND	VSS	Power Ground
23	PIO0/USB_D M	Bi-directional	Programmable input/output line Alternative Function: USB_DM
24	PIO1/USB_DP	Bi-directional	Programmable input/output line Alternative Function: USB_DP
25	PIO2/SWCLK	Bi-directional	Debugging through the clk line(Default) Alternative Function: Programmable input/output line
26	PIO3/SWDIO	Bi-directional	Debugging through the data line(Default) Alternative Function: Programmable input/output line
27	PIO4	Bi-directional	Programmable input/output line **Alternative Function: PA_EN pin, active high**
28	PIO5/Tran/AIO 0	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line.

			Alternative Function 2: Host MCU change UART transmission mode.
29	PIO6	Bi-directional	Programmable input/output line Alternative Function: I^2C Serial Clock input/output
30	PIO7	Bi-directional	Programmable input/output line Alternative Function:I^2C Serial Data input/output
31	PIO8/Disc/AIO 1	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU disconnect bluetooth.
32	PIO9	Bi-directional	Programmable input/output line Alternative Function: LED(Default)
33	PIO10	Bi-directional	Programmable input/output line Alternative Function: BT Status(Default)
34	PIO11/UART_ RTS	CMOS output/ Bi-directional	UART request to send active low Alternative Function: Programmable input/output line
35	GND	VSS	Power Ground
36	EXT_ANT	RF signal output	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact **ValueHD Corporation** for modification.

Table 2

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

The module should not continuously run under extreme conditions. The absolute maximum ratings are summarized in Table below. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Temperature/Voltage	Min	Max	Unit
Storage temperature	-40	85	°C
Operating temperature	-40	85	°C
Supply voltage	-0.3	3.6	V
Terminal voltages	VSS - 0.4	Vdd + 0.4	V

Table 3

5.2 Recommended Operating Conditions

The recommended operating conditions are summarized in Table below.

FSC-BT906 operates as low as 2.7 V supply voltage. However, to safely meet the USB specification for minimum voltage for USB data lines, minimum of 3.1 V supply is required.

Temperature/Voltage	Min	Typ	Max	Unit
Operating temperature	-40	20	85	°C
Supply voltage	2.7	3.3	3.6	V
Terminal voltages	0		Vdd	V

Table 4

5.3 Terminal Characteristics

FSC-BT906's terminal characteristics are summarized Table below.

Characteristics	Min	Typ	Max	Unit
I/O static characteristics				
VIL input logic level low	-	-	0.3V_{DD}	V
VIH input logic level high	0.4V_{DD}	-	-	V
V_{HYS} input hysteresis	-	10% V_{DD}	-	V
I_{lkg} input leakage current	-	-	±1	uA
R_{PU} Weak pull-up equivalent resistor	30	40	50	KΩ
R_{PD} Weak pull-down equivalent resistor	30	40	50	KΩ
C_{IO} pin capacitance	-	5	-	pF
VOL output logic level low	-	-	0,2	V
VOH output logic level high	Vdd -0.4	-	-	V
NRST pin characteristics				
VTH,res threshold voltage	1.65	1.8	VDD	V
RIRES input resistance	-	10	-	kΩ
CIRES input capacitance	-	100	-	nF

Table 5

5.4 Current Consumption

FSC-BT906's current consumption is summarized in Table below.

Operation Mode	Connection Type	Average	Unit
Discoverable	Inquiry/page:1280mS interval ,11.25mS window Advertising :1280mS interval	1.5	mA
ACL	Sniff Mode：1280mS interval,8 attempts,1 timeout	857	uA
	File transfer ,throughput	38	mA
SCO	Active Mode	36	mA
LE Connected	240mS Interval	860	uA
	File transfer ,throughput	22	mA
ACL & LE Both connected	ACL:1280mS interval LE:240mS interval	1.7	mA
Maximum Current	Send 2441MHZ fixed frequency signals	83.2	mA

Table 6

5.5 Radio Characteristics

5.5.1 Transmitter Radio Characteristics

TX output is guaranteed to be unconditionally stable over the guaranteed temperature range. Refer to Table below. Measurement conditions: T = 20℃, Vdd = 3.3V.

Item	Typical Value	Bluetooth Specification	Unit
Maximum output power1,2	+8.5	-6 to 20	dBm
RF power control range	33	≧16	dB
20dB bandwidth for modulated carrier	788	≦1000	kHz
Adjacent channel transmit power F = F0 ± 2MHz	-32	≦ 20	dBm
Adjacent channel transmit power F = F0 ± 3MHz	-46	-40	dBm
Adjacent channel transmit power F = F0 ± > 3MHz	-51	-40	dBm
Δf1avg Maximum Modulation	163	140<f1avg<175	kHz
Δf2max Maximum Modulation	158	115	kHz
Δf1avg / Δf2avg	0.91	≧0.80	-
Initial carrier frequency tolerance	13	≦75	kHz
Drift Rate	8	≦20	kHz/50μs
Drift (single slot packet)	7	≦ 25	kHz
Drift (five slot packet)	9	≦ 40	kHz

2nd Harmonic content	-65	≦ -30	dBm
3rd Harmonic content	-45	≦ -30	dBm

Table 7

5.5.2 Receiver Radio Characteristics

RX input is guaranteed to be unconditionally stable over the guaranteed temperature range. Refer to Table below. Measurement conditions: T = 20℃, Vdd = 3.3V.

	Frequency(GHz)	Typ.	Unit	Bluetooth Specification
Sensitivity@0.1% BER for all packet types	2.402	-87	dBm	<-75dBm
	2.441	-88	dBm	
	2.480	-86	dBm	
BER@ Maximum received signal(-20dBm)	2.402	0	dBm	<0.1%
	2.441	0	dBm	
	2.480	0	dBm	

Table 8

6. Interface Characteristics

6.1 UART Interface

Four signals are used to implement the UART function. When FSC-BT906 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below:

Signal name	Driving source	Description
UART-TX	FSC-BT906 module	Data from FSC-BT906 module
UART-RX	Host	Data from Host
UART-RTS	FSC-BT906 module	Request to send output of FSC-BT906 module
UART-CTS	Host	Clear to send input of FSC-BT906 module

Table 9

Possible UART Settings

Property	Possible Values
Baud Rate	1200bps to 921Kbps
Flow Control	RTS/CTS or None
Data bit length	8bits

Parity	None, Odd or Even
Number of Stop Bits	1 or 2

Table 10

Default Data Format

Property	Possible Values
Baud Rate	115.2Kbps
Flow Control	None
Data bit length	8bit
Parity	None
Number of Stop Bits	1

Table 11

6.2 PCM/I^{2}S Interface

The I^{2}S can be operated in master or slave mode, in full duplex and simplex communication modes and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^{2}S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The I^{2}S can be served by the DMA controller.

6.2.1 I^{2}S dynamic characteristics

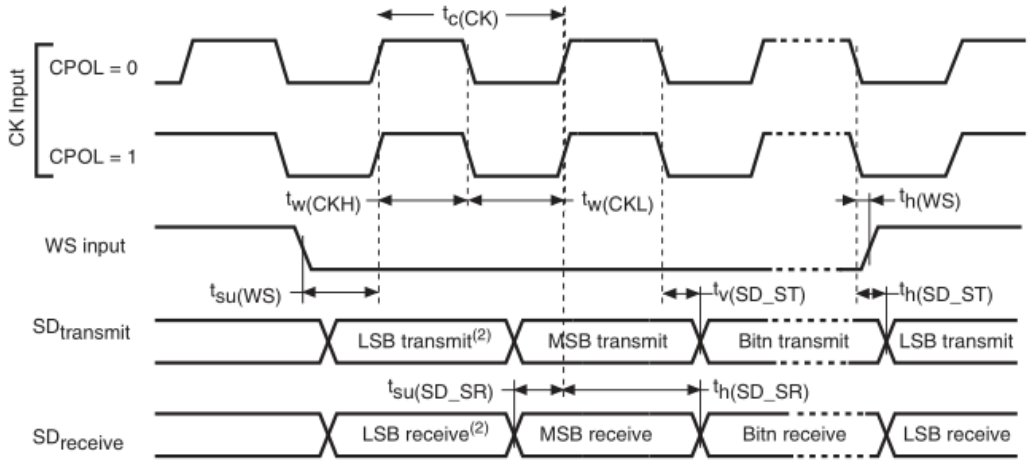
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	6	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	7.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	27	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Guaranteed by characterization.

2. The maximum value of 256xFs is 42 MHz (APB1 maximum frequency).

Table 12 I^2S dynamic characteristics

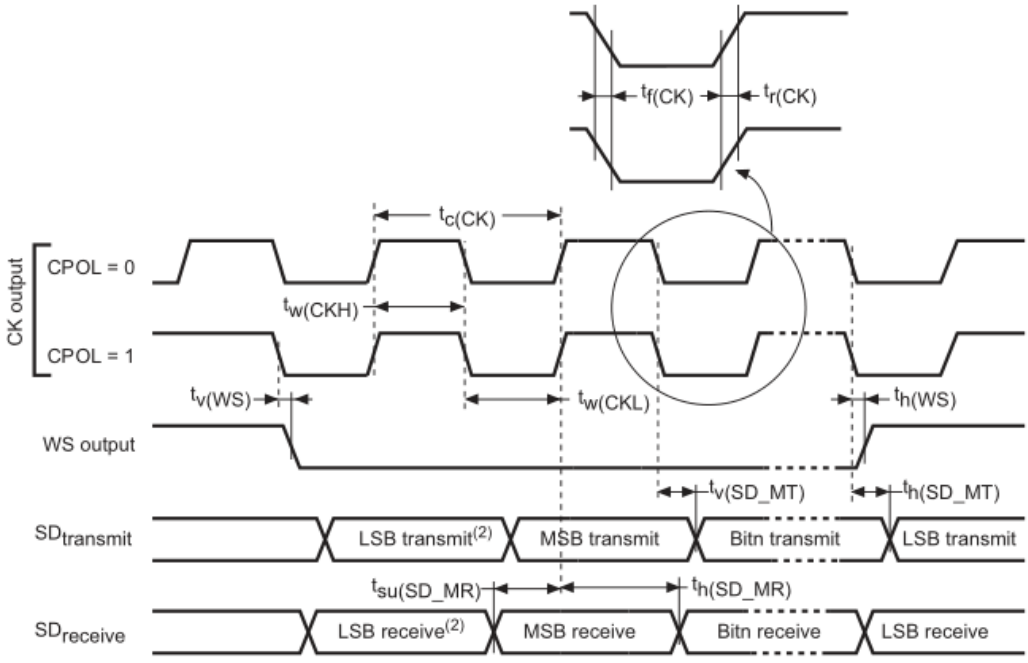
Note: Refer to the I2S section of the reference manual for more details on the sampling frequency(F_S).
f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F S maximum value is supported for each mode/condition.



360

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 4: I^2S slave timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent

before the first byte.

Figure 5: I²S master timing diagram (Philips protocol)

6.3 AIO , PIO lines and I²C

Up to 16 programmable bidirectional input/output (I/O) can be used.
Two general purpose analogue interface pin can be used.
PIO6 and PIO7 can be used as I2C interface.

Inter-Integrated Circuit Interface (I²C)

I²C bus interfaces can operate in multi-master and slave modes. They can support the standard (up to 100 kHz) and fast (up to 400 kHz) modes. The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative. They also support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SMBus 2.0/PMBus.
The devices also include programmable analog and digital noise filters

Analog to Digital Converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.
The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.
To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1,TIM2, TIM3, TIM4 or TIM5 timer.

6.4 USB Interface

USB 2.0 full-speed device/host/OTG controller with on-BT Module PHY.

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design.

Table 13: USB OTG FS startup time

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PIO0,PIO1 (USB_FS_DM/DP)	$V_{IN} = V_{DD}$	17	21	24	kΩ
R_{PU}		PIO0,PIO1 (USB_FS_DM/DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	

1. All the voltages are measured from the local ground potential.
2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V_{VDD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG FS drivers.

Table 14: USB OTG FS DC electrical characteristics

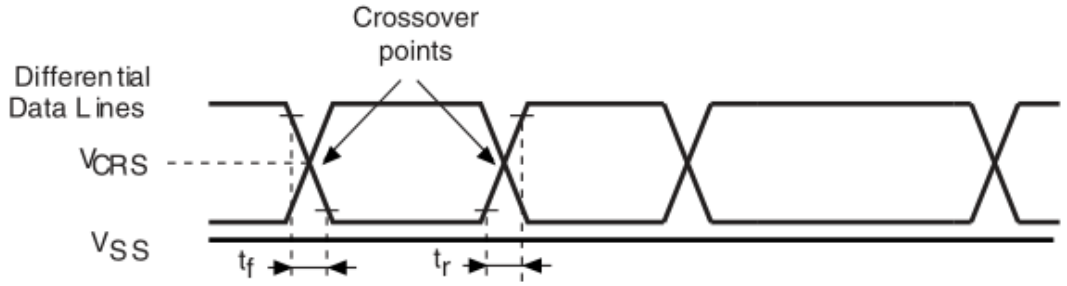


Figure 6: USB OTG FS timings: definition of data signal rise and fall time

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

Table 15: USB OTG FS electrical characteristics (1)

6.5 Audio Interface

FSC - BT906 built-in a ultra-low power, high quality stereo codec.

The Codec main features as follows:

- DAC with auto attenuate : 124dB SNR; without auto mute: 113dB SNR, (A-weighted) @ 0dB gain, 1.8V and -89dB THD @ 20mW and R L = 32Ω, DAC playback to headphone output mode.
- ADC : 101dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48kHz and -91dB THD , 1.8V, MIC gain 0dB, OSR 128x.
- Dynamic Range Compressor (DRC).
- Programmable Biquad filter.
- 1 Differential Analog Mic input, Line-input, or two single-ended Mic input.
- Class G Headphone Amplifier(28mW @ 32Ω,1% THD+N).

6.5.1 Audio Electrical Characteristics

Conditions: $V_{DD}A = V_{DD}C = 1.8V$; $V_{DD}B = V_{DD}MIC = 3.3V$.
R_L(Headphone)=32Ω, f=1kHz, MCLK=12.88MHz, unless otherwise specified.
Limits apply for T_A= 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
ISD	Shutdown Current	$V_{DD}A$ in Shutdown Mode	0.2	1	μA
		$V_{DD}A$ When $V_{DD}C$=1.2V	17.2		
		$V_{DD}B$	0.2	1	
		$V_{DD}C$	2	10	
		$V_{DD}MIC$	0.2	1	
I_{DD}	Standby Mode	MCLK off, Jack Insertion, IRQ enabled	5		μA

		Headphone Amplifier			
P_O	Output Power	Stereo R_L = 32Ω, DAC Input, CPV_{DD}= 1.8V, f=1kHz, 22kHz BW, THD+N = 1%(CSP package), w. headset switch	TBD		mW
		Stereo R_L = 32Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (QFN package), w. headset switch	28		mW
		Stereo R_L = 16Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (CSP Package), w. headset switch	TBD		mW
		Stereo R_L = 16Ω, DAC Input, CPV_{VDD} = 1.8V, f=1kHz, 22kHz BW, THD+N = 1% (QFN Package), w. headset switch	35		mW
THD+N	Total Harmonic Distortion + Noise	R_L = 32Ω, f=1kHz, P_O = 20mW, w. headset switch	-89		dB
SNR	Signal to Noise Ratio	VOUT = 1VRMS, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1kHz, A-Weighted), w. headset switch	113		dB
		VOUT = 1 V_{RMS}, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1kHz, A-Weighted, auto mute enabled, w. headset switch	124		dB
PSRR	Power Supply Rejection Ratio	f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} Input Referred, HP_GAIN = 0dB DAC Input, DAC_Gain = 0dB Ripple Applied to $V_{DD}A$	81		dB
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1kHz, MIC/GND Switching Off without HCS	88		dB
		Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1kHz, MIC/GND Switching On with HCS (QFN)	91		dB

Symbol	**Parameter**	**Conditions**	**Typical**	**Limit**	**Units (Limit)**
		Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1kHz, MIC/GND Switching On with HCS (CSP)	TBD		dB
	Interchannel Level Mismatch	Head phone Right and Left Channel Difference with 0dBFS Input Sweap from 20Hz to 20KHz	+/- 0.1		dB
	Frequency Response	F = 20Hz ~ 20KHz	+/-0.005		dB
e_{OS}	Output Noise	DAC_Gain = 0dB, HP_Gain = 0dB, f_S=48kHz, OSR_{DAC} = 128, A-Weighted	2.2		uV_{RMS}
	Out of Band Noise Level	BW=400Hz to 500KHz	-86		dB
V_{OS}	Output Offset Voltage	HP_Gain = 0dB, DAC_Gain= 0dB, DAC Input	0.1	±0.5	mV
	Power Consunption	No Load, No Signal, Amp on f_S = 48kHz, Stereo DAC On, Amp On, P_{OUT} = 0mW. R_L = 32Ω	5.7		mW
	Pop and Click Noise	Into or out of DAC to Headphone shutdown, Headphone Impedance &Crosstalk detection disabled	.1		mVrms
	Ground Switch ON resistance	ON resistance between JKR2 and GND or JKSLV and GND(QFN)	.09		ohm
		ON resistance between JKR2 and GND or JKSLV and GND(CSP)	TBD		ohm
	Loading Capacitance	External capacitance at HPL and HPR		<500	pF

ADC					
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1KHz, fs = 48KHz, Mono Differential Input	-91		dB
		MIC Input, MIC_GAIN = 30dB, Volume = 0dB, Vin=28.5Vrms, f=1k, Digital Gain = 0dB, Mono Differential Input	-80		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 8KHz, Mono Differential Input	101		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 8KHz, Mono Differential Input	98		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP} applied to V_{DD}A, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	78		dB
CMRR	Common Mode Rejection Ratio	Differential Input 100Vrms, PGA gain = 20dB, frequency sweep from 20Hz to 20KHz	64		dB
FS_{ADC}	ADC Full Scale Input Level	V_{DD}A= 1.8V	1		V_{RMS}
	Minimum Input Impedance		12		KOhm
	Frequency Response	f = 20Hz ~ 20KHz	+/-0.02		dB
	Power Consumption	No Load, No Signal, ADC on, PGA on, fS = 44.1kHz	5.4		mW

Table 16: Analogue Inputs to ADC out & Analogue Outputs

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

The re-flow profiles are illustrated in Figure 4 and Figure 5 below.

- Follow: IPC/JEDEC J-STD-020 C
- Condition:
  - Average ramp-up rate(217℃ to peak):1~2℃/sec max.
  - Preheat:150~200C,60~180 seconds
  - Temperature maintained above 217℃:60~150 seconds
  - Time within 5℃ of actual peak temperature:20~40 sec.
  - Peak temperature:250+0/-5℃ or 260+0/-5℃
  - Ramp-down rate:3℃/sec.max.
  - Time 25℃ to peak temperature:8 minutes max
  - Cycle interval：5 mintutes

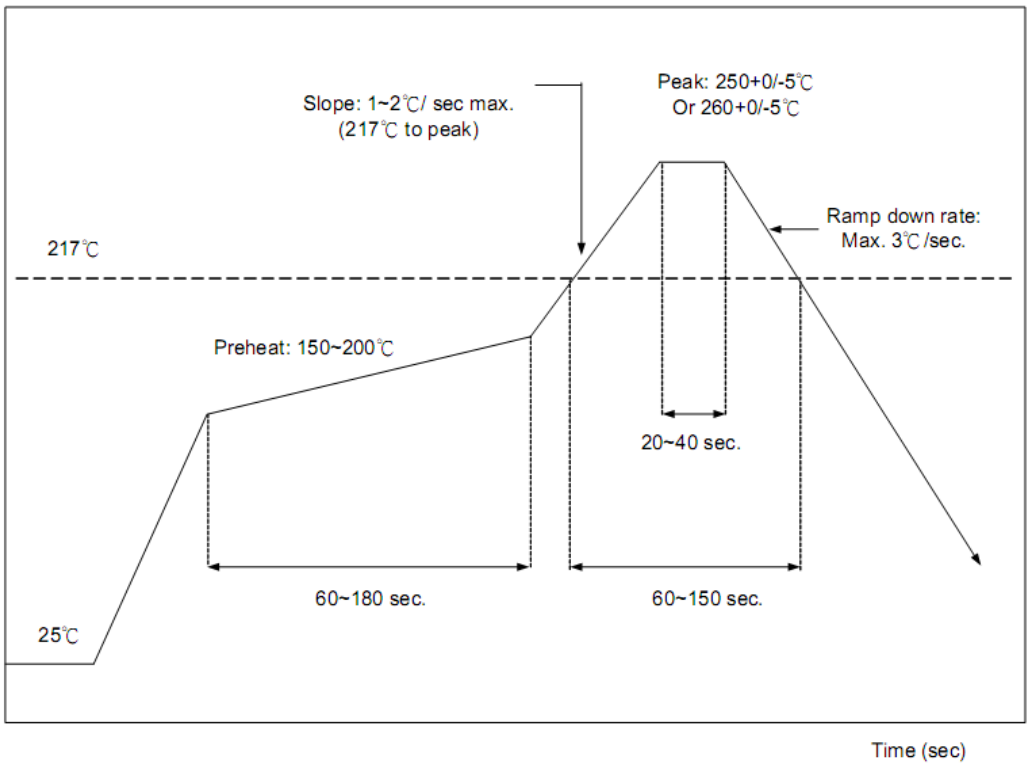


Figure 7: Typical Lead-free Re-flow Solder Profile

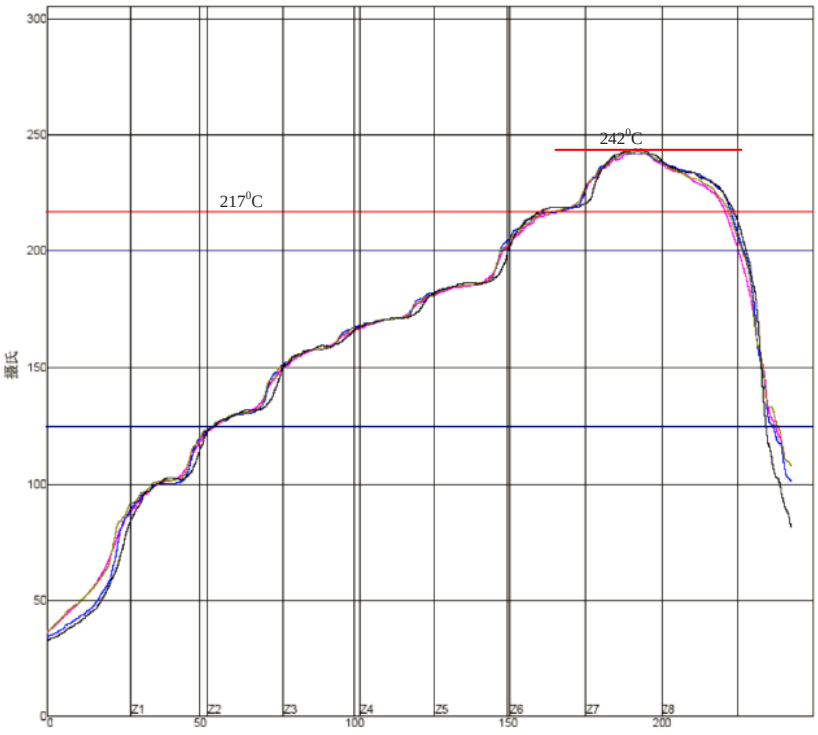


Figure 8: Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow.

FSC-BT906 will withstand up to two re-flows to a maximum temperature of 245°C.

8. Reliability and Environmental Specification

8.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the －40℃ space for 1 hour and then move to +85℃ space within 1minute, after 1 hour move back to －40℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

8.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

8.3 Desquamation test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

8.4 Drop test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

8.5 Packaging information

After unpacking, the module should be stored in environment as follows:

Temperature: 25℃ ± 2℃

Humidity: <60%

No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

9. Layout and Soldering Considerations

9.1 Soldering Recommendations

FSC-BT906 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat

transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

ValueHD Corporation will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

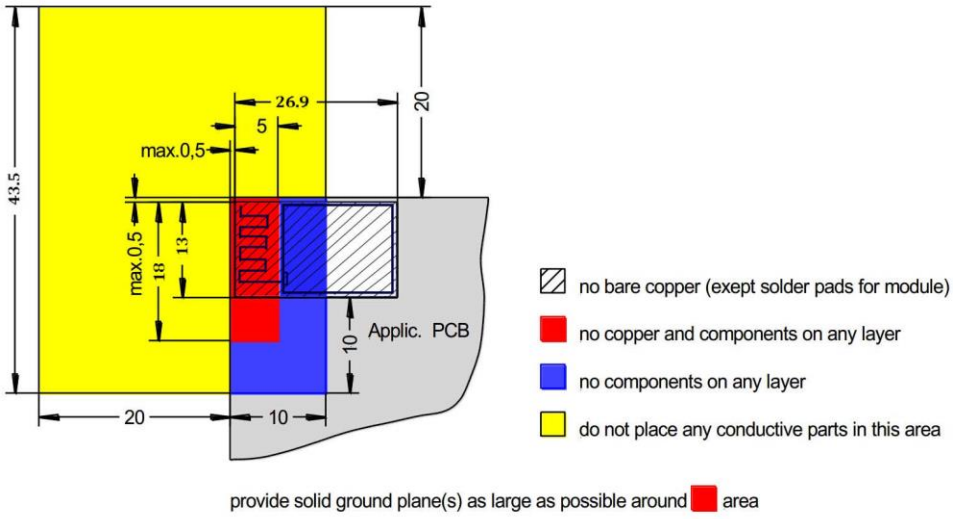


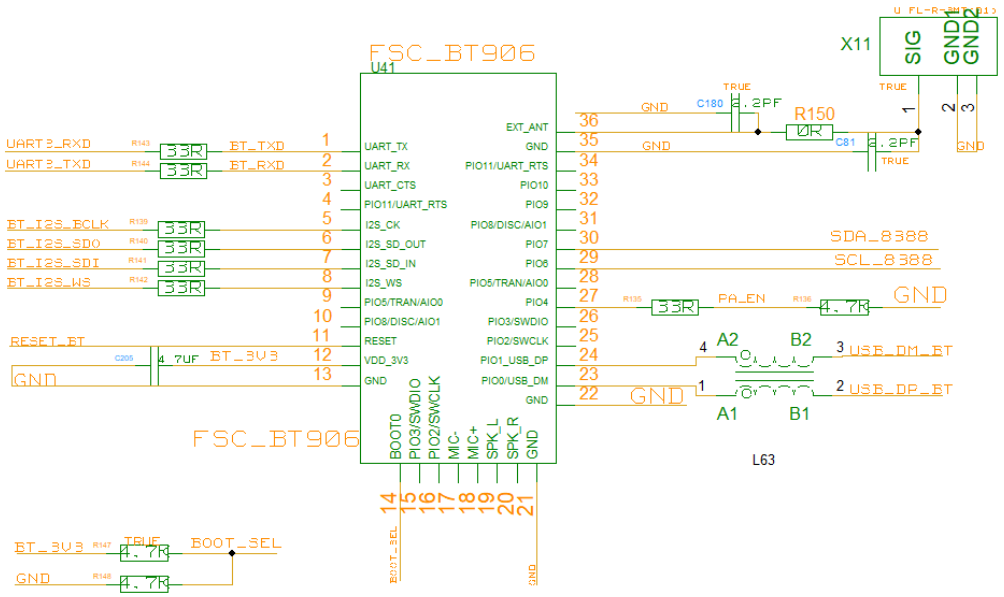
Figure 9: FSC-BT906 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line.

If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

10. Application Schematic



FCC statements

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE: The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications or changes to this equipment. Such modifications or changes could void the user's authority to operate the equipment.

This device is intended only for OEM integrators under the following conditions: 1.The antenna must be installed such that 20 cm is maintained between the antenna and users. 2. The transmitter module may not be co-located with any other transmitter or antenna. As long as the two conditions above are met, additional transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required for the installed module.

Important Note: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the Federal Communications Commission of the U.S. Government (FCC) and the Canadian Government authorizations are no longer considered valid and the FCC ID cannot be used on the final product. In these

circumstances, the OEM integrator shall be responsible for re-evaluating the end-product (including the transmitter) and obtaining a separate FCC authorization in the U.S. and canada.

OEM Integrators – End Product Labeling Considerations: This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: " Contains, FCC ID: 2ATFO-BT906 ". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

OEM Integrators – End Product Manual Provided to the End User: The OEM integrator shall not provide information to the end user regarding how to install or remove this RF module in end product user manual. The end user manual must include all required regulatory information and warnings as outlined in this document.

IC Warning

Le présent appareil est conforme aux CNR d'Industrie Canada applicables
aux appareils radio exempts de licence.
L'exploitation est autorisée aux deux conditions suivantes :
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage
radioélectrique subi, même si le brouillage est susceptible d'en
compromettre le fonctionnement.
Attention : exposition au rayonnement de radiofréquences
Cet équipement est conforme aux limites d'exposition aux
radiofréquences IC fixées pour un environnement non contrôlé et aux
Lignes directrices relatives à l'exposition aux radiofréquences (RF).
Co-location
Ce transmetteur ne peut pas être installé en colocation ou être utilisé
avec une autre antenne ou transmetteur, quel qu'en soit le type.