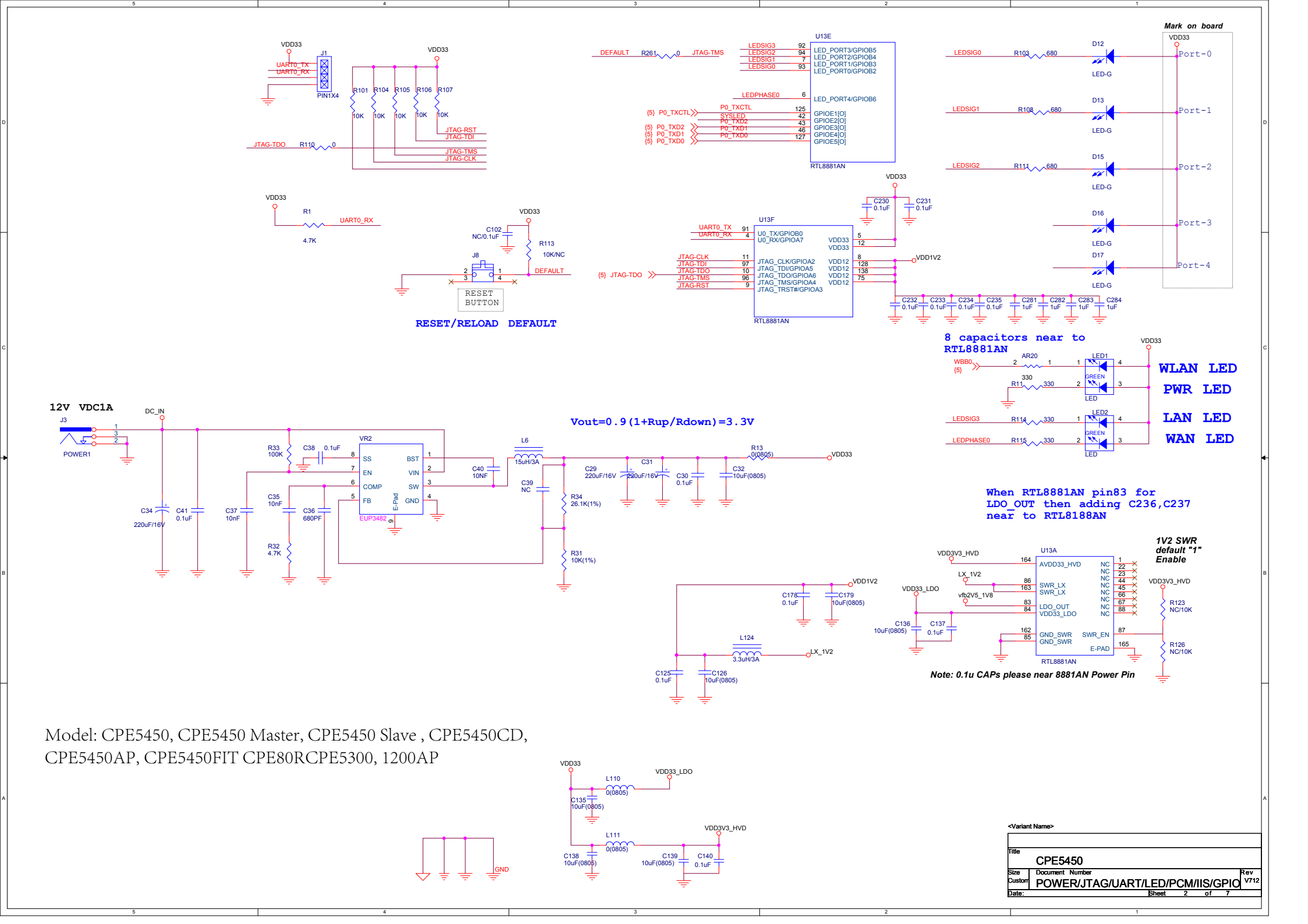
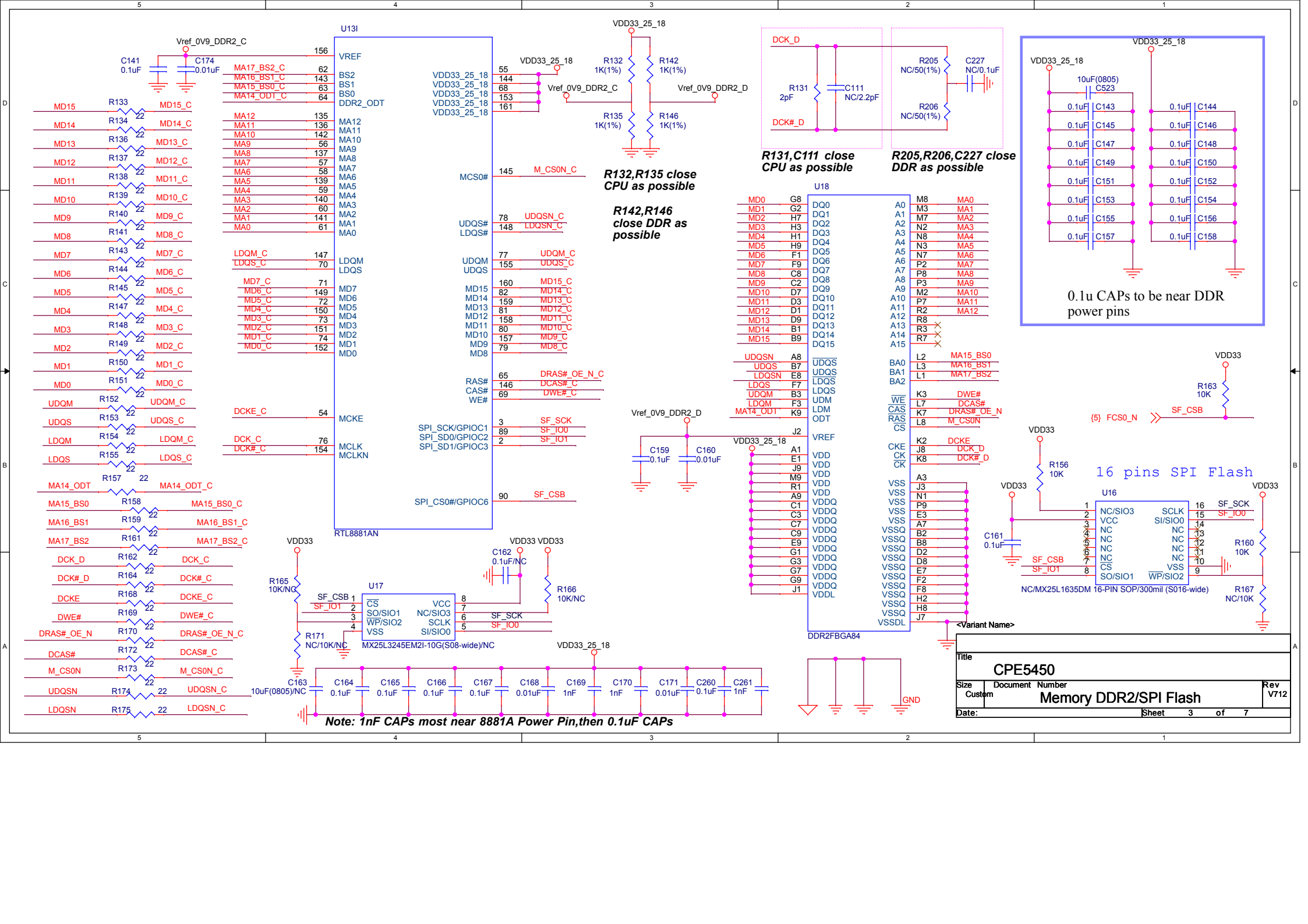
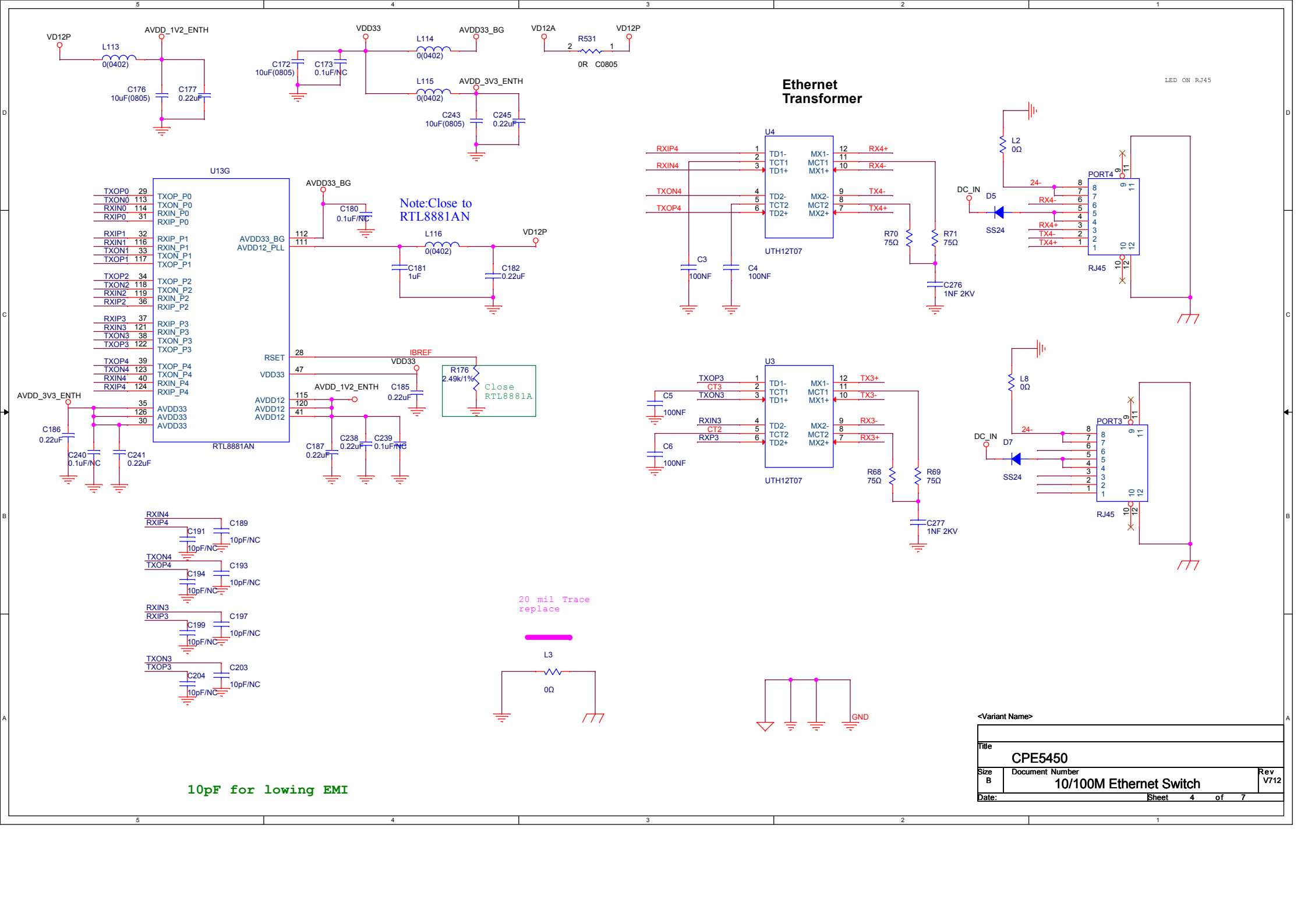
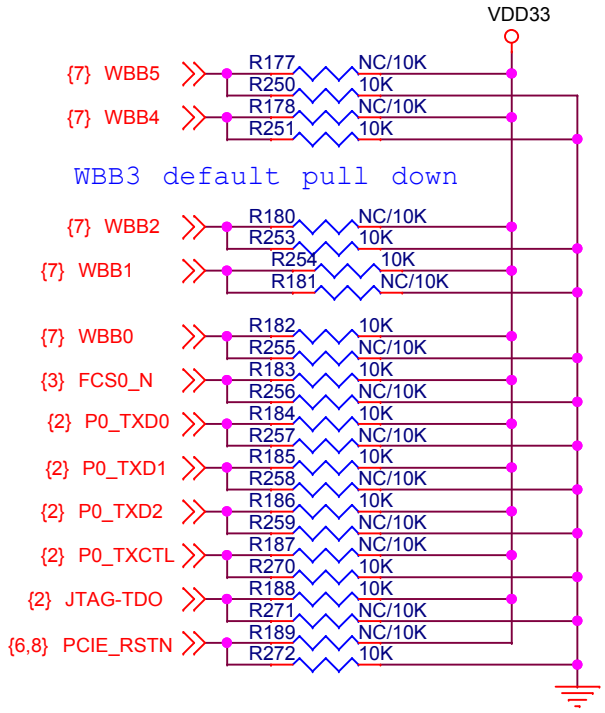

Mark on board
VDD33
J1
UART0_TX
UART0_RX
PIN1X4
R101 R104 R105 R106 R107
10K 10K 10K 10K 10K
JTAG-RST
JTAG-TDI
JTAG-TMS
JTAG-CLK
JTAG-TDO R110 0
U13E
DEFAULT R261 0 JTAG-TMS
LEDSIG3 92
LEDSIG2 94
LEDSIG1 7
LEDSIG0 93
LED_PORT3/GPIOB5
LED_PORT2/GPIOB4
LED_PORT1/GPIOB3
LED_PORT0/GPIOB2
LEDPHASE0 6
LED_PORT4/GPIOB6
P0_TXCTL 125
SYSLED 42
P0_TXD2 43
P0_TXD1 46
P0_TXD0 127
GPIOE1[O]
GPIOE2[O]
GPIOE3[O]
GPIOE4[O]
GPIOE5[O]
{5} P0_TXCTL
{5} P0_TXD2
{5} P0_TXD1
{5} P0_TXD0
RTL8881AN
LEDSIG0 R103 680
LEDSIG1 R108 680
LEDSIG2 R111 680
D12 D13 D15 D16 D17
LED-G
Port-0
Port-1
Port-2
Port-3
Port-4
R1
UART0_RX
4.7K
C102
NC/0.1uF
R113
10K/NC
J8
DEFAULT
RESET
BUTTON
RESET/RELOAD DEFAULT
U13F
UART0_TX 91
UART0_RX 4
U0_TX/GPIOB0
U0_RX/GPIOA7
JTAG-CLK 11
JTAG-TDI 97
JTAG-TDO 10
JTAG-TMS 96
JTAG-RST 9
JTAG_CLK/GPIOA2
JTAG_TDI/GPIOA5
JTAG_TDO/GPIOA6
JTAG_TMS/GPIOA4
JTAG_TRST#/GPIOA3
{5} JTAG-TDO
VDD33 5 12
VDD12 8 128 138 75
VDD1V2
C230 C231 0.1uF
C232 C233 C234 C235 0.1uF
C281 C282 C283 1uF
C284 1uF
RTL8881AN
8 capacitors near to RTL8881AN
WLAN LED
PWR LED
LAN LED
WAN LED
WBB0
{5}
AR20
R11 330
LED1
LED2
GREEN
LED
LEDSIG3 R114 330
LEDPHASE0 R115 330
12V VDC1A
J3
POWER1
DC_IN
C34 220uF/16V
C41 0.1uF
C37 10nF
C35 10nF
C36 680PF
R32 4.7K
R33 100K
C38 0.1uF
VR2
SS EN COMP FB BST VIN SW GND E-Pad
EUP3482
C40 10NF
L6 15uH/3A
C39 NC
R34 26.1K(1%)
R31 10K(1%)
Vout=0.9(1+Rup/Rdown)=3.3V
C29 220uF/16V
C31 220uF/16V
C30 0.1uF
C32 10uF(0805)
R13 0(0805)
When RTL8881AN pin83 for LDO_OUT then adding C236,C237 near to RTL8188AN
1V2 SWR default "1" Enable
U13A
VDD3V3_HVD 164
LX_1V2 86 163
vfb2V5_1V8
VDD33_LDO
LDO_OUT 83 84
GND_SWR 162 85
SWR_EN 87
E-PAD 165
AVDD33_HVD
SWR_LX
SWR_LX
VDD33_LDO
GND_SWR
GND_SWR
NC 1 22 23 44 45 66 67 88
C136 10uF(0805)
C137 0.1uF
R123 NC/10K
R126 NC/10K
RTL8881AN
Note: 0.1u CAPs please near 8881AN Power Pin
C178 0.1uF
C179 10uF(0805)
L124 3.3uH/3A
C125 0.1uF
C126 10uF(0805)
VDD1V2
LX_1V2
Model: CPE5450, CPE5450 Master, CPE5450 Slave , CPE5450CD, CPE5450AP, CPE5450FIT CPE80RCPE5300, 1200AP
VDD33
L110 0(0805)
VDD33_LDO
C135 10uF(0805)
L111 0(0805)
VDD3V3_HVD
C138 10uF(0805)
C139 10uF(0805)
C140 0.1uF
GND
<Variant Name>
Title
CPE5450
Size
Custom
Document Number
POWER/JTAG/UART/LED/PCM/IIS/GPIO
Rev
V712
Date:
Sheet 2 of 7


U13I
RTL8881AN
Vref_0V9_DDR2_C
Vref_0V9_DDR2_D
VDD33_25_18
VDD33
R132,R135 close CPU as possible
R142,R146 close DDR as possible
R131,C111 close CPU as possible
R205,R206,C227 close DDR as possible
0.1u CAPs to be near DDR power pins
U18
DDR2FBGA84
U16
16 pins SPI Flash
NC/MX25L1635DM 16-PIN SOP/300mil (S016-wide)
U17
MX25L3245EM2I-10G(S08-wide)/NC
Note: 1nF CAPs most near 8881A Power Pin,then 0.1uF CAPs
GND
<Variant Name>
Title
CPE5450
Size Custom
Document Number
Memory DDR2/SPI Flash
Rev V712
Date:
Sheet 3 of 7



<Variant Name>

Title	CPE5450	
Size B	Document Number 10/100M Ethernet Switch	Rev V712
Date:	Sheet 4 of 7	



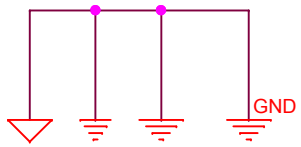
pin name	function name	function detail
PIN_WBB5 PIN_WBB4 PIN_WBB3	boot_sel[0] boot_sel[1] boot_sel[2]	boot_select[2:0] 000: SPI 100: ROM0_1 001: ROM1 101: ROM0_2 010: NFBI 110: ROM0_3 011: NAND 111: ROM0_4
PIN_WBB2	DRAM_TYPE[0]_INV	DRAM_TYPE[0]_INV 1=DDR1 0=DDR2 (Default)
PIN_WBB1	DRAM_TYPE[1]	DRAM_TYPE[1] 1=DDR 0=SDR (Default)
PIN_JTAG_TDO	Sel_40m	sel_40m 1=40MHZ 0=25MHZ(default)
PIN_PCIE_RSTN	Test_mode	strap_test_mode 1=TEST mode 0=Normal mode(default)
PIN_WBB0 PIN_FCS0_N	dbg_olt_mode[1] dbg_olt_mode[0]	dbg_olt_mode[1:0] 10: EXT PHYmode(Default) 11: Analog PHYmode 00: en_olt_auto_test 01: strap_ctl_sys_dbg_sel

Firmware Ctl	ck_m2x_freq_sel[0]
PIN_P_TXD0	ck_m2x_freq_sel[1]
PIN_P_TXD1	ck_m2x_freq_sel[2]
PIN_P_TXD2	ck_m2x_freq_sel[3]
PIN_P_TXCTL	ck_m2x_freq_sel[4]

DDR2 CLK default is 193.75MHz

ck_Mem_freq_sel[4:0] (MHZ)

00000:106.25	00001:112.5	00010:118.75	00011:127	00100:131.25	00101:137.5	00110:143.75	00111:150
01000:156.25	01001:162.5	01010:168.75	01011:175	01100:181.25	01101:187.5	01110:193.75	01111:200
10000:212.5	10001:225	10010:237.5	10011:250	10100:262.5	10101:275	10110:287.5	10111:300
11000:312.5	11001:325	11010:337.5	11011:350	11100:362.5	11101:375	11110:387.5	11111:400

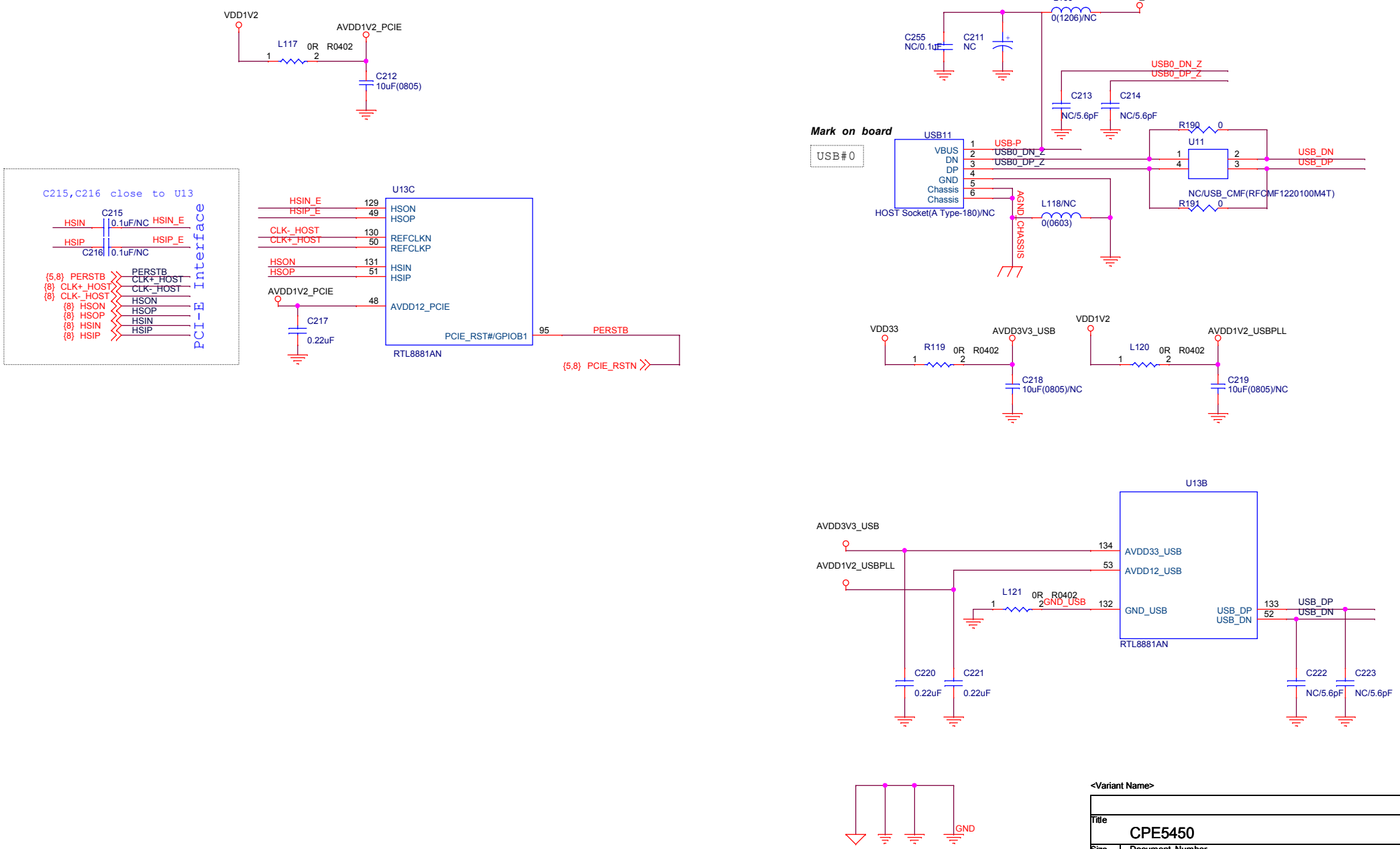


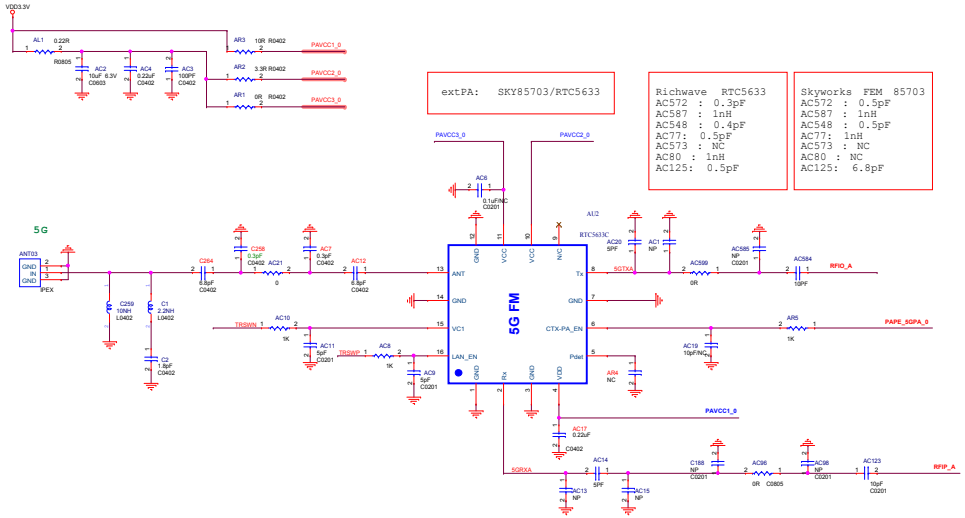
<Variant Name>

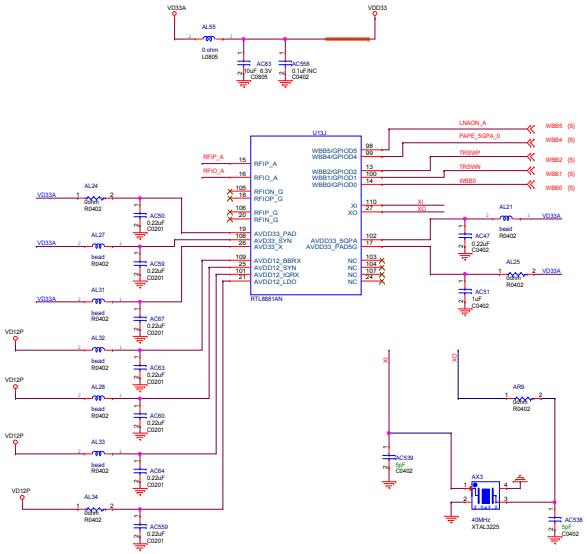
Title: CPE5450

Size: A | Document Number: Configure Interface | Rev: V712

Date: | Sheet 5 of 7

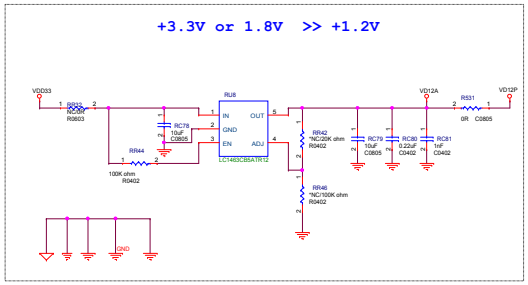

VDD1V2
L117 0R R0402
AVDD1V2_PCIE
C212 10uF(0805)
C215,C216 close to U13
C215 0.1uF/NC
C216 0.1uF/NC
HSIN
HSIP
HSIN_E
HSIP_E
PCI-E Interface
{5,8} PERSTB
{8} CLK+_HOST
{8} CLK-_HOST
{8} HSON
{8} HSOP
{8} HSIN
{8} HSIP
U13C
HSIN_E 129 HSON
HSIP_E 49 HSOP
CLK-_HOST 130 REFCLKN
CLK+_HOST 50 REFCLKP
HSON 131 HSIN
HSOP 51 HSIP
AVDD1V2_PCIE
48 AVDD12_PCIE
C217 0.22uF
PCIE_RST#/GPIOB1 95 PERSTB
RTL8881AN
{5,8} PCIE_RSTN
L100 0(1206)/NC
VDD5_ATX
C255 NC/0.1uF
C211 NC
USB0_DN_Z
USB0_DP_Z
C213 NC/5.6pF
C214 NC/5.6pF
Mark on board
USB#0
USB11
VBUS
DN
DP
GND
Chassis
Chassis
HOST Socket(A Type-180)/NC
USB-P
USB0_DN_Z
USB0_DP_Z
AGND
CHASSIS
L118/NC 0(0603)
R190 0
U11
R191 0
NC/USB_CMF(RFCMF1220100M4T)
USB_DN
USB_DP
VDD33
R119 0R R0402
AVDD3V3_USB
C218 10uF(0805)/NC
VDD1V2
L120 0R R0402
AVDD1V2_USBPLL
C219 10uF(0805)/NC
U13B
AVDD3V3_USB
AVDD1V2_USBPLL
134 AVDD33_USB
53 AVDD12_USB
L121 0R R0402
GND_USB
132 GND_USB
USB_DP
USB_DN
133 USB_DP
52 USB_DN
RTL8881AN
C220 0.22uF
C221 0.22uF
C222 NC/5.6pF
C223 NC/5.6pF
GND
<Variant Name>
Title
CPE5450
Size B
Document Number
USB/PCI-E
Rev V712
Date:
Sheet 6 of 7





Layout Note:
Crystal and 15pF caps MUST close to 8881A!

State	CTX	CRX	LEN
ANT – TX (Transmit Mode)	H	L	L
ANT – RX (Receive High Gain Mode)	L	H	H
ANT – RX (Receive Bypass Mode)	L	H	L



<variant_name>

Title	CPE5450	
Size: D	Document Number: BB+RF+RTL8188ER	Rev: V12
Date:	Sheet 7 of 7	