REDPINE SIGNALS

RS9113-N00-S1C

Overview:

The RS9113 modules' family is based on Redpine Signals' RS9113 ultra-low-power Convergence SoC. These modules offer dual-band 1x1 802.11n in a single device. They are high performance, long range and ultra-low power modules and include a multi-threaded MAC processor called ThreadArch®, digital and analog peripheral interfaces, baseband digital signal processor, calibration OTP memory, dual-band RF transceiver, dual-band high-power amplifiers, baluns, diplexers, diversity switch and Quad-SPI flash.

The modules are offered with two software architectures – hosted and embedded. The hosted variant (n-Link®) realizes a host-based architecture where the necessary MAC and PHY layers are implemented in the device to support high-performance, long range WLAN, applications in a 32-bit host processor over SDIO or USB interfaces. The embedded variants realize WLAN protocols along with Wi-Fi Direct™, WPA/WPA2-PSK, WPA/WPA2-Enterprise (EAP-TLS, EAP-FAST, EAP-TTLS, EAP-PEAP) and a feature-rich networking stack thus providing a fully-integrated solution for embedded low-end wireless applications. These modules can be connected to 8/16/32-bit host processors through SPI, UART, USB and USB-CDC interfaces.

The modules are available in two hardware footprints. One footprint type comes with an integrated antenna and a U.FL connector and the other footprint comes without an integrated antenna.

Applications:

- Smartphones, Tablets and e-Readers
- VoWi-Fi phones
- Smart meters and in-home displays
- Industrial automation and telemetry
- MP3 music and MP4 video players
- Medical devices
- Industrial monitoring and control
- Home and building automation
- Wireless Headset

Module Features:

WLAN:

- Compliant to single-spatial steam IEEE 802.11 b/g/n with 2.4 GHz band support.
- Support for 20MHz bandwidths.
- Transmit power up to +17dBm with integrated PA.
- Receive sensitivity of -97dBm.

General:

- FCC, IC, ETSI/CE Certified
- U.FL connector for external antenna connection.
- Dual external antenna for antenna diversit .
- Wireless firmware upgrade
- Options for Single supply of 3.0 to 3.6 V operationor multiple supplies for power saving .
- Operating temperature range: -40 o C to +85 o C

1. Overview

The RS9113 Connect-io-n® modules are M2M Combo modules based on Redpine Signals' RS9113 ultra-low-power Convergence SoC. They differ in terms of the features embedded in the module's firmware and their performance. The Connect-io-n® modules offer WLAN protocols along with Wi-Fi Direct™, WPA/WPA2-PSK, WPA/WPA2-Enterprise (EAP-TLS, EAP-FAST, EAP-TTLS, EAP-PEAP) and a feature-rich networking stack embedded in the device, thus providing a fully-integrated solution for embedded wireless applications. These modules can be interfaced to 8/16/32-bit host processors through SPI, UART, USB and USB-CDC interfaces. All three modules are offered with and without an integrated antenna. The module with the integrated antenna also offers a U.FL connector for connecting an external antenna with an option to select either one of them.

1.1 Block Diagram

The following figures are the block diagrams for the modules with and without the integrated antenna.

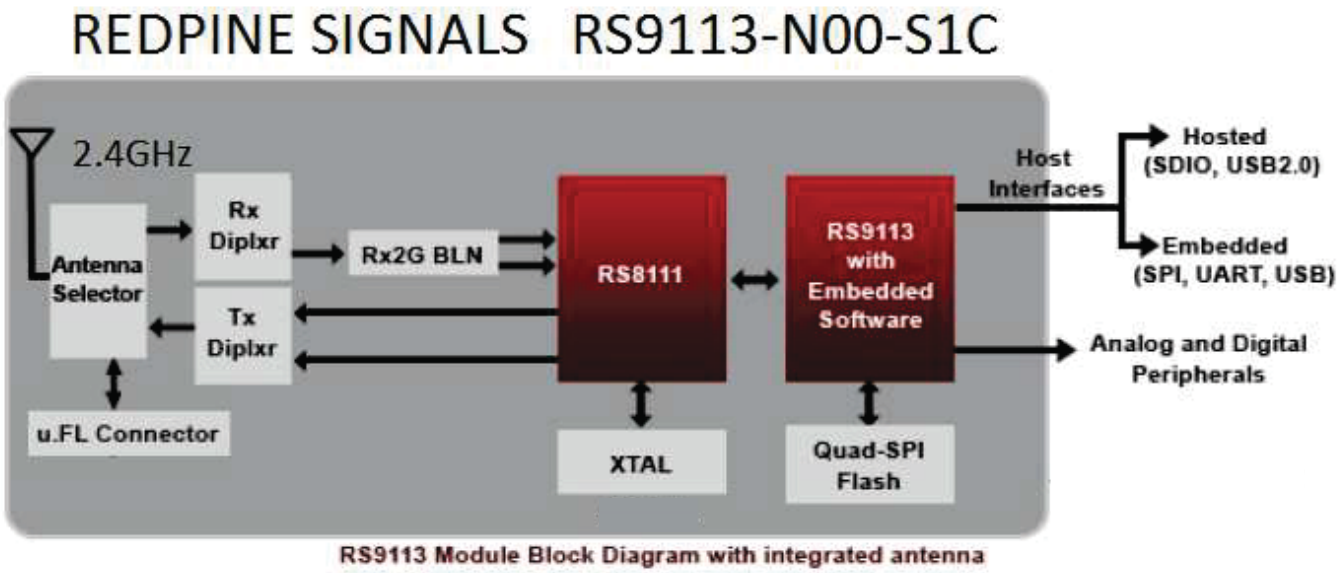
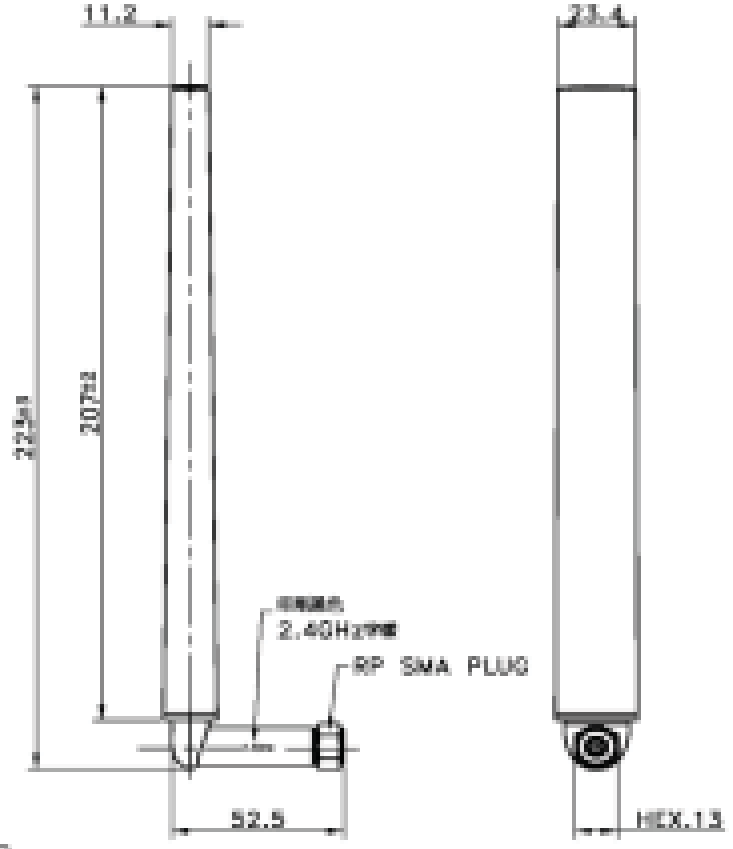


Figure 2: Block Diagram of RS9113 Module with Integrated Antenna

1.2 Antenna Specifications

Frequency Range	2.4~2.5 GHz	Antenna Cover	PC
Impedance	50Ω	Antenna Base	PC
VSWR	≤2.0	Connector	R-SMA
Return Loss	-9.54 dB Max	Color	White
Radiation	Omni	Operating Temp	-20℃~+65℃
Gain	3.86 dBi	Storage Temp	-25℃~+70℃
Polarization	Vertical		
Admitted Power	1W		

REV	ZONE	DESCRIPTION	ENG	APPROVED	DATE



Electrical Properties	
Frequency Range	2.4~2.5 GHz
Impedance	50Ω
V.S.W.R.	≤2.0
Radiation	Omni
Gain	2.0 dBi
Polarization	Vertical
Mechanical Properties	
Plug	RP-SMA
Connector	Male
Weight	g
Operating Temp.	-20℃~+60℃

	DATE: 2019/8/5	MAT'L:	Master Wave Technology CO.,LTD
	UNIT: mm	FINISH: WHITE	
	THIRD ANGLE PROJECTION	SCALE: 1/2	TITLE : 8623 Replacement Antenna
APPROVED BY:	CHECKED BY:	DESIGNED BY: Mars	DRAWN BY:
		WEIGHT: 53.5g	MODEL NO. : 98623MRSX004 REV 00
			PART NO. :

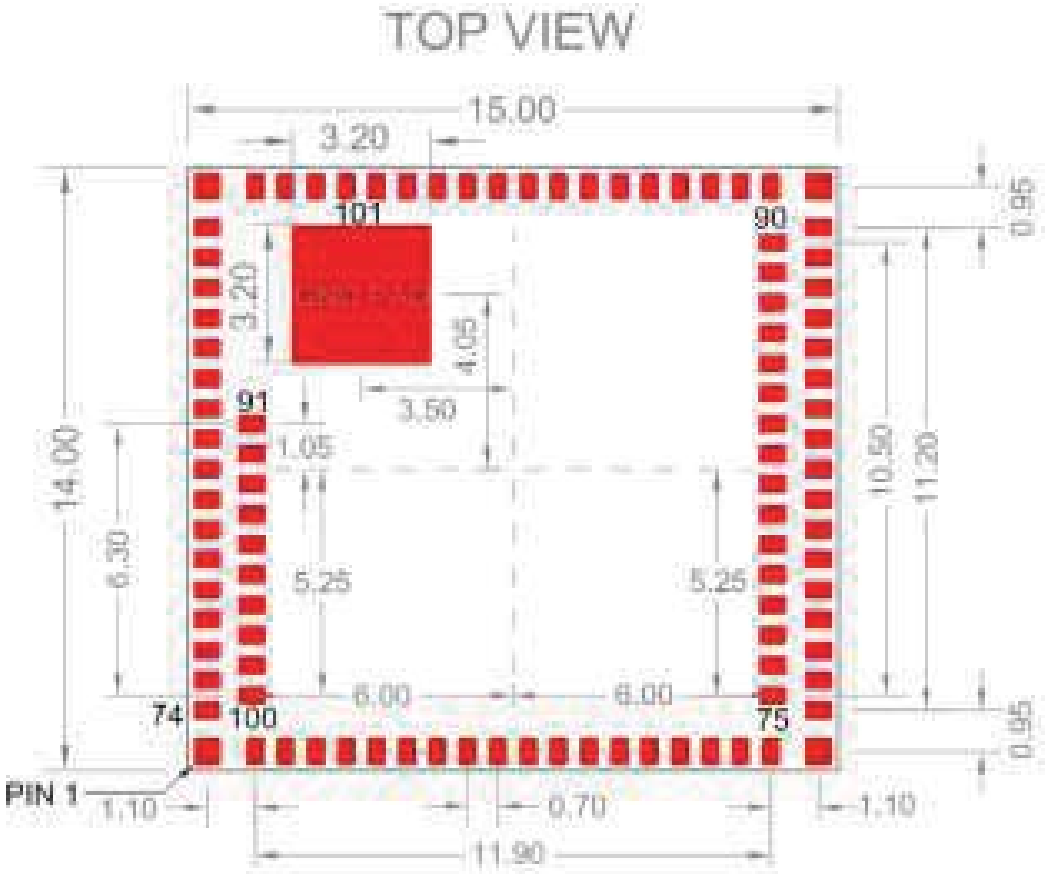
2. Features

The table below lists the features supported by the Connect-io-n® module.

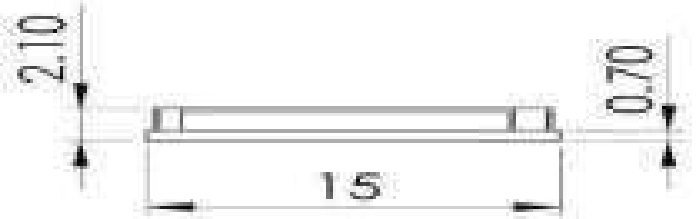
No.	Feature	Connect-io-n®
1	Wireless Protocols	IEEE 802.11b, 802.11g, 802.11n
2	Operational Modes Supported	Wi-Fi Access Point with support for upto 8 clients and limited packet buffering Wi-Fi Client
3	WLAN Bandwidth	20 MHz
4	WLAN Data Rates	802.11b: 1, 2, 5.5, 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n: MCS0 to MCS7 with and without Short GI
5	WLAN Operating Frequency Range	2412 MHz – 2462 MHz
6	WLAN Modulation	OFDM with BPSK, QPSK, 16-QAM, and 64-QAM 802.11b with CCK and DSSS
7	WLAN Transmit Power	19.05 dbm
8	WLAN Receive Sensitivity	-97 dBm
9	Deep Sleep Current Consumption	< 10 µA in disconnected state < 30 µA in connected state
10	Host Interfaces	SPI UART USB 2.0/1.1 USB-CDC
11	SPI Host Interface	Maximum clock speed of 80MHz
12	UART Host Interface	Supported Baud Rates (bps): 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 Support for AT and Binary Commands for Configuration and Data Transfer Support for 8 bits encoding Support for 1 stop bit Support for Auto Flow Control Support for Transparent Mode
13	Wireless Security Features	WPA/WPA2-Personal WPS (embedded in the device)

14	Advanced Security Features	PUF Based Security AES 128/256-bit RSA
15	Application throughputs	P Upto 70 Mbps TCP With embedded TCP/IP Stack: Upto 25 Mbps UDP Upto 20 Mbps TCP With TCP/IP Stack in Host: Upto 40 Mbps UDP Upto 25 Mbps TCP
16	Operating Temperature Range	-40 o C to +85 o C
17	Supply Voltages and Options	Single 3.0 to 3.6V Supply
18	WLAN Features	Dynamic selection of data rate depending on the channel statistics. Hardware accelerators for WEP 64/128-bit, TKIP, AES and WPS Support for WMM Support for AMPDU Aggregation/De-aggregation and AMSDU De-aggregation
19	TCP/IP Features	TCP/IP Stack with IPv4, IPv6 HTTP Server/Client Static and Dynamic Webpages with JSON Objects (for HTML Server) DHCP Server/Client for IPv4 and IPv6 HTTPS Server/Client ICMP
20	Antenna type	Dipole antenna
21	Tx Power	15.86dBm(Min), 17.67(Max)
22	Spurious emissions	37.51 dBµV/m @ 3m
23	Operating fundamental frequencies	2412MHz, 2437MHz, 2462MHz

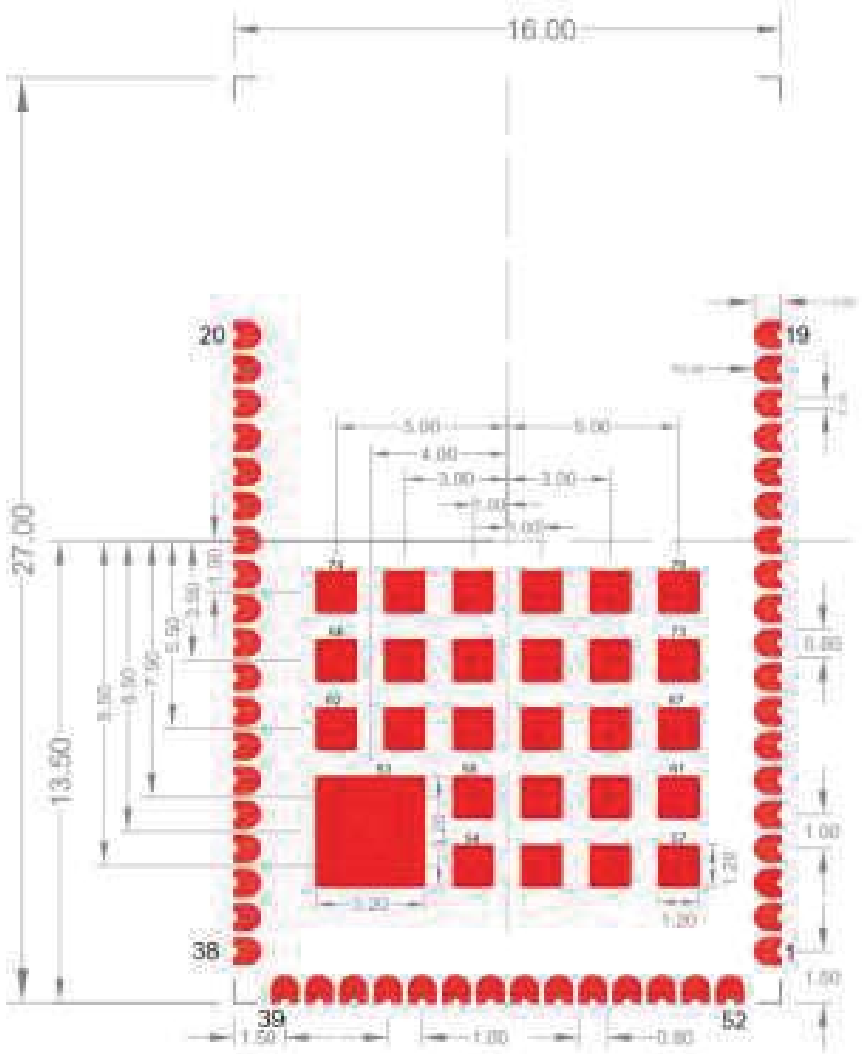
3. Package Description



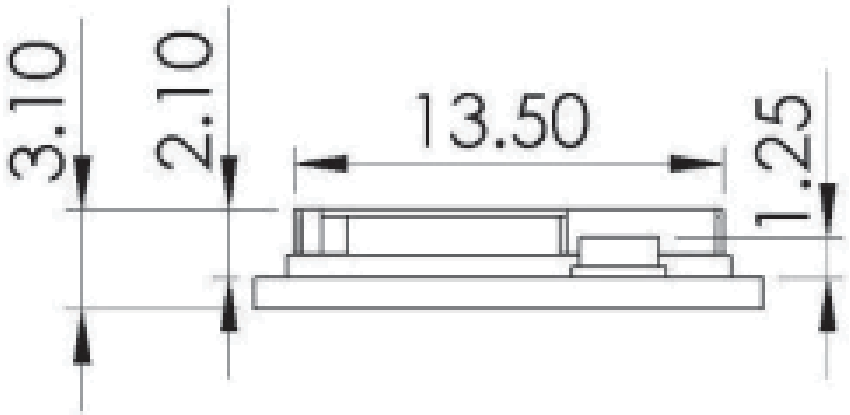
PAD SIZE 0.40mm x 0.60mm
CORNERPAD SIZE 0.60mm x 0.60mm
PAD PITCH:0.70mm
ALL DIMENSIONS ARE IN mm



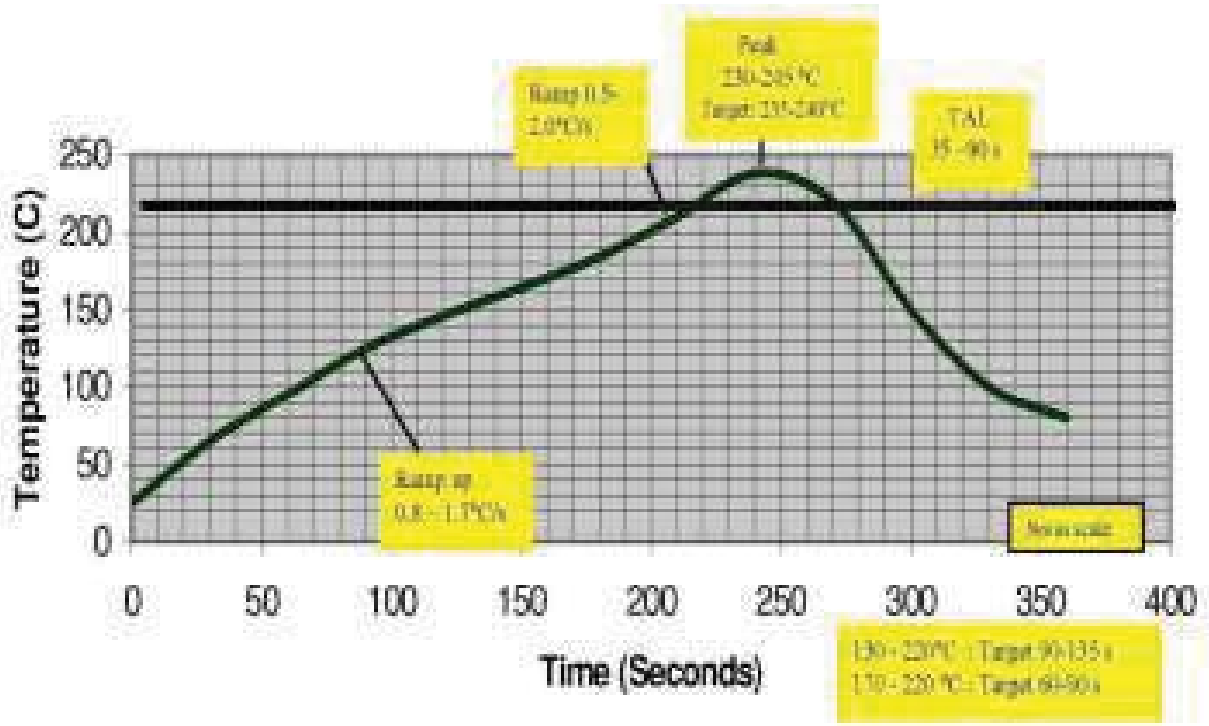
Top view



All Dimensions are in mm

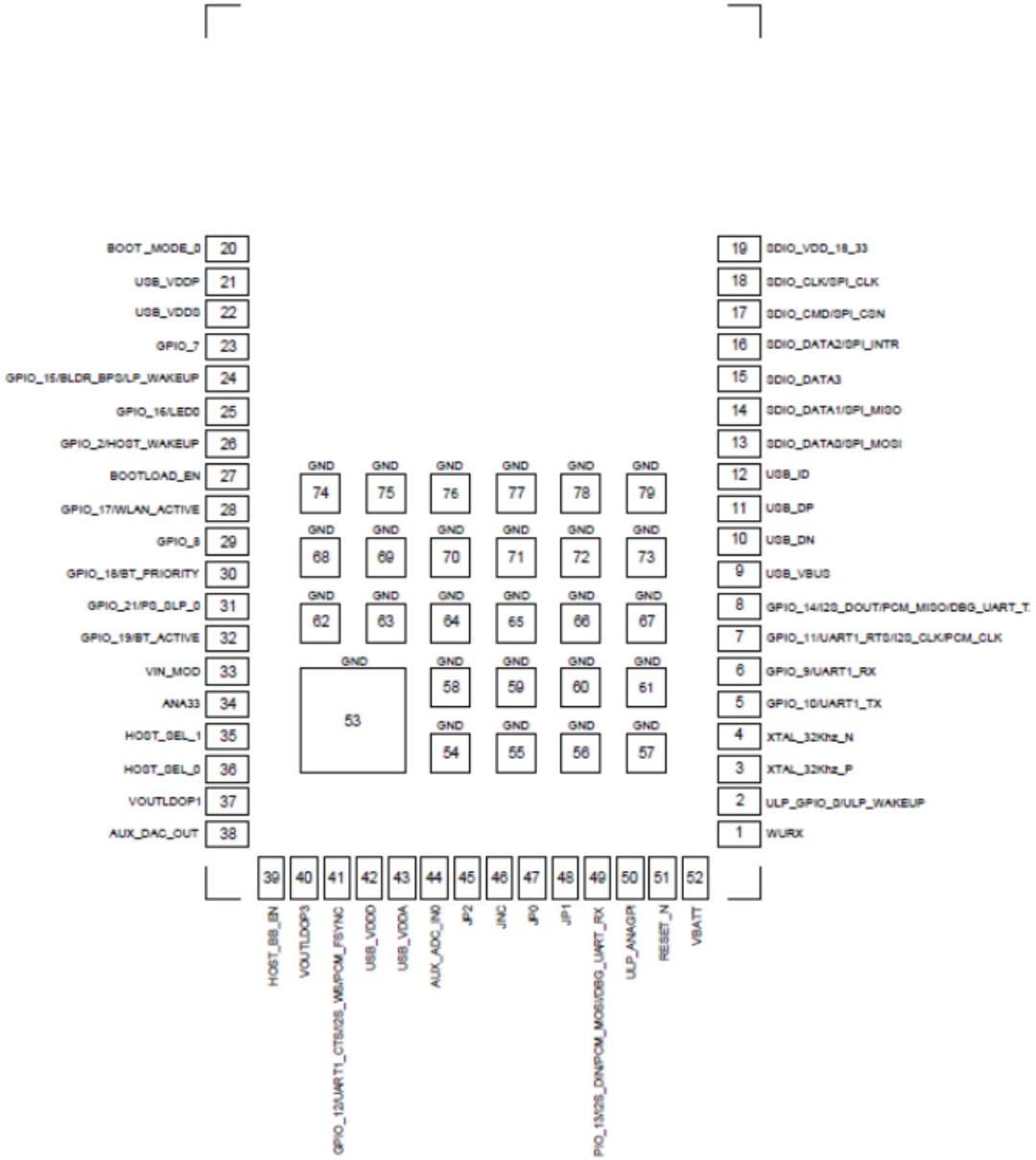


4. Recommended Reflow Profile



Note: The profile shown is based on SAC 305 solder (3% silver, 0.5% copper). We recommend the ALPHA OM-338 lead-free solder paste. This profile is provided mainly for guidance. The total dwell time depends on the thermal mass of the assembled board and the sensitivity of the components on it. The recommended belt speed is 50-60 Cm/Min. A finished module can go through 2 more reflow processes

5. Pinout of Module with Integrated Antenna



6. Pin Description

This section describes the pins of the two packages of the RS9113 Module family. The information contained here should be used along with the information in the Module Integration Guide.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
Control and RF Interface					
1.	RESET_N	74	51	Input	Active-low asynchronous reset signal. The minimum reset assertion time is 20 ms.
2.	RF_OUT_2	32	---	RF In/RF Out	Default Antenna port. Connect to Antenna with a 50 Ω impedance. Refer to Module Integration Guide for details.
3.	RF_OUT_1	37	---	RF In/RF Out	Used in the case of Antenna Diversity[26]. If used, connect to Antenna with a 50 Ω impedance and follow same guidelines as RF_OUT_2 from Module Integration Guide. If unused, leave unconnected.
Power and Ground Interface[27]					
4.	VIN_MOD	49	33	Input	3.3V Digital Power Supply
5.	ANA33	50	34	Input	1.9V to 3.6V Analog Power Supply
6.	SDIO_VDD_18_33	27	19	Input	3.3V Digital Power Supply
7.	VBATT	100	52	Input	1.8V to 3.6V Digital Power Supply.
8.	VRF33	52, 53	---	Input	3.3V Analog Supply for the RF Transceiver.
9.	VDD33	59	---	Input	3.3V Digital Supply for the RF Transceiver.
10.	VOUTLDOP1	92	37	Output	USB Mode: Connect to USB_VDDD. Other Modes: Leave unconnected.
11.	VOUTLDOP3	66	40	Output	USB Mode: Connect to USB_VDDP. Other Modes: Leave unconnected.
12.	VOUTLDOP1A	63	---	Output	Connect to BBP_LMAC_VDD_12 through a filter. Refer to the Module Integration Guide for more details.
13.	BBP_LMAC_VDD_12	91	---	Input	Connect to the VOUTLDOP1A pin through a filter. Refer to the Module Integration Guide for more details.
14.	USB_VDDA	14	43	Input	USB Mode: 3.3V Analog Supply.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
					Other Modes: Connect to Ground.
15.	USB_VDDS	23	22	Input	USB Mode: 3.3V Digital Supply. Other Modes: Connect to Ground.
16.	USB_VDDP	77	21	Input	USB Mode: Connect to VOUTLDOP3. Other Modes: Connect to Ground.
17.	USB_VDDD	15	42	Input	USB Mode: Connect to VOUTLDOP1. Other Modes: Connect to Ground.
18.	GND	1, 20, 33, 34, 35, 36, 38, 42, 43, 44, 45, 47, 48, 51, 57, 67, 85, 86, 87, 88, 90, 101	53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79	Ground	Common Ground
SDIO, Slave SPI and USB Interfaces					
19.	SDIO_CLK/SPI_CLK	25	18	Input	SDIO & SPI Modes: Interface clock from Host processor
				Input	Other modes: Reserved. Connect to Ground.
20.	SDIO_CMD/SPI_CSN	24	17	Inout	SDIO Mode: SDIO Interface Command Signal
				Input	SPI Mode: Active-low SPI Chip Select Signal
				Input	Other Modes: Reserved. Connect to Ground.
21.	SDIO_DATA0/SPI_MOSI	78	13	Inout	SDIO Mode: SDIO Interface Data0 Signal
				Input	SPI Mode: SPI Master-Out-Slave-In Signal
				Output	Other Modes: Reserved. Leave unconnected.
22.	SDIO_DATA1/SPI_MISO	79	14	Inout	SDIO Mode: SDIO Interface DATA1 Signal

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
				Output	SPI Mode: SPI Master-In-Slave-Out Signal
				Input	Other Modes: Reserved. Connect to Ground.
23.	SDIO_DATA2/SPI_INTR	26	16	Inout	SDIO Mode: SDIO Interface DATA2 Signal
				Output	SPI Mode: Interrupt Signal to the Host. Active-high level, Active-low level and Open Drain modes are supported. In ULP mode, a pull-up or pull-down resistor of 100 kΩ might be required depending on whether the signal is configured as Active-low or Active-high. The pull-up/pull-down resistor can be avoided if the Host can mask this interrupt before the module enters ULP Sleep mode and unmask it after it exits ULP Sleep mode.
				Input	Other modes: Reserved. Connect to Ground.
24.	SDIO_DATA3	80	15	Inout	SDIO Mode: SDIO Interface DATA3 Signal
				Input	Other Modes: Reserved. Connect to Ground.
25.	USB_VBUS	16	9	Input	USB Mode: 5V VBUS Signal from USB Connector.
				Input	Other Modes: Leave unconnected.
26.	USB_DN	17	10	Inout	Negative Data Channel from USB Connector.
				Inout	Other Modes: Leave unconnected.
27.	USB_DP	18	11	Inout	Positive Data Channel from USB Connector.
				Inout	Other Modes: Leave unconnected.
28.	USB_ID	19	12	Inout	ID signal from USB Connector.
				Inout	Other Modes: Leave unconnected.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
GPIO Interface[28]					
29.	GPIO_0	75	---	Inout	Reserved – connect a 100 kΩ pull-down resistor.
30.	GPIO_1	11	---	Inout	Reserved – connect a 100 kΩ pull-up resistor.
31.	GPIO_2/HOST_WAKE UP	10	26	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Host Wakeup Interrupt Mode: This pin is used by firmware to indicate a pending packet to the Host processor. It should be used only if the Host processor is not able to wake up from a sleep state using the host interface specific interrupt like SDIO_DATA2/SPI_INTR. A pull up or pull down has to be placed on this pin based on whether the pin is configured as active low or active high interrupt in the Host processor, respectively. This feature can be enabled and configured through API (for WiSeConnect®/Connect-io-n®) and driver settings (for n-Link®).
32.	GPIO_3	22	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
33.	GPIO_4	12	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
34.	GPIO_5	13	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
					HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
35.	GPIO_6	76	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
36.	GPIO_7	30	23		Reserved – leave this pin unconnected.
37.	GPIO_8	83	29		Reserved – leave this pin unconnected.
38.	GPIO_9/UART1_RX	7	6	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 1 Serial Input. This pin is configured as UART pin if UART is selected as the Host Interface.
39.	GPIO_10/UART1_TX	6	5	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 1 Serial Output. This pin is configured as UART pin if UART is selected as the Host Interface.
40.	GPIO_11/UART1_RTS /I2S_CLK/PCM_CLK	8	7	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 1 Request To Send. This pin is configured as UART pin if UART is selected as the Host Interface.
				Input	I2S Mode: I2S Clock signal. Not supported in the current firmware.
				Input	PCM Mode: PCM Clock signal. Not supported in the current firmware.
41.	GPIO_12/UART1_CTS /I2S_WS/PCM_FSYN C	98	41	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 1 Clear To Send. This pin is configured as UART pin if UART is selected as the Host Interface.
				Input	I2S Mode: I2S WS signal. Not supported in the current firmware.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
				Input	PCM Mode: PCM FSYNC signal. Not supported in the current firmware.
42.	GPIO_13/I2S_DIN/PCM_MOSI/DBG_UART_RX	71	49	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 2 (Debug) Serial Input.
				Input	I2S Mode: I2S Data Input signal. Not supported in the current firmware.
				Input	PCM Mode: PCM Master-Out-Slave-In signal. Not supported in the current firmware.
43.	GPIO_14/I2S_DOUT/PCM_MISO/DBG_UART_TX	9	8	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 2 (Debug) Serial Output.
				Output	I2S Mode: I2S Data Output signal. Not supported in the current firmware.
				Output	PCM Mode: PCM Master-In-Slave-Out signal. Not supported in the current firmware.
44.	GPIO_15/BLDR_BPS/LP_WAKEUP	29	24	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	BLDR_BPS/LP_WAKEUP – in this mode, the signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module should wakeup from its Low Power (LP) sleep mode. The BLDR_BPS functionality is valid only for WiSeConnect®/Connect-io-n® modules.
45.	GPIO_16/LED0	28	25	Inout	GPIO Mode: Reserved – leave this pin unconnected.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
				Output	LED Mode: Control signal for an external LED.
46.	GPIO_17/WLAN_ACTIVE	84	28	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Bluetooth Coexistence Mode: Active-high signal to indicate to an external Bluetooth IC that WLAN transmission is active. Not supported in the current firmware.
47.	GPIO_18/BT_PRIORITY	82	30	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	Bluetooth Coexistence Mode: Active-high signal used to indicate to the module that Bluetooth transmissions are higher priority. Not supported in the current firmware.
48.	GPIO_19/BT_ACTIVE	21	32	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	Bluetooth Coexistence Mode: Active-high signal used to indicate to the module that an external Bluetooth IC is transmitting. Not supported in the current firmware.
49.	GPIO_21/PS_SLP_0	81	31	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Power Save Mode: This signal is used to indicate to the Host processor when the module enters (logic low) and exits (logic high) the LP and ULP Sleep modes when the GPIO Handshake mode is enabled. For ULP mode, connect a 100 kΩ pull-down resistor. For ULP mode, the ULP_GPIO_1 signal, if available in the package, may be used instead of GPIO_21 for the same purpose but without the need for the pull-down resistor.
50.	ULP_GPIO_0/ULP_WAKEUP	3	2	Inout	GPIO Mode: Reserved – leave this pin unconnected.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
				Input	Power Save Mode: Active-high input to indicate that the module should exit its Ultra low power sleep mode.
51.	ULP_GPIO_1/PS_SLP_1	68	---	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Power Save Mode: This signal is used to indicate to the Host processor when the module enters (logic low) and exits (logic high) the ULP Sleep mode. The GPIO_21 signal may be used for the same purpose in case the package does not have the ULP_GPIO_1 signal available – GPIO_21 will need a pull-down resistor.
52.	ULP_GPIO_2	99	---	Inout	Reserved – leave this pin unconnected.
53.	ULP_ANAGPI	73	50	Input	Reserved – leave this pin unconnected.
Host Selection Interface[29]					
54.	HOST_SEL_0	60	36	Inout	SDIO Mode: Leave unconnected. SPI Mode: Connect a 4.7 kΩ pull-down resistor. USB Mode: Leave unconnected. USB-CDC Mode: Leave unconnected. UART Mode: Connect a 4.7 kΩ pull-down resistor.
55.	HOST_SEL_1	55	35	Inout	SDIO Mode: Leave unconnected. SPI Mode: Leave unconnected. USB Mode: Connect a 4.7 kΩ pull-down resistor. USB-CDC Mode: Connect a 4.7 kΩ pull-down resistor. UART Mode: Connect a 4.7 kΩ pull-down resistor.
56.	BOOTMODE_0	40	20	Inout	SDIO Mode: Leave unconnected. SPI Mode: Leave unconnected.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
					USB Mode: Connect a 4.7 kΩ pull-down resistor. USB-CDC Mode: Leave unconnected. UART Mode: Leave unconnected.
Miscellaneous Signals					
57.	HOST_BB_EN	94	39	Output	Control signal used to indicate the entry (logic low) and exit (logic high) of the module into ULP mode. May be used to control an external Load Switch and/or DC-DC for switching off the 3.3V supplies (other than VBATT) and reduce current consumption in ULP Mode. Refer to the Module Integration Guide for more details.
58.	JP0	69	47	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
59.	JP1	96	48	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
60.	JP2	97	45	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
61.	JNC	70	46	Output	Reserved – leave this pin unconnected.
62.	AUX_DAC_OUT	93	38	Output	Reserved – leave unconnected.
63.	AUX_ADC_IN0	65	44	Input	Reserved – leave unconnected.
64.	BOOTLOAD_EN	41	27	Inout	Reserved – leave unconnected.
65.	XTAL_32KHZ_N	5	4	Input	Reserved – leave unconnected.
66.	XTAL_32Khz_P	4	3	Input	Reserved – leave unconnected.
67.	EXT_PA_ON	64	---	Output	Reserved – leave unconnected.
68.	WURX	2	1	Input	Reserved – leave unconnected.
69.	PDN	58	---	Input	Reserved – connect to 100 kΩ pull-down resistor.
70.	NC	31, 39, 46, 54, 56, 61, 62, 72, 89, 95	---	NC (No Connect)	Leave unconnected.

7. WLAN 2.4 GHz Receiver Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Sensitivity for 20MHz Bandwidth[32]	1 Mbps DSSS		-97.0		dBm
	2 Mbps DSSS		-92.0		dBm
	5.5 Mbps CCK		-89.5		dBm
	11 Mbps CCK		-88.0		dBm
	6 Mbps OFDM		-93.0		dBm
	9 Mbps OFDM		-91.5		dBm
	12 Mbps OFDM		-90.5		dBm
	18 Mbps OFDM		-88.5		dBm
	24 Mbps OFDM		-85.5		dBm
	36 Mbps OFDM		-82.0		dBm
	48 Mbps OFDM		-78.0		dBm
	54 Mbps OFDM		-76.0		dBm
	MCS0 Mixed Mode		-91.5		dBm
	MCS1 Mixed Mode		-89.5		dBm
	MCS2 Mixed Mode		-87.0		dBm
	MCS3 Mixed Mode		-84.5		dBm
	MCS4 Mixed Mode		-81.0		dBm
	MCS5 Mixed Mode		-76.5		dBm
	MCS6 Mixed Mode		-74.5		dBm
	MCS7 Mixed Mode		-73.0		dBm
Sensitivity for 40MHz Bandwidth	MCS0 Mixed Mode		-88.0		dBm
	MCS7 Mixed Mode		-69.5		dBm
Maximum Input Level for PER below 10%	1 Mbps DSSS		-4		dBm
	11 Mbps CCK		-4		dBm

Parameter	Condition	Min.	Typ.	Max.	Units
	54 Mbps OFDM		-16		dBm
	MCS0 Mixed Mode		-15		dBm
Adjacent Channel Rejection[33]	1 Mbps DSSS		35		dB
	11 Mbps CCK		32		dB
	6 Mbps OFDM	32			dB
	54 Mbps OFDM	18			dB
PER Floor				0.1	%
RSSI Accuracy			±1	±3	dB

Table 18: WLAN 2.4 GHz Receiver Characteristics

Additional notes:

For All device

(15.21) Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user authority to operate the equipment.

For mobile device

1. To comply with FCC RF exposure compliance requirements, a separation distance of at least 20 cm must be maintained between the antenna of this device and all persons. (Not including low power device (below 20mW))
2. This Transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

For Class B digital device or peripheral or cordless phone (15.105)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is needed.
- Consult the dealer or an experienced radio/TV technician for help.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users. For laptop installations, the antenna must be installed to ensure that the proper spacing is maintained in the event the users places the device in their lap during use (i.e. positioning of antennas must be placed in the upper portion of the LCD panel only to ensure 20 cm will be maintained if the user places the device in their lap for use) and
2) The transmitter module may not be co-located with any other transmitter or antenna. As long as the 2 conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements require with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). IMPORTANT NOTE: In the event that these conditions can not be met (for example certain lapt configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

This transmitter module is authorized only for use in devices where the antenna may be installed such that 20 cm may be maintained between the antenna and users (for example access points, routers, wireless ASDL modems, certain laptop configurations, and similar equipment). The final end product must be labeled in a visiblearea with the following: "Contains TX FCC ID: 2ARTO-N00-S1C-1

Un-license band: This device complies with Part 15 of the FCC Rules.
Operation is subject to the following two conditions:
(1)this device maynot cause harmful interference, and
(2)this device must accept any interference received, including interference that may cause undesiredoperation.

NCC警語
依據 低功率電波輻射性電機管理辦法:
第十二條
經型式認證合格之低功率射頻電機，非經許可，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。
第十四條
低功率射頻電機之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。
前項合法通信，指依電信法規定作業之無線電通信。功率射頻電機須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。
本模組於取得認證後，將依規定於模組本體標示審驗合格標籤；
並要求平台廠商於平台上標示『本產品內含射頻模組: CCXXxxYYyyyZzW 』字樣。