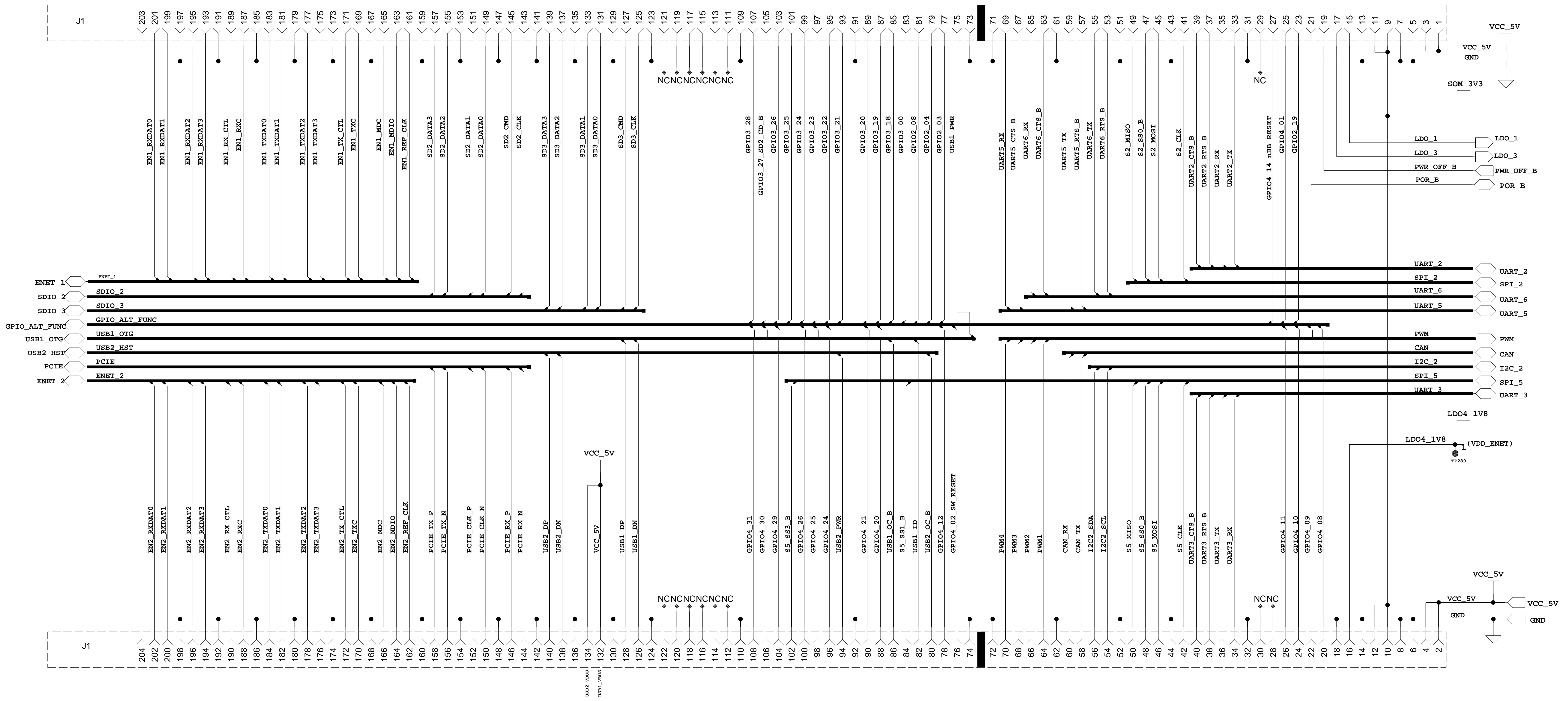


CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE CURRENT DESIGN ACTIVITY				
REVISION HISTORY - ALL SHEETS ARE THE SAME REVISION				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	-	E.O. 1234567	30JUL2020	

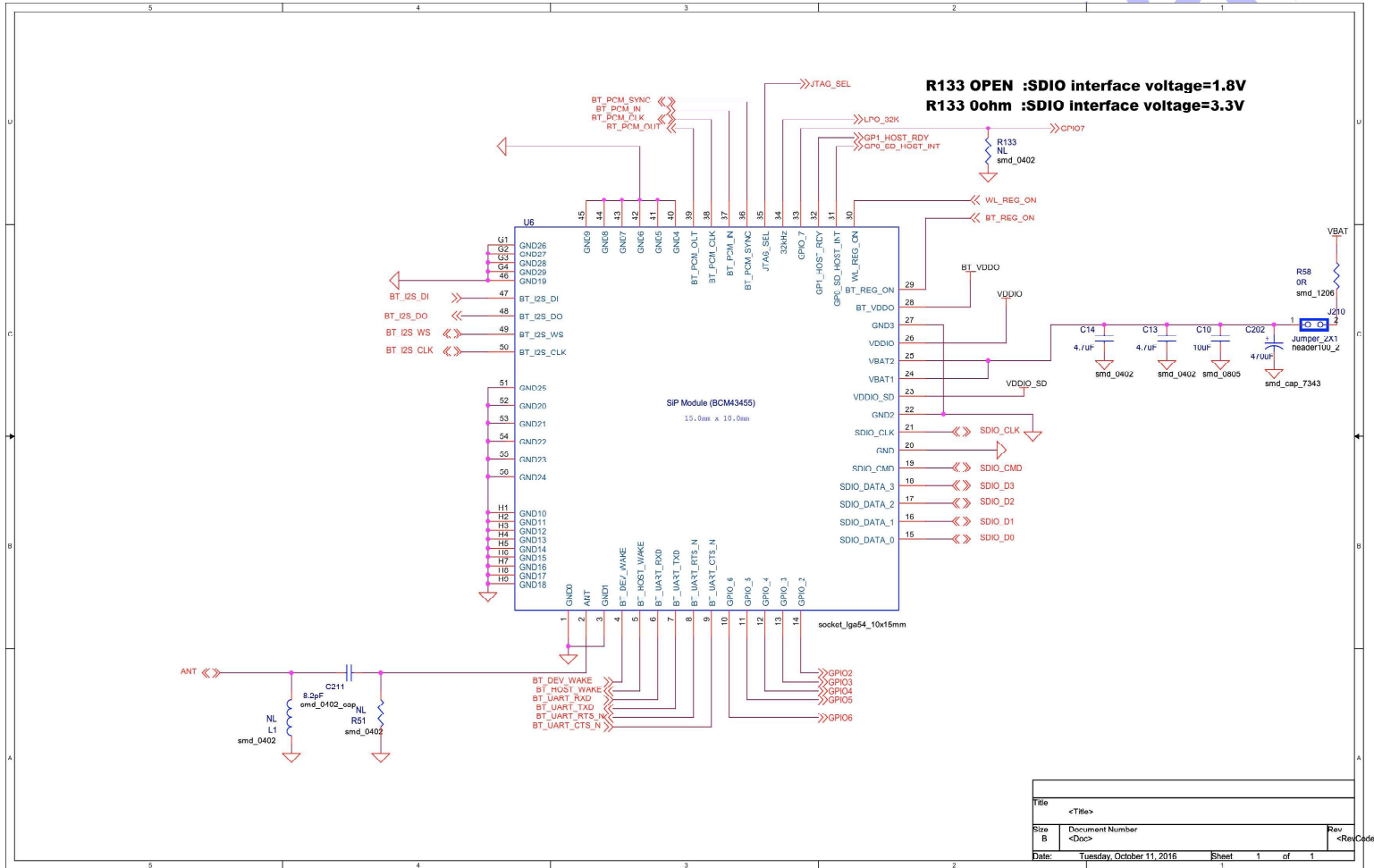
Note:
Pins 75, 77, 79, and 81
are on the 1.8V (VDD_ENET)
power domain.



HONEYWELL CONFIDENTIAL AND PROPRIETARY		HONEYWELL INTERNATIONAL INC. Honeywell	
DRAWN BY Tony.Gao DESIGNER Tony.Gao		HONEYWELL BUILDING TECHNOLOGIES	
30JUL2020		NAME	
30JUL2020		SCHEMATIC SMB_Gateway	
REFERENCE: 32350759-001	THIRD ANGLE PROJECTION	SIZE	DRAWING NO.
USED ON: GW-1000-WE		D	32350760
NEXT ASSY: 32350760-001		SCALE: NONE	WT: NA
INITIAL APPLICATION	PROJECT NUMBER 73268	REV	A

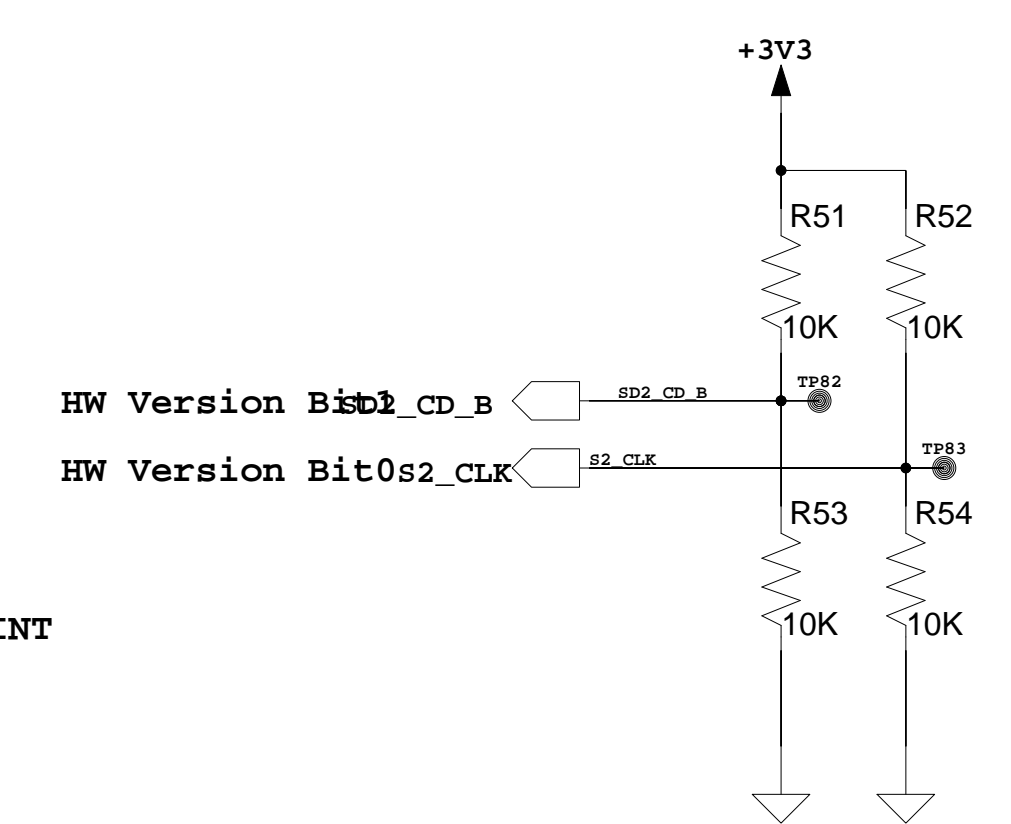
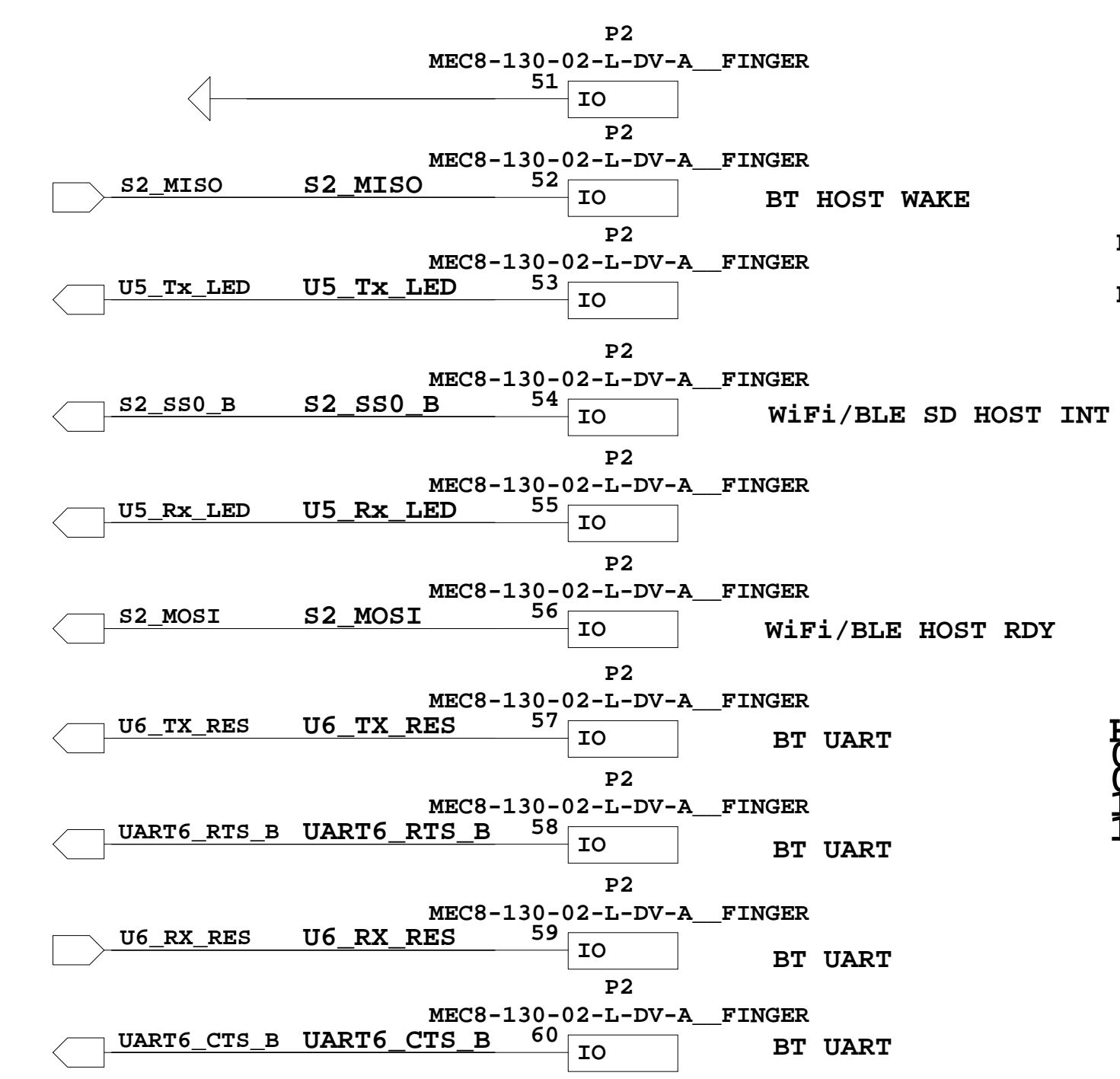
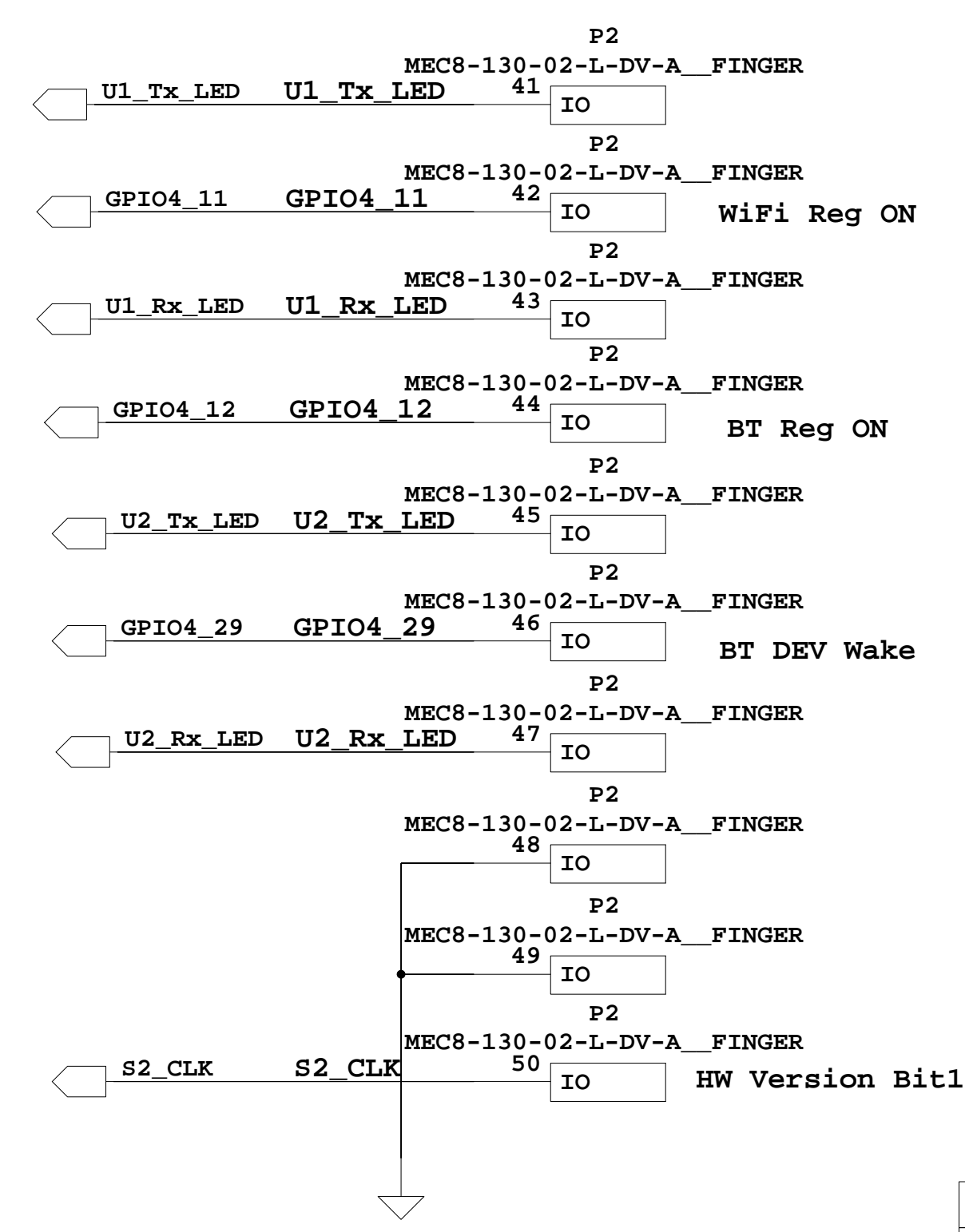
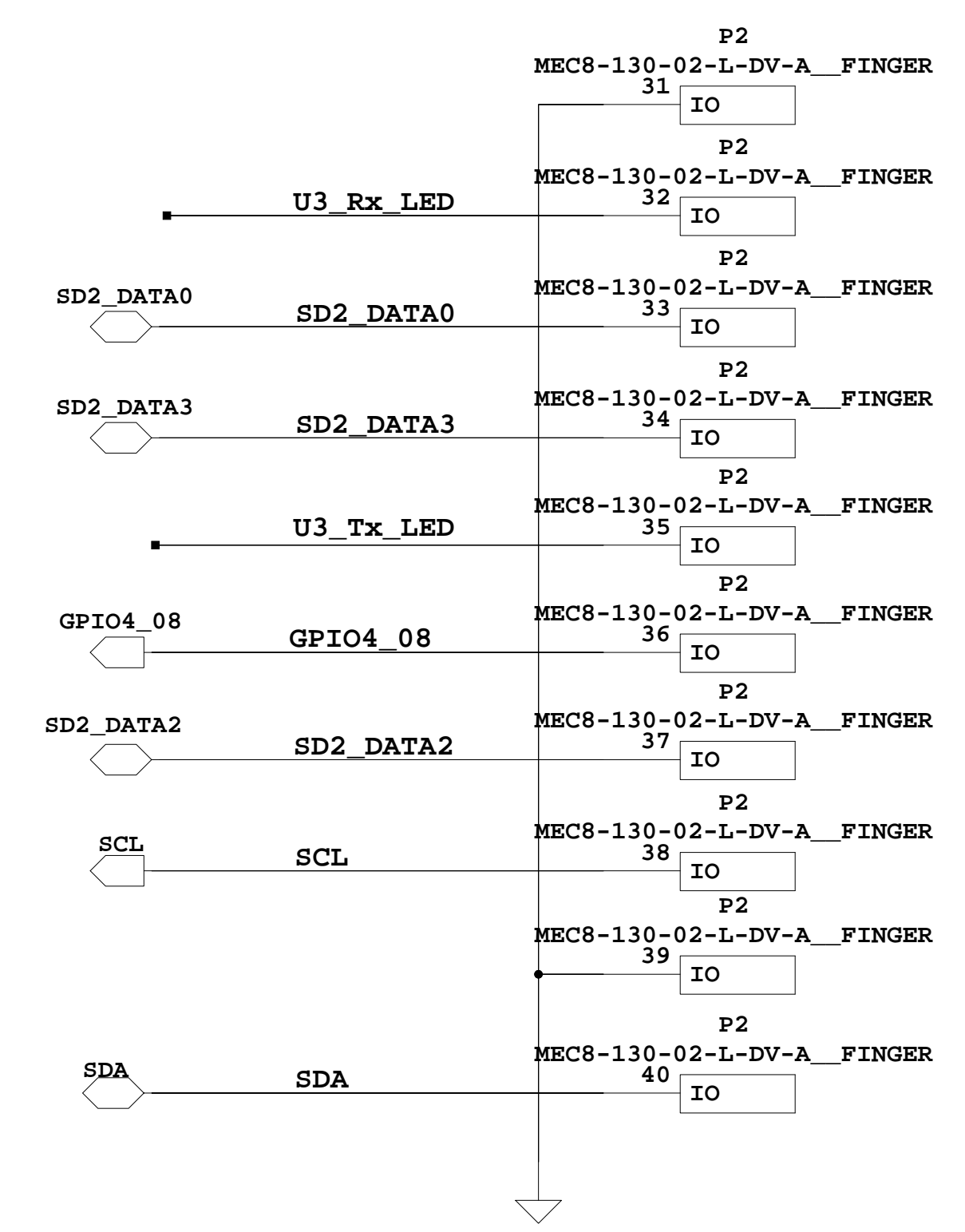
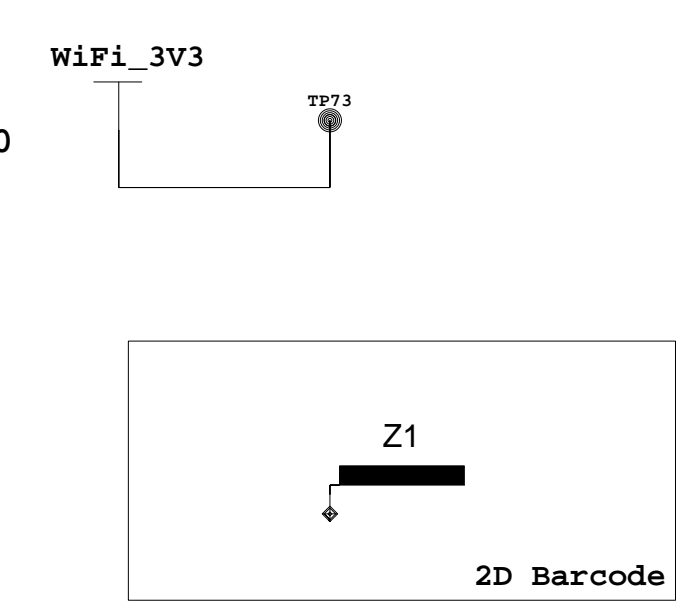
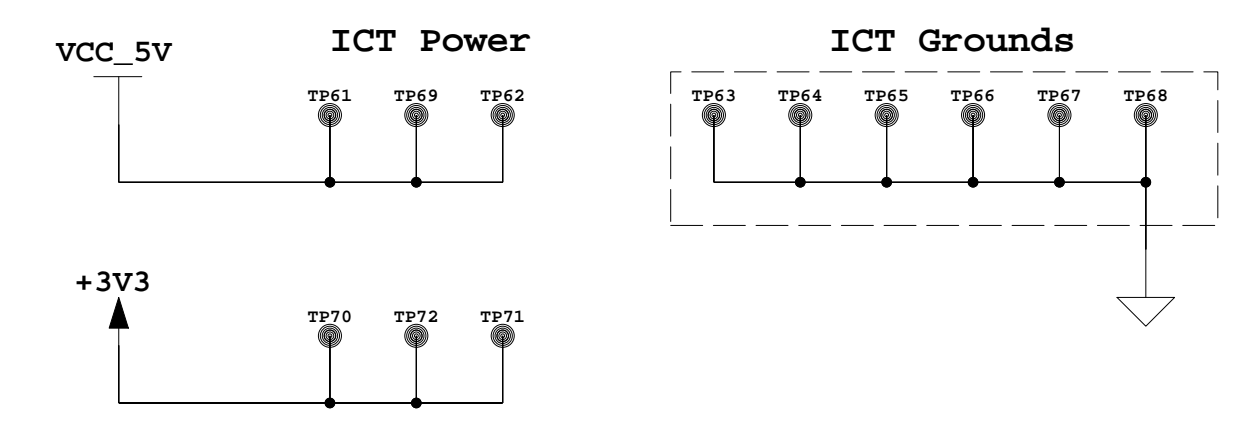
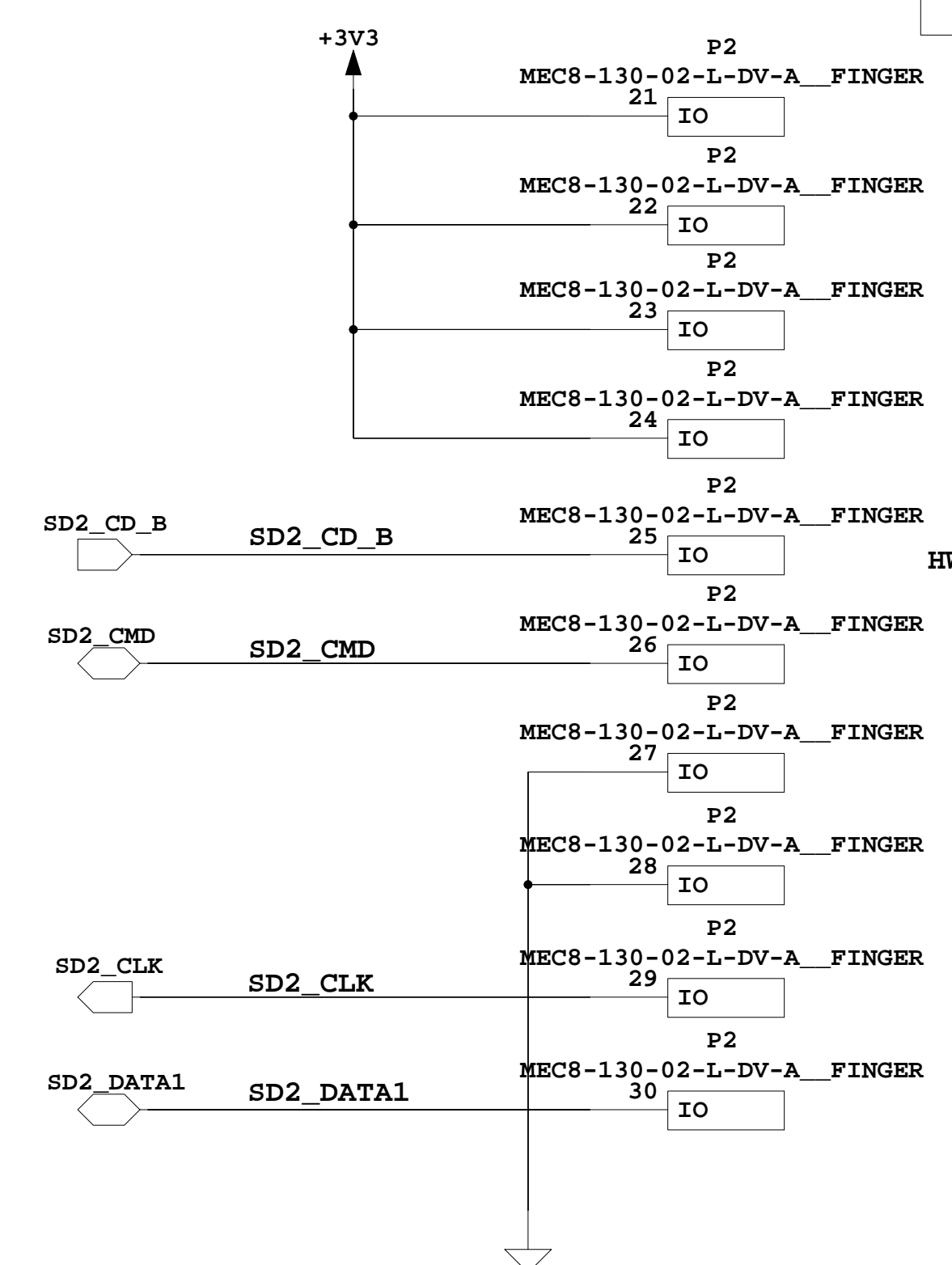
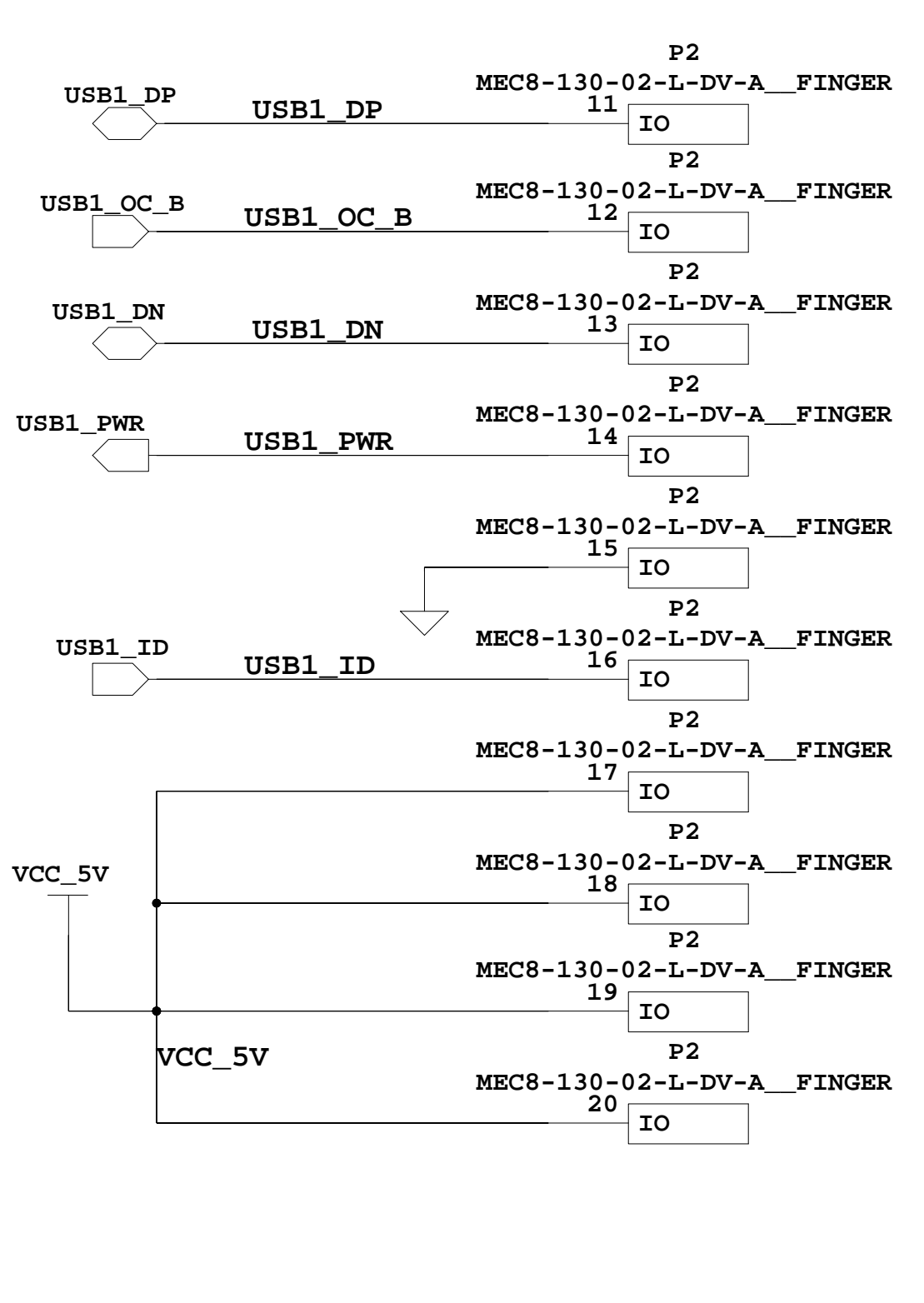
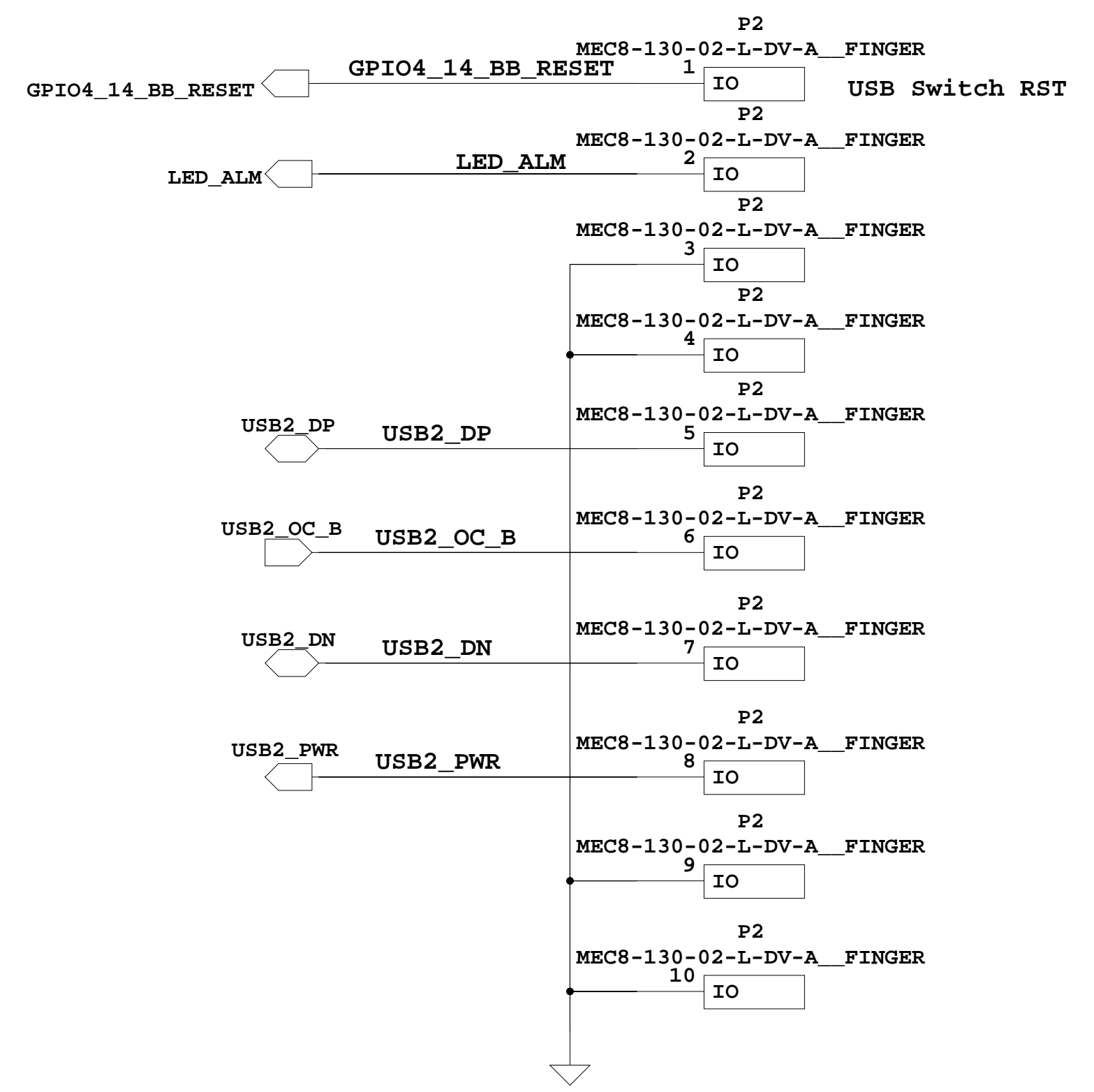
802.11a/b/g/n/ac + BT Wireless LAN Module V1.6

4.7 REFERENCE CIRCUIT



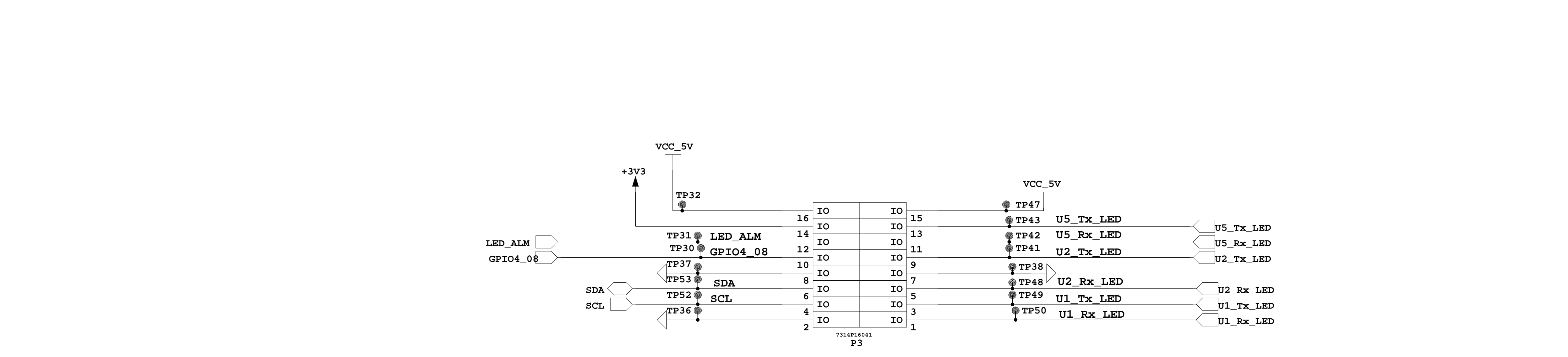
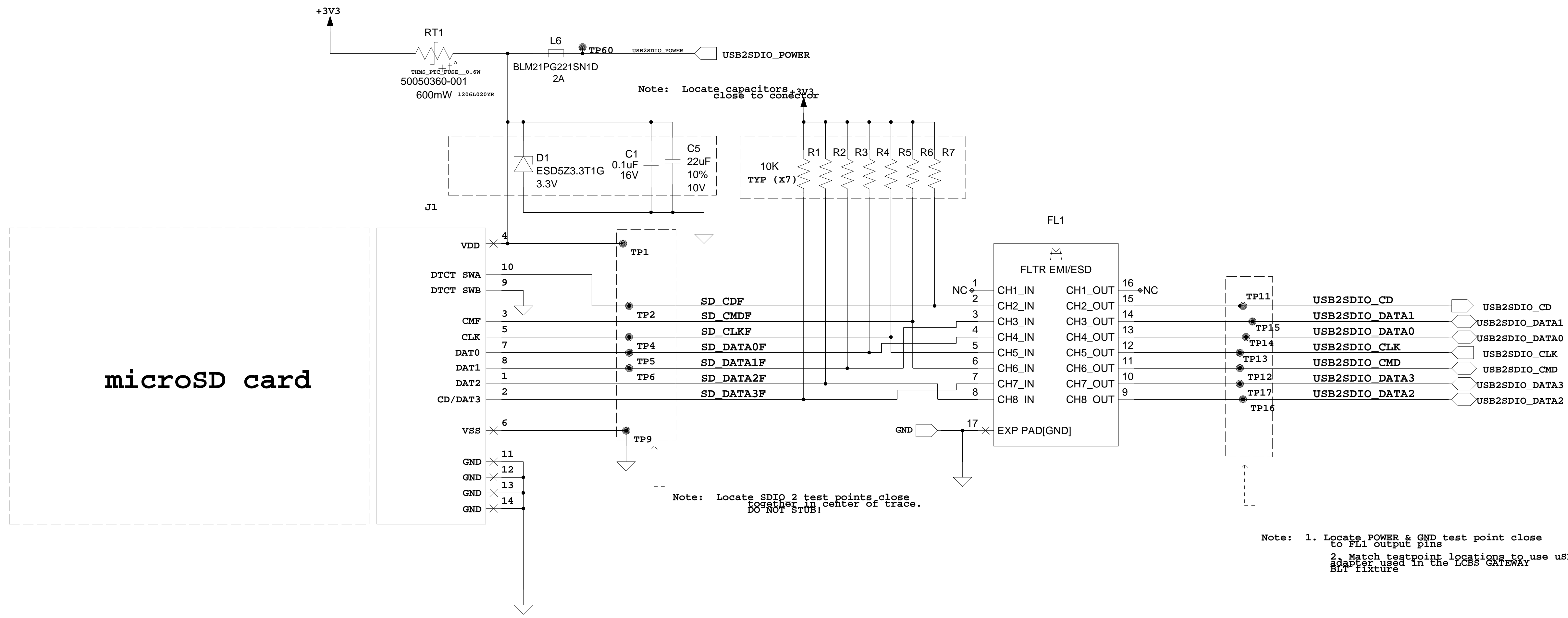
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CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE CURRENT DESIGN ACTIVITY				
REVISION HISTORY - ALL SHEETS ARE THE SAME REVISION				
ZONE	REV	DESCRIPTION	DATE	APPROVED
B	E.O. 0154044		13 Dec 2018	



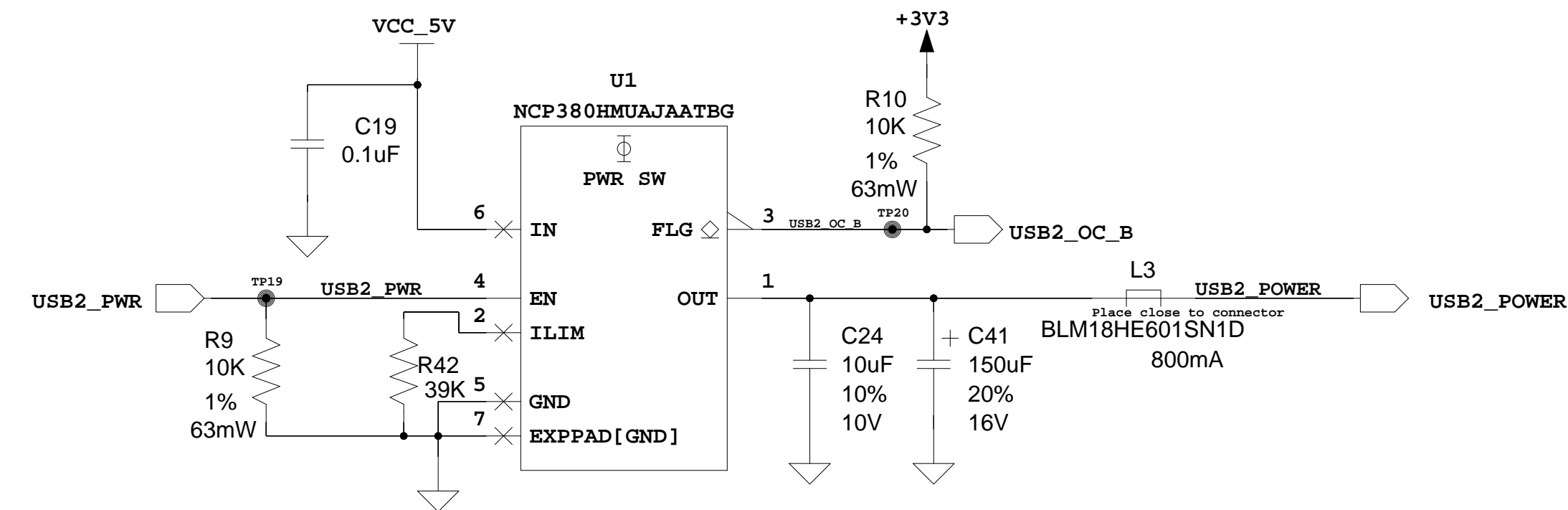
HW Rev Bit1, Bit0 =
 00: No TF, No WiFi
 01: No TF, WiFi
 10: TF, No WiFi
 11: TF and WiFi

HONEYWELL CONFIDENTIAL AND PROPRIETARY		HONEYWELL INTERNATIONAL INC. Honeywell	
DRAWN BY: H135733 H275008 30 Sep 2018		HOME & BUILDING TECHNOLOGIES	
DESIGNER: H135733 H275008 30 Sep 2018		NAME: SCHEMATIC Everest USB board	
REFERENCE: 32336512-001	THIRD ANGLE PROJECTION	SIZE: D	DRAWING NO.: 32336513
USED ON: CPO-PC400/200/400-W		SCALE: NONE	WT: NA
NEXT ASSY: 32336513-001/002		PROJECT NUMBER: 47612	REV: B
INITIAL APPLICATION			

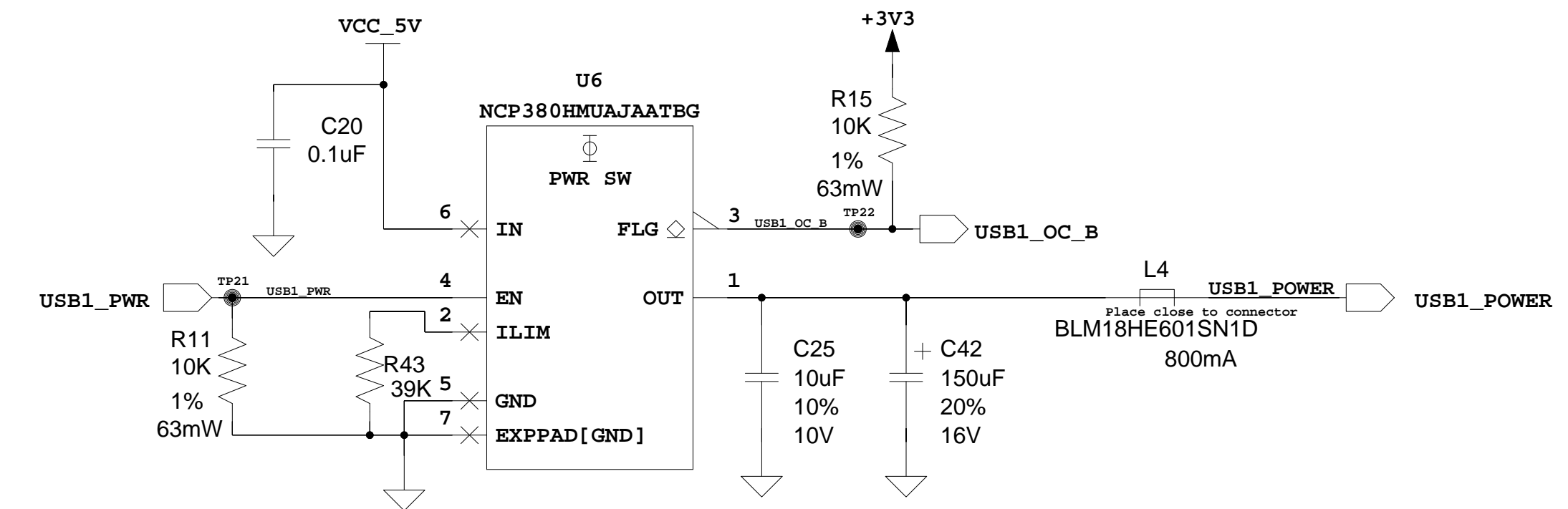


Note: 1. Locate POWER & GND test point close to FL1 output pins
 2. Match testpoint locations to use USD card adapter used in the LCBS GATEWAY BLT fixture

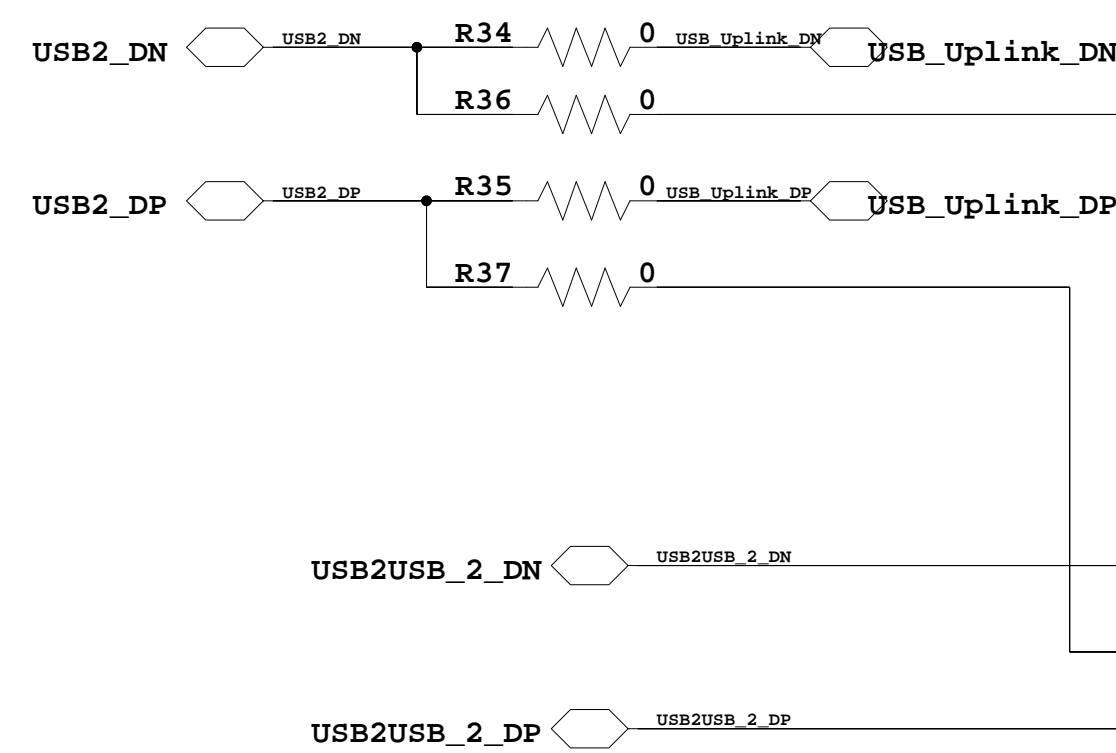
DRAWN BY H135733 H275008	30 Sep 2018	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES
DESIGNER H135733 H275008	30 Sep 2018	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D DRAWING NO. 32336513
		SCALE: NONE



HOST

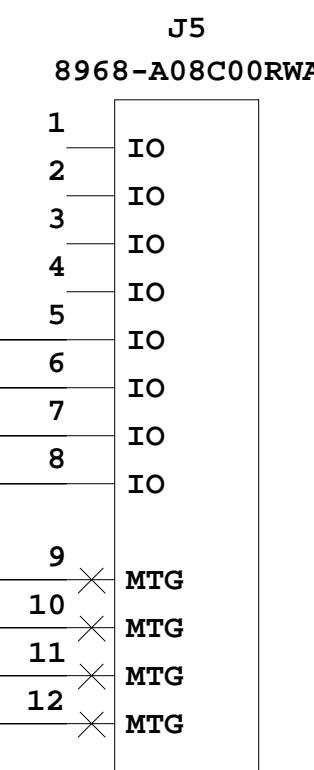
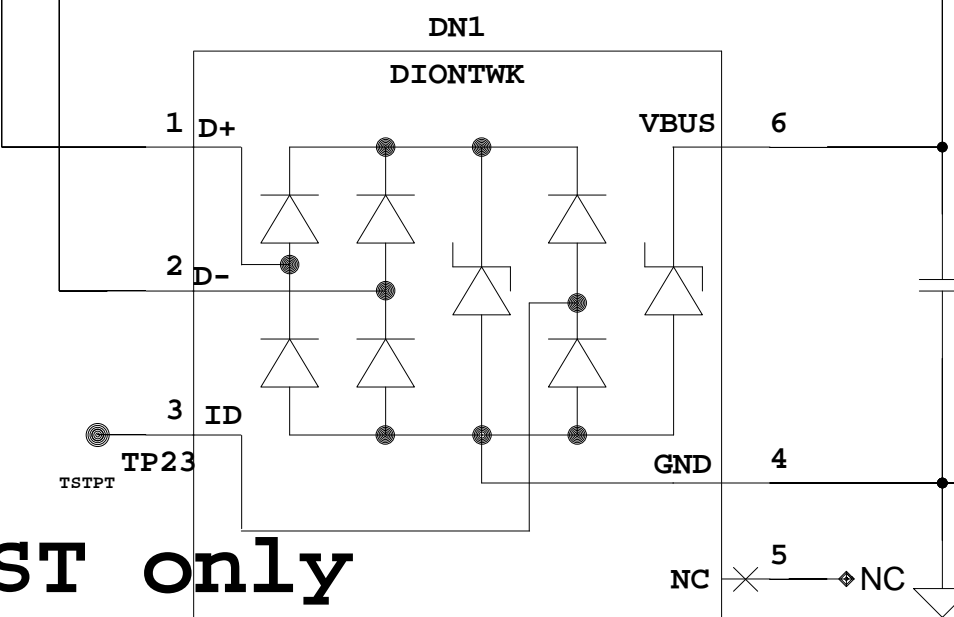


OTG



Place CM choke and protection array close to USB connector.

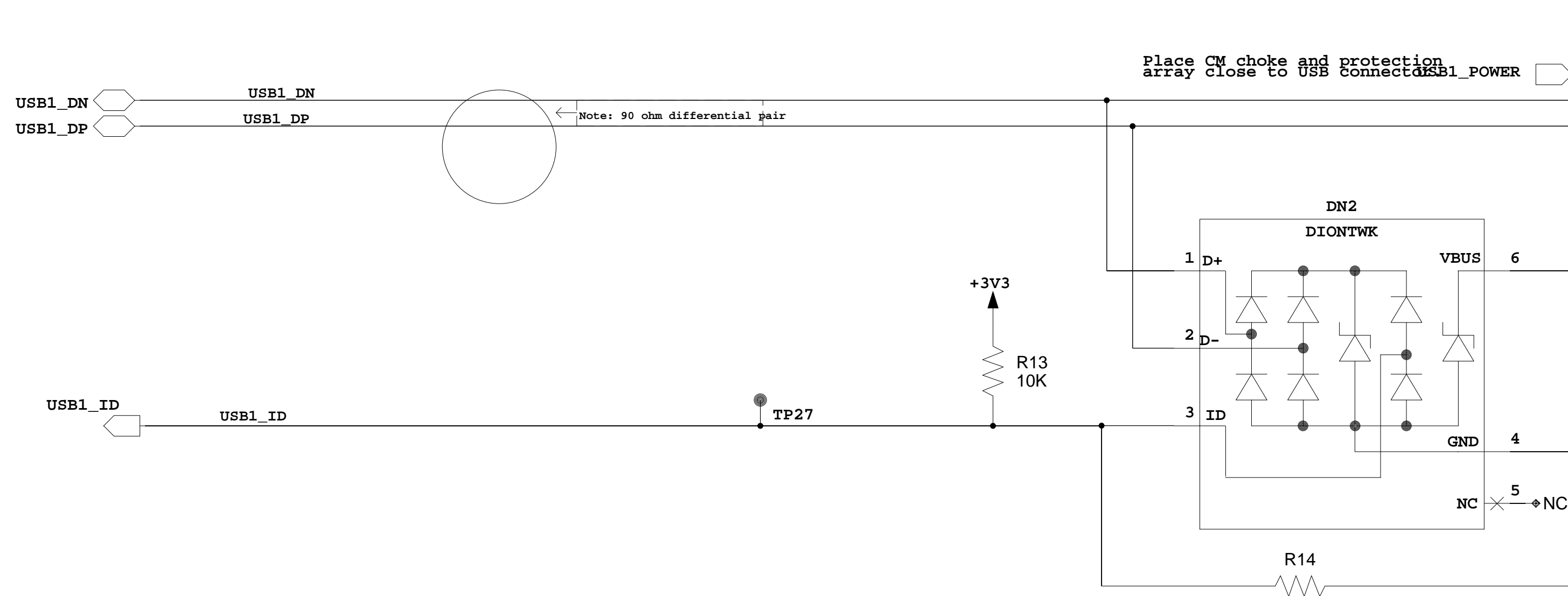
Note: 90 ohm differential pair



Route differential pair through protection array and test points without creating stubs.

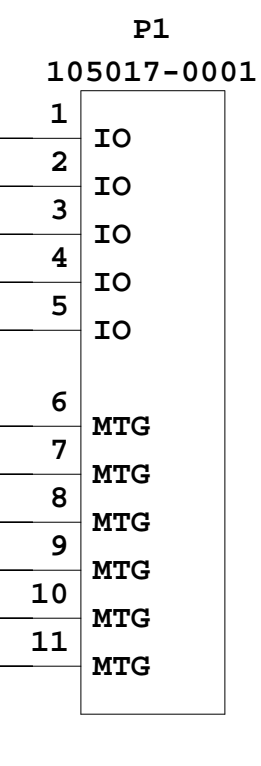
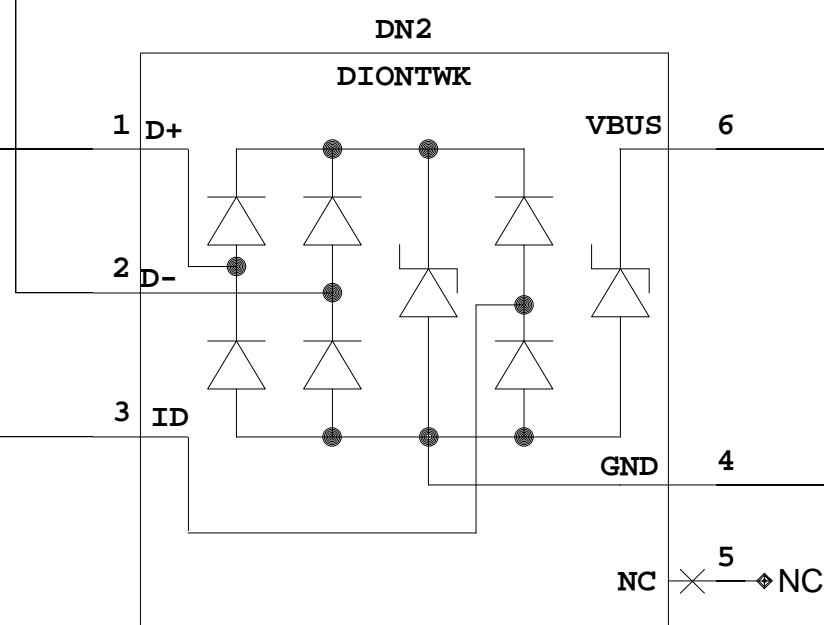
HOST USB

Note: USB1 From SOM is OTG
USB2 From SOM/USB Switch are HOST only



Place CM choke and protection array close to USB connector.

Note: 90 ohm differential pair

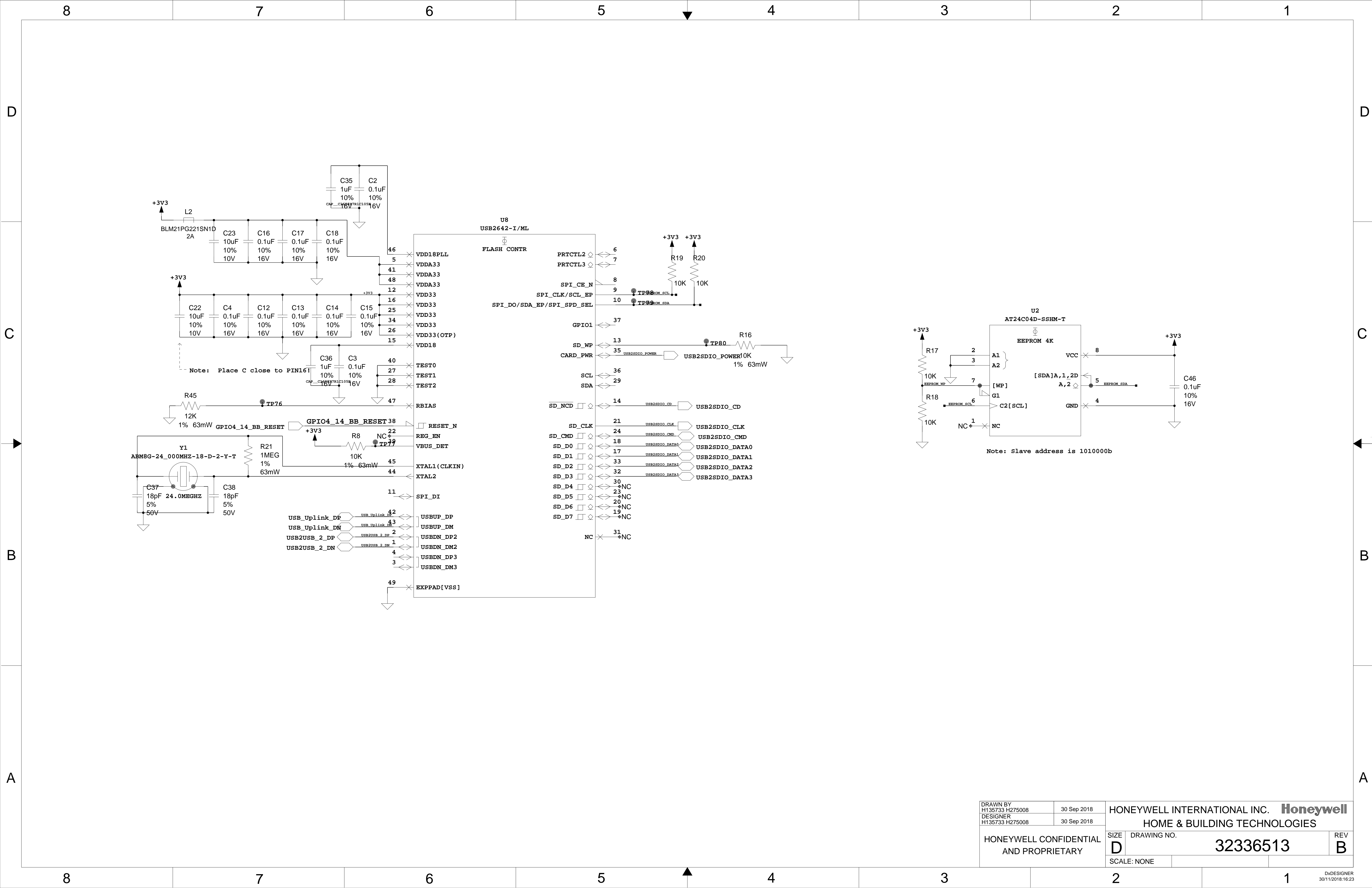


Route differential pair through protection array and test points without creating stubs.

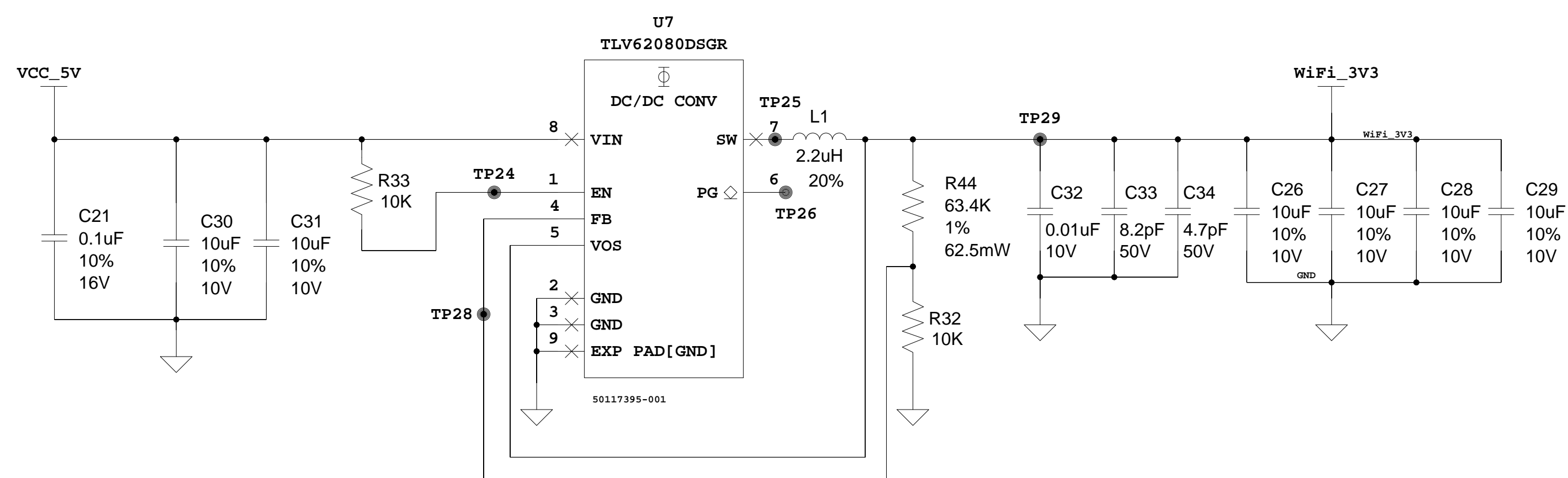
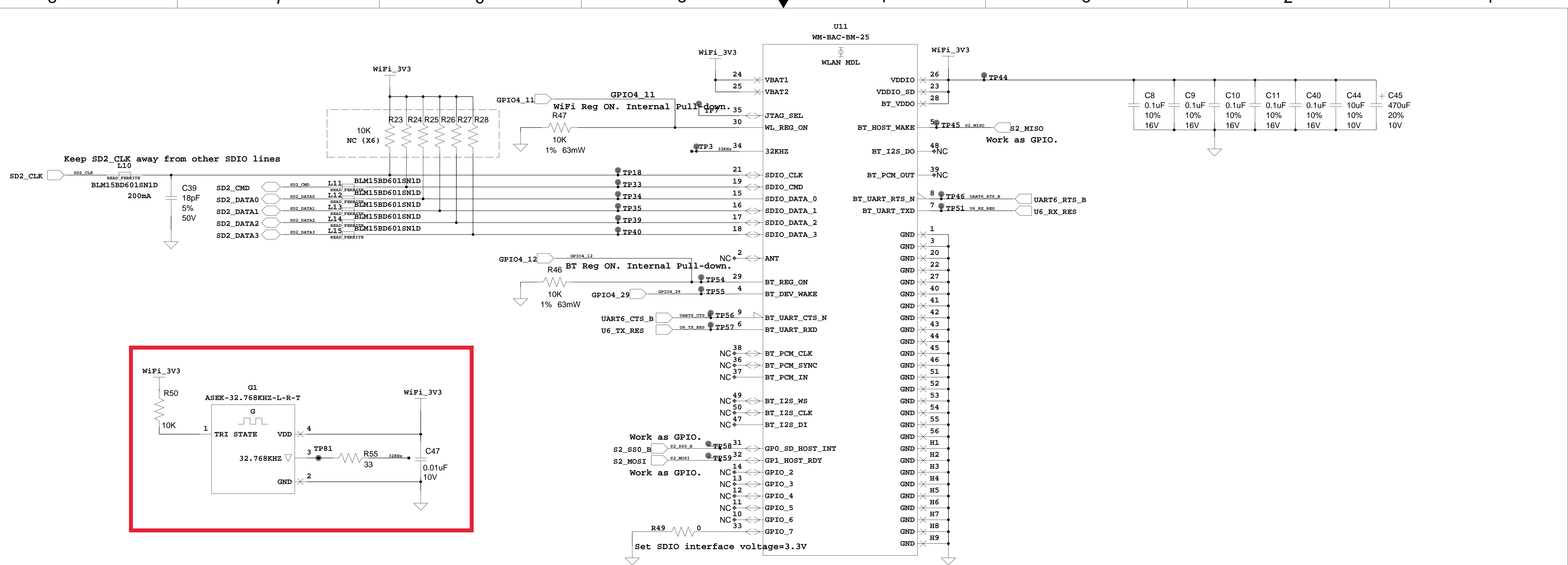
DEV/OTG USB

D+, D-, and ID pins are exact equivalent ESD clamp circuits. Any of these pins can be connected to any other D+, D-, or ID pin if it becomes easier to route the traces from the USB connector.

DRAWN BY H135733 H275008	30 Sep 2018	HONEYWELL INTERNATIONAL INC. Honeywell	
DESIGNER H135733 H275008	30 Sep 2018	HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. 32336513
		SCALE: NONE	REV B



DRAWN BY H135733 H275008	30 Sep 2018	HONEYWELL INTERNATIONAL INC. Honeywell	
DESIGNER H135733 H275008	30 Sep 2018	HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	REV B
		DRAWING NO. 32336513	
		SCALE: NONE	



DRAWN BY H135733 H275008	30 Sep 2018	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES
DESIGNER H135733 H275008	30 Sep 2018	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE: D DRAWING NO. 32336513 SCALE: NONE
		REV B

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. THIS DRAWING IS CAD GENERATED AND MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE CURRENT DESIGN ACTIVITY.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER, ASSEMBLY DESIGNATIONS AND SUBASSEMBLY DESIGNATIONS PLEASE SEE BOM.
3. RESISTOR VALUES ARE GIVEN IN OHMS.
4. CAPACITOR VALUES ARE GIVEN IN MICRO FARADS.
5. NOT-INSTALLED (DNI) COMPONENTS ARE SHOWN FOR REFERENCE ONLY.
6. I2C ADDRESS GIVEN AS 8-BIT VALUE. BIT 0 RESERVED FOR READ/WRITE.
7. THIS SCHEMATIC USES NAMED BUS SIGNALS, ENSURE THE FOLLOWING SETTINGS ARE SET:
"SHOW RIPPER INDEXES" AND "USE FULL BUS RIPPER NAME ON RIPPER".

NET NAMING CONVENTION:

ACTIVE HIGH SIGNALS: SIG
ACTIVE LOW SIGNALS: SIG_B

DIFFERENTIAL PAIRS: SIG_P/SIG_N

SHEET FUNCTION DESCRIPTION

SHEET	DESCRIPTION
1	Title Page
2	System Block Diagram
3	Top level schematic block
4	Power Supply
5	Processor - Clocks; debug; crypto & comms i/f
6	Processor - DRAM & SPI interface
7	Processor - Boot config; eMMC & Ethernet i/f
8	Processor - Power, ground and decoupling
9	DRAM - Bank 1
10	DRAM - Bank 2
11	eMMC Flash
12	Board Interface - SODIMM pins 1-122
13	Board Interface - SODIMM pins 123-204

DRAWN BY M Back Number SOM Board	23Jun2017	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
SCALE: NONE		REV A	

8

7

6

5

4

3

2

1

BLOCK DIAGRAM

D

D

C

C

B

B

A

A

<small>DRAWN BY</small> M Back <small>Number</small> SOM Board	23Jun2017	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES
HONEYWELL CONFIDENTIAL AND PROPRIETARY	<small>SIZE</small> D	<small>DRAWING NO.</small> CPO-PC200,CPO-PC400,CPO-PC400W
	<small>SCALE:</small> NONE	<small>REV</small> A

8

7

6

5

4

3

2

1

D\DESIGNER
12/09/2018:13:40

SODIMM_CONNECTOR

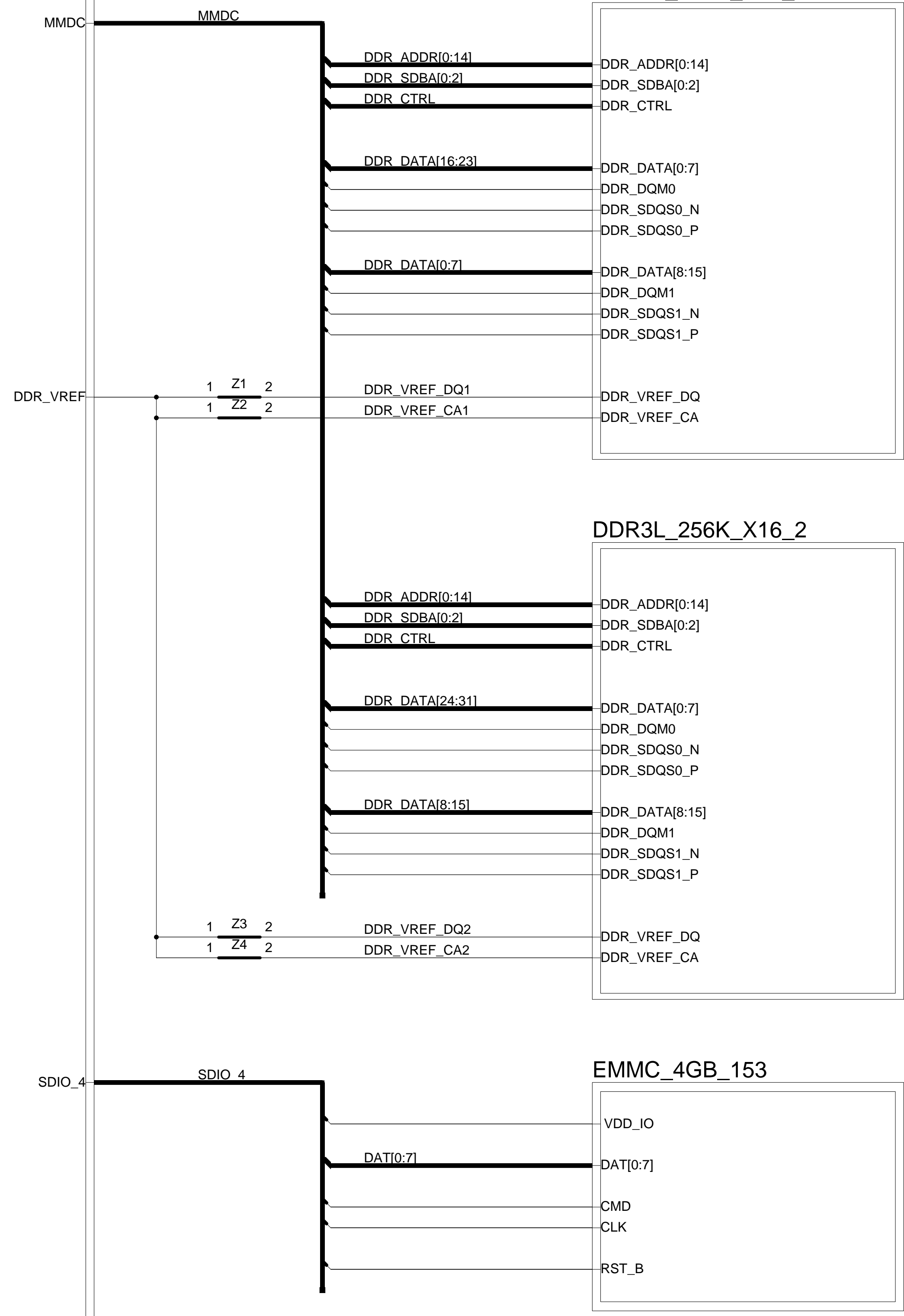
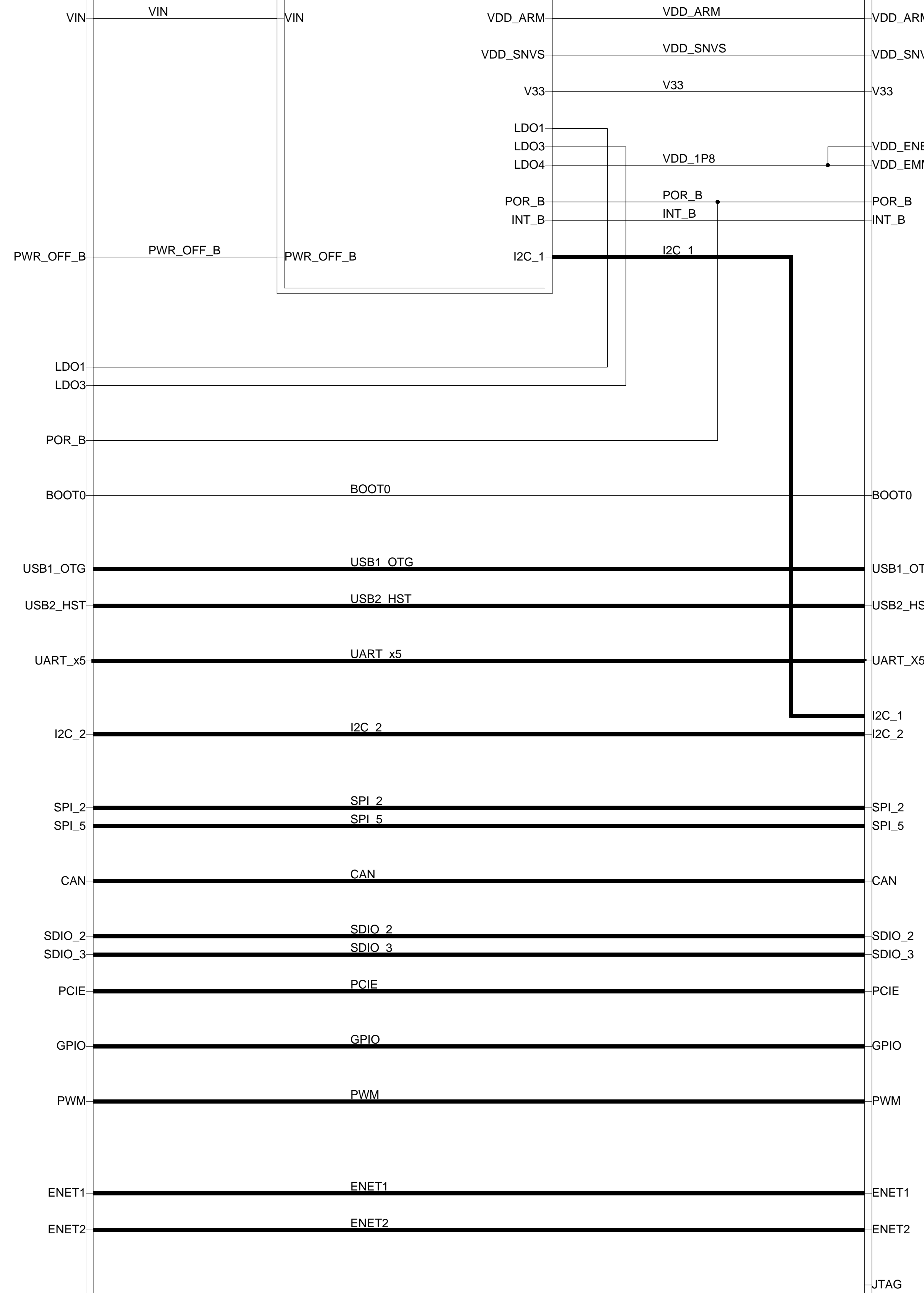
POWER

PROCESSOR

DDR3L_256K_X16_1

DDR3L_256K_X16_2

EMMC_4GB_153



DDR Byte lanes swapped to optimise layout

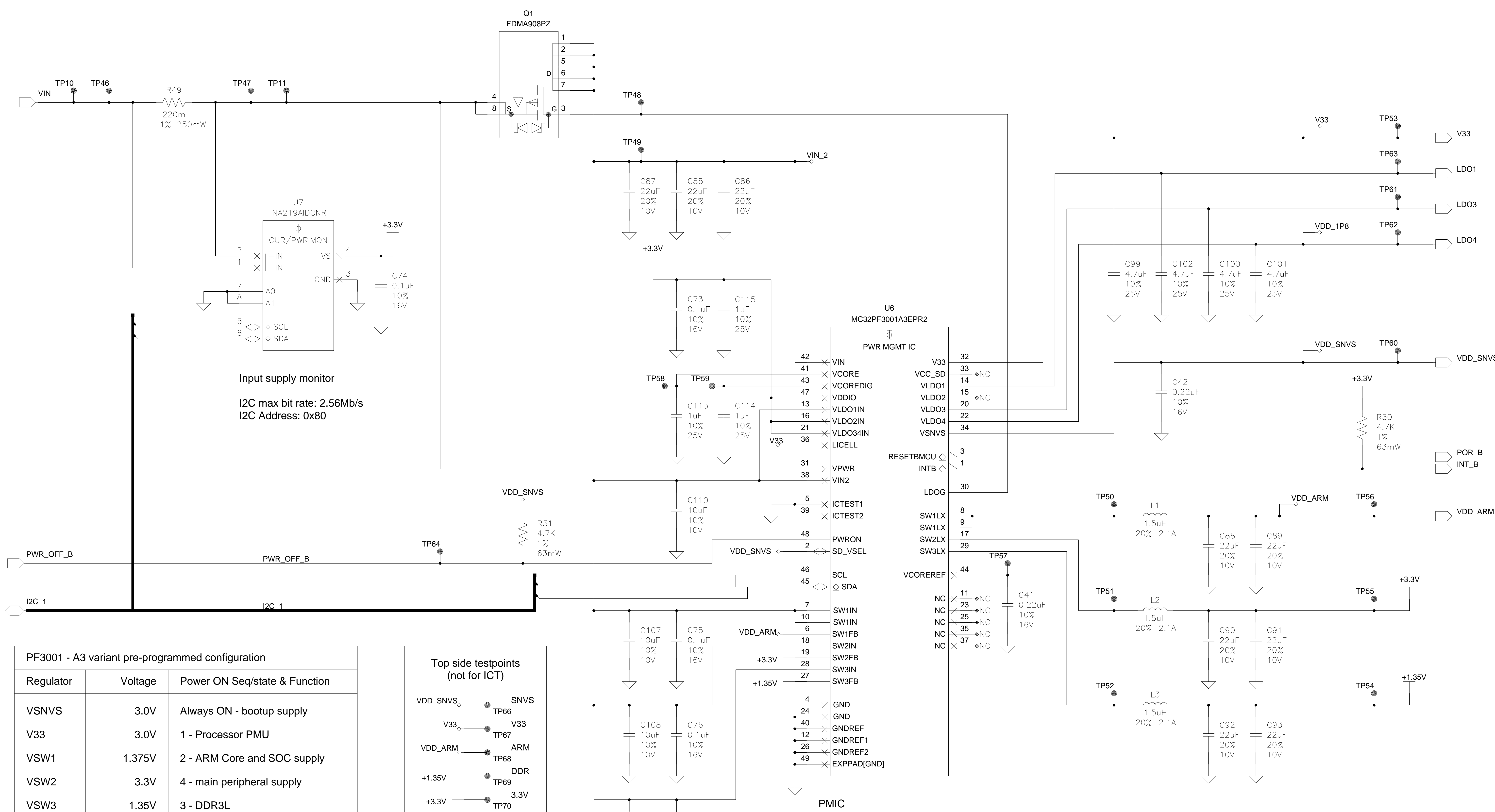
Byte	Order
0	2
1	0
2	3
3	1

DDR data lines swapped to optimise layout

Byte	Order
0	D7 D3 D5 D1 D4 D6 D2 D0
1	D15 D13 D11 D14 D12 D10 D9 D8
2	Not swapped
3	Not swapped

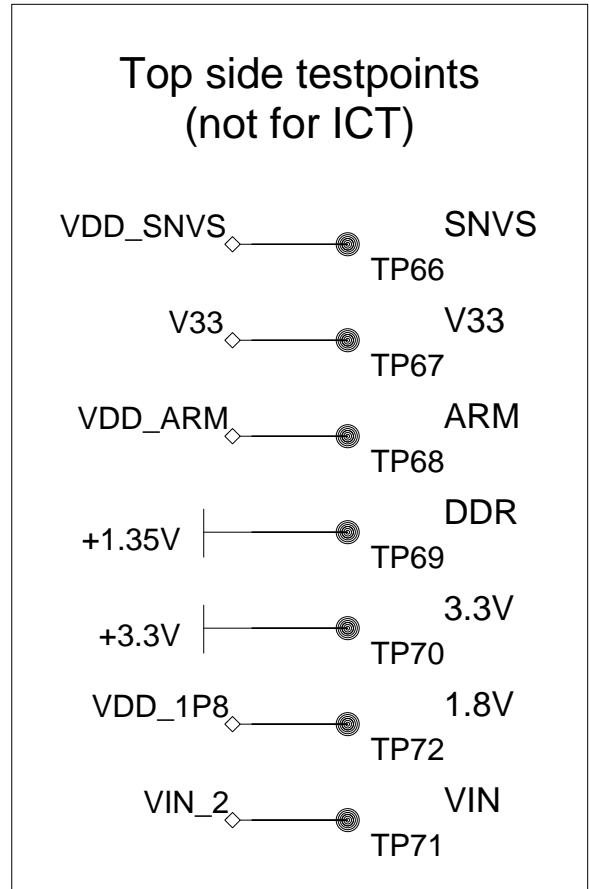
E&ES COMMON CPU BOARD
Top Level Schematic - Block diagram

DRAWN BY M Back Number SOM Board	23Jun2017	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES
HONEYWELL CONFIDENTIAL AND PROPRIETARY	SIZE D DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W	REV A
SCALE: NONE		D:\DESIGNER 12/09/2018:13:41



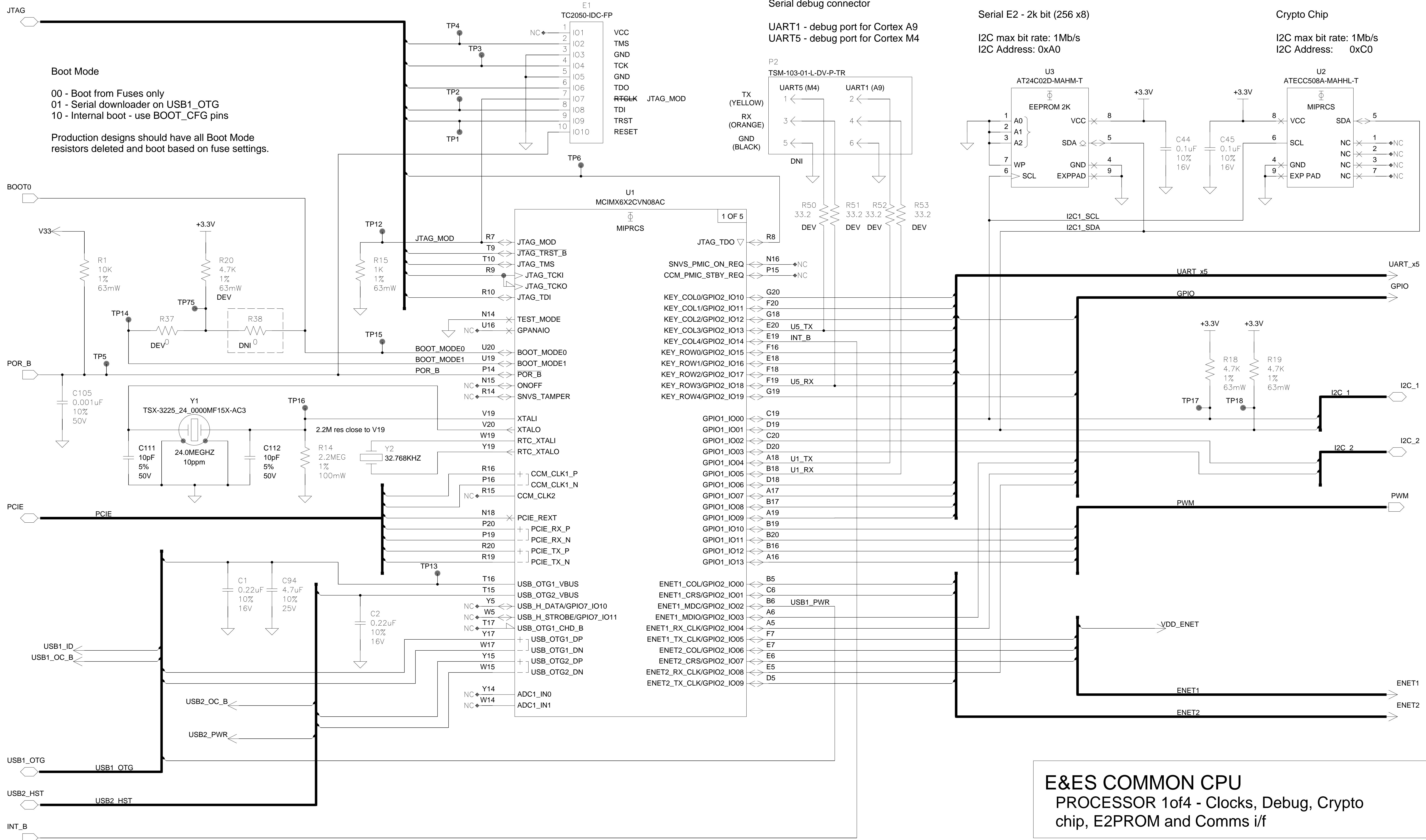
PF3001 - A3 variant pre-programmed configuration

Regulator	Voltage	Power ON Seq/state & Function
VSNVS	3.0V	Always ON - bootup supply
V33	3.0V	1 - Processor PMU
VSW1	1.375V	2 - ARM Core and SOC supply
VSW2	3.3V	4 - main peripheral supply
VSW3	1.35V	3 - DDR3L
VLDO1	3.3V	OFF - available for external use
VLDO2	1.5V	OFF - not used
VLDO3	2.5V	OFF - available for external use
VLDO4	1.8V	4 - eMMC I/O and RGMII I/O
VCC_SD	3.3V/1.85V	5 - not used



E&S COMMON CPU BOARD PMIC

DRAWN BY M Bock Number SOM Board	29Jun2017	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE DRAWING NO. D CPO-PC200,CPO-PC400,CPO-PC400W
SCALE: NONE		REV A



Boot Mode

00 - Boot from Fuses only
 01 - Serial downloader on USB1_OTG
 10 - Internal boot - use BOOT_CFG pins

Production designs should have all Boot Mode resistors deleted and boot based on fuse settings.

Serial debug connector

UART1 - debug port for Cortex A9
 UART5 - debug port for Cortex M4

Serial E2 - 2k bit (256 x8)

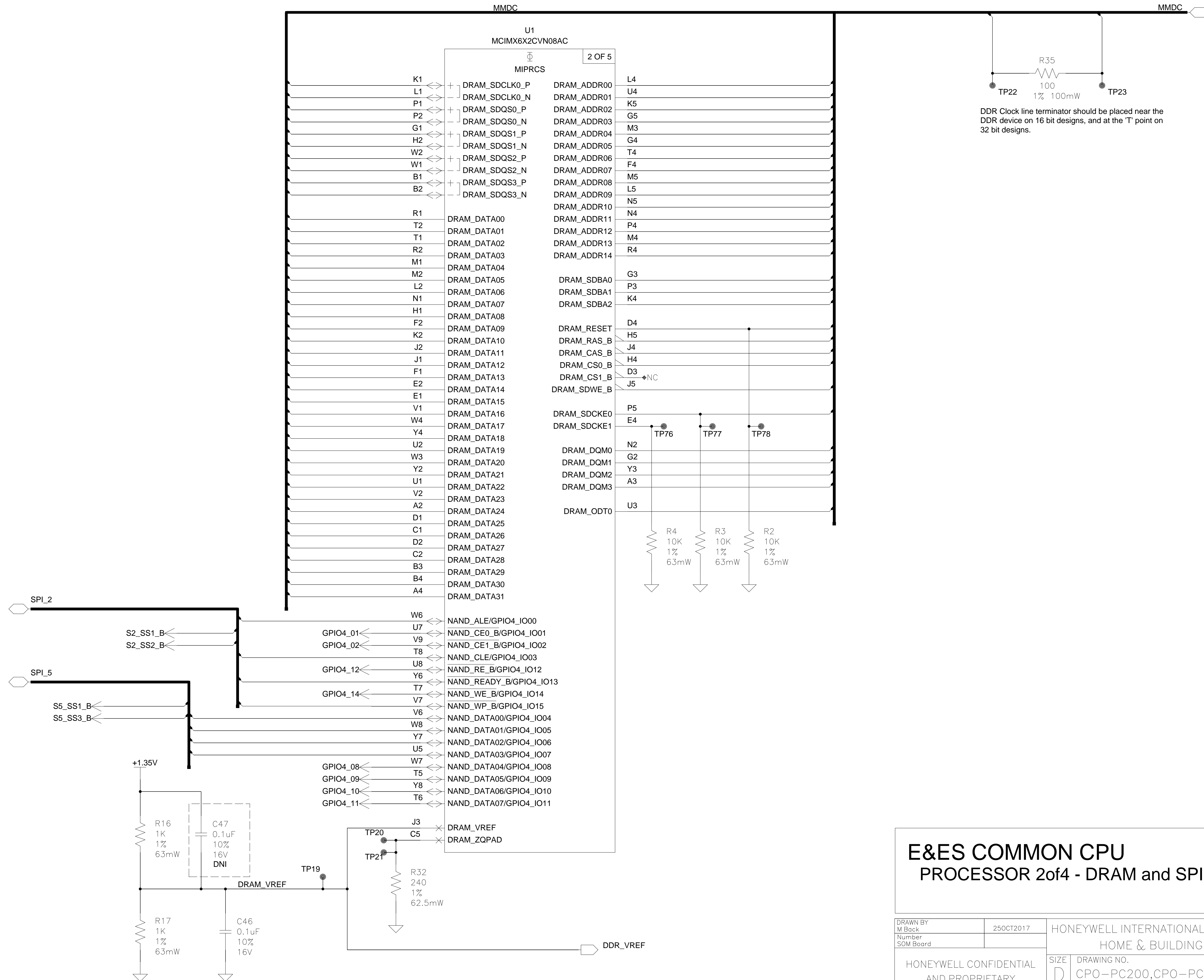
I2C max bit rate: 1Mb/s
 I2C Address: 0xA0

Crypto Chip

I2C max bit rate: 1Mb/s
 I2C Address: 0xC0

E&S COMMON CPU PROCESSOR 1of4 - Clocks, Debug, Crypto chip, E2PROM and Comms i/f

DRAWN BY M Back Number SOM Board	250CT2017	HONEYWELL INTERNATIONAL INC. HOME & BUILDING TECHNOLOGIES	Honeywell
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE: D DRAWING NO.: CPO-PC200,CPO-PC400,CPO-PC400W	REV: A
SCALE: NONE			



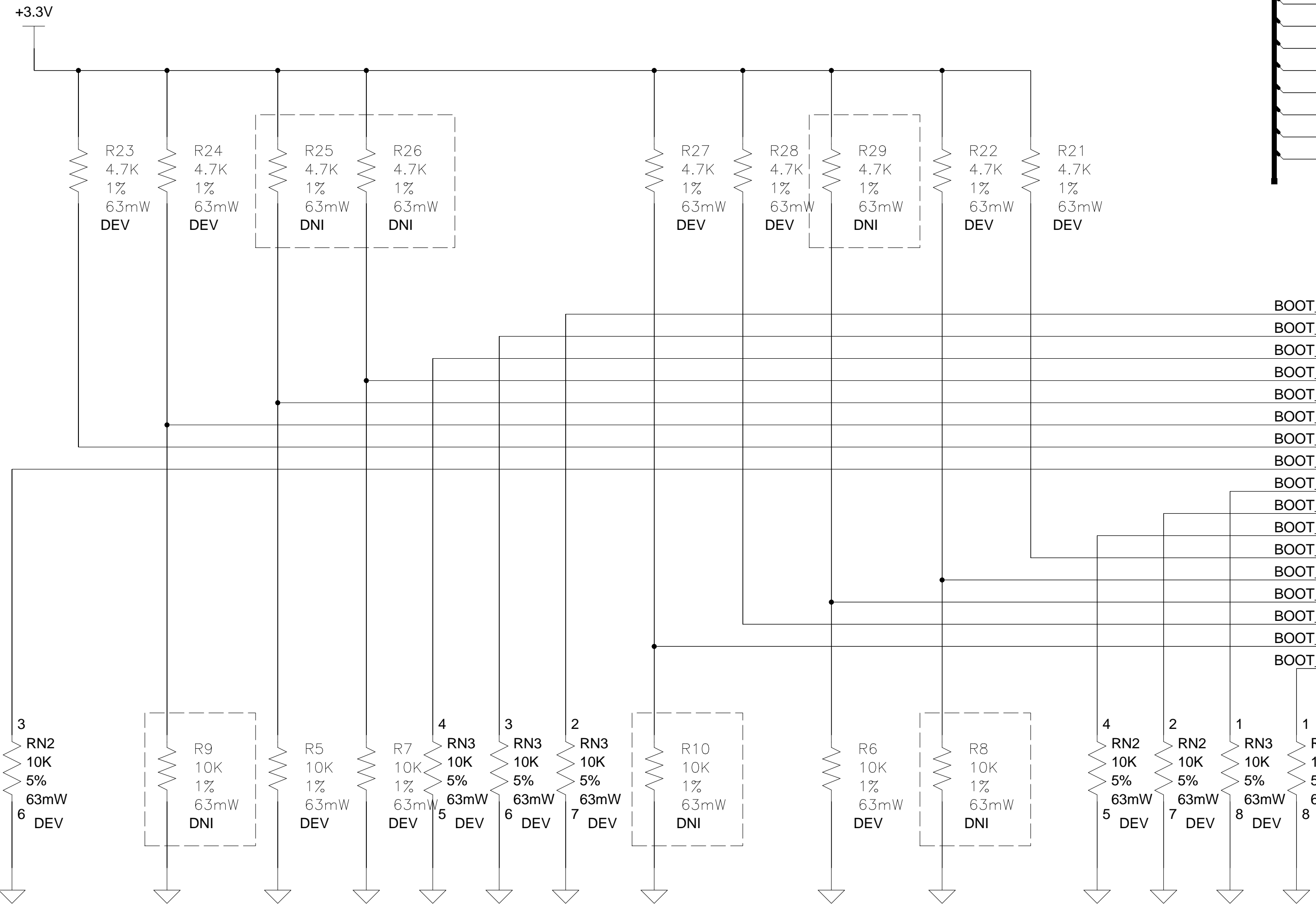
DDR Clock line terminator should be placed near the DDR device on 16 bit designs, and at the 'T' point on 32 bit designs.

E&ES COMMON CPU PROCESSOR 2of4 - DRAM and SPI

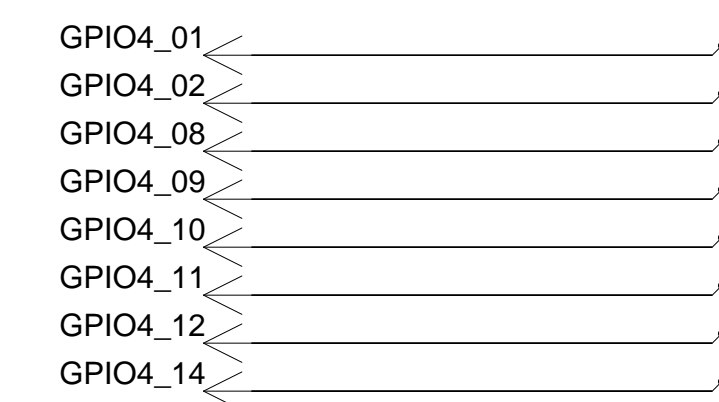
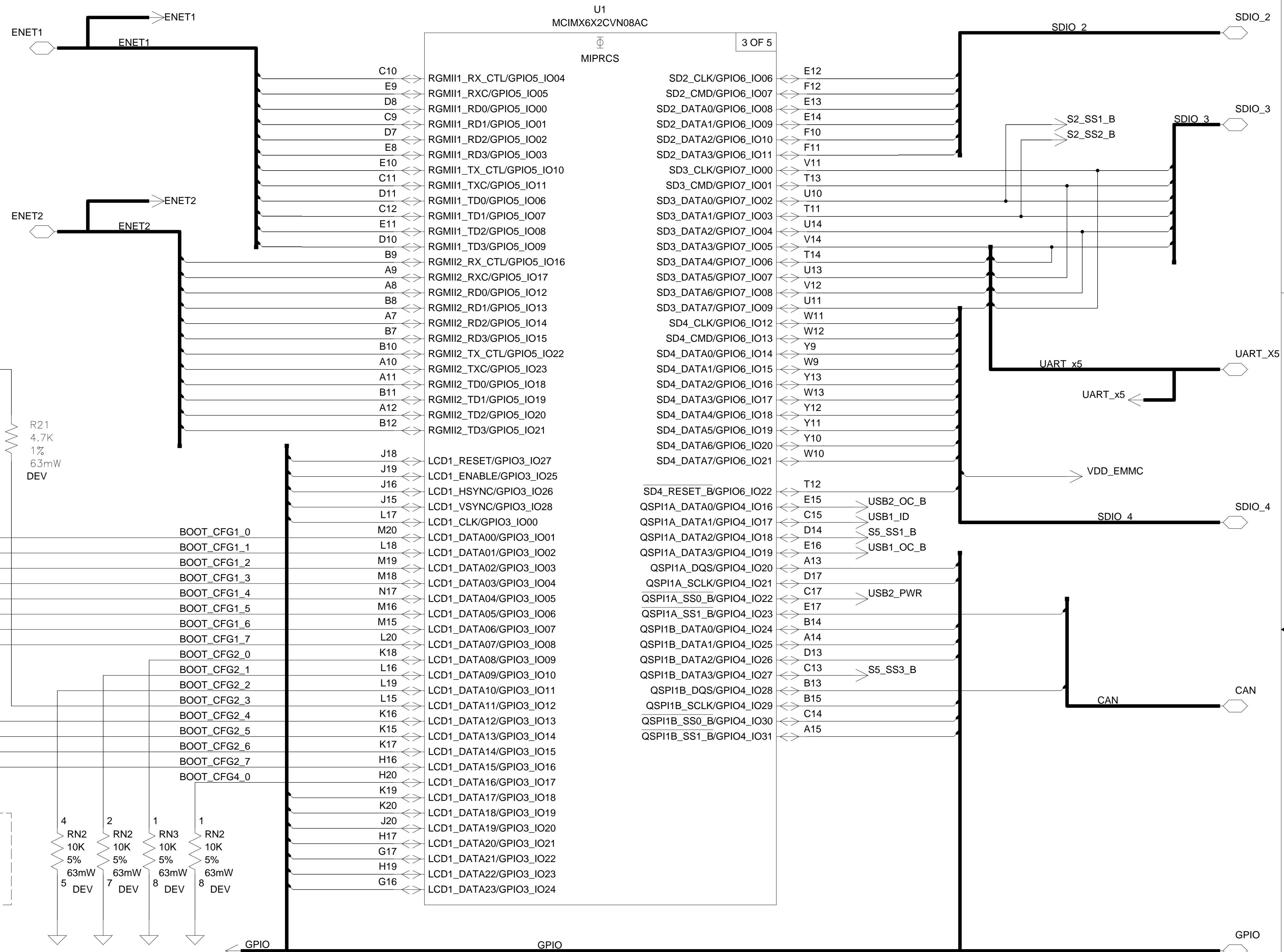
DRAWN BY M'Bock	250CT2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE DRAWING NO. D CPO-PC200,CPO-PC400,CPO-PC400W	REV A
		SCALE: NONE	

Boot configuration for development only. Production boot configuration should be programmed into internal fusebox.
Production designs may have all of these resistors below deleted.

Boot configuration set for eMMC device on USDHC4 with normal boot. Fast boot can be set once normal boot is operating properly. It is also possible to configure to boot from a micro-SD card connected on USDHC2.

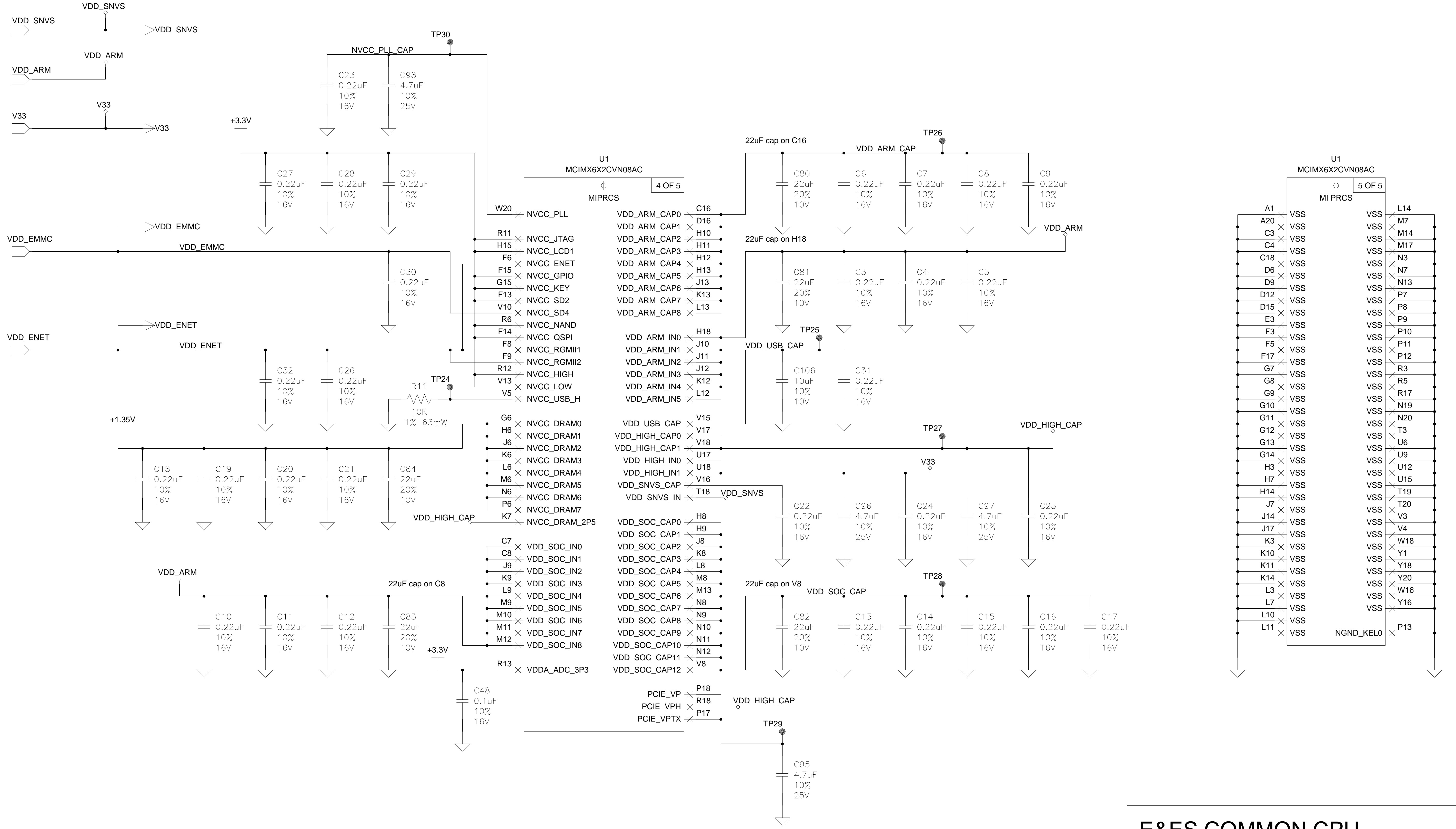


BOOT_CFG1								BOOT_CFG2								BC4	
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	0	
0	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	0	
Boot dev select 01=USDHC	Type 0=SD; 1=MMC/eMMC	Fast Boot 0=Norm; 1=Fast	SD/MMC Speed mode MMC: 00=High speed with fast boot ack SD:00 = Normal speed	SD Power Cycle En eMMC Reset Enable 0=Disabled	SD loopback clk - n/a	Bus Width & SD cal MMC: 010=8-bit SDR 110=8-bit DDR SD: 111=4-bit, with 3 delay cells	Port select MMC: 11=USDHC4 SD: 01=USDHC2	Boot Frequency 0=792/400MHz	USHDC3 Voltage - n/a	Use L2 cache as OCRAM	Reserved						



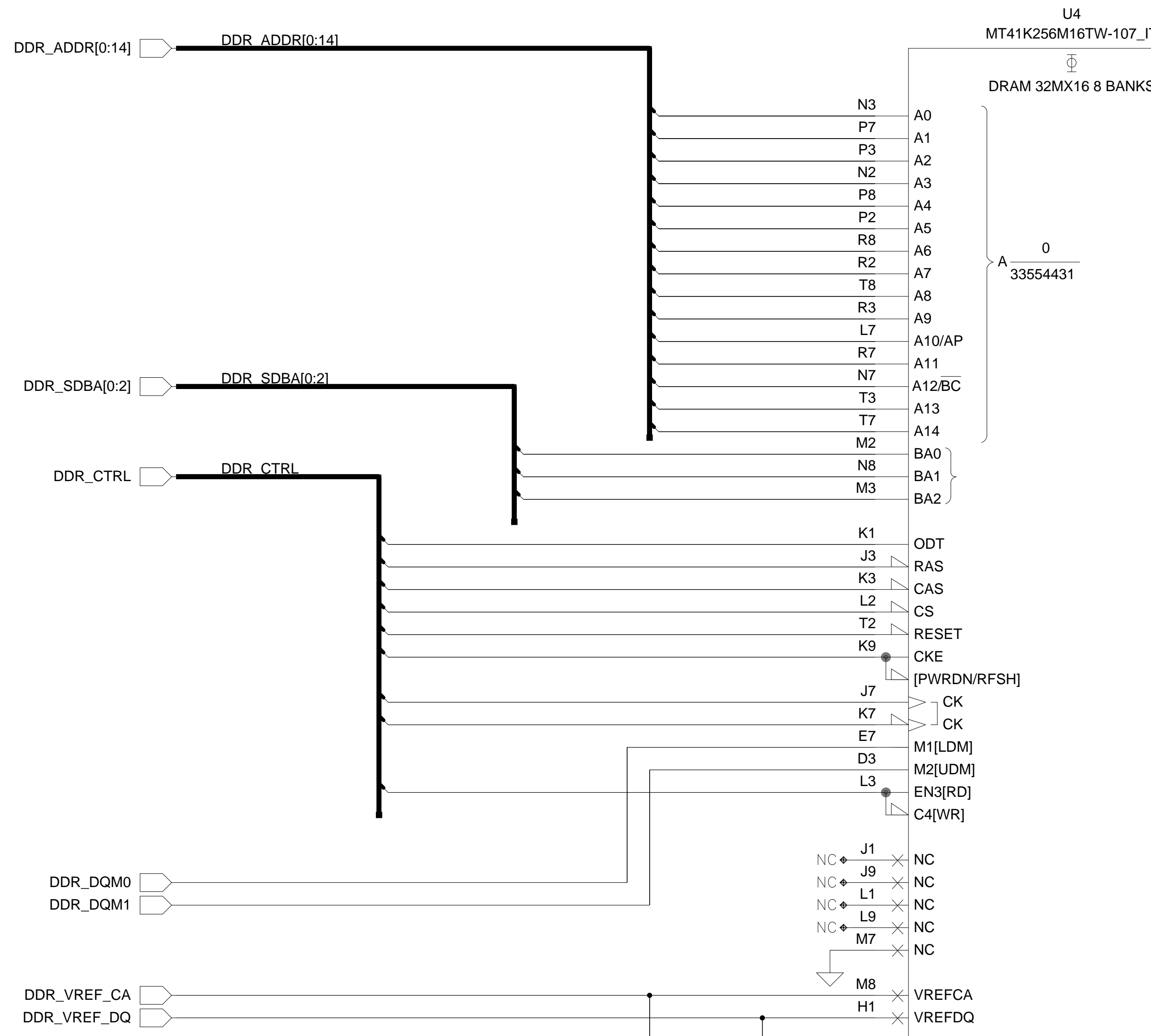
E&S COMMON CPU PROCESSOR 3of4 - eMMC, SDIO, Ethernet , GPIO and Boot Config

DRAWN BY M Back	250CT2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A

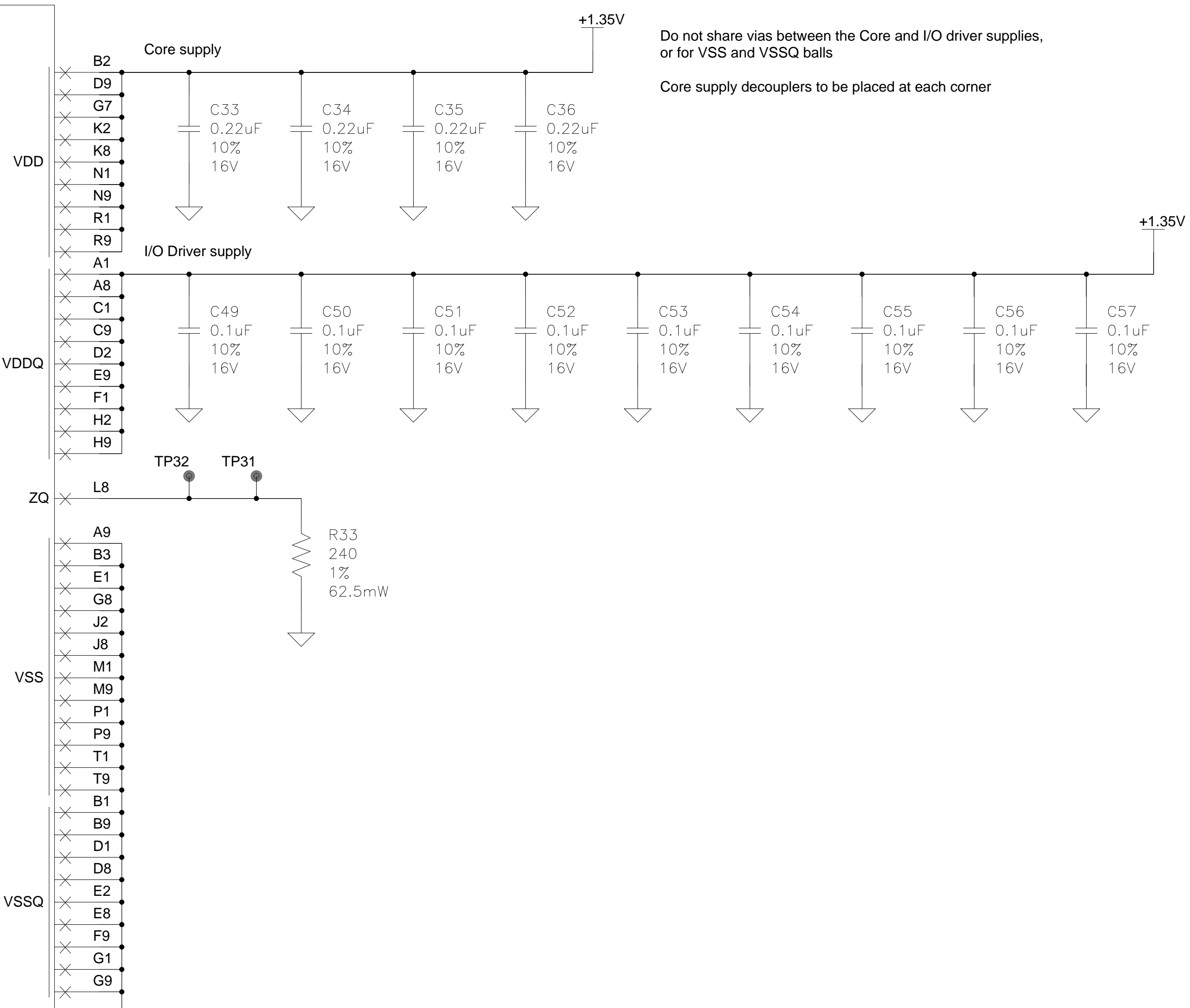


E&S COMMON CPU PROCESSOR 4of4 - Power, Ground and decoupling

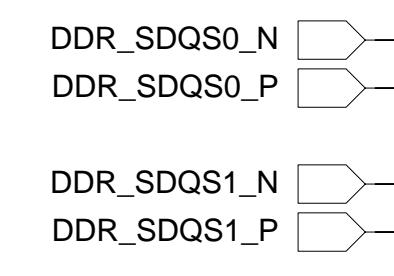
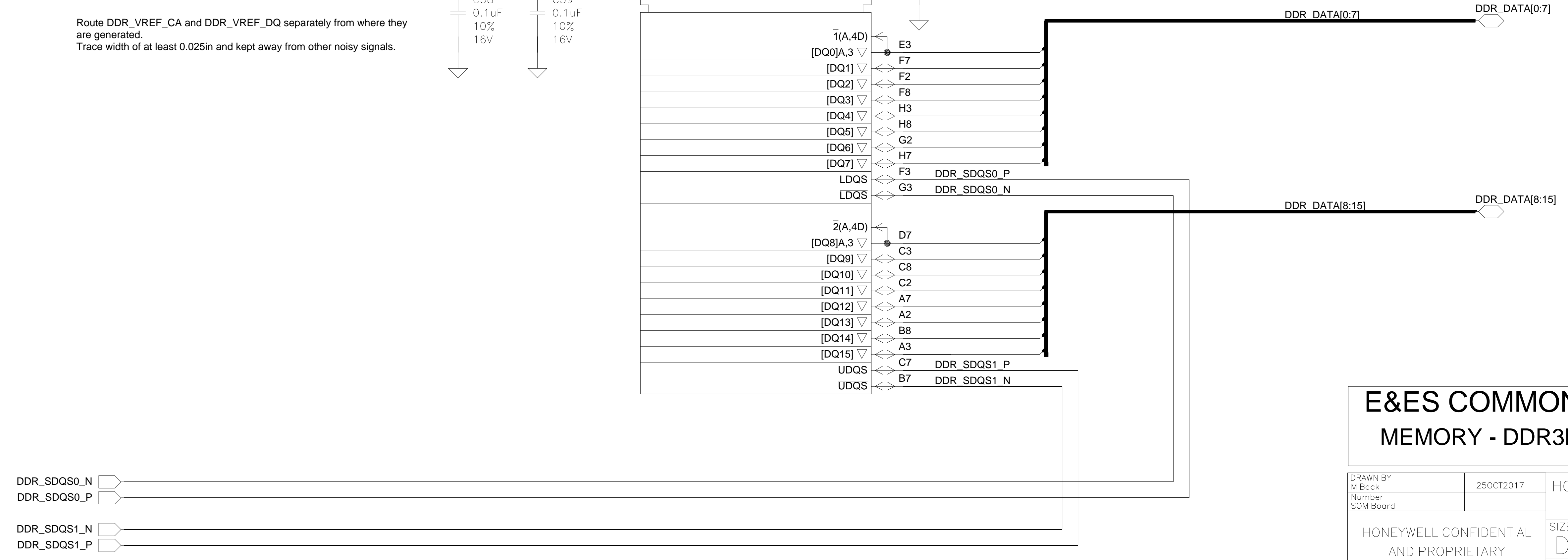
DRAWN BY M Beck	25OCT2017	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES	
Number SOM Board		SIZE DRAWING NO. D CPO-PC200,CPO-PC400,CPO-PC400W	REV A
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SCALE: NONE	



Route DDR_VREF_CA and DDR_VREF_DQ separately from where they are generated.
Trace width of at least 0.025in and kept away from other noisy signals.

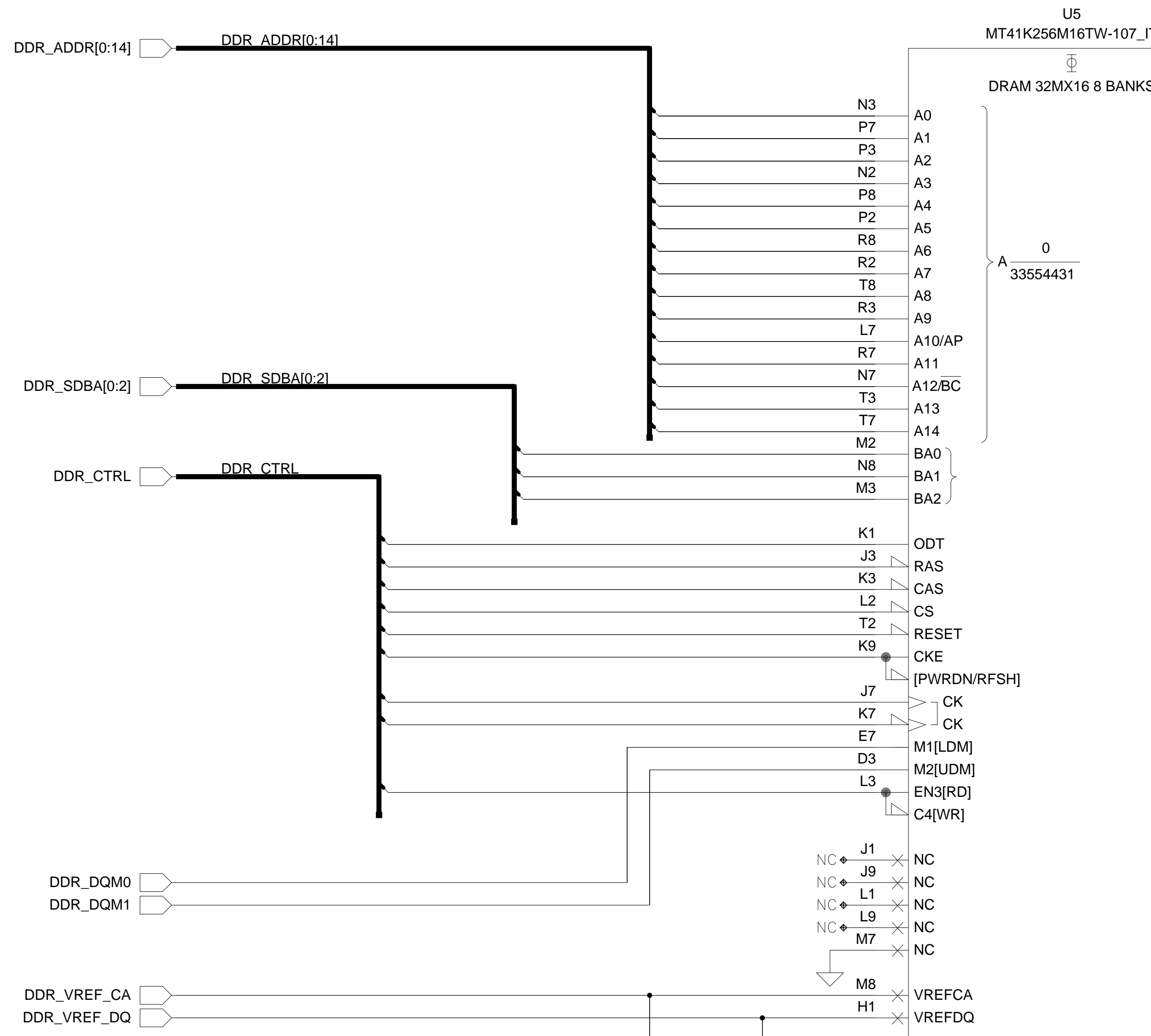


Do not share vias between the Core and I/O driver supplies, or for VSS and VSSQ balls
Core supply decouplers to be placed at each corner

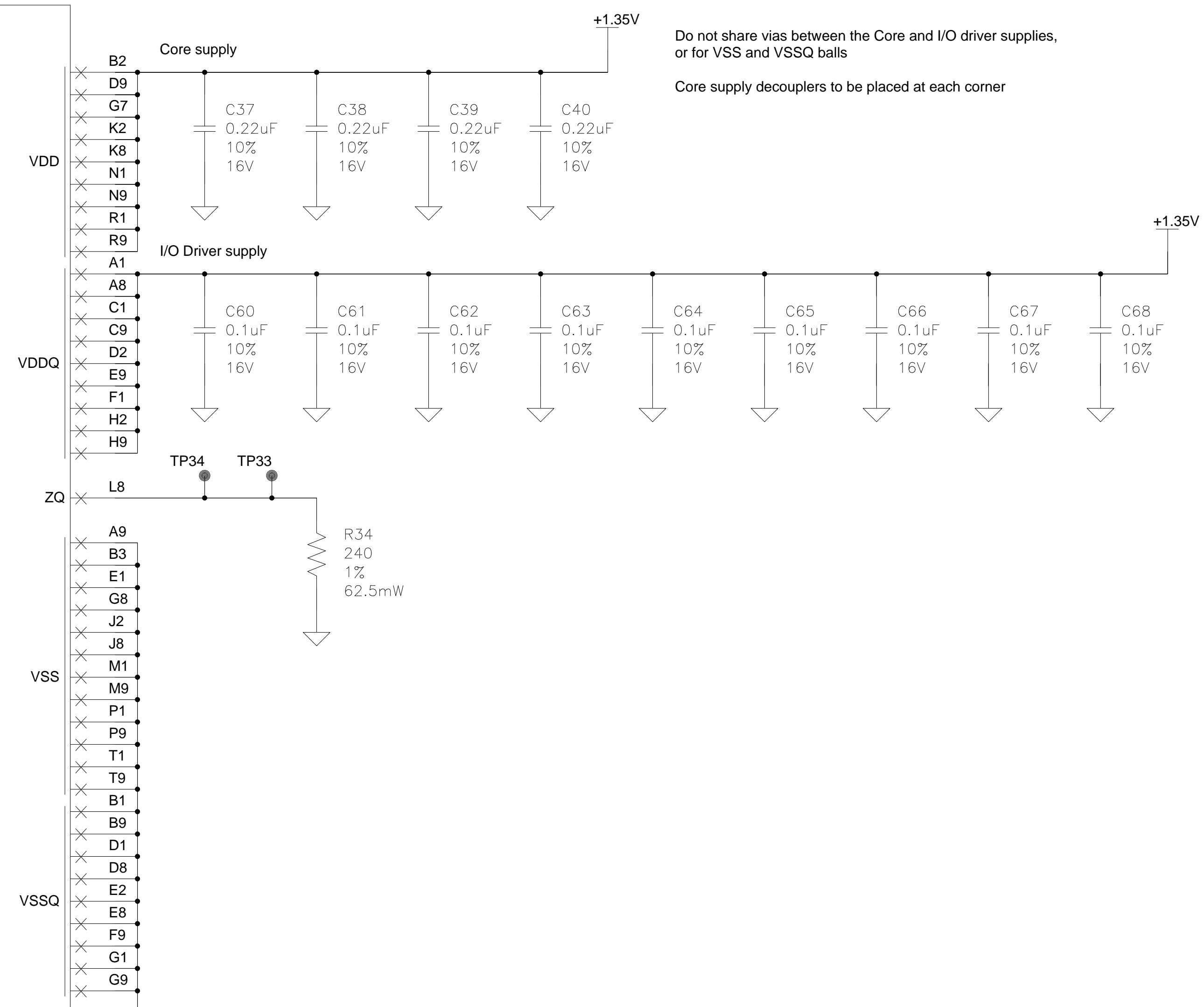


E&ES COMMON CPU MEMORY - DDR3L 256k x16 LOWER

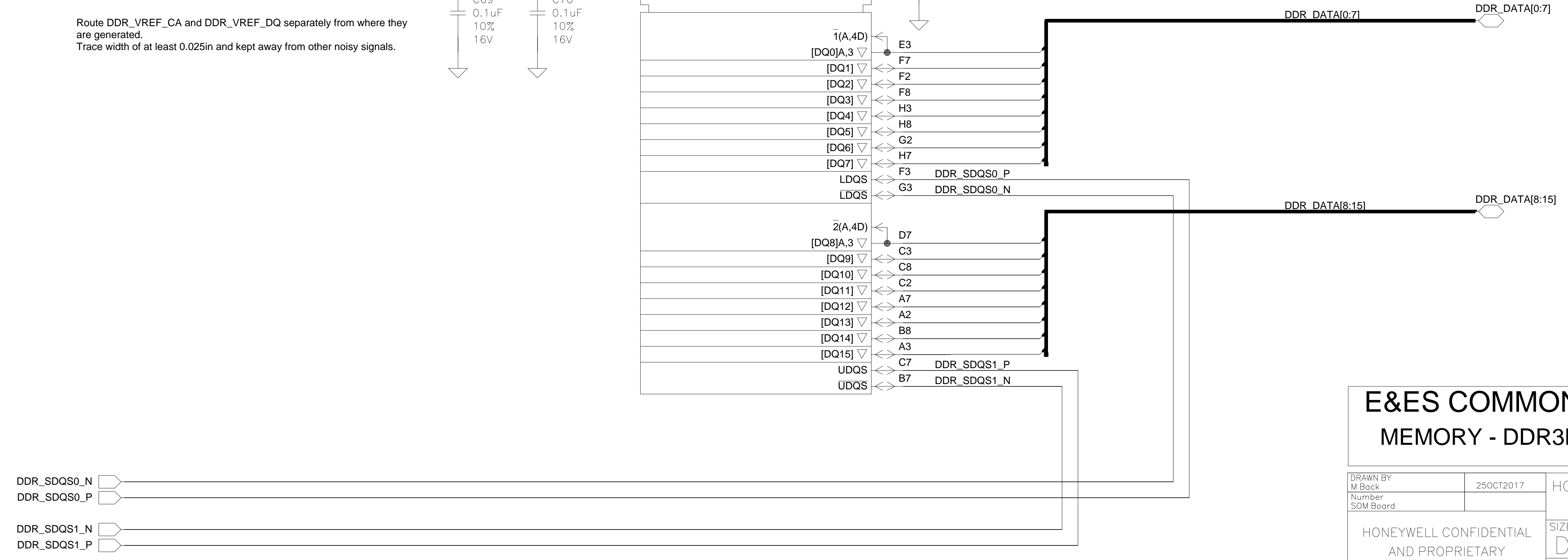
DRAWN BY M Bock	250CT2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A



Route DDR_VREF_CA and DDR_VREF_DQ separately from where they are generated.
Trace width of at least 0.025in and kept away from other noisy signals.

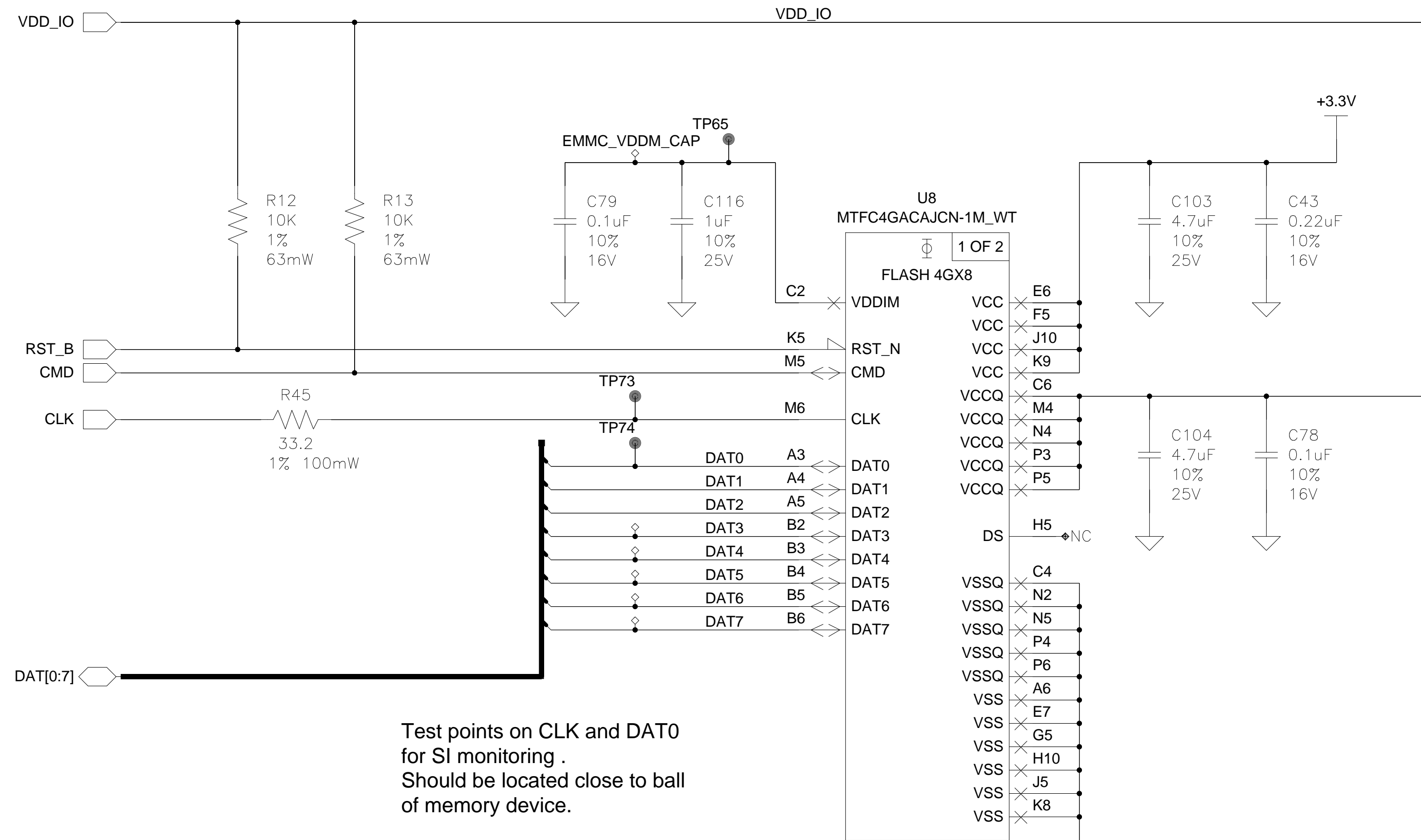


Do not share vias between the Core and I/O driver supplies, or for VSS and VSSQ balls
Core supply decouplers to be placed at each corner

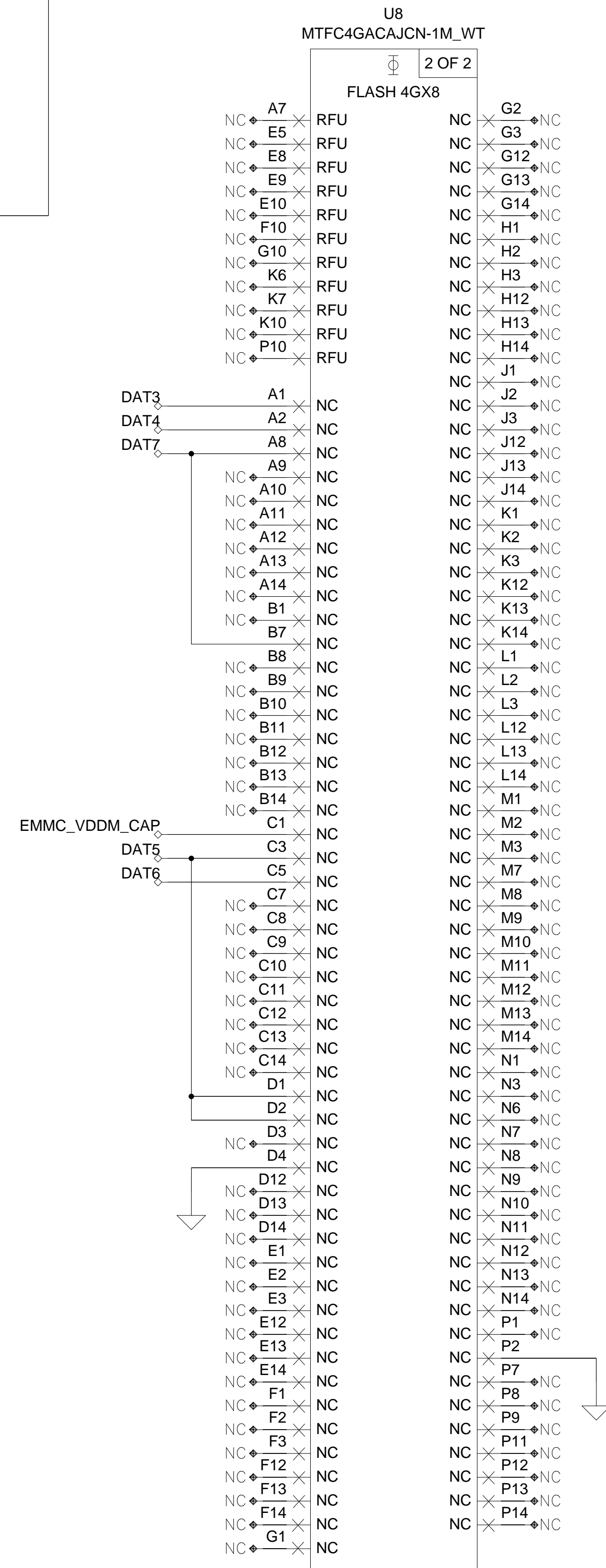


E&ES COMMON CPU MEMORY - DDR3L 256k x16 UPPER

DRAWN BY M Bock	250CT2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE	REV
		D	A
		DRAWING NO.	
		CPO-PC200,CPO-PC400,CPO-PC400W	
		SCALE: NONE	



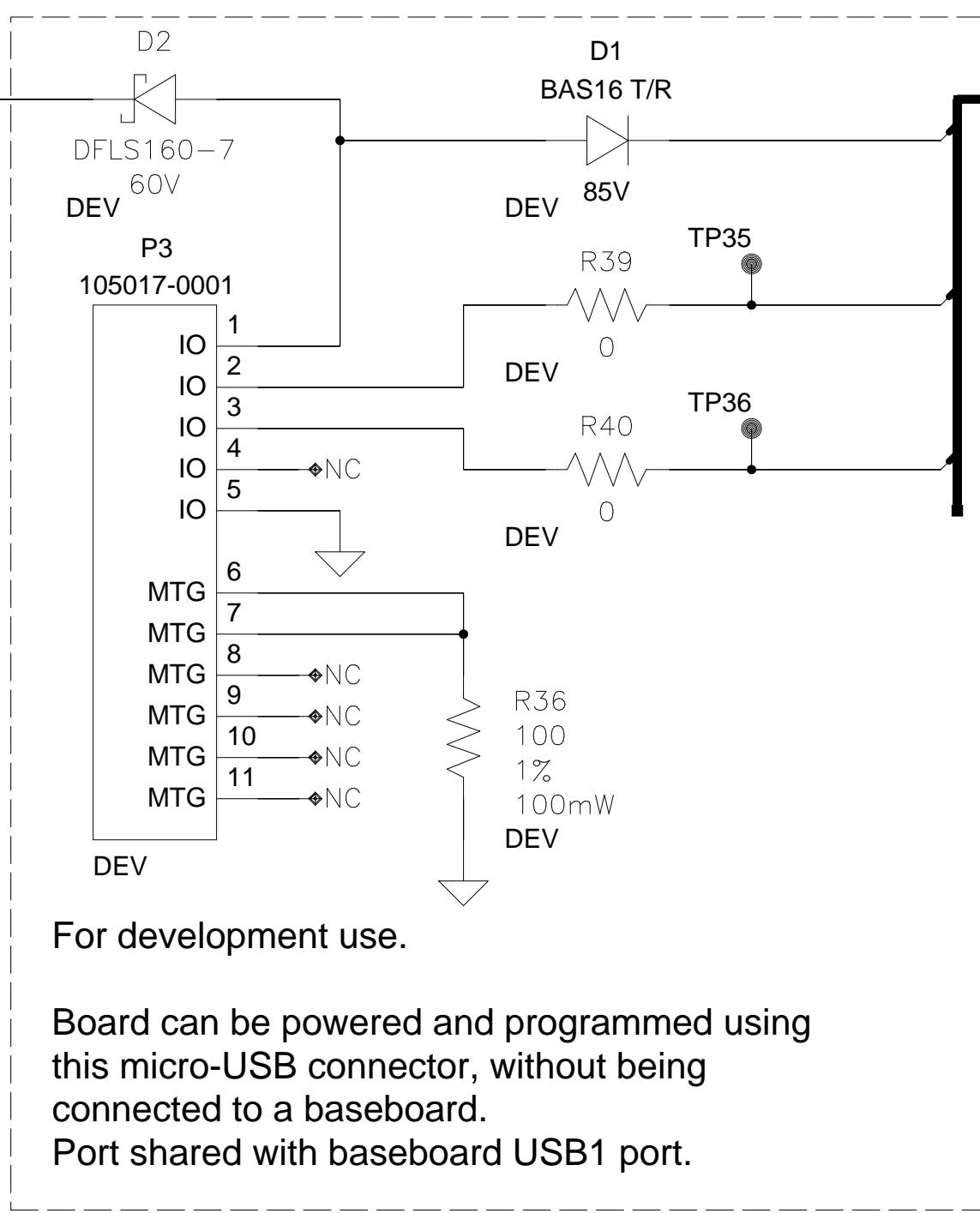
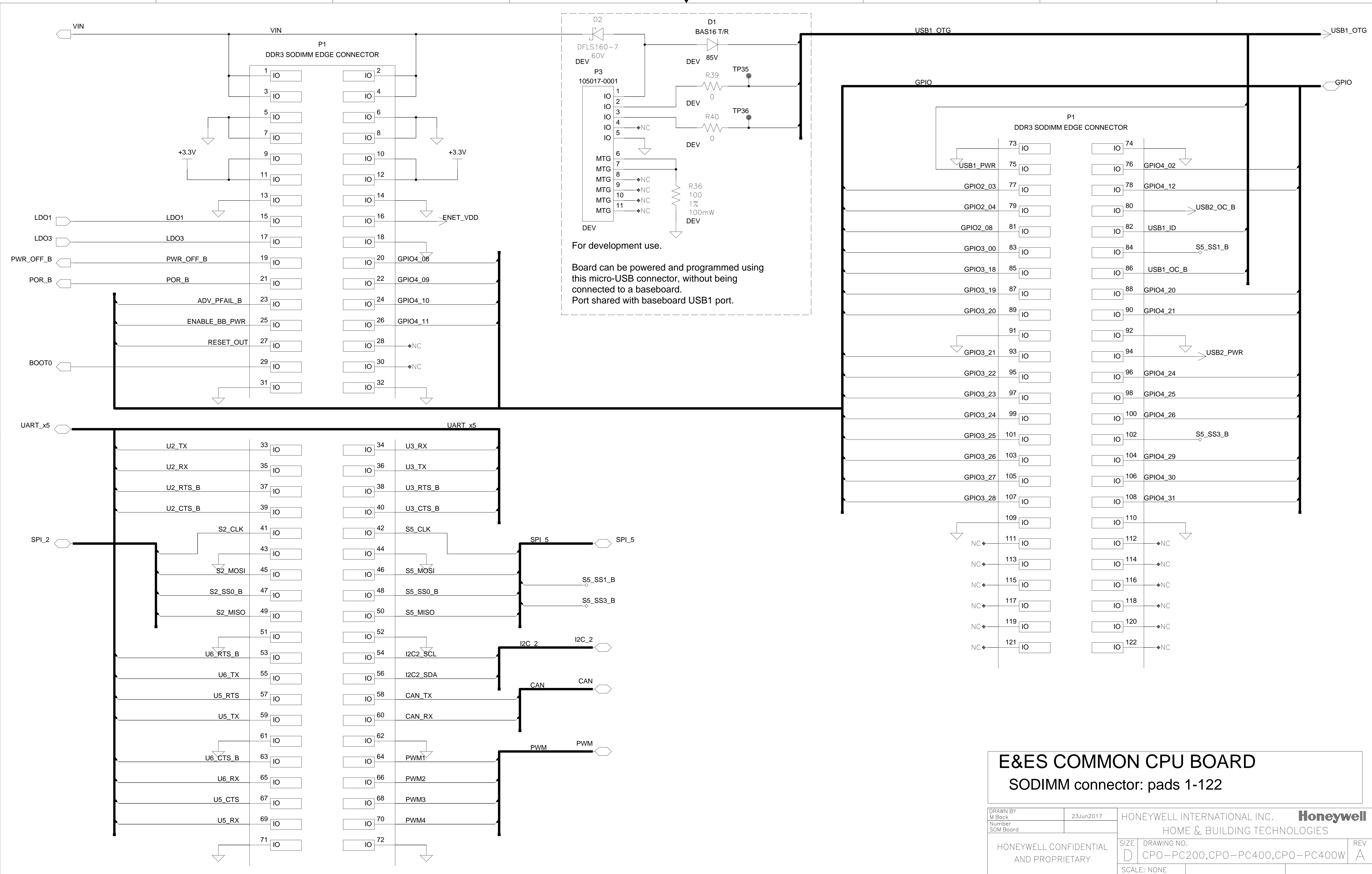
Test points on CLK and DAT0
for SI monitoring .
Should be located close to ball
of memory device.



No Connect balls have no internal
connection and are used to fanout
enclosed signals to avoid the use of
micro-vias.

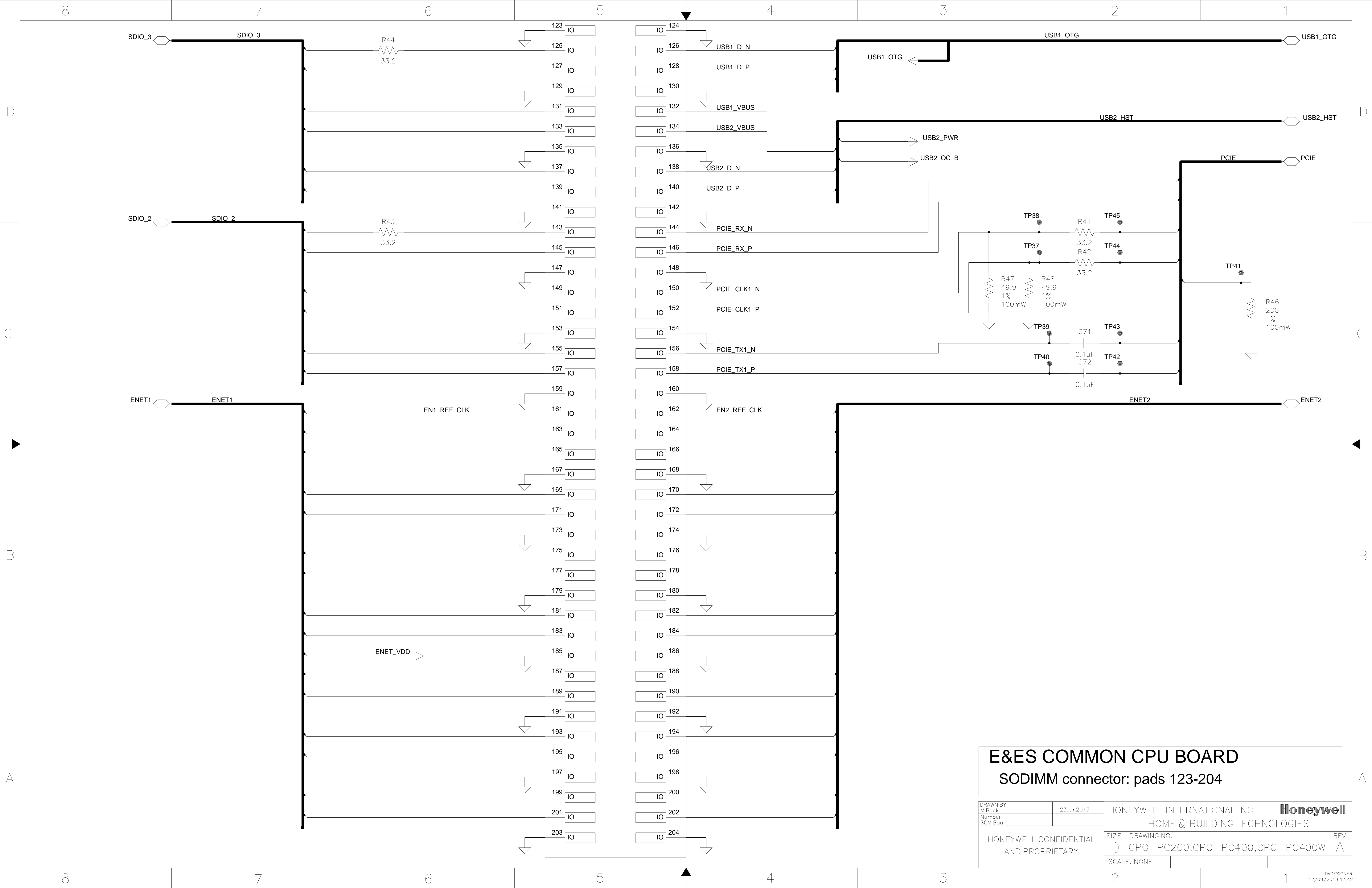
E&ES COMMON CPU MEMORY - eMMC NAND FLASH (4GB) BGA153

DRAWN BY M Back	25OCT2017	HONEYWELL INTERNATIONAL INC.	Honeywell
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A



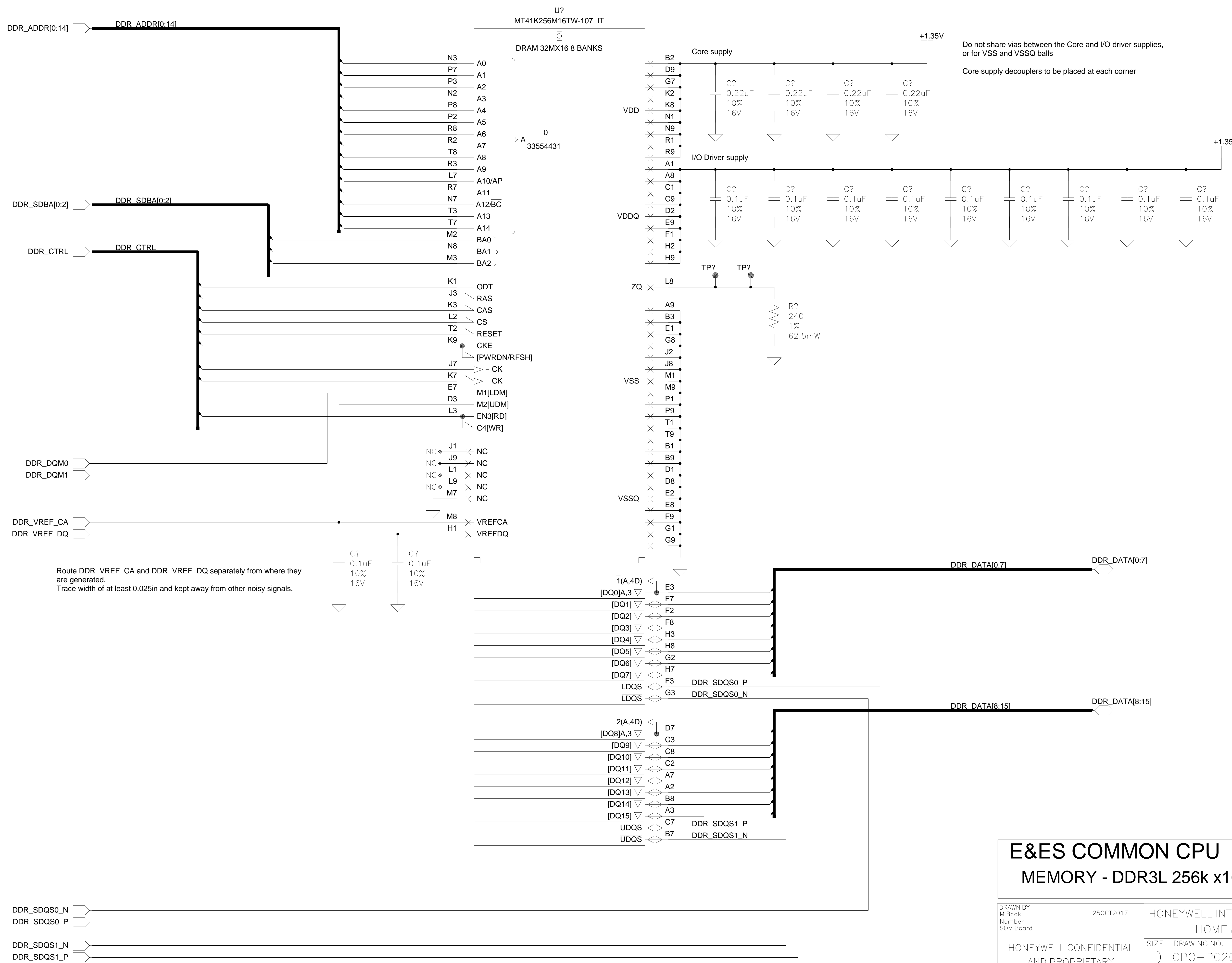
E&ES COMMON CPU BOARD
 SODIMM connector: pads 1-122

DRAWN BY M Back	23Jun2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A



E&S COMMON CPU BOARD
SODIMM connector: pads 123-204

DRAWN BY M Back Number SOM Board	23Jun2017	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE DRAWING NO. D CPO-PC200,CPO-PC400,CPO-PC400W REV SCALE: NONE A

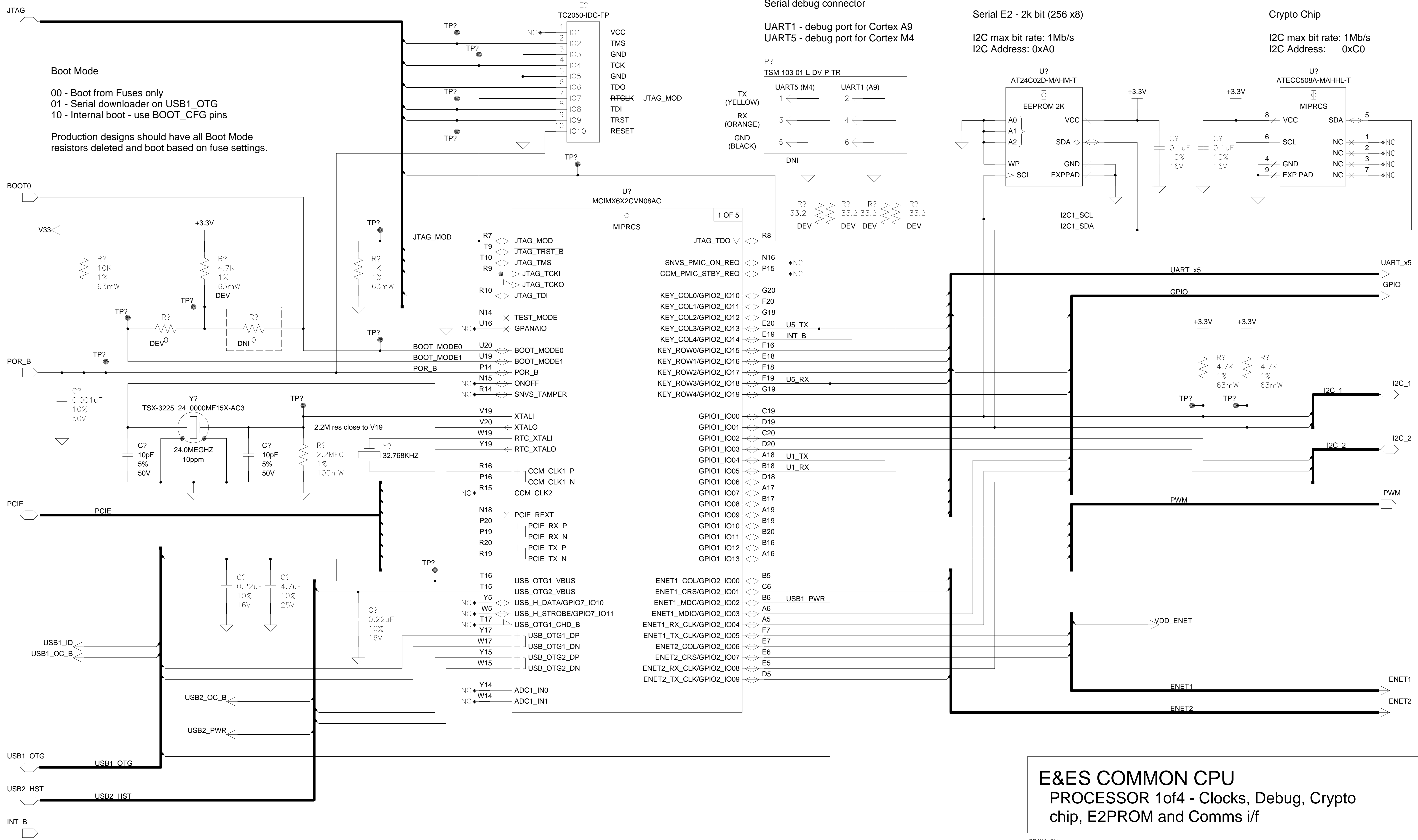


Do not share vias between the Core and I/O driver supplies, or for VSS and VSSQ balls
Core supply decouplers to be placed at each corner

Route DDR_VREF_CA and DDR_VREF_DQ separately from where they are generated.
Trace width of at least 0.025in and kept away from other noisy signals.

E&ES COMMON CPU MEMORY - DDR3L 256k x16

DRAWN BY M Back	250CT2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A



Boot Mode

00 - Boot from Fuses only
 01 - Serial downloader on USB1_OTG
 10 - Internal boot - use BOOT_CFG pins

Production designs should have all Boot Mode resistors deleted and boot based on fuse settings.

Serial debug connector

UART1 - debug port for Cortex A9
 UART5 - debug port for Cortex M4

Serial E2 - 2k bit (256 x8)

I2C max bit rate: 1Mb/s
 I2C Address: 0xA0

Crypto Chip

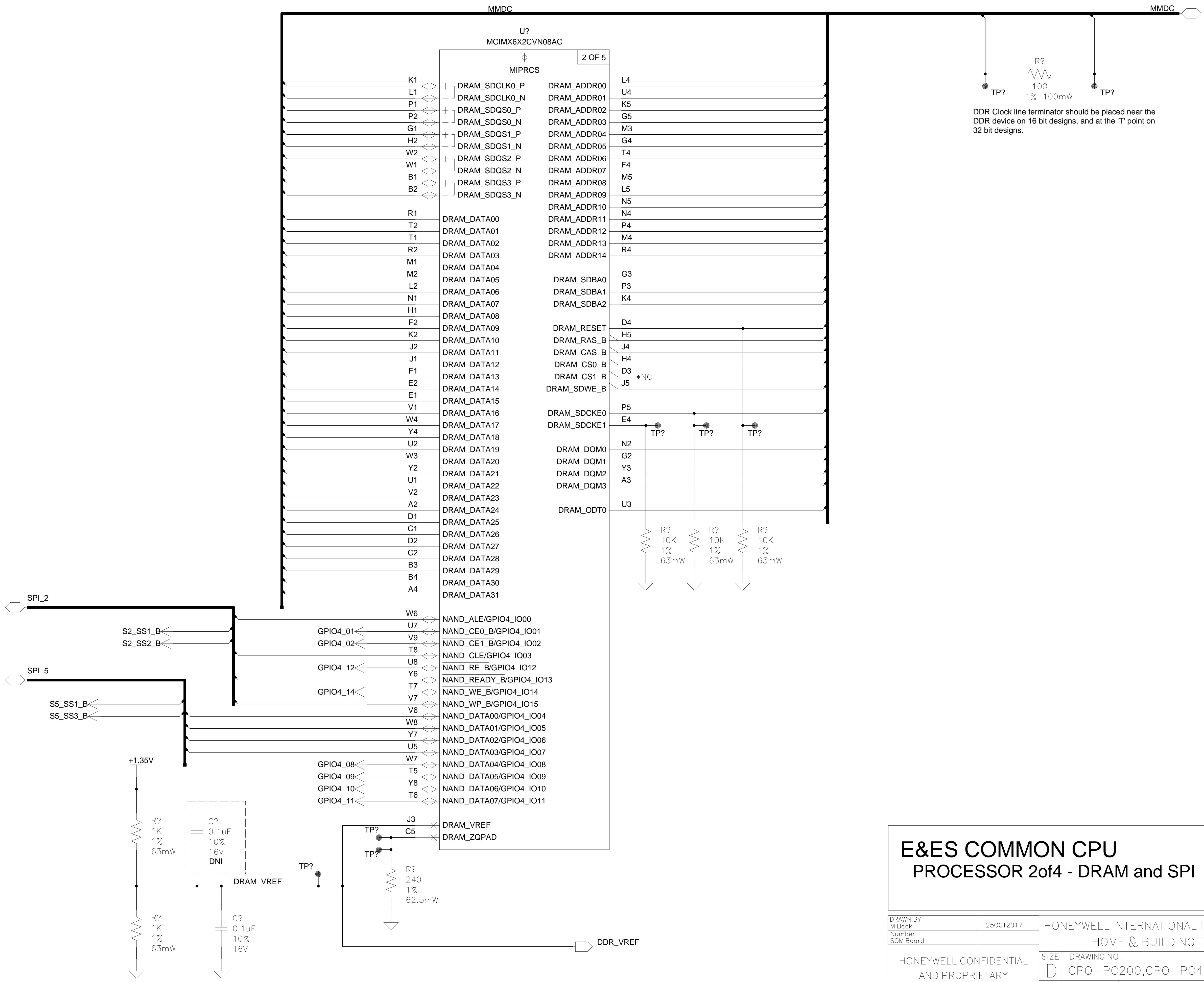
I2C max bit rate: 1Mb/s
 I2C Address: 0xC0

U? MCIMX6X2CVN08AC

JTAG_MOD	R7	JTAG_MOD
JTAG_TRST_B	T9	JTAG_TRST_B
JTAG_TMS	T10	JTAG_TMS
JTAG_TCKI	R9	JTAG_TCKI
JTAG_TCKO	R10	JTAG_TCKO
JTAG_TDI	R10	JTAG_TDI
TEST_MODE	N14	TEST_MODE
GPANAIO	U16	GPANAIO
BOOT_MODE0	U20	BOOT_MODE0
BOOT_MODE1	U19	BOOT_MODE1
POR_B	P14	POR_B
ONOFF	N15	ONOFF
SNVS_TAMPER	R14	SNVS_TAMPER
XTALI	V19	XTALI
XTALO	V20	XTALO
RTC_XTALI	W19	RTC_XTALI
RTC_XTALO	Y19	RTC_XTALO
CCM_CLK1_P	R16	CCM_CLK1_P
CCM_CLK1_N	P16	CCM_CLK1_N
CCM_CLK2	R15	CCM_CLK2
PCIE_REXT	N18	PCIE_REXT
PCIE_RX_P	P20	PCIE_RX_P
PCIE_RX_N	P19	PCIE_RX_N
PCIE_TX_P	R20	PCIE_TX_P
PCIE_TX_N	R19	PCIE_TX_N
USB_OTG1_VBUS	T16	USB_OTG1_VBUS
USB_OTG2_VBUS	T15	USB_OTG2_VBUS
USB_H_DATA/GPIO7_IO10	Y5	USB_H_DATA/GPIO7_IO10
USB_H_STROBE/GPIO7_IO11	W5	USB_H_STROBE/GPIO7_IO11
USB_OTG1_CHD_B	T17	USB_OTG1_CHD_B
USB_OTG1_DP	Y17	USB_OTG1_DP
USB_OTG1_DN	W17	USB_OTG1_DN
USB_OTG2_DP	Y15	USB_OTG2_DP
USB_OTG2_DN	W15	USB_OTG2_DN
ADC1_IN0	Y14	ADC1_IN0
ADC1_IN1	W14	ADC1_IN1
GPIO1_IO00	C19	GPIO1_IO00
GPIO1_IO01	D19	GPIO1_IO01
GPIO1_IO02	C20	GPIO1_IO02
GPIO1_IO03	D20	GPIO1_IO03
GPIO1_IO04	A18	U1_TX
GPIO1_IO05	B18	U1_RX
GPIO1_IO06	D18	GPIO1_IO06
GPIO1_IO07	A17	GPIO1_IO07
GPIO1_IO08	B17	GPIO1_IO08
GPIO1_IO09	A19	GPIO1_IO09
GPIO1_IO10	B19	GPIO1_IO10
GPIO1_IO11	B20	GPIO1_IO11
GPIO1_IO12	B16	GPIO1_IO12
GPIO1_IO13	A16	GPIO1_IO13
ENET1_COL/GPIO2_IO00	B5	ENET1_COL/GPIO2_IO00
ENET1_CRS/GPIO2_IO01	C6	ENET1_CRS/GPIO2_IO01
ENET1_MDC/GPIO2_IO02	B6	ENET1_MDC/GPIO2_IO02
ENET1_MDIO/GPIO2_IO03	A6	ENET1_MDIO/GPIO2_IO03
ENET1_RX_CLK/GPIO2_IO04	A5	ENET1_RX_CLK/GPIO2_IO04
ENET1_TX_CLK/GPIO2_IO05	F7	ENET1_TX_CLK/GPIO2_IO05
ENET2_COL/GPIO2_IO06	E7	ENET2_COL/GPIO2_IO06
ENET2_CRS/GPIO2_IO07	E6	ENET2_CRS/GPIO2_IO07
ENET2_RX_CLK/GPIO2_IO08	E5	ENET2_RX_CLK/GPIO2_IO08
ENET2_TX_CLK/GPIO2_IO09	D5	ENET2_TX_CLK/GPIO2_IO09

E&S COMMON CPU
 PROCESSOR 1of4 - Clocks, Debug, Crypto
 chip, E2PROM and Comms i/f

DRAWN BY M Back	250CT2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A



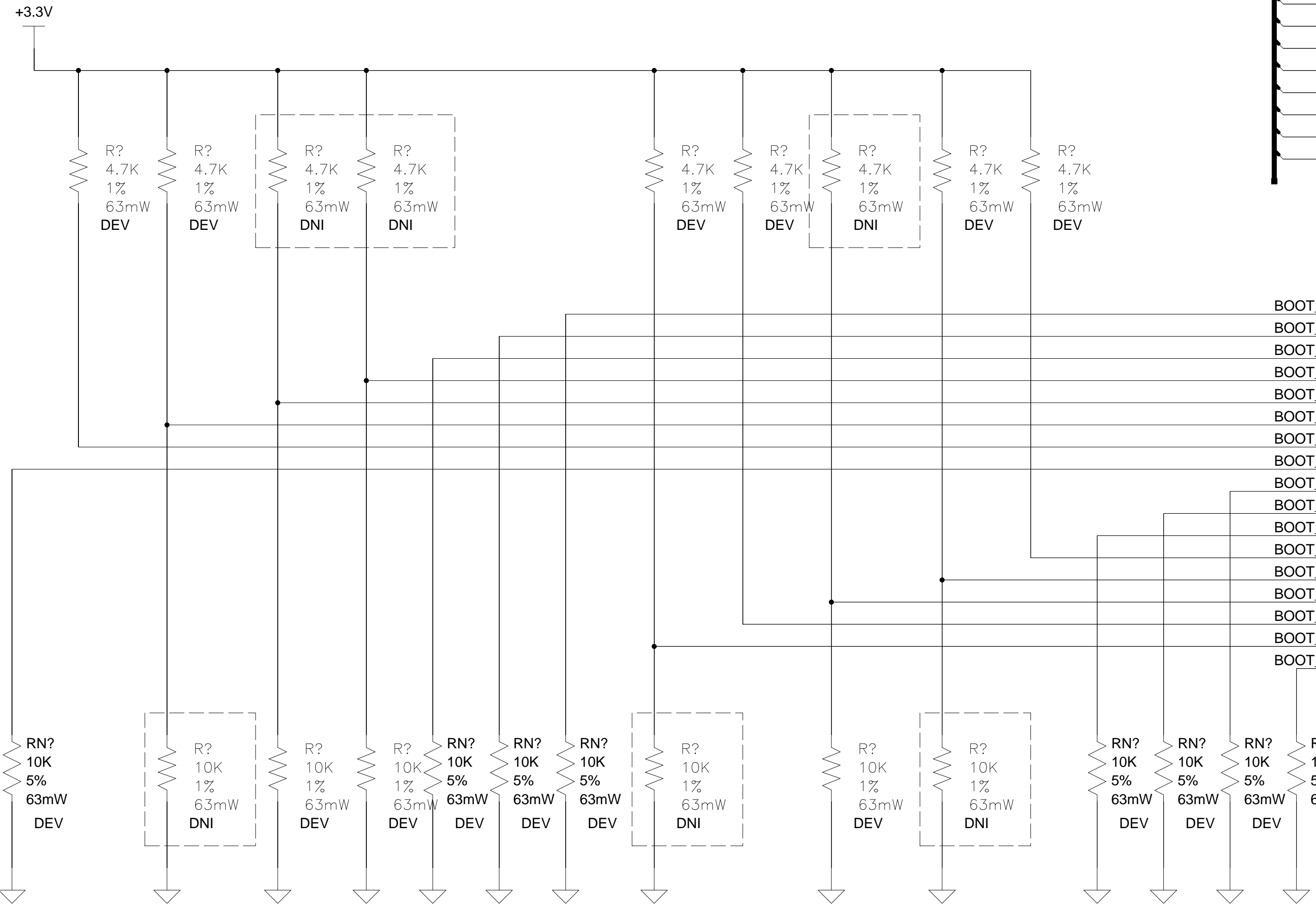
DDR Clock line terminator should be placed near the DDR device on 16 bit designs, and at the 'T' point on 32 bit designs.

E&ES COMMON CPU PROCESSOR 2of4 - DRAM and SPI

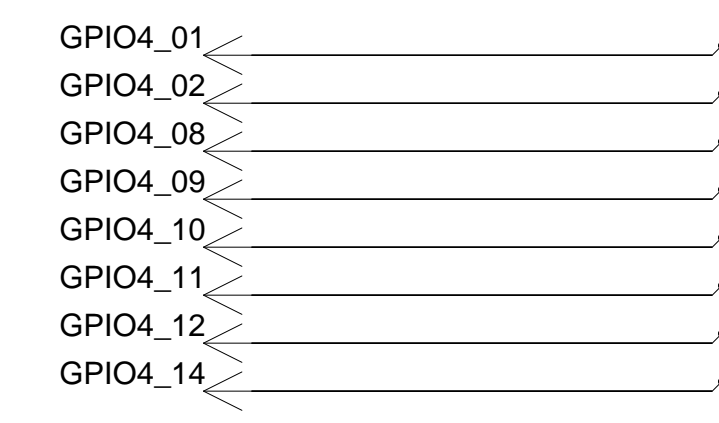
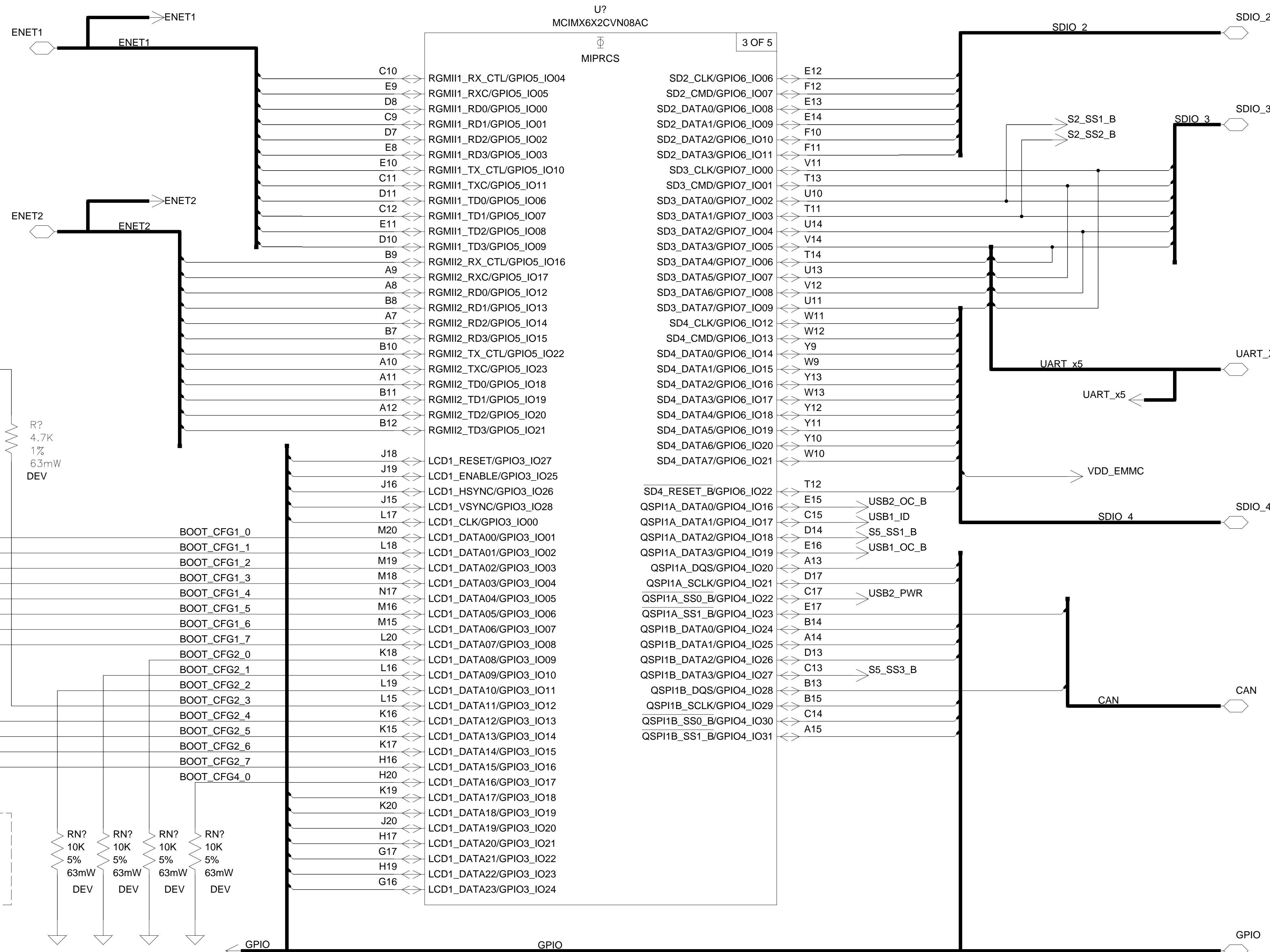
DRAWN BY M Back	250CT2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE DRAWING NO. D CPO-PC200,CPO-PC400,CPO-PC400W	REV A
		SCALE: NONE	

Boot configuration for development only. Production boot configuration should be programmed into internal fusebox.
Production designs may have all of these resistors below deleted.

Boot configuration set for eMMC device on USDHC4 with normal boot. Fast boot can be set once normal boot is operating properly. It is also possible to configure to boot from a micro-SD card connected on USDHC2.

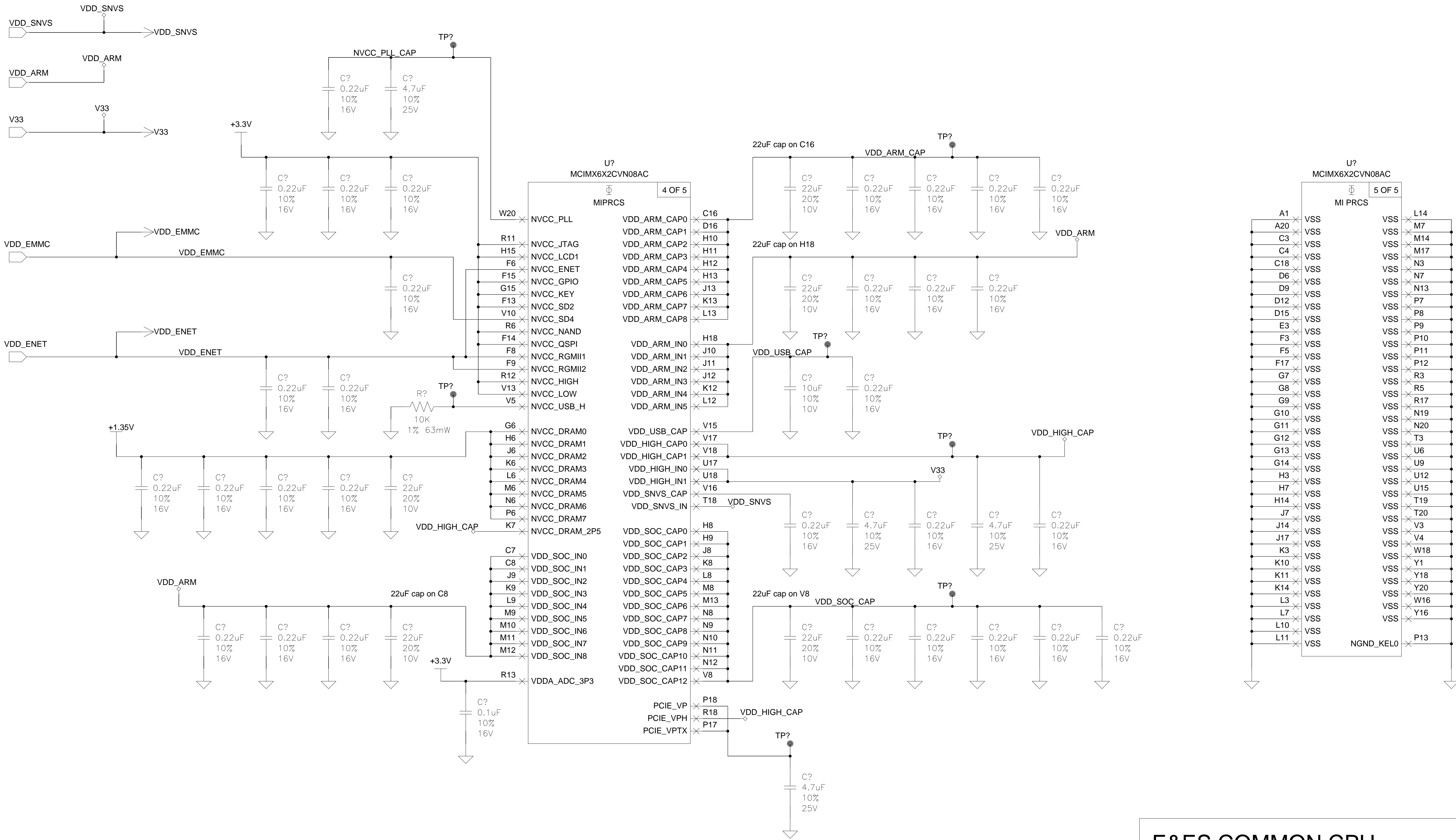


BOOT_CFG1								BOOT_CFG2								BC4
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	0
0	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	0
Boot dev select 01=USDHC	Type 0=SD; 1=MMC/eMMC	Fast Boot 0=Norm; 1=Fast	SD/MMC Speed mode MMC: 00=High speed with fast boot ack SD:00 = Normal speed	SD Power Cycle En eMMC Reset Enable 0=Disabled	SD loopback clk - n/a	Bus Width & SD cal MMC: 010=8-bit SDR 110=8-bit DDR SD: 111=4-bit, with 3 delay cells	Port select MMC: 11=USDHC4 SD: 01=USDHC2	Boot Frequency 0=792/400MHz	USHDC3 Voltage - n/a	Use L2 cache as OCRAM	Reserved					



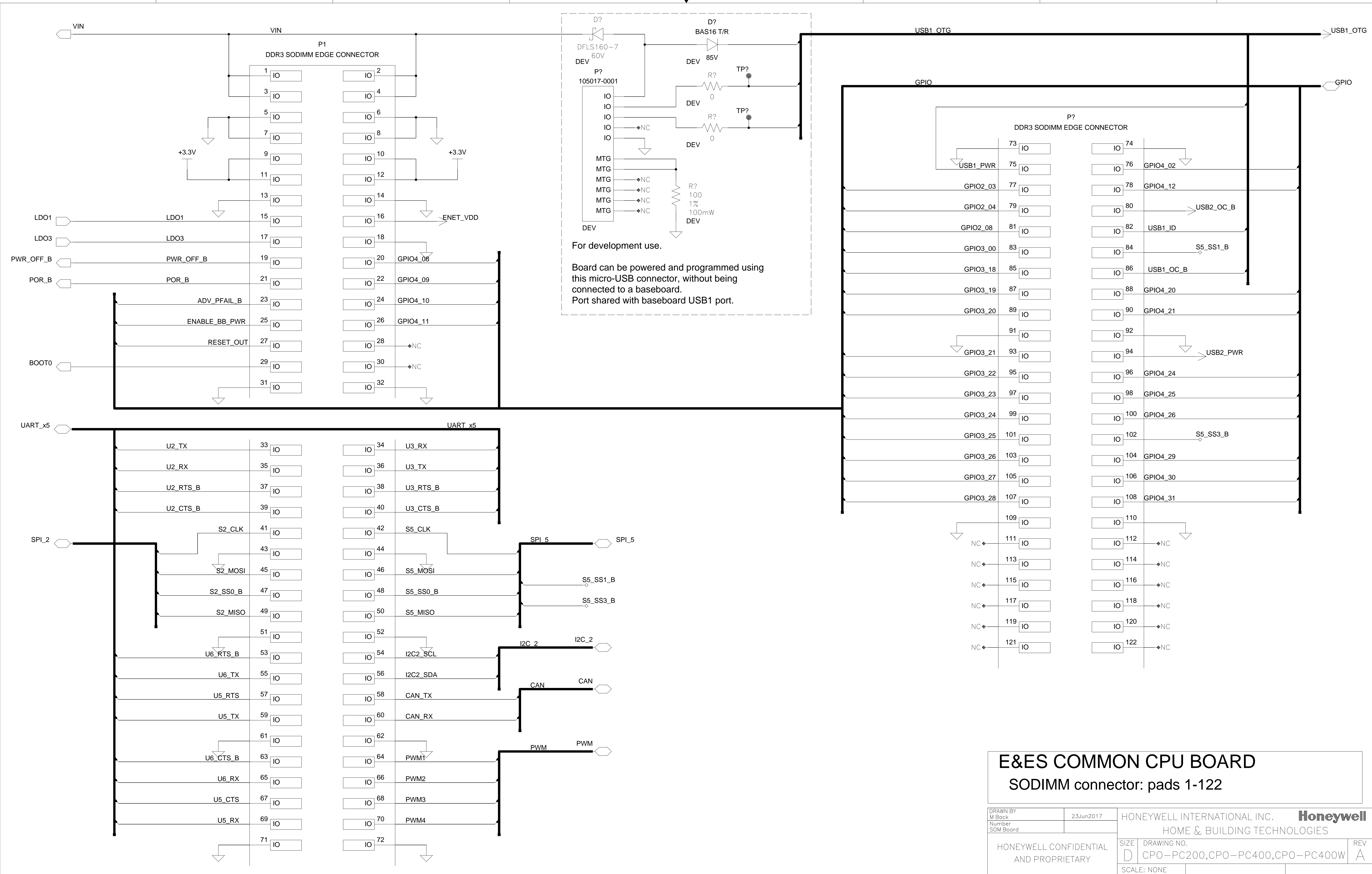
E&S COMMON CPU PROCESSOR 3of4 - eMMC, SDIO, Ethernet , GPIO and Boot Config

DRAWN BY M Back	250CT2017	HONEYWELL INTERNATIONAL INC. Honeywell	
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A



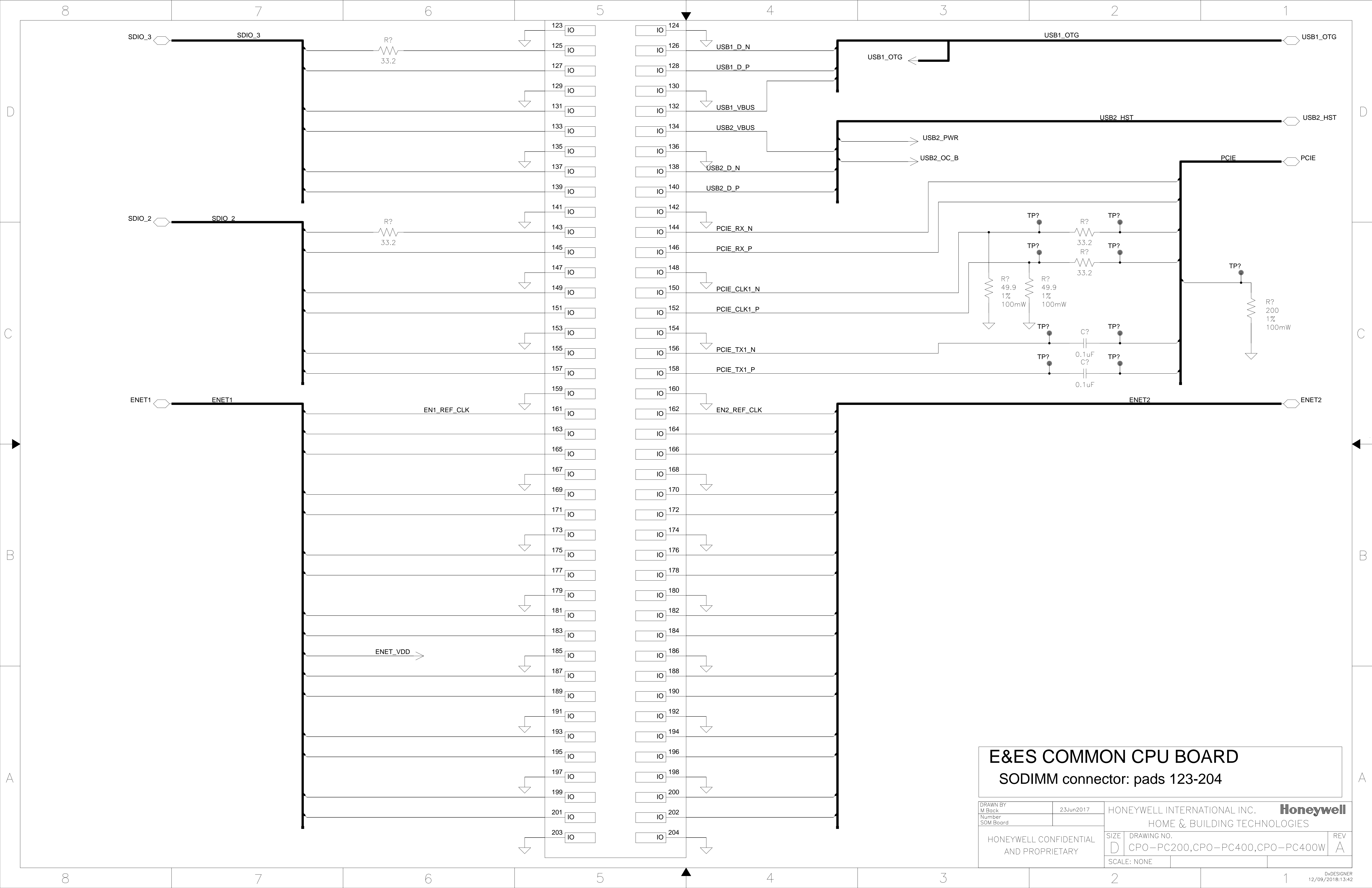
E&ES COMMON CPU PROCESSOR 4of4 - Power, Ground and decoupling

DRAWN BY M Back Number SOM Board	25OCT2017	HONEYWELL INTERNATIONAL INC. HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE DRAWING NO. D CPO-PC200,CPO-PC400,CPO-PC400W	REV A
		SCALE: NONE	



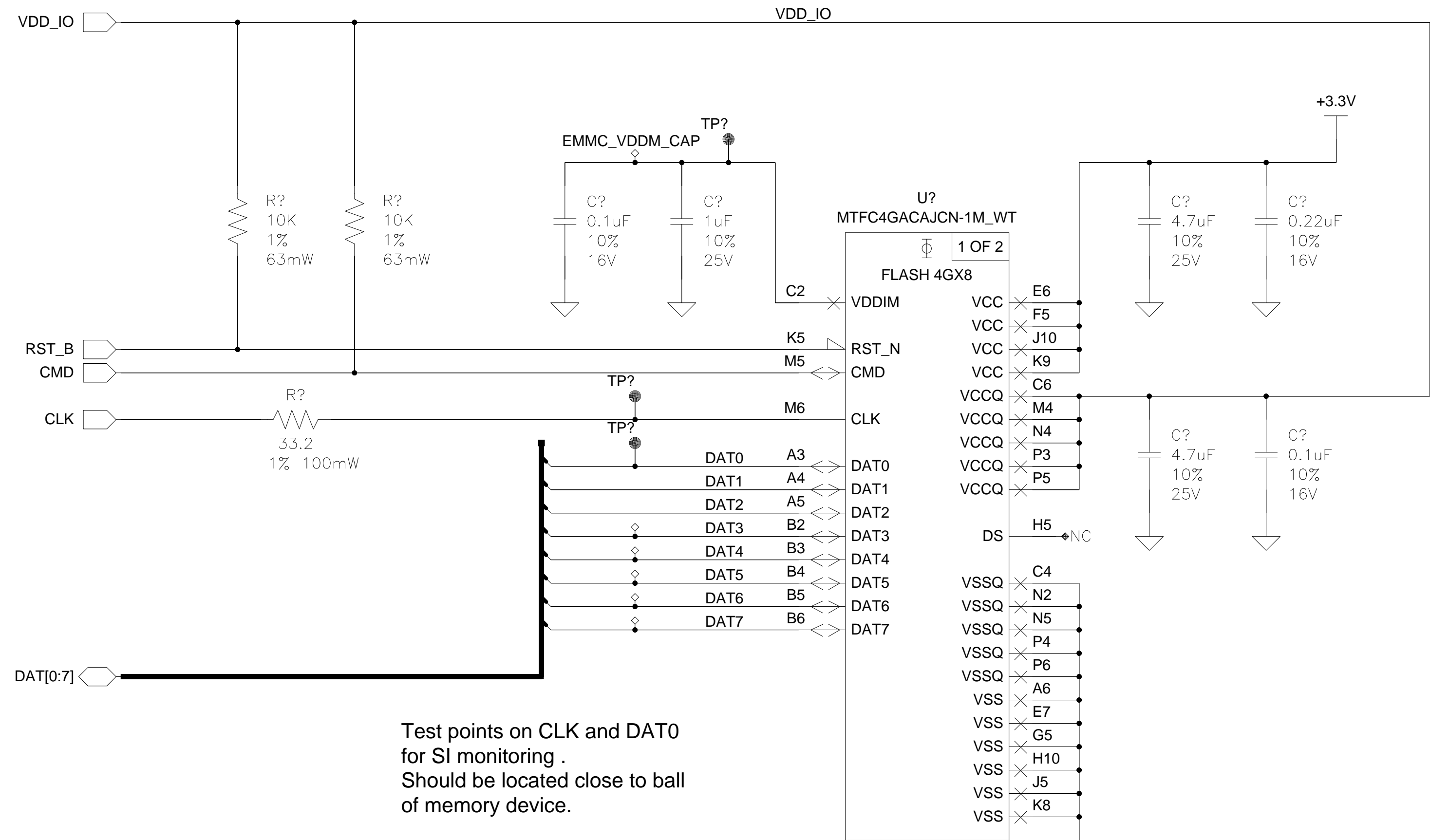
E&ES COMMON CPU BOARD
SODIMM connector: pads 1-122

DRAWN BY M Back Number SOM Board	23Jun2017	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W SCALE: NONE
		REV A

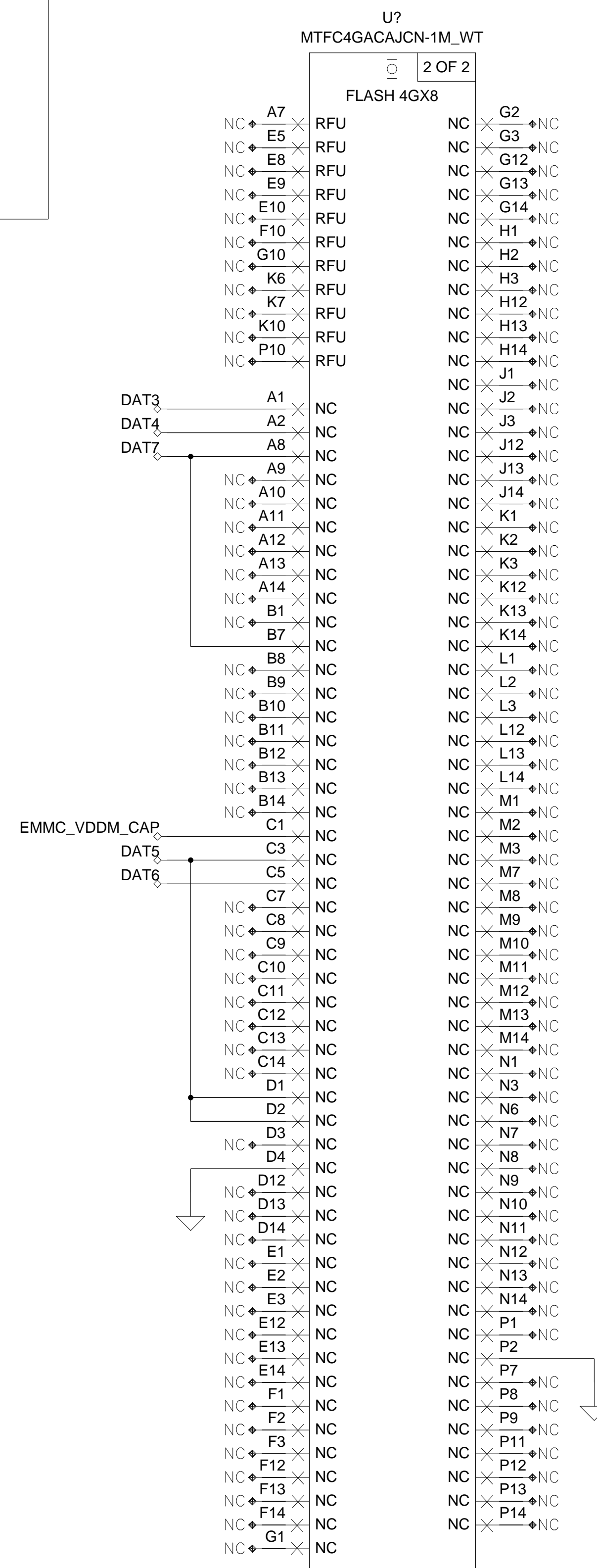


E&ES COMMON CPU BOARD
SODIMM connector: pads 123-204

DRAWN BY M Back Number SOM Board	23Jun2017	HONEYWELL INTERNATIONAL INC. HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W	REV A
		SCALE: NONE	



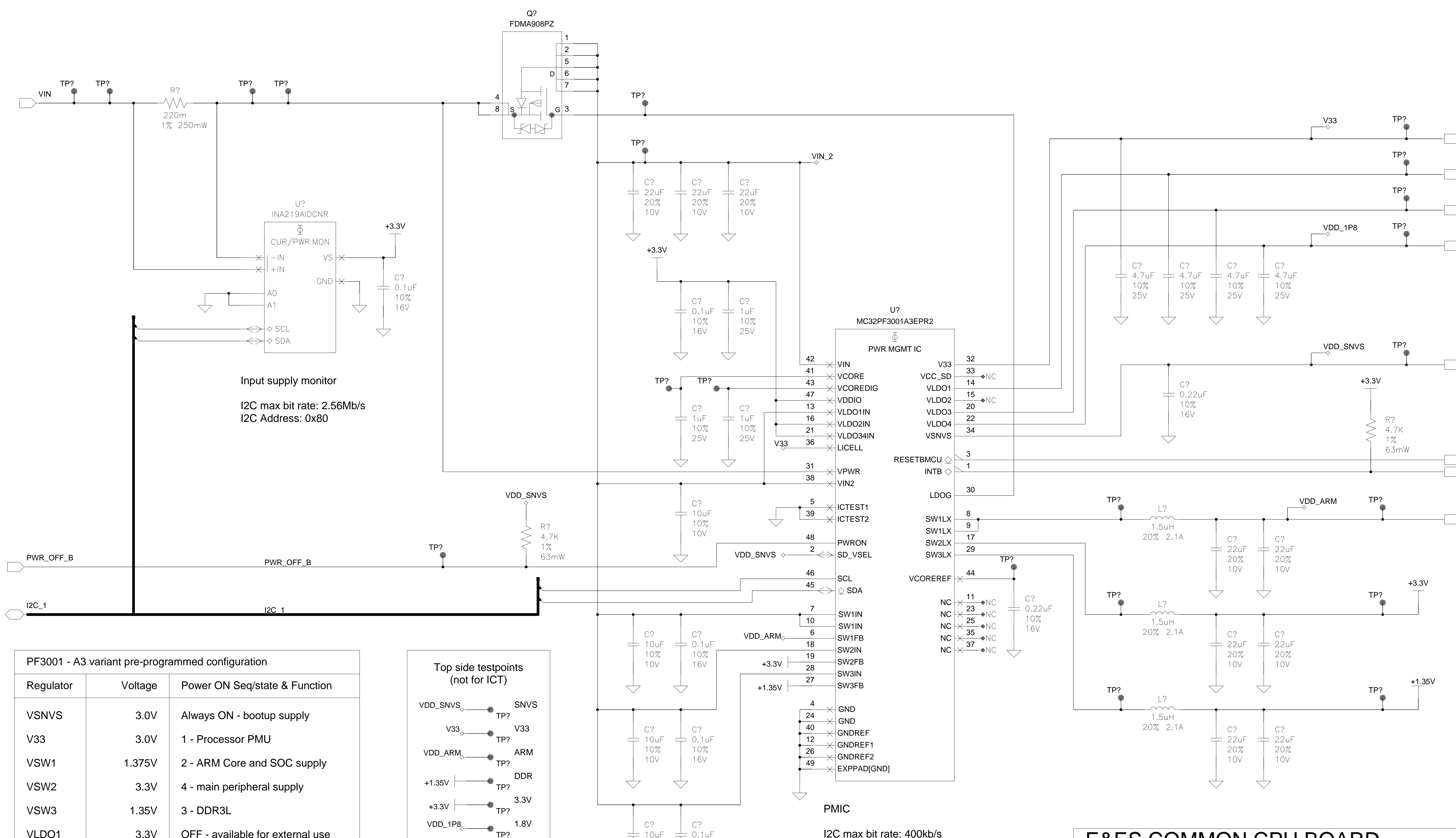
Test points on CLK and DAT0 for SI monitoring. Should be located close to ball of memory device.



No Connect balls have no internal connection and are used to fanout enclosed signals to avoid the use of micro-vias.

E&ES COMMON CPU MEMORY - eMMC NAND FLASH (4GB) BGA153

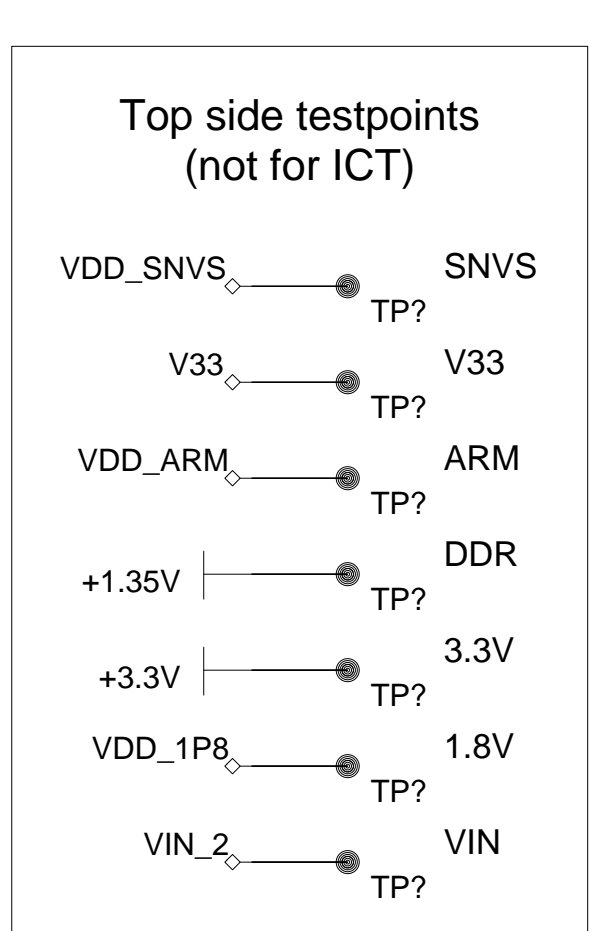
DRAWN BY M Back	25OCT2017	HONEYWELL INTERNATIONAL INC.	Honeywell
Number SOM Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A



Input supply monitor
 I2C max bit rate: 2.56Mb/s
 I2C Address: 0x80

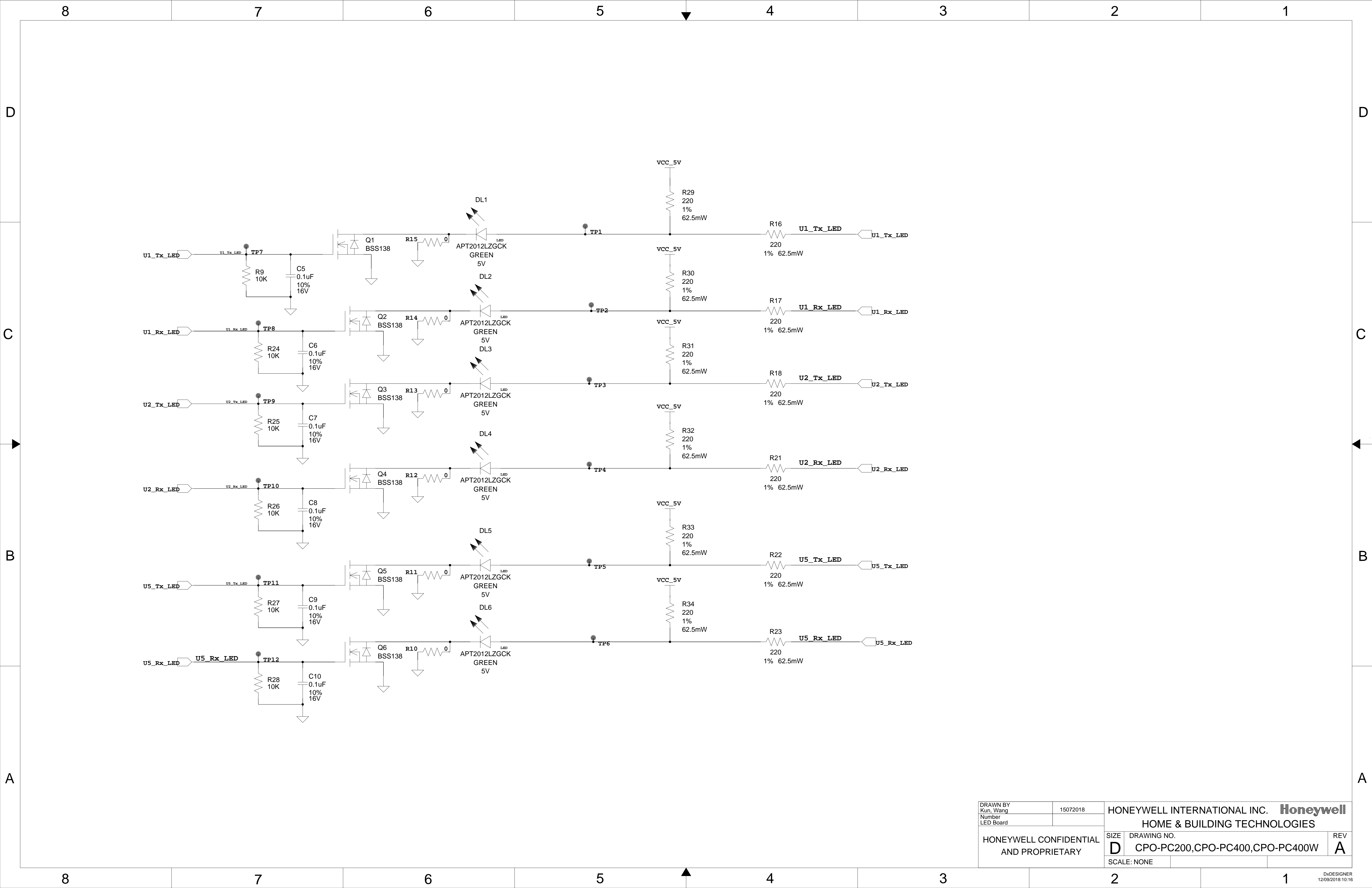
PMIC
 I2C max bit rate: 400kb/s
 I2C Address: 0x10

PF3001 - A3 variant pre-programmed configuration		
Regulator	Voltage	Power ON Seq/state & Function
VSNVS	3.0V	Always ON - bootup supply
V33	3.0V	1 - Processor PMU
VSW1	1.375V	2 - ARM Core and SOC supply
VSW2	3.3V	4 - main peripheral supply
VSW3	1.35V	3 - DDR3L
VLDO1	3.3V	OFF - available for external use
VLDO2	1.5V	OFF - not used
VLDO3	2.5V	OFF - available for external use
VLDO4	1.8V	4 - eMMC I/O and RGMII I/O
VCC_SD	3.3V/1.85V	5 - not used

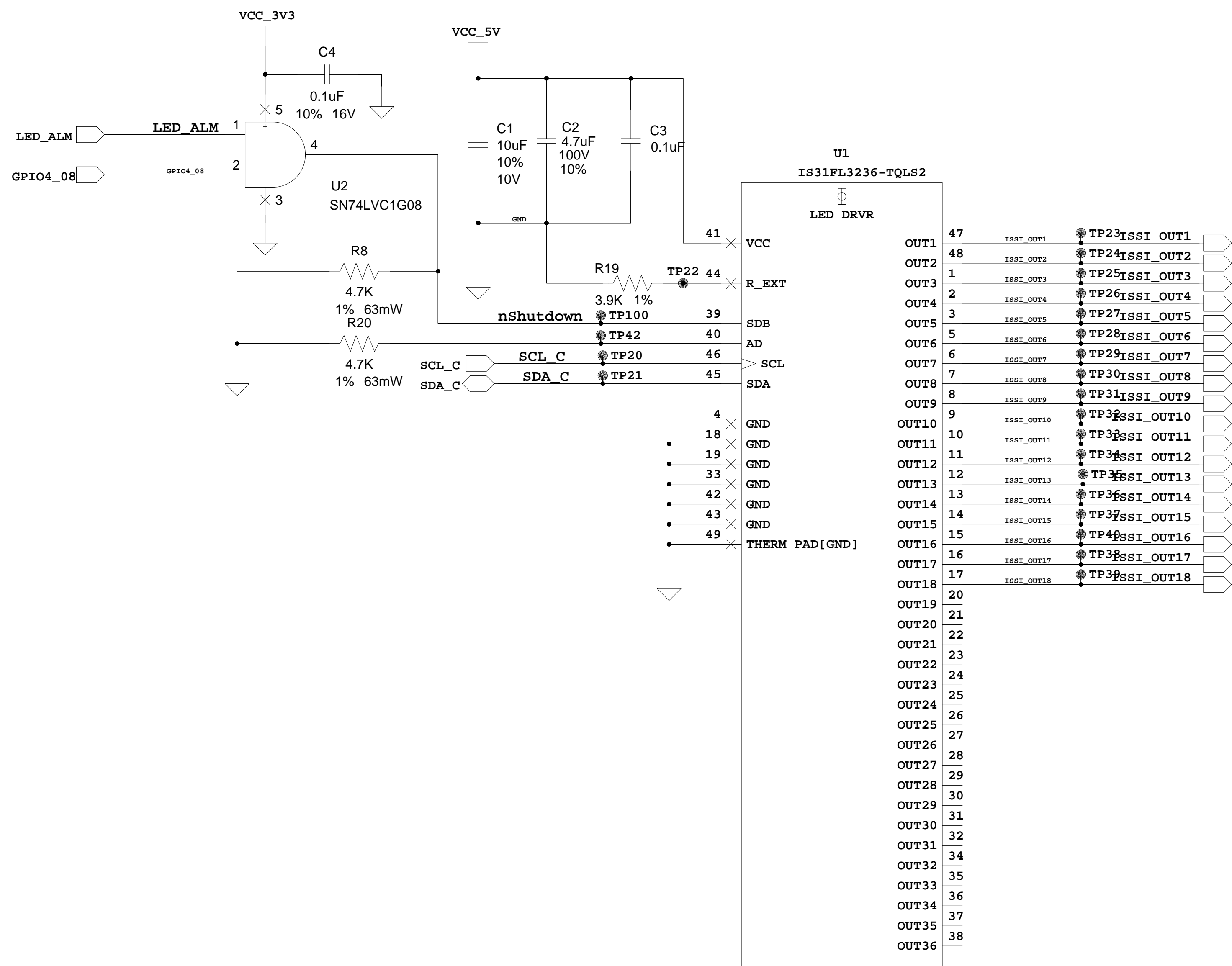


E&ES COMMON CPU BOARD PMIC

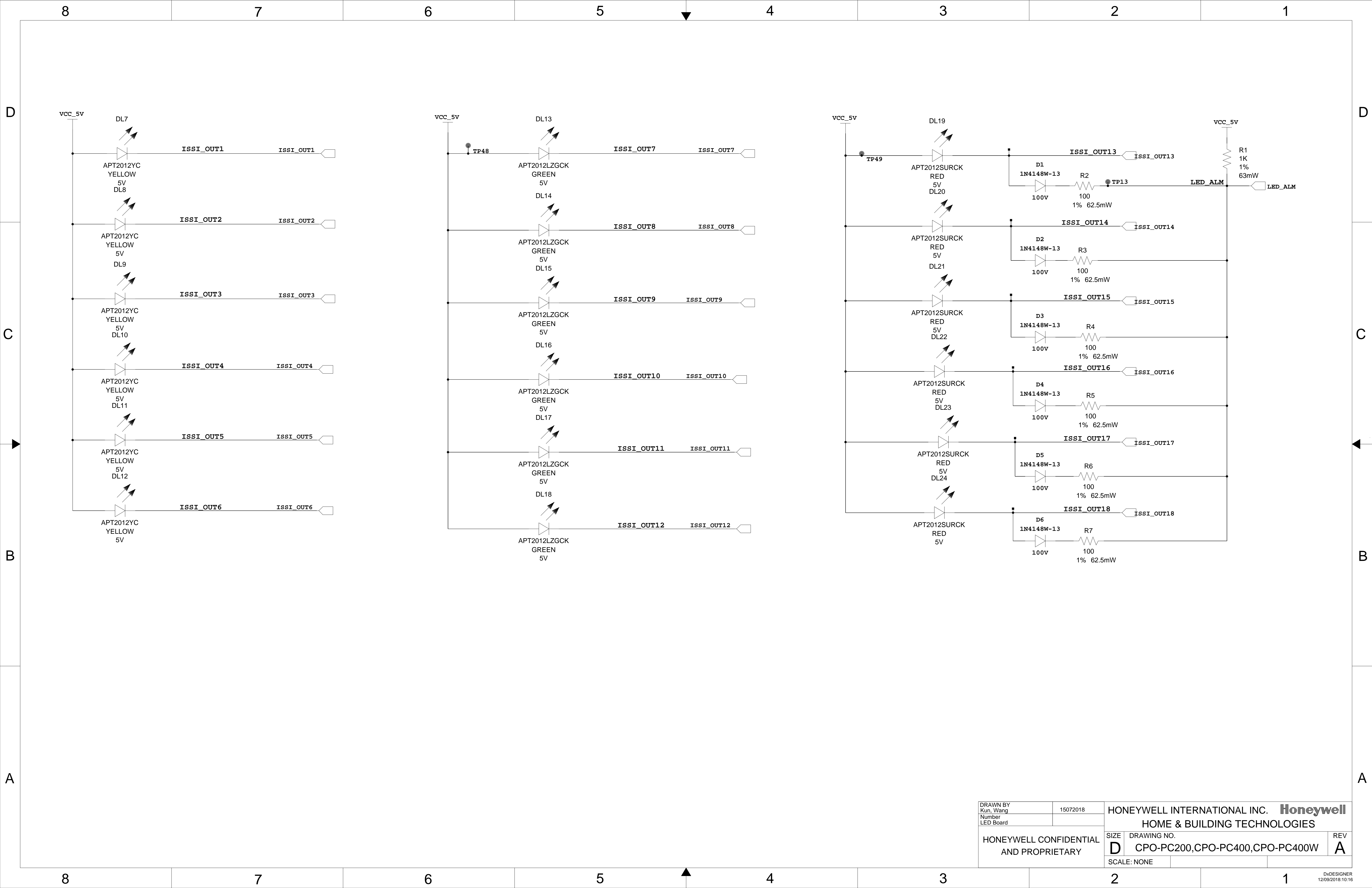
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HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE DRAWING NO. D CPO-PC200,CPO-PC400,CPO-PC400W SCALE: NONE
		REV A



DRAWN BY Kun, Wang	15072018	HONEYWELL INTERNATIONAL INC. Honeywell	
Number LED Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A



DRAWN BY Kun Wang	15072018	HONEYWELL INTERNATIONAL INC. Honeywell	
Number LED Board		HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	REV A
		DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W	
		SCALE: NONE	



DRAWN BY Kun, Wang	15072018	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES	
Number LED Board		SIZE D	REV A
HONEYWELL CONFIDENTIAL AND PROPRIETARY		DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W	
		SCALE: NONE	

8

7

6

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D

D

C

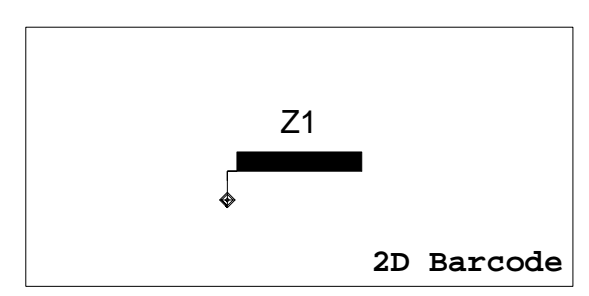
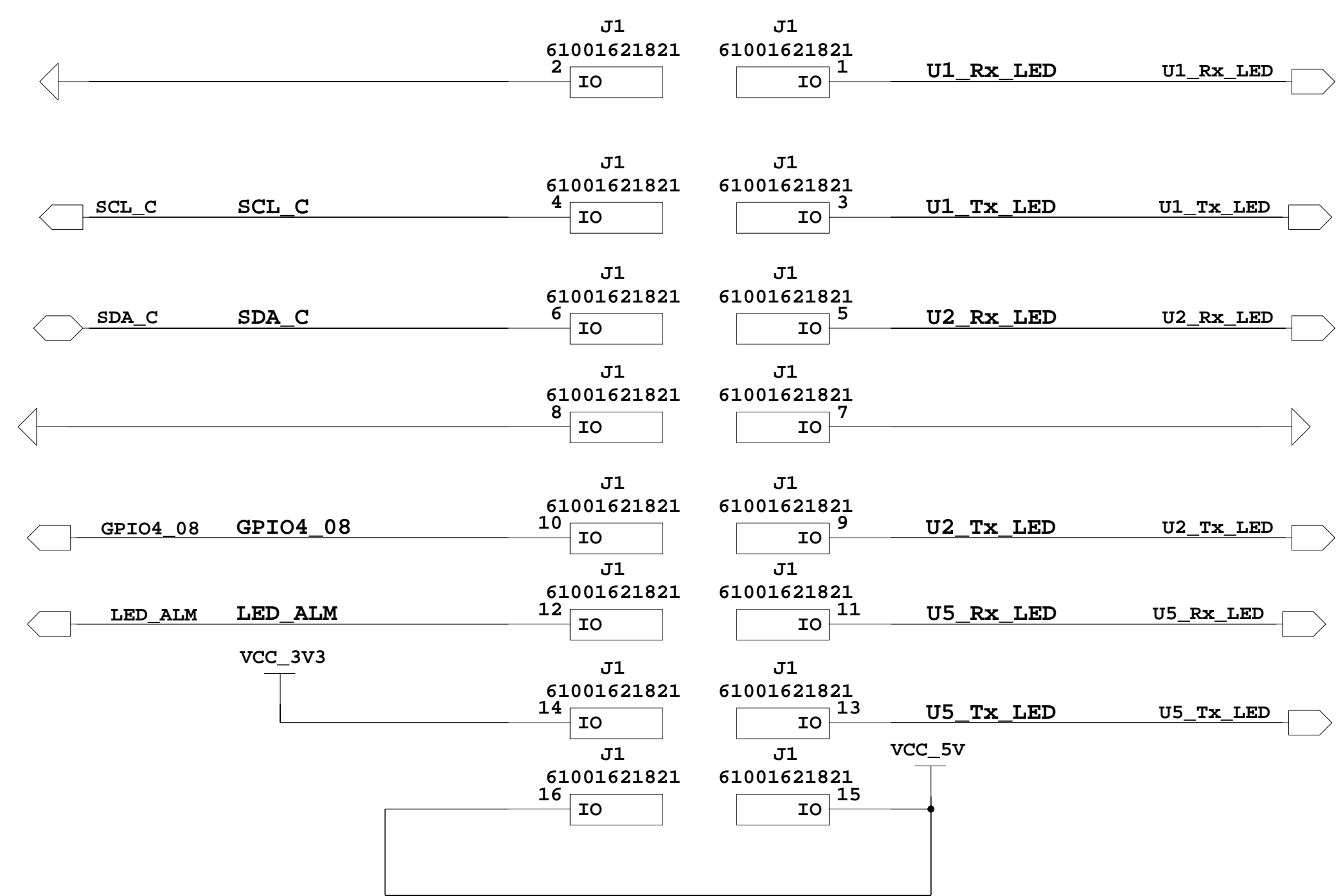
C

B

B

A

A



DRAWN BY Kun, Wang Number LED Board	15072018	HONEYWELL INTERNATIONAL INC. Honeywell HOME & BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. CPO-PC200,CPO-PC400,CPO-PC400W
		SCALE: NONE	REV A

8

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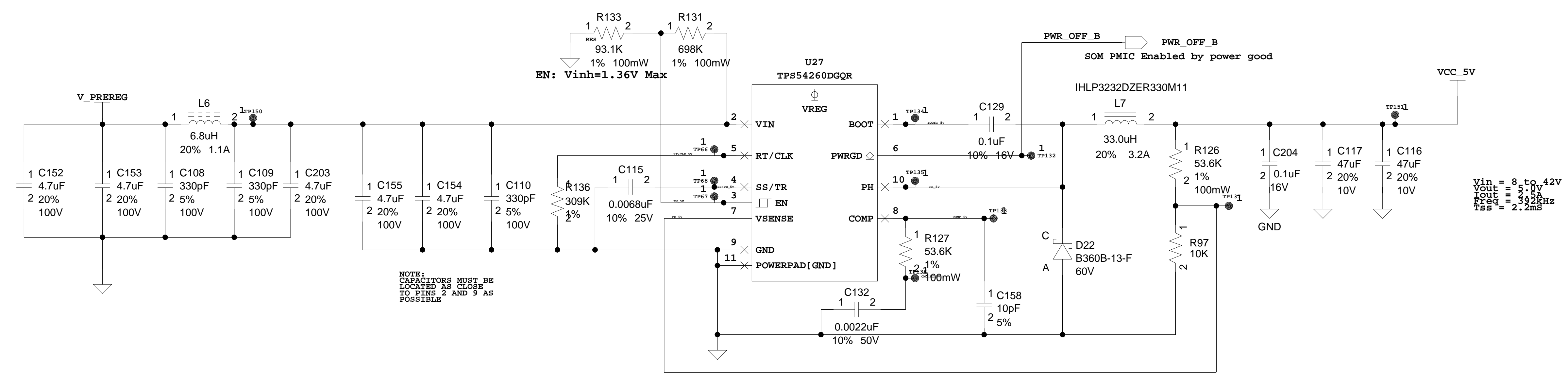
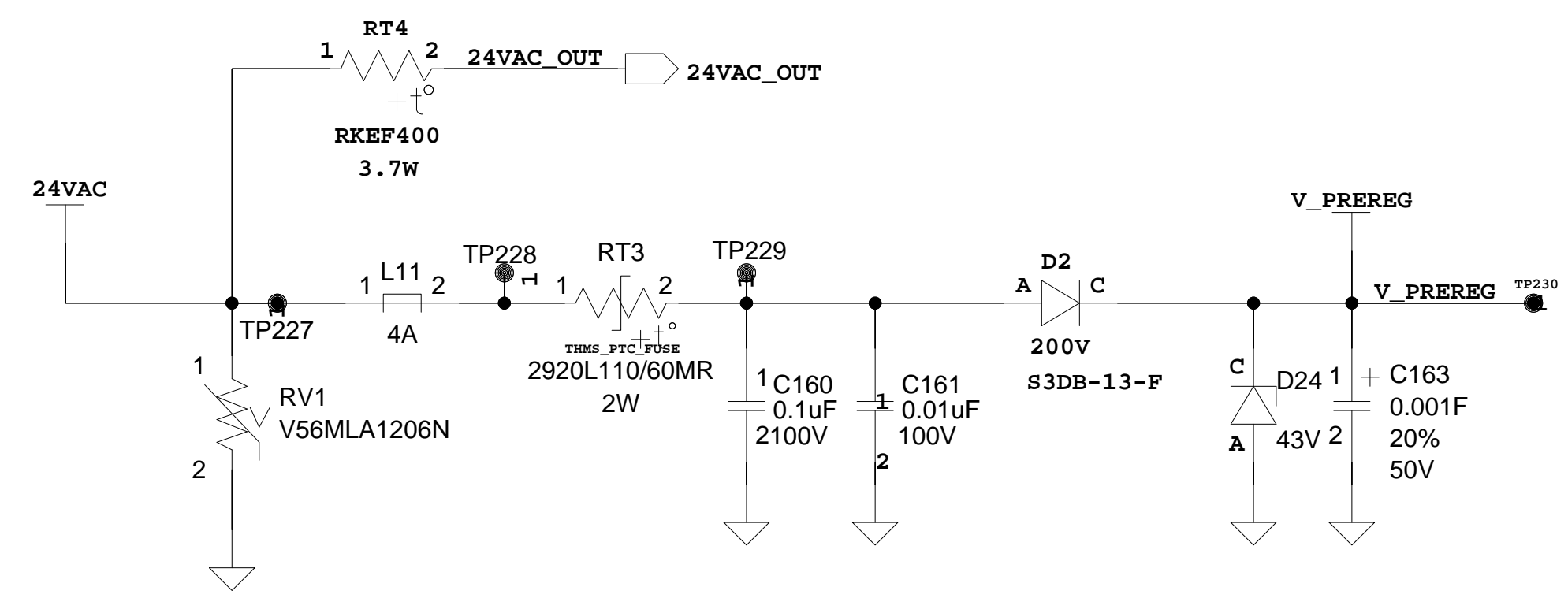
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D\DESIGNER
12/09/2018:10:15

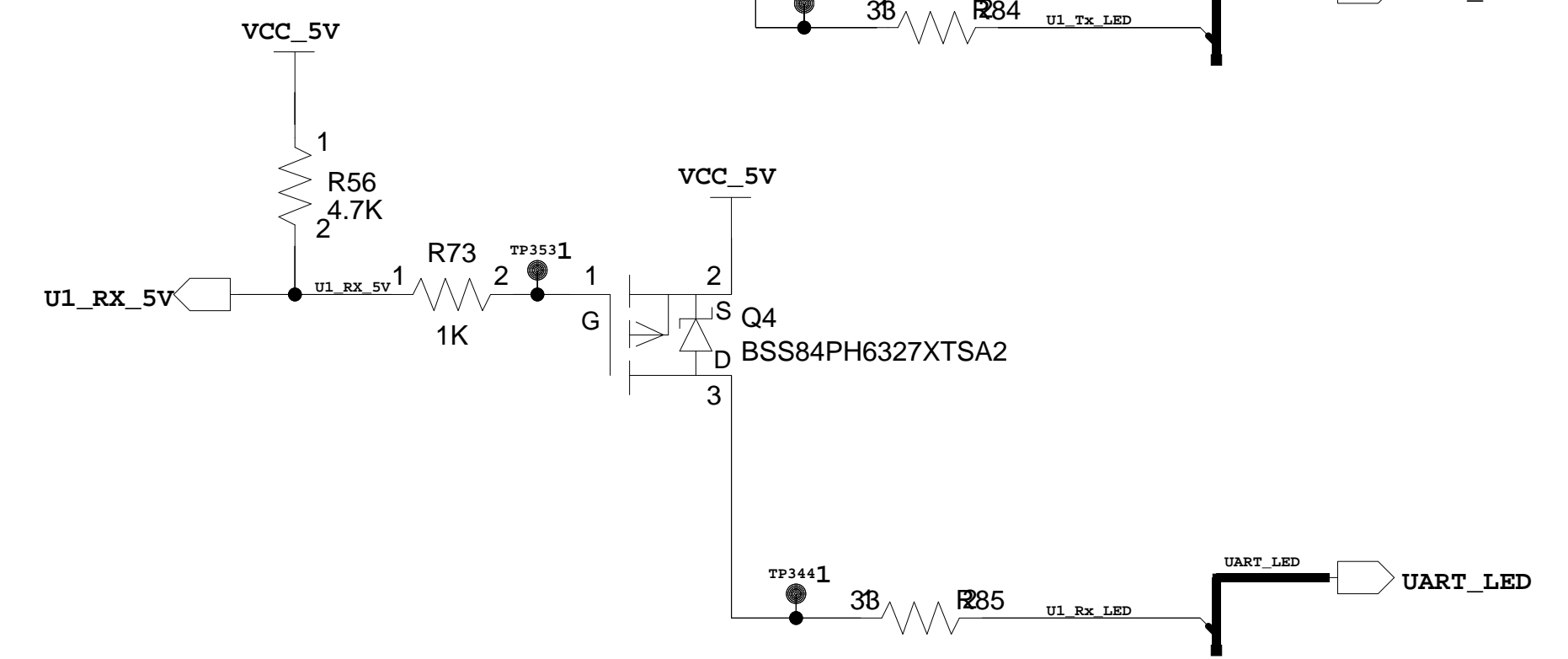
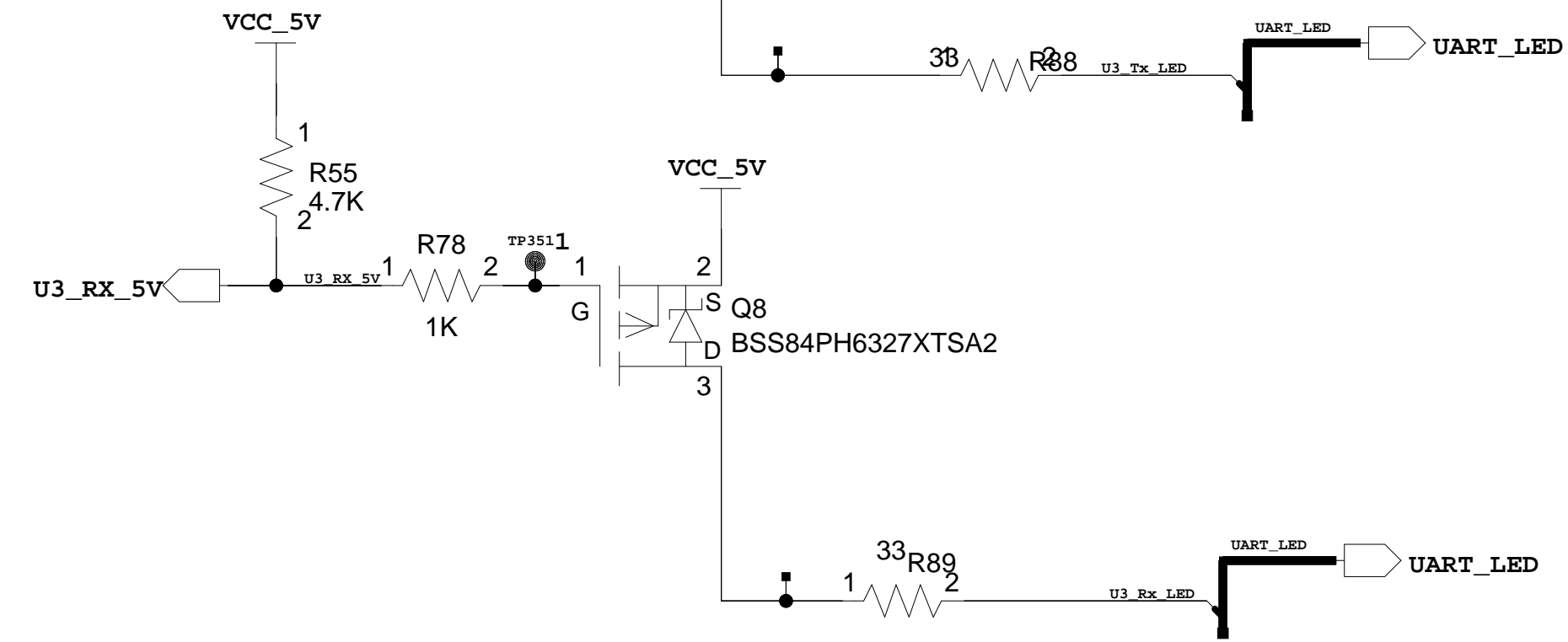
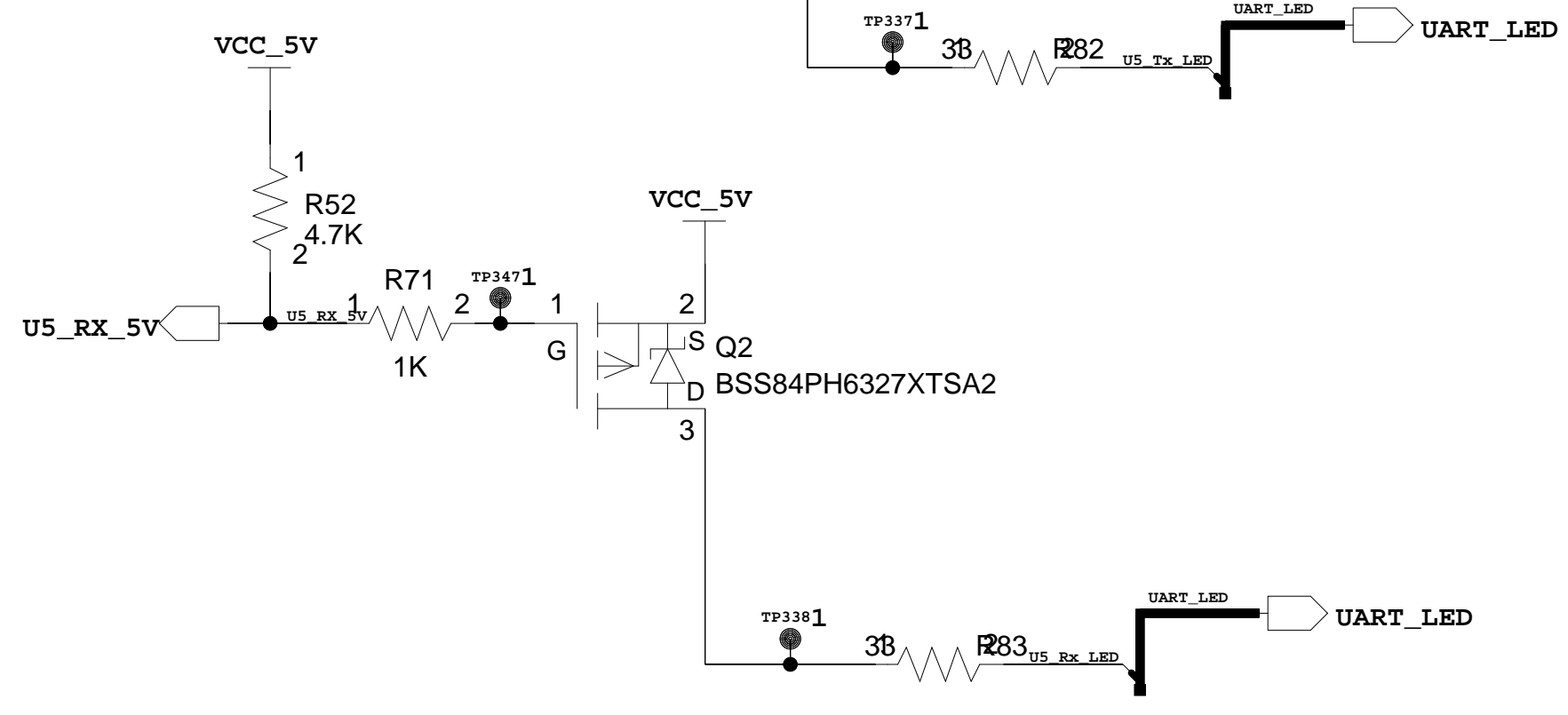
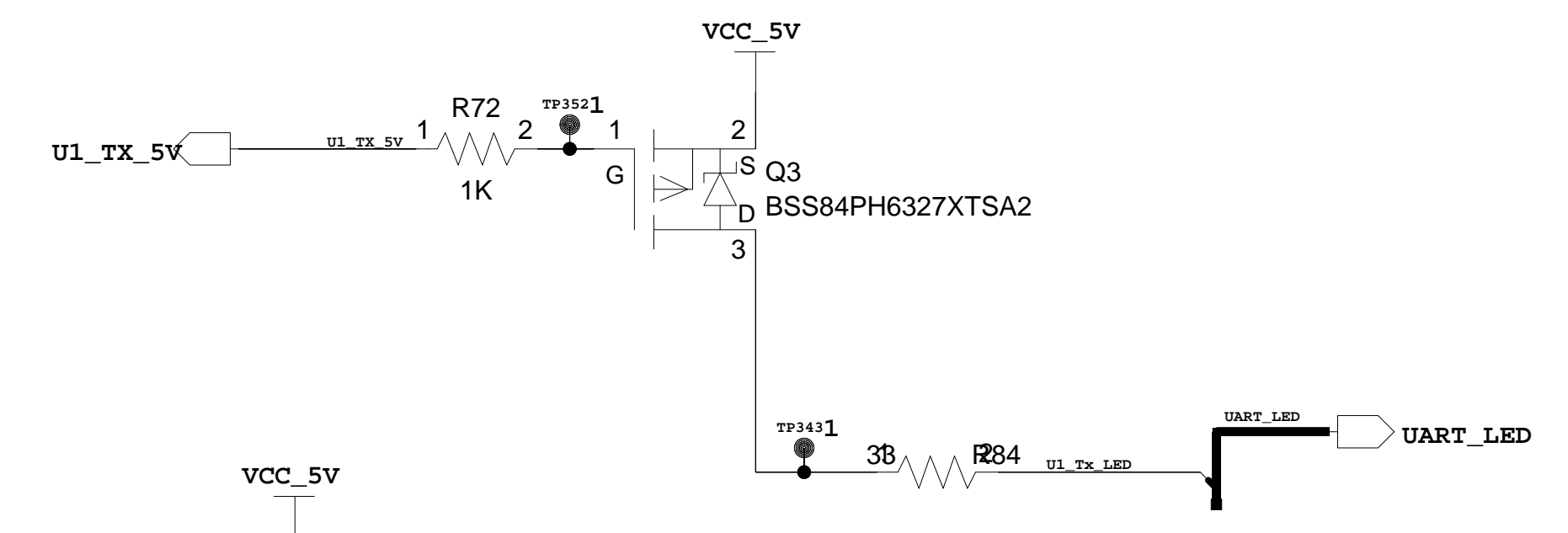
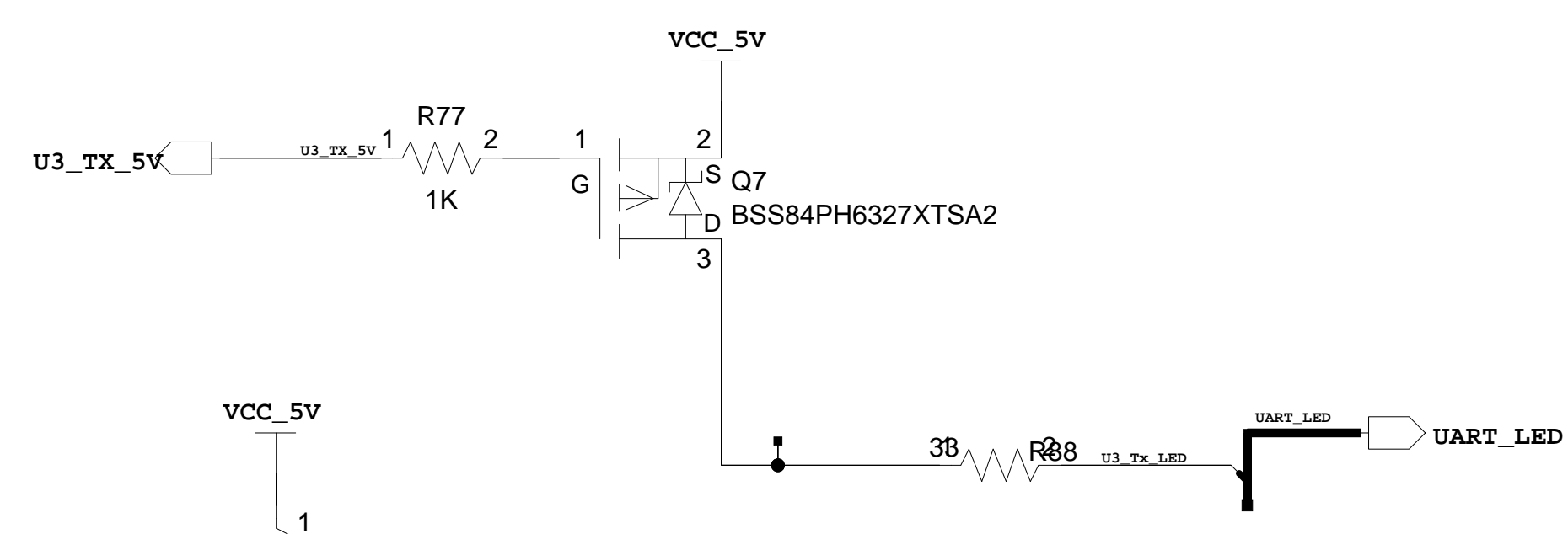
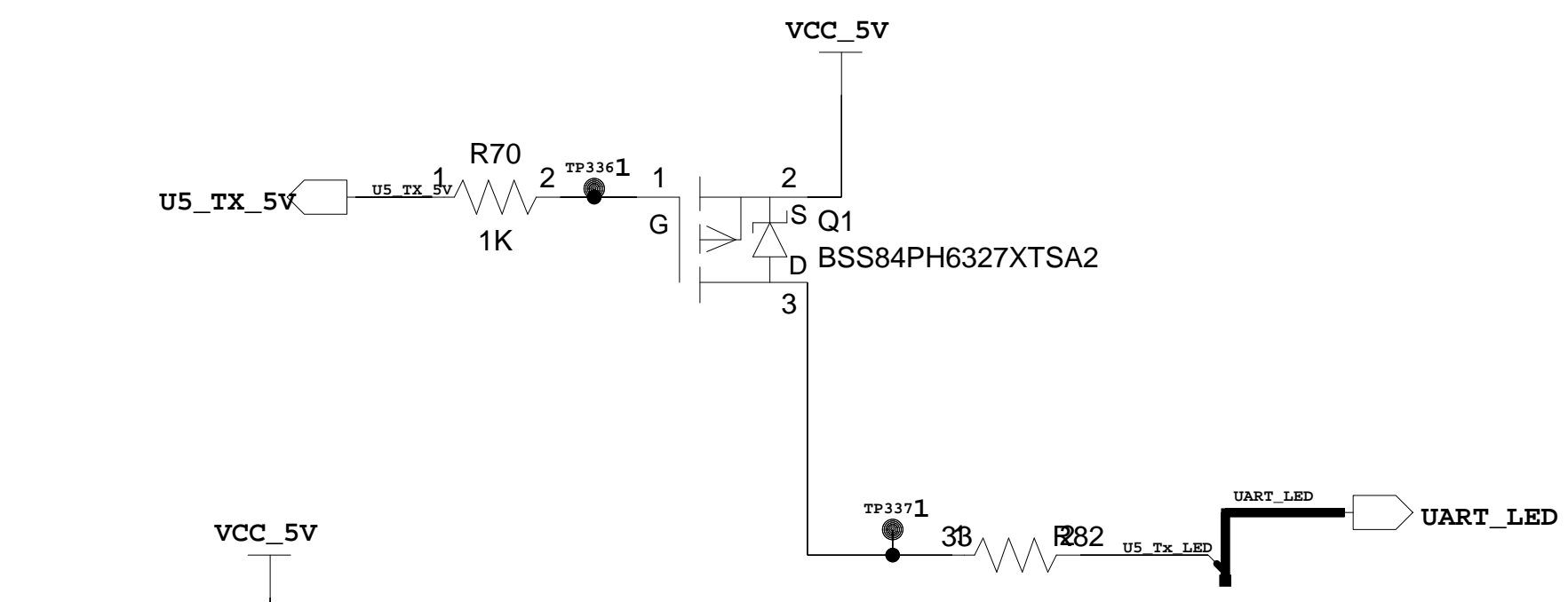


DRAWN BY Tony.Gao	30JUL2020	HONEYWELL INTERNATIONAL INC. Honeywell	
DESIGNER Tony.Gao	30JUL2020	HONEYWELL BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. 32350760
		SCALE:NONE	REV A

8 7 6 5 4 3 2 1

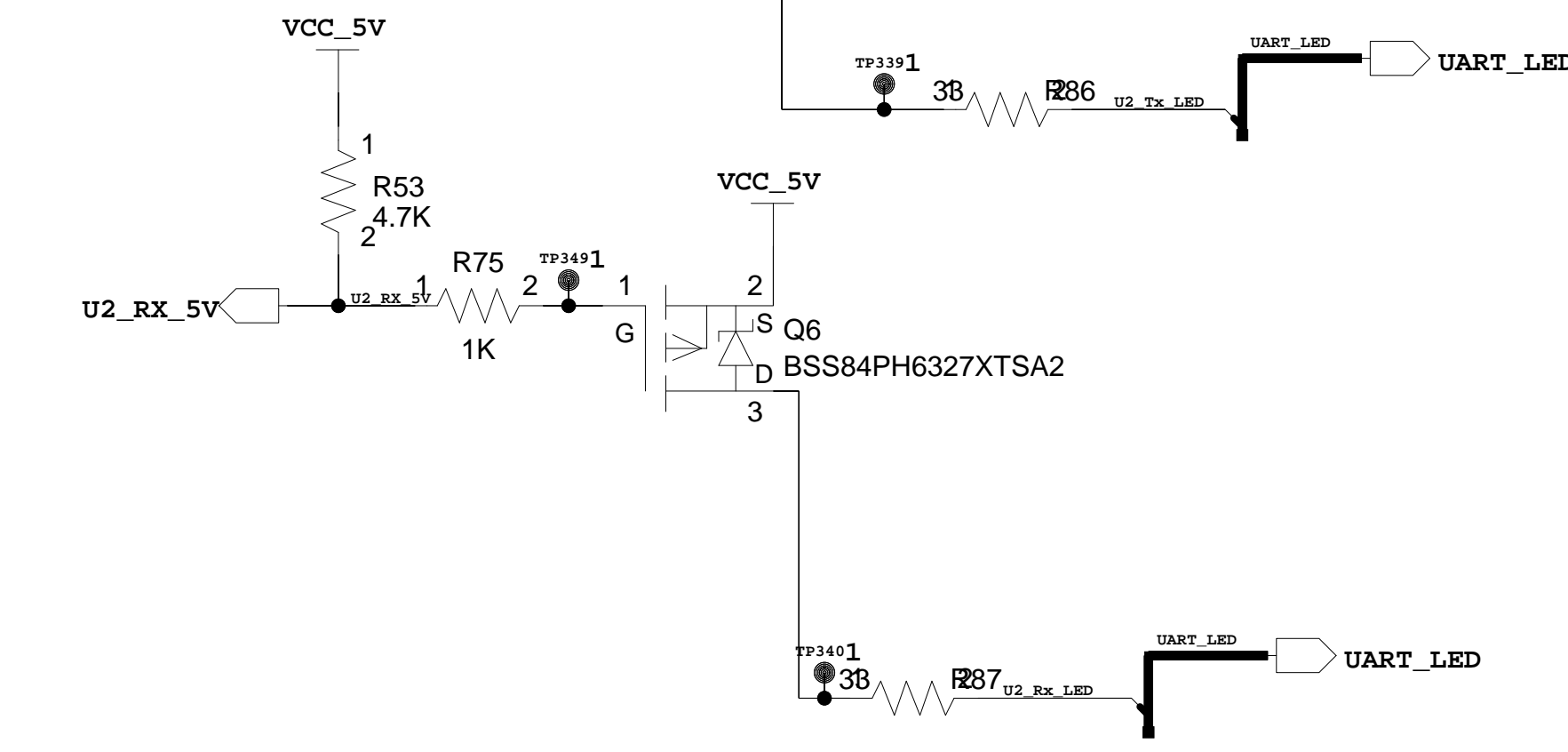
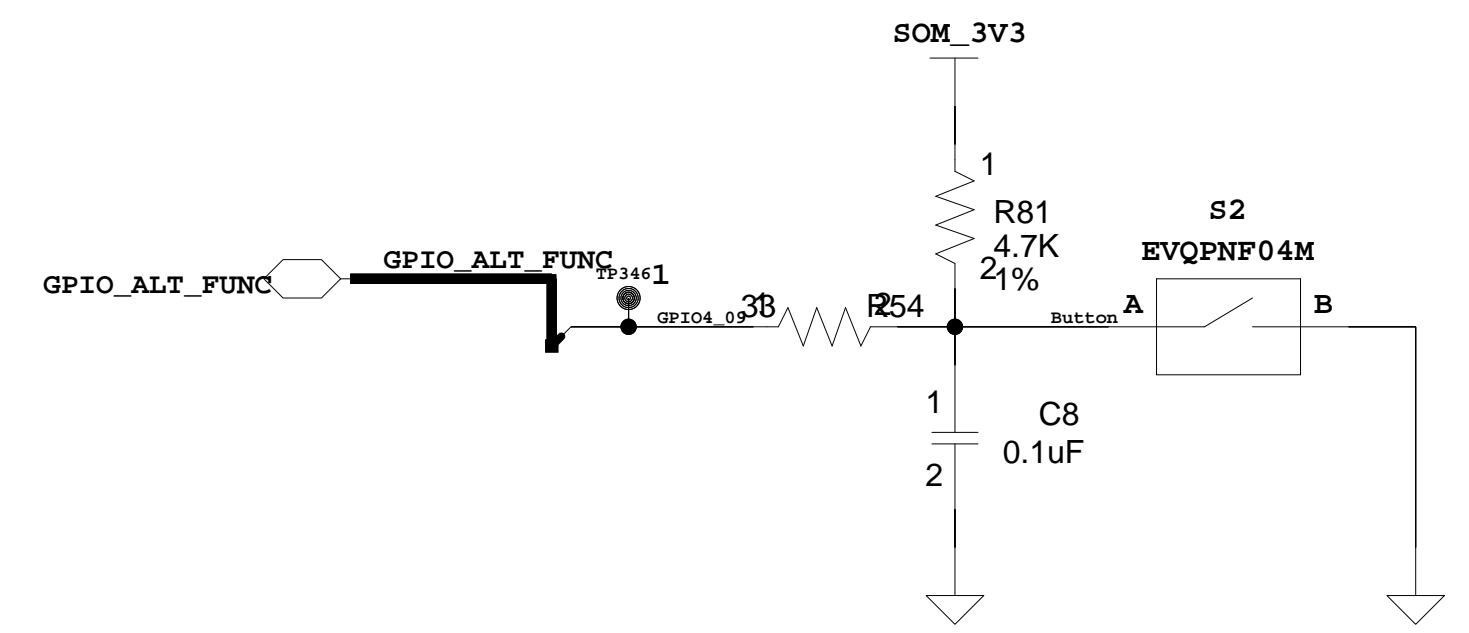
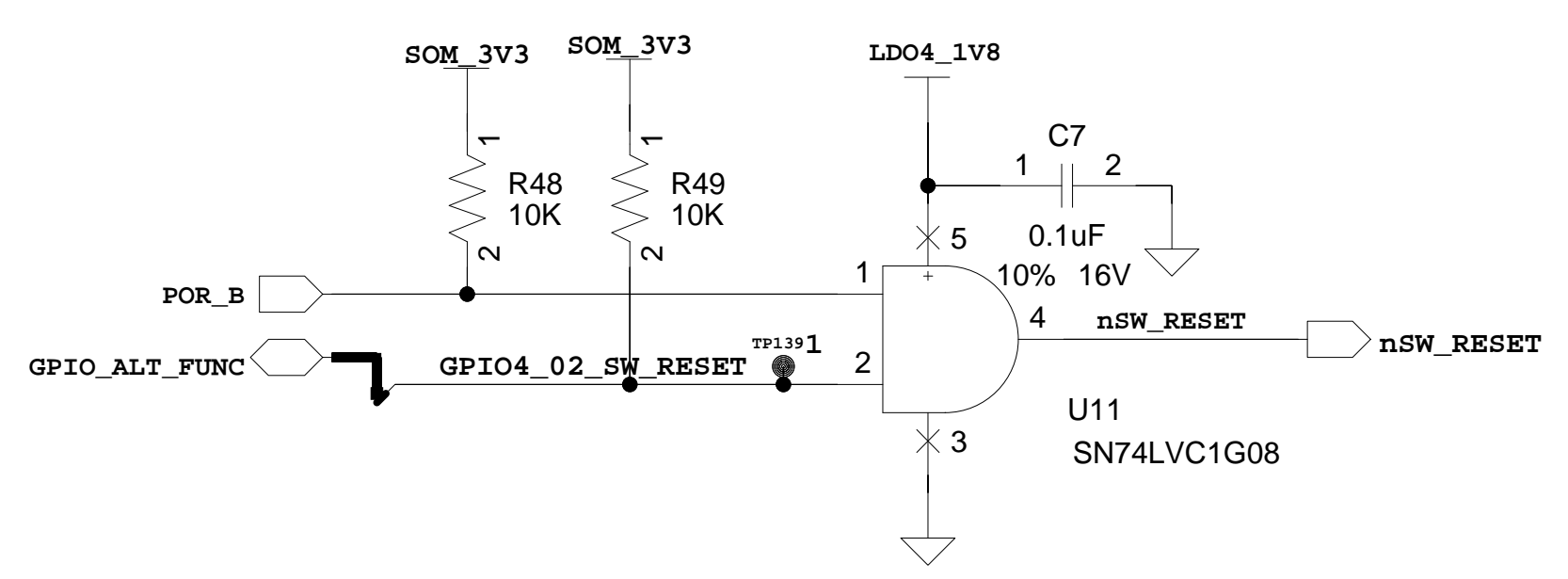
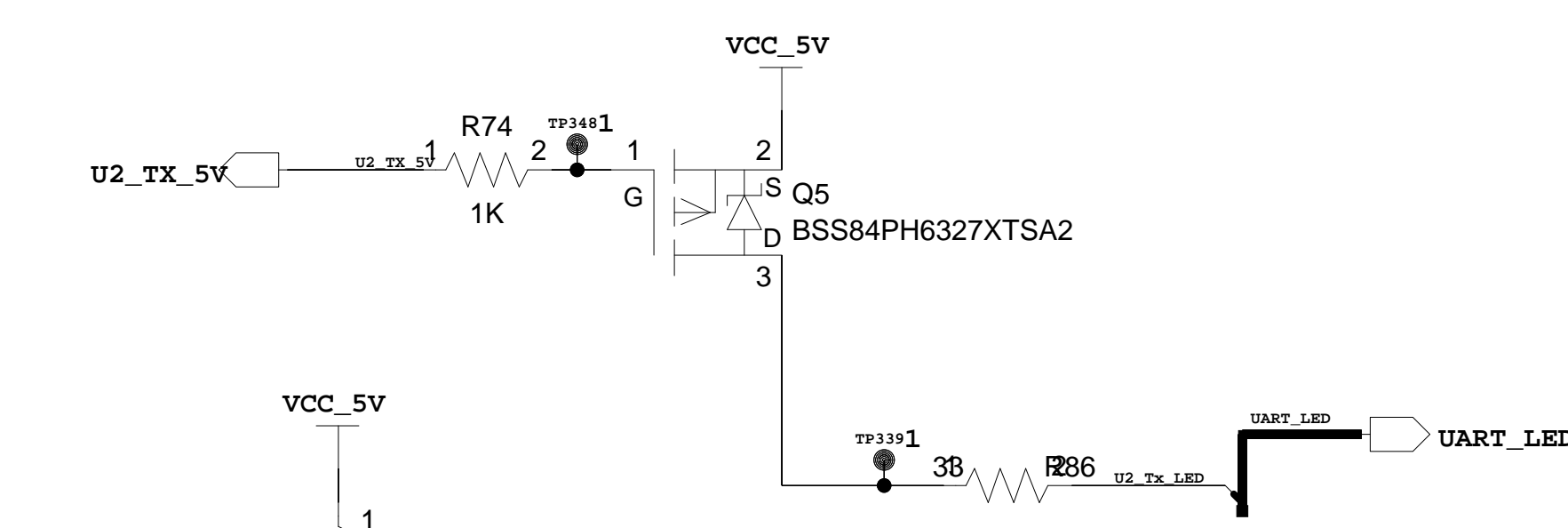
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D



C

C



B

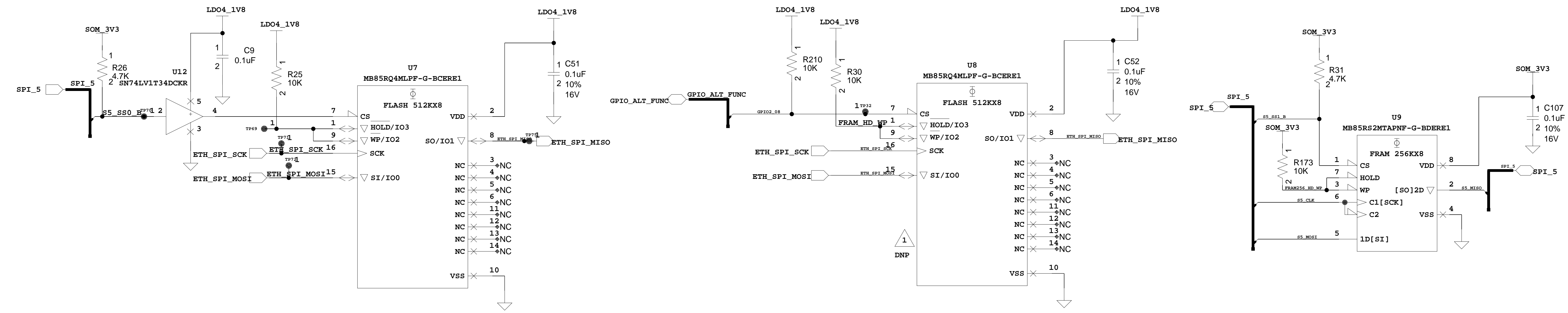
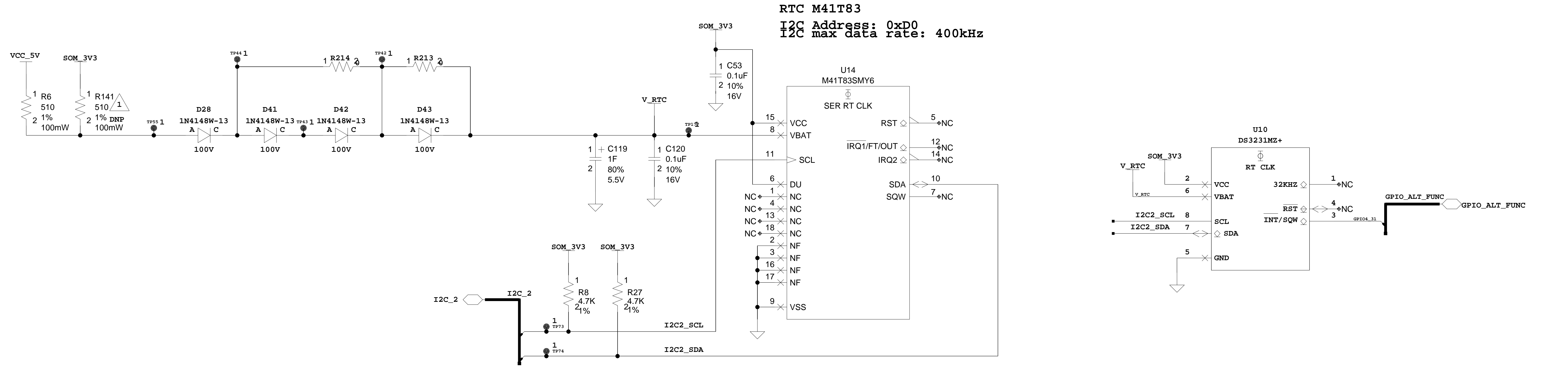
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A

A

8 7 6 5 4 3 2 1

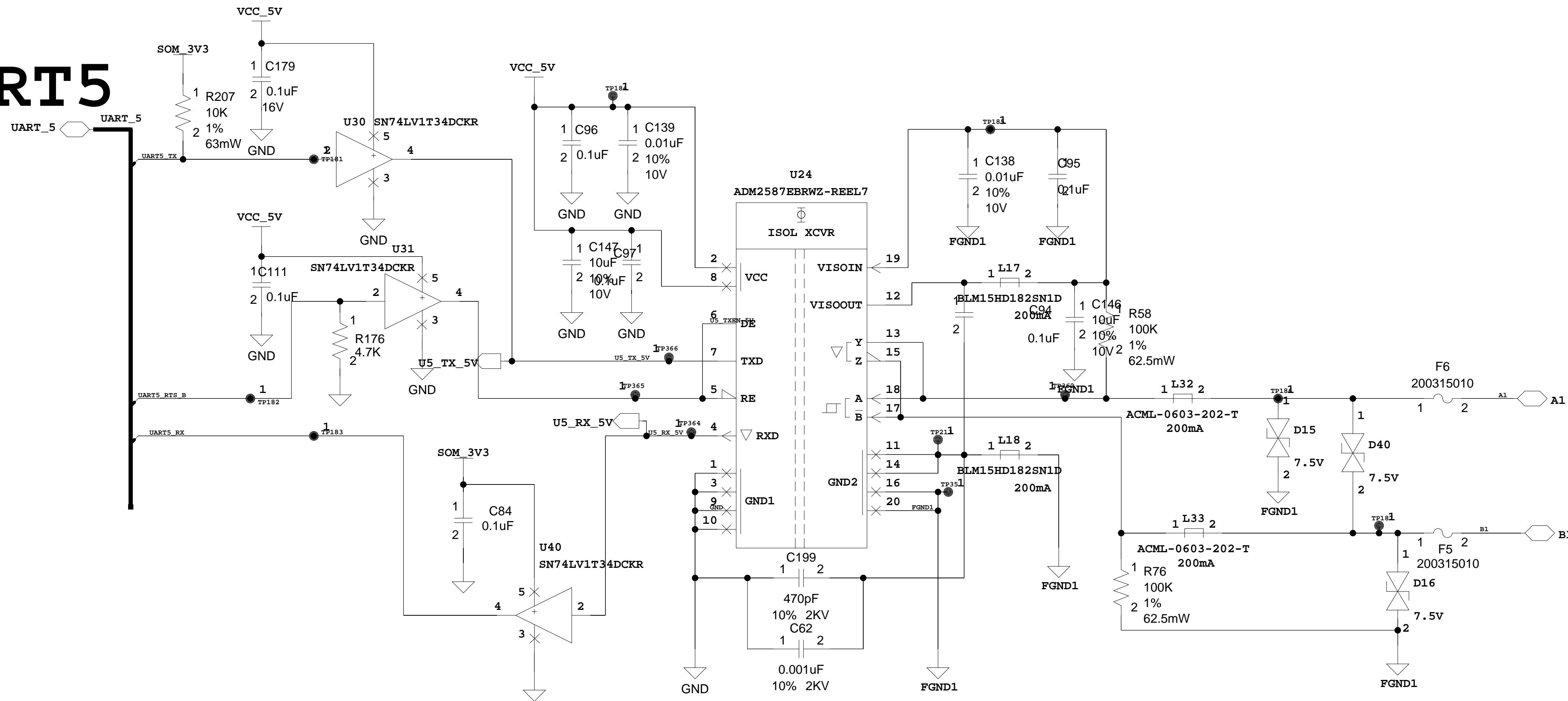
DRAWN BY Tony.Gao	30JUL2020	HONEYWELL INTERNATIONAL INC. Honeywell	
DESIGNER Tony.Gao	30JUL2020	HONEYWELL BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. 32350760
		SCALE: NONE	REV A



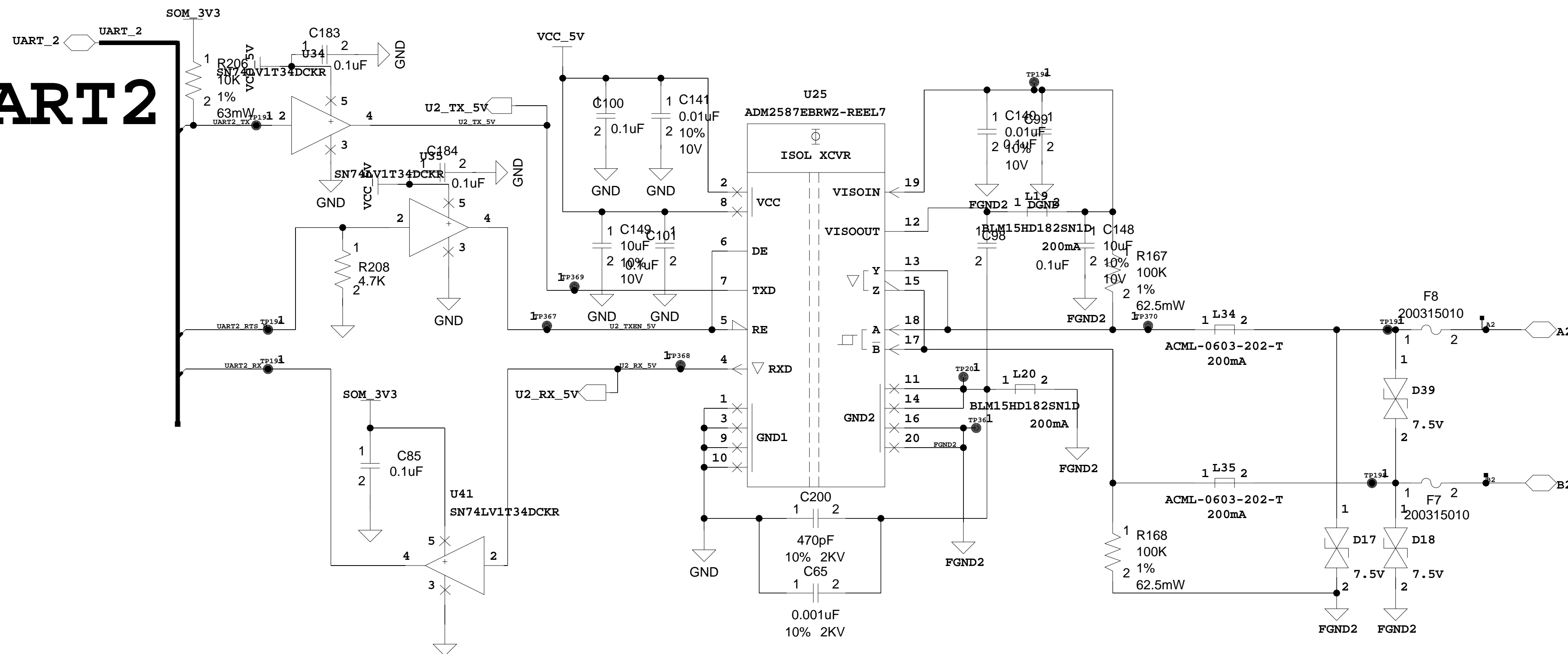
FRAM
 SPI Bus: SPI_5
 U7:SPI Chip Select: SPI5_SS0
 U8 and U9:SPI Chip select: SPI5_SS1

DRAWN BY Tony.Gao	30JUL2020	HONEYWELL INTERNATIONAL INC. Honeywell	
DESIGNER Tony.Gao	30JUL2020	HONEYWELL BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. 32350760
		SCALE: NONE	REV A

UART5

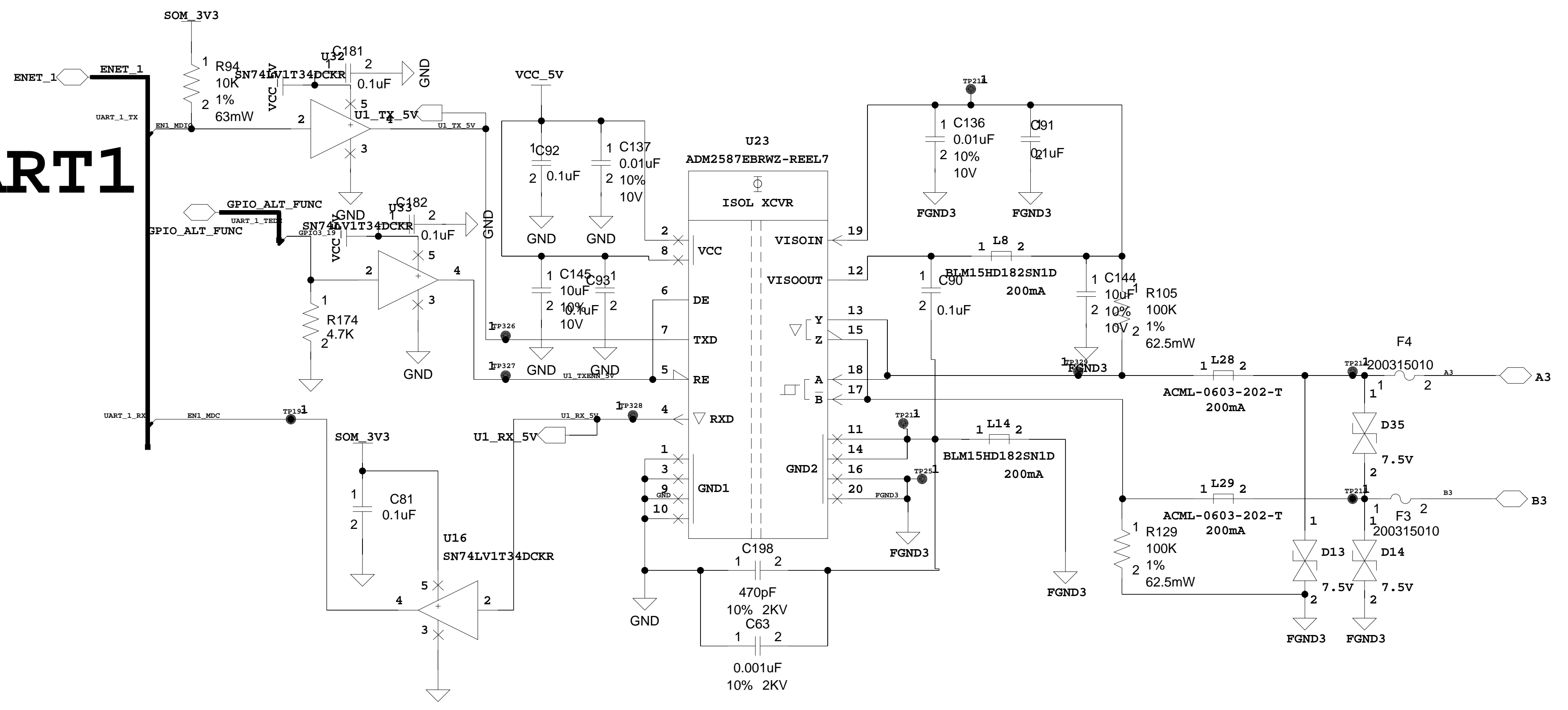


UART2

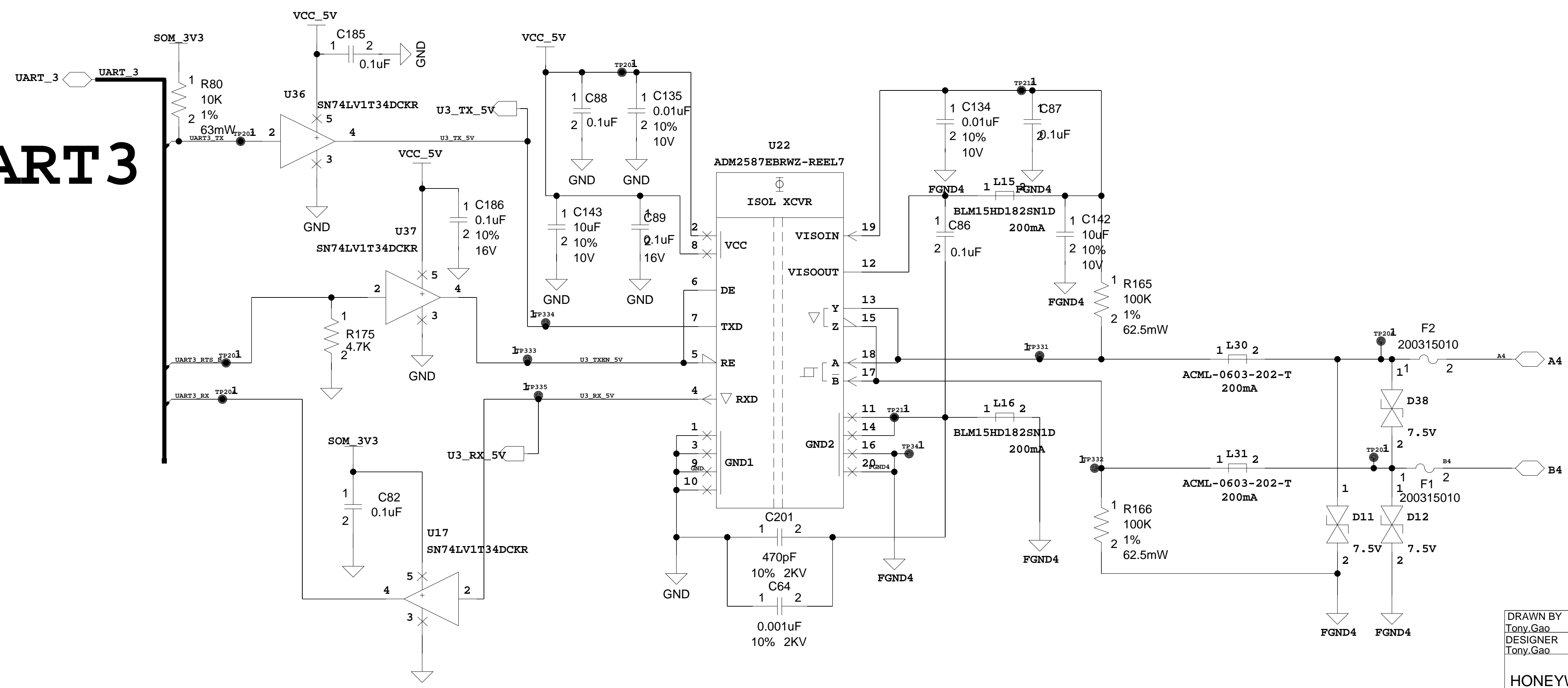


DRAWN BY Tony.Gao	30JUL2020	HONEYWELL INTERNATIONAL INC. Honeywell	
DESIGNER Tony.Gao	30JUL2020	HONEYWELL BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. 32350760
		SCALE: NONE	REV A

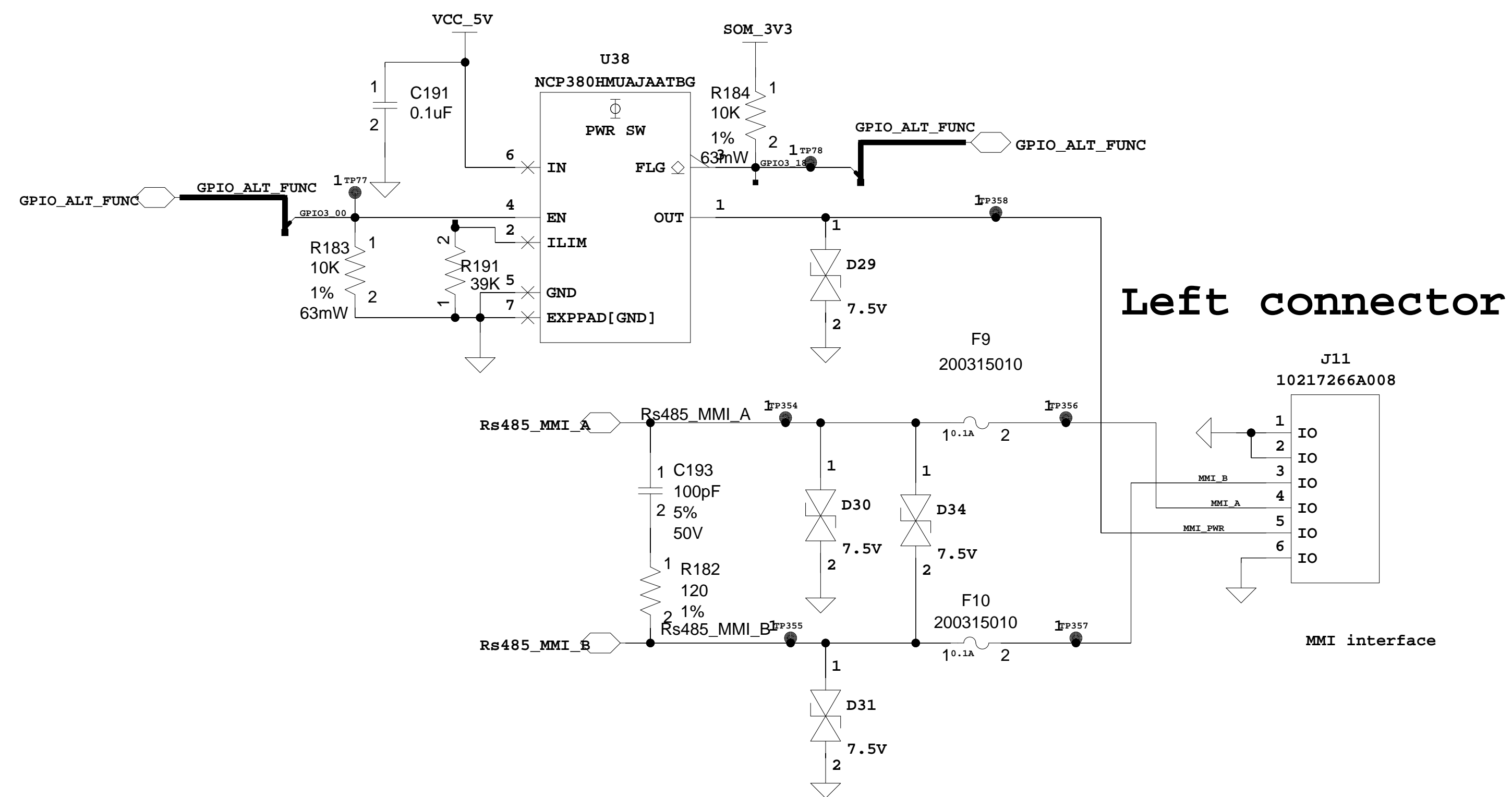
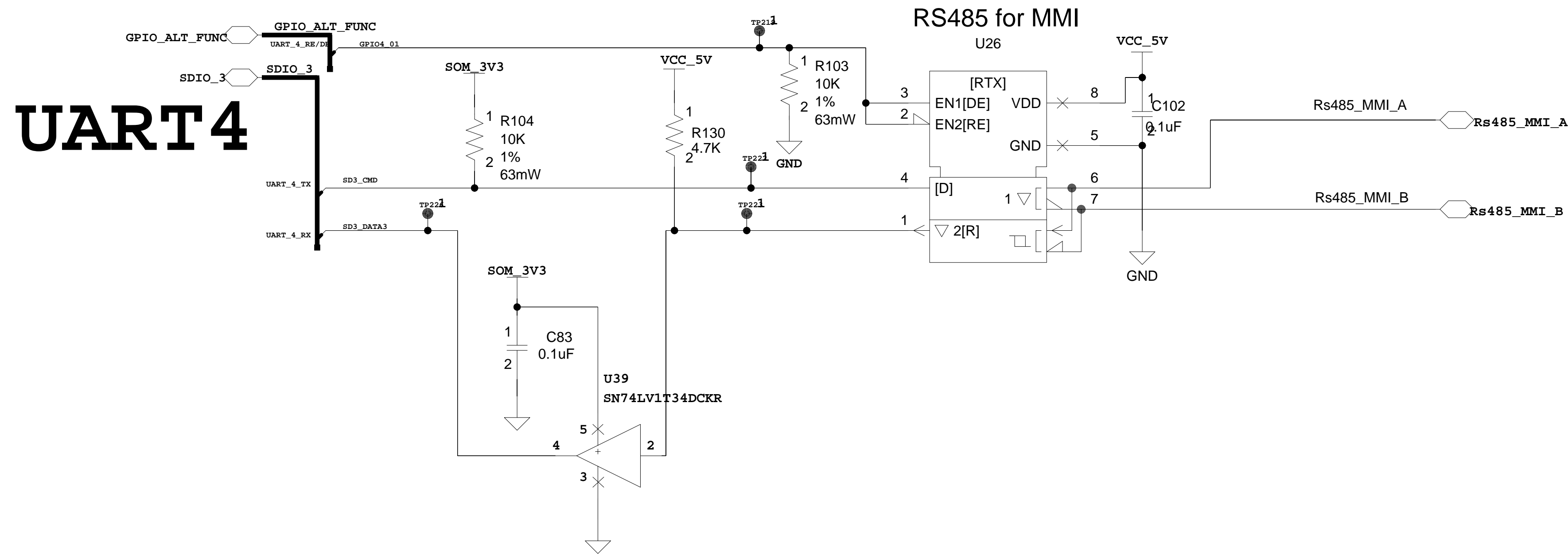
UART1



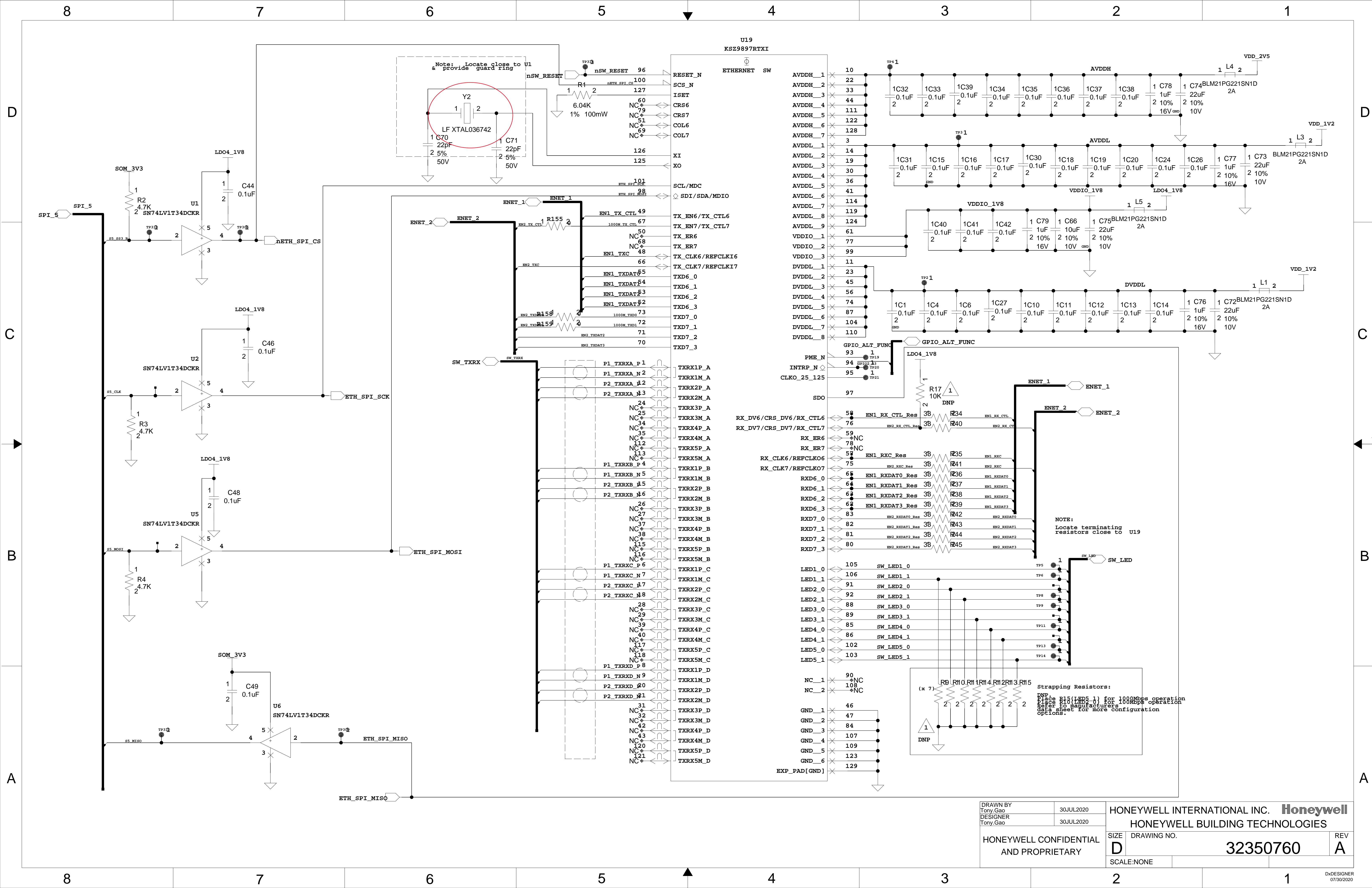
UART3



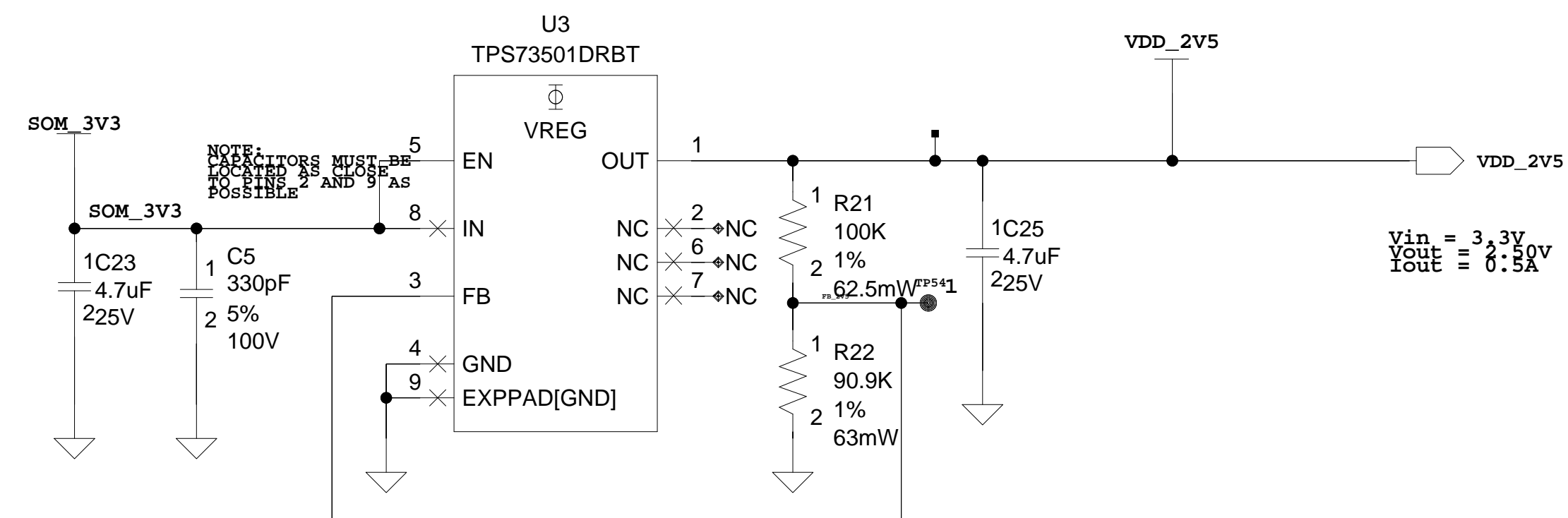
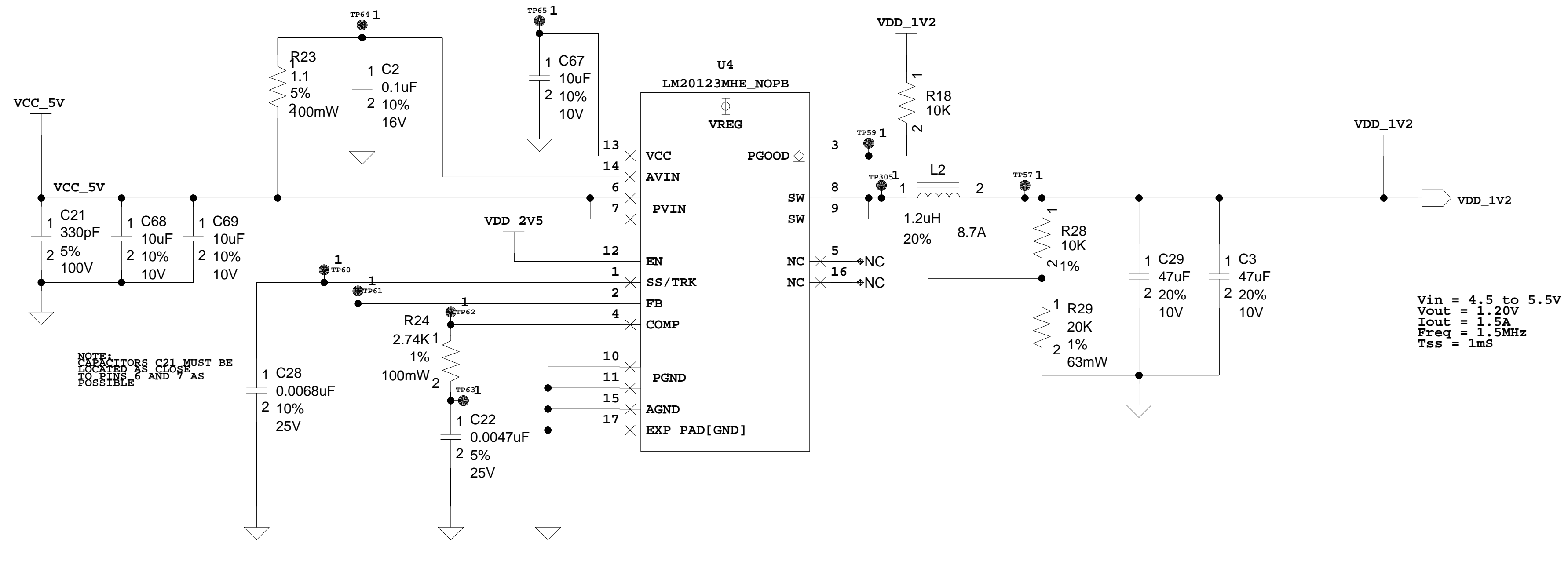
DRAWN BY Tony.Gao	30JUL2020	HONEYWELL INTERNATIONAL INC. Honeywell	
DESIGNER Tony.Gao	30JUL2020	HONEYWELL BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. 32350760
		SCALE:NONE	REV A



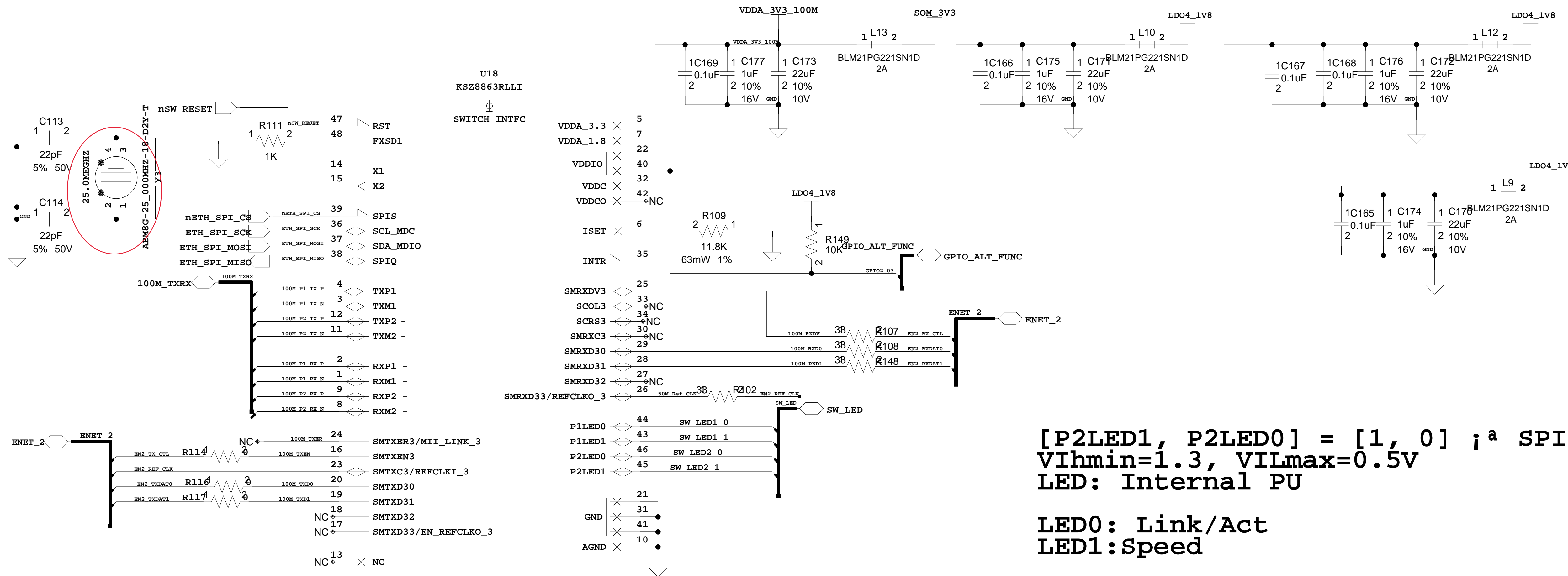
DRAWN BY Tony.Gao	30JUL2020	HONEYWELL INTERNATIONAL INC. Honeywell	
DESIGNER Tony.Gao	30JUL2020	HONEYWELL BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	REV A
SCALE: NONE		DRAWING NO. 32350760	



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DESIGNER Tony.Gao	30JUL2020	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SCALE: NONE
SIZE D		DRAWING NO. 32350760
REV A		

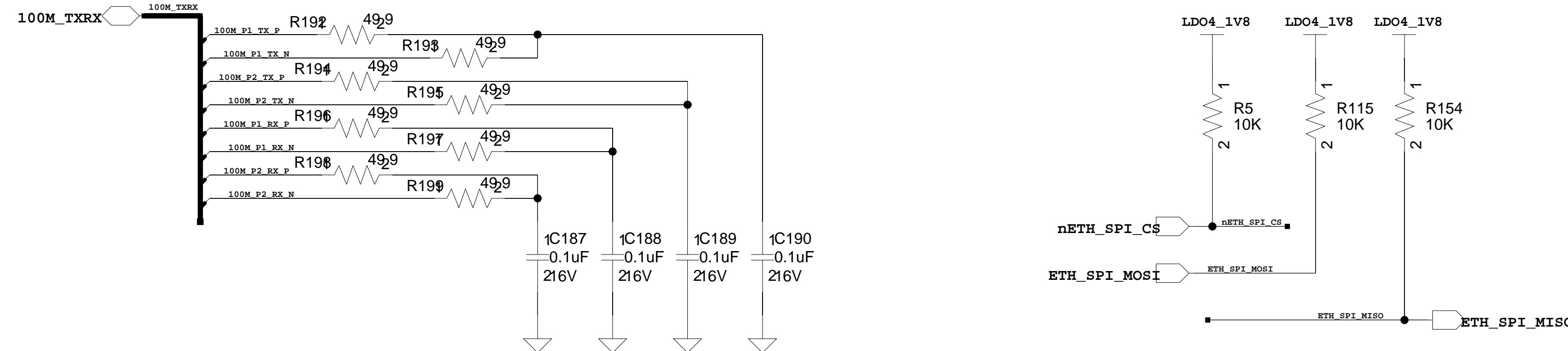


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DESIGNER Tony.Gao	30JUL2020	HONEYWELL BUILDING TECHNOLOGIES	
HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. 32350760
		SCALE: NONE	REV A

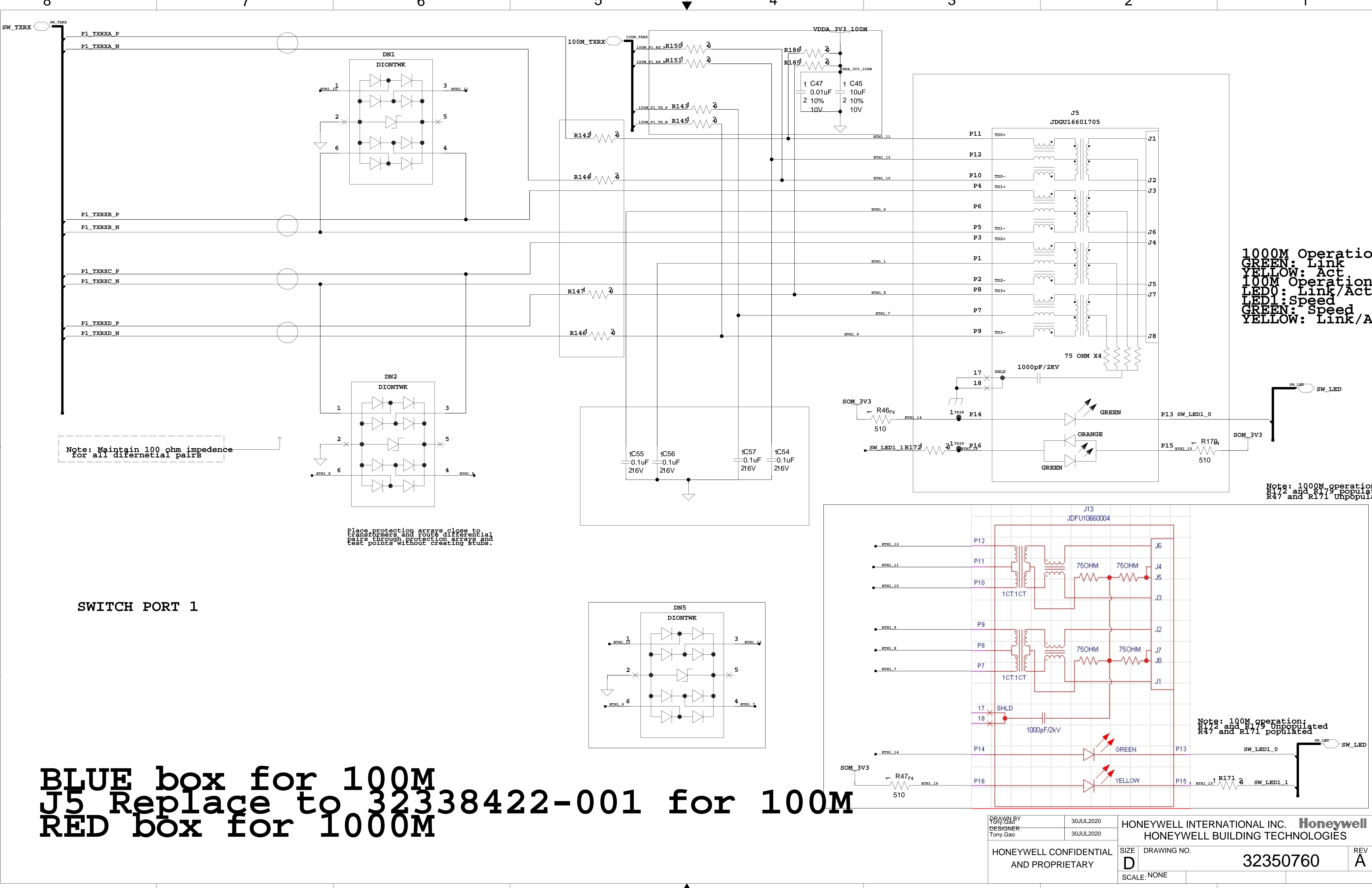


[P2LED1, P2LED0] = [1, 0] ;^a SPI slave mode
 Vihmin=1.3, VILmax=0.5V
 LED: Internal PU

LED0: Link/Act
 LED1: Speed



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Note: Maintain 100 ohm impedance for all differential pairs

Place protection arrays close to transformers and route differential pairs through protection arrays and test points without creating stubs.

1000M Operation:
 GREEN: Link
 YELLOW: Act
 100M Operation:
 LED0: Link/Act
 LED1: speed
 GREEN: speed
 YELLOW: Link/Act

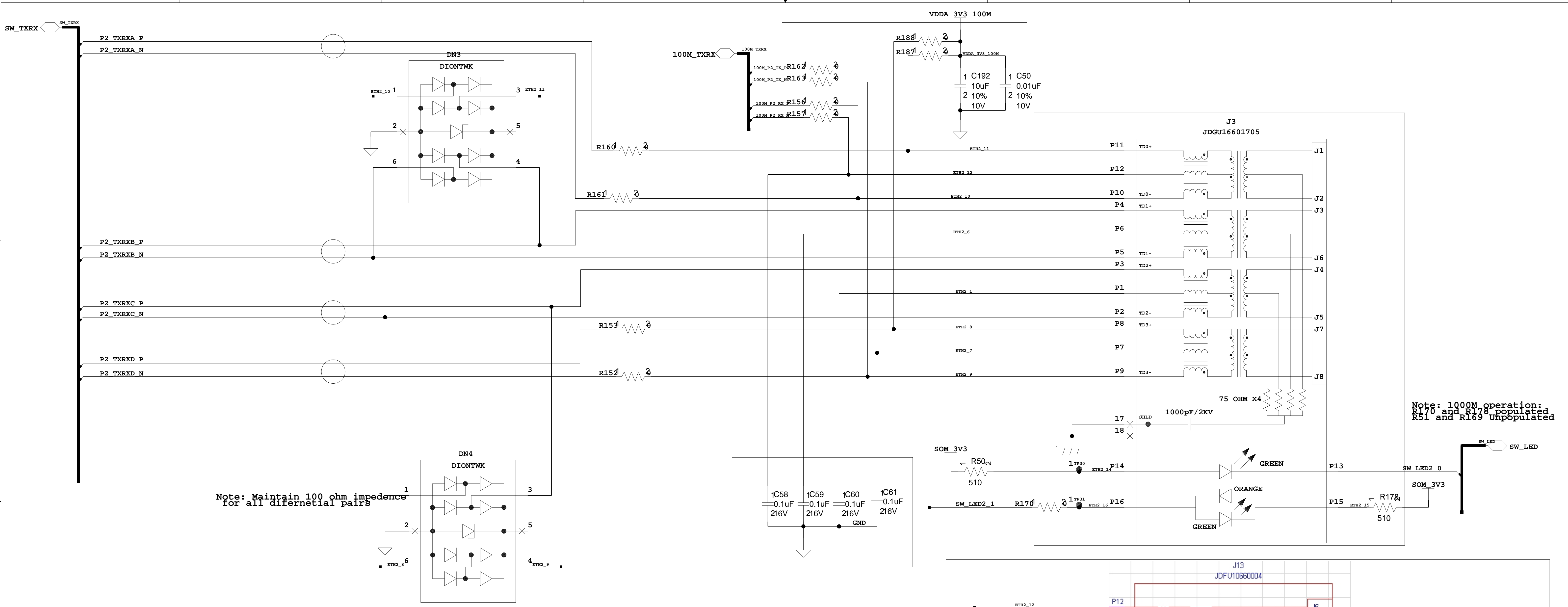
Note: 1000M operation:
 R172 and R179 populated
 R47 and R171 unpopulated

Note: 100M operation:
 R47 and R171 unpopulated
 R172 and R179 populated

BLUE box for 100M
J5 Replace to 32338422-001 for 100M
RED box for 1000M

SWITCH PORT 1

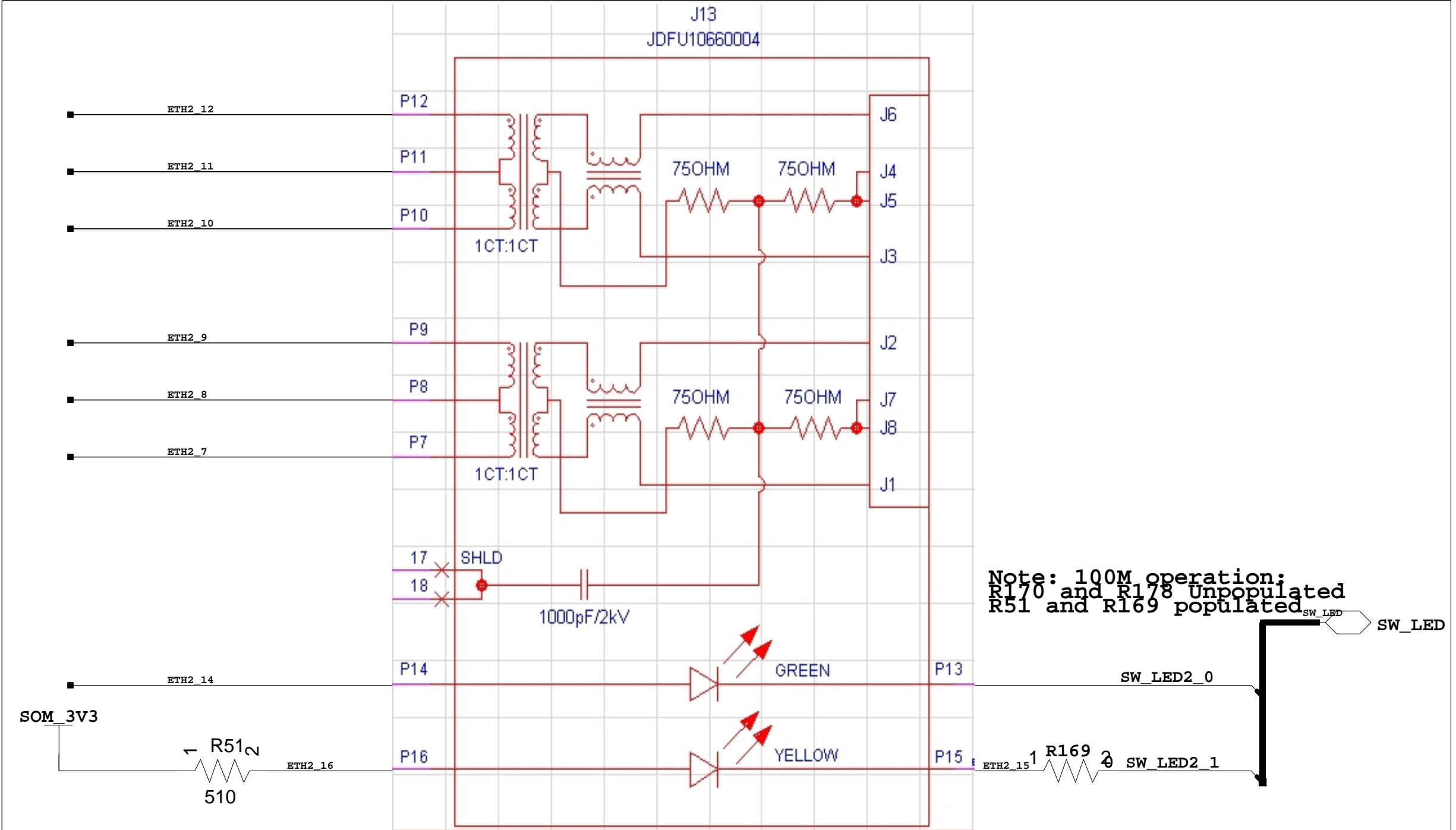
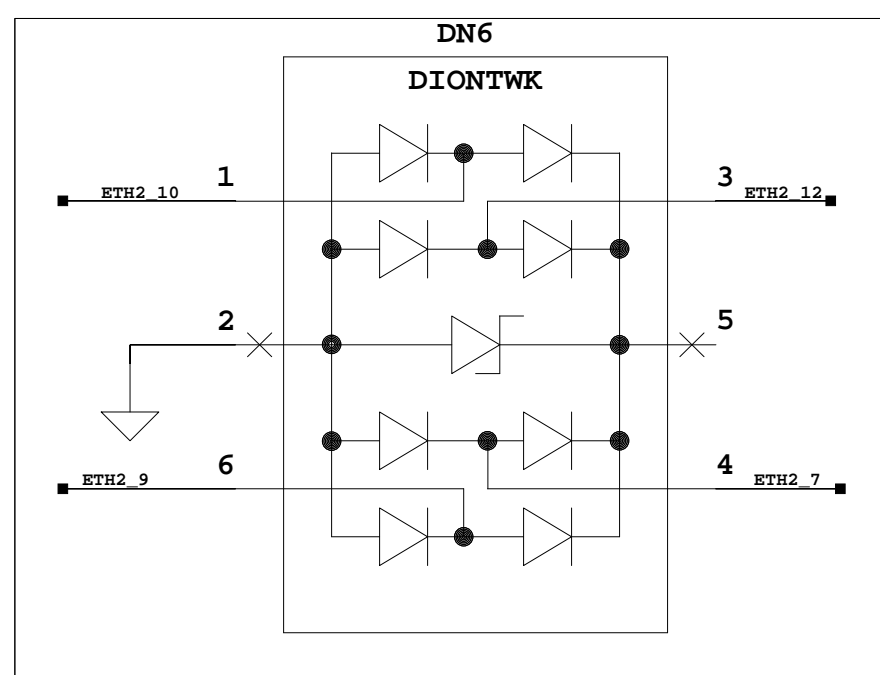
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HONEYWELL CONFIDENTIAL AND PROPRIETARY		SIZE D	DRAWING NO. 32350760
		SCALE: NONE	REV A



Note: Maintain 100 ohm impedance for all difernential pairs

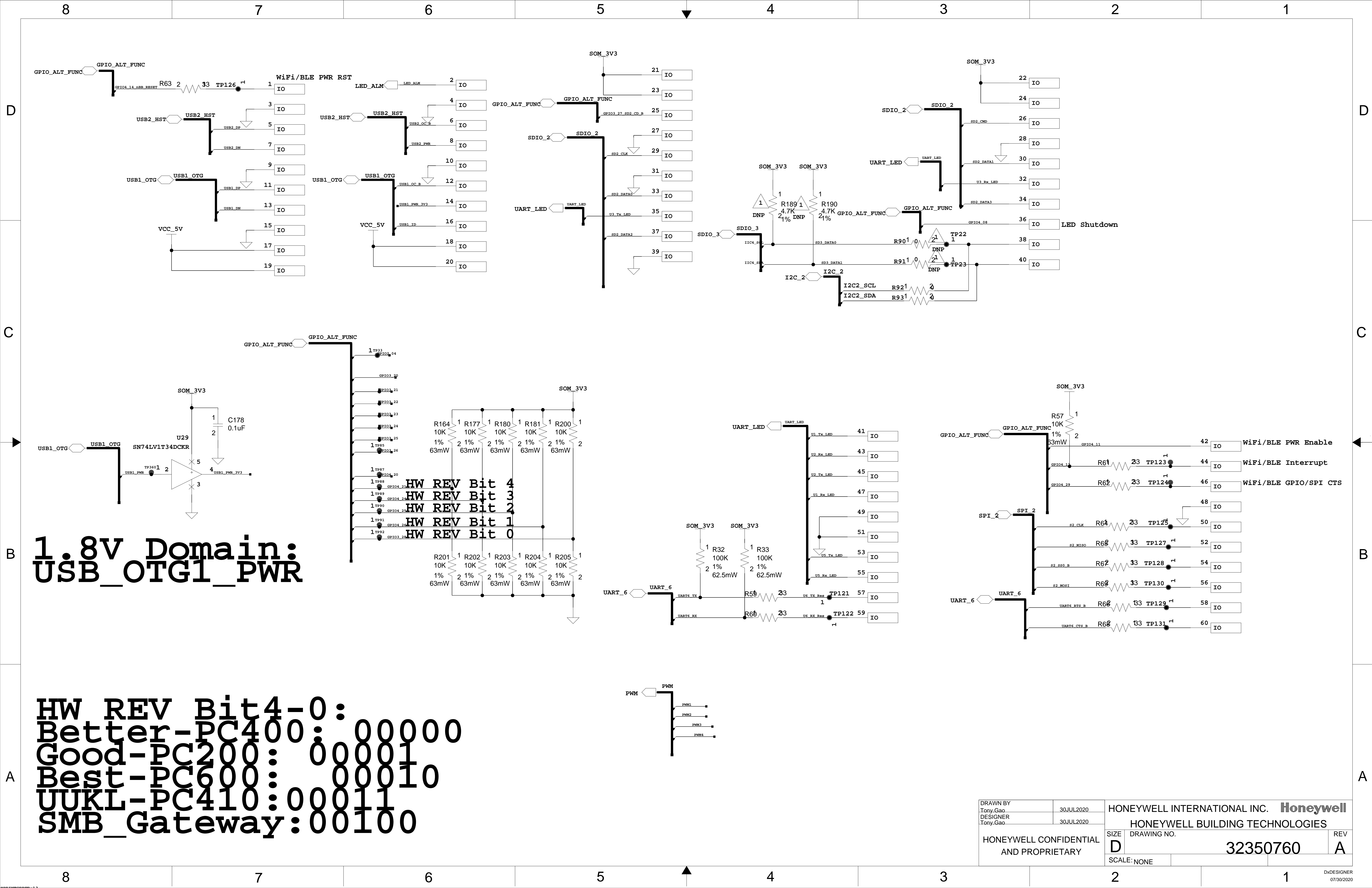
Note: 1000M operation: R170 and R178 populated, R51 and R169 unpopulated

SWITCH PORT 2



BLUE box for 100M
J3 Replace to 32338422-001 for 100M
RED box for 1000M

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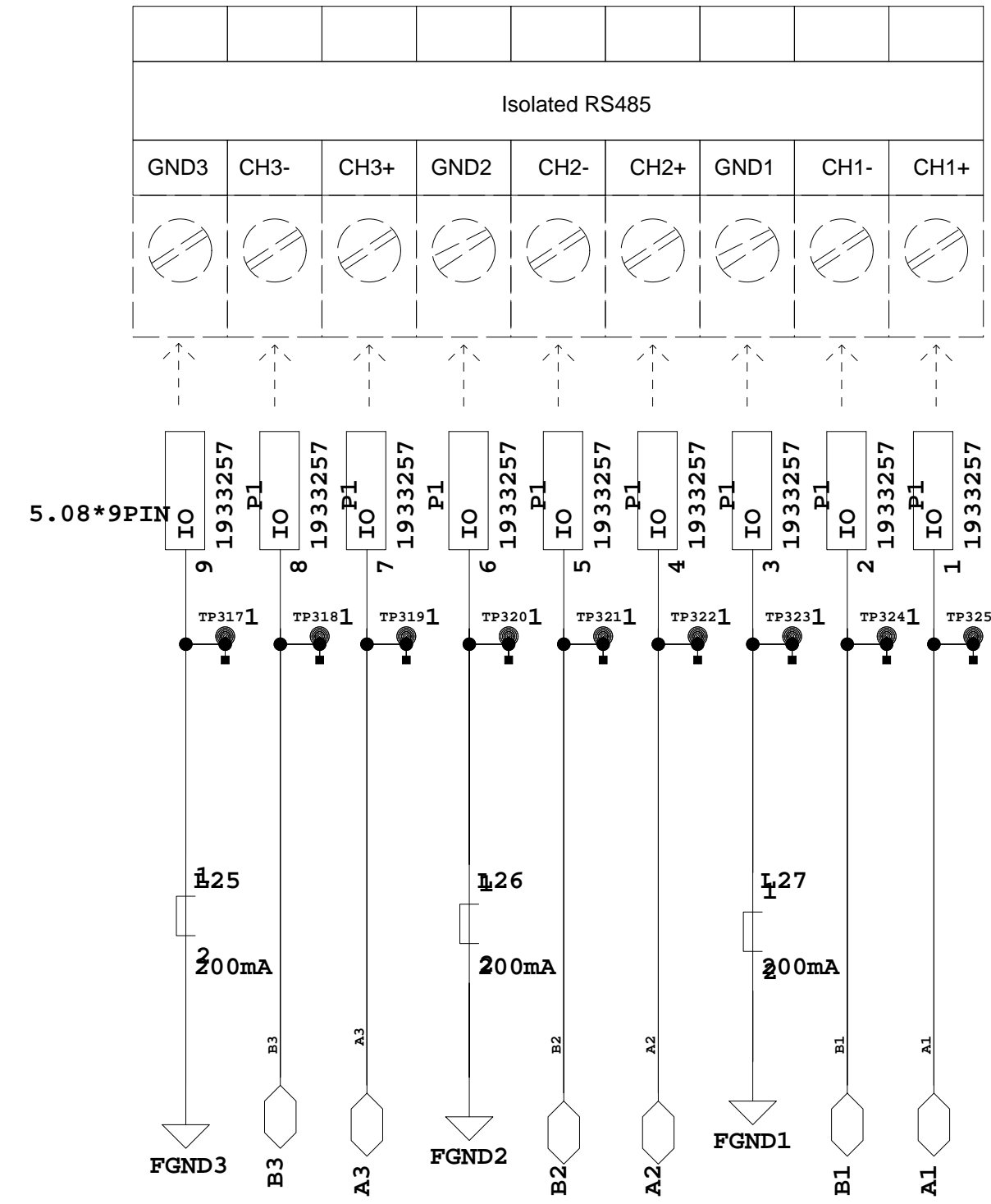


1.8V Domain: USB_OTG1_PWR

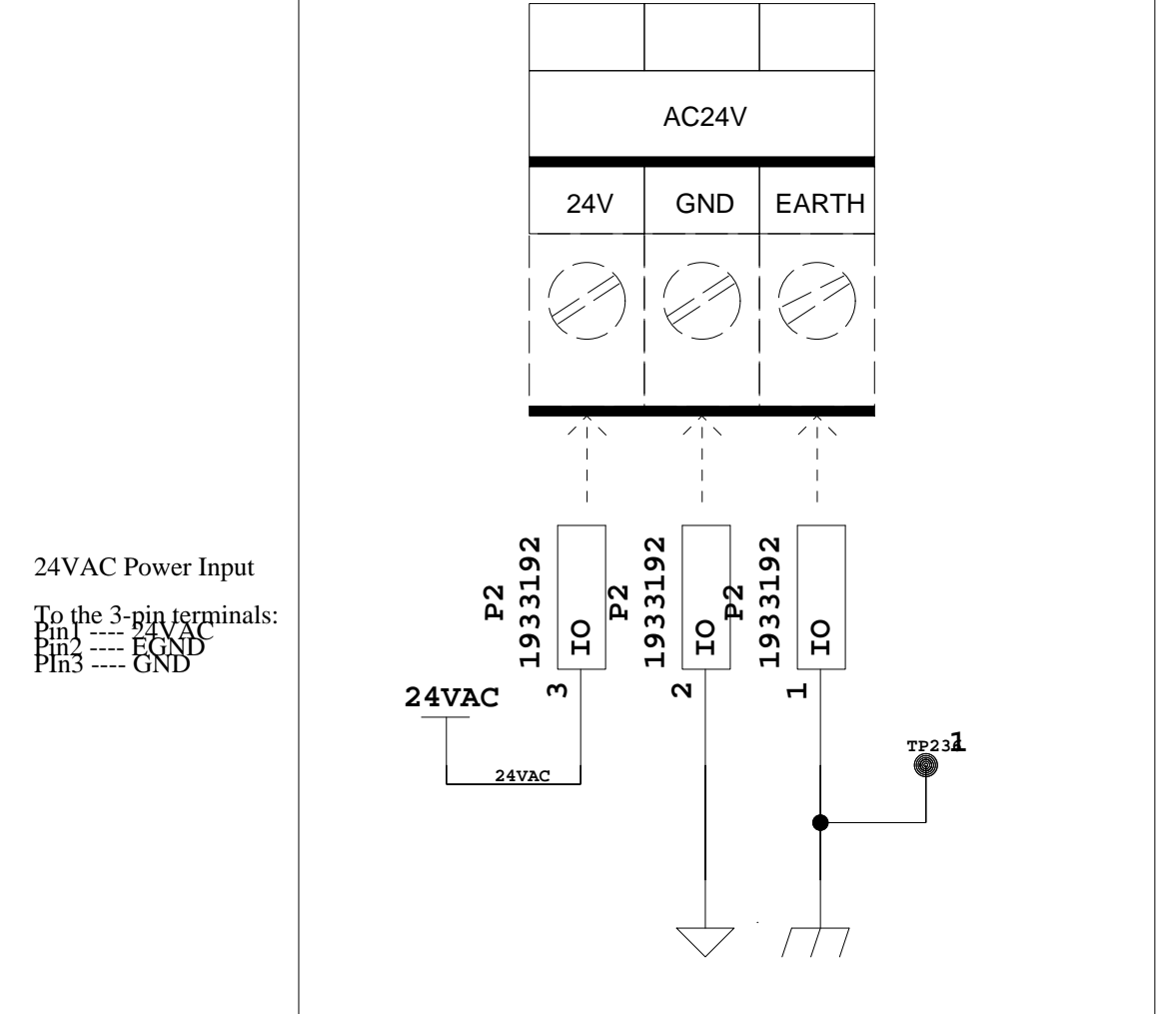
HW REV Bit 4-0:
 Better-PC400: 00000
 Good-PC200: 00001
 Best-PC600: 00010
 UUKL-PC410: 00011
 SMB_Gateway: 00100

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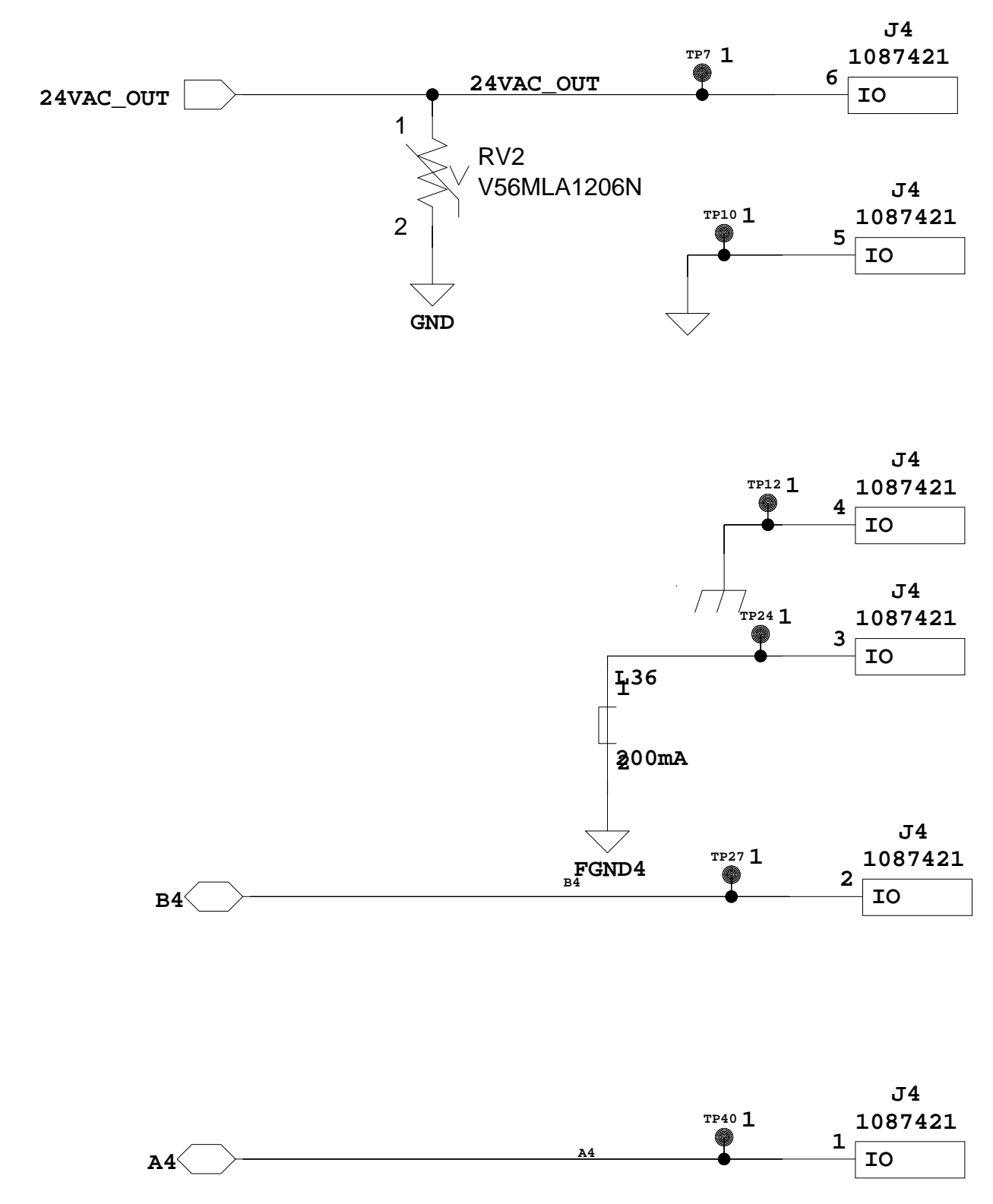
Top connector



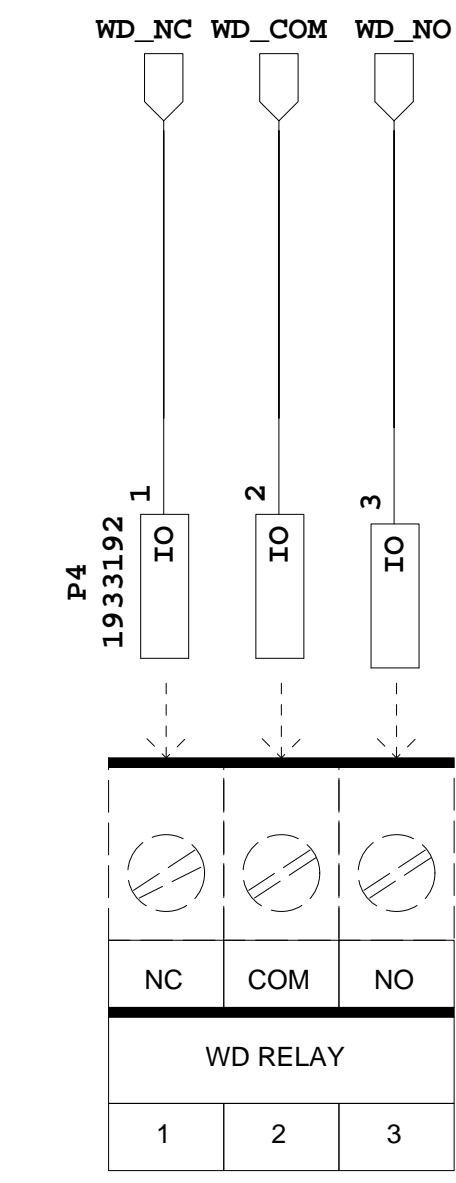
Top connector



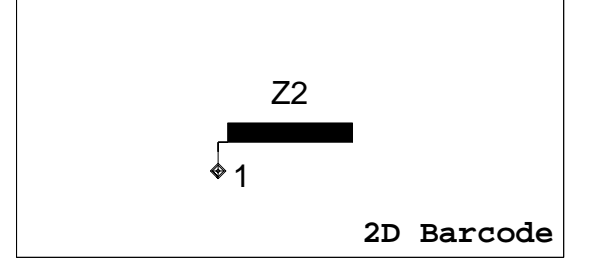
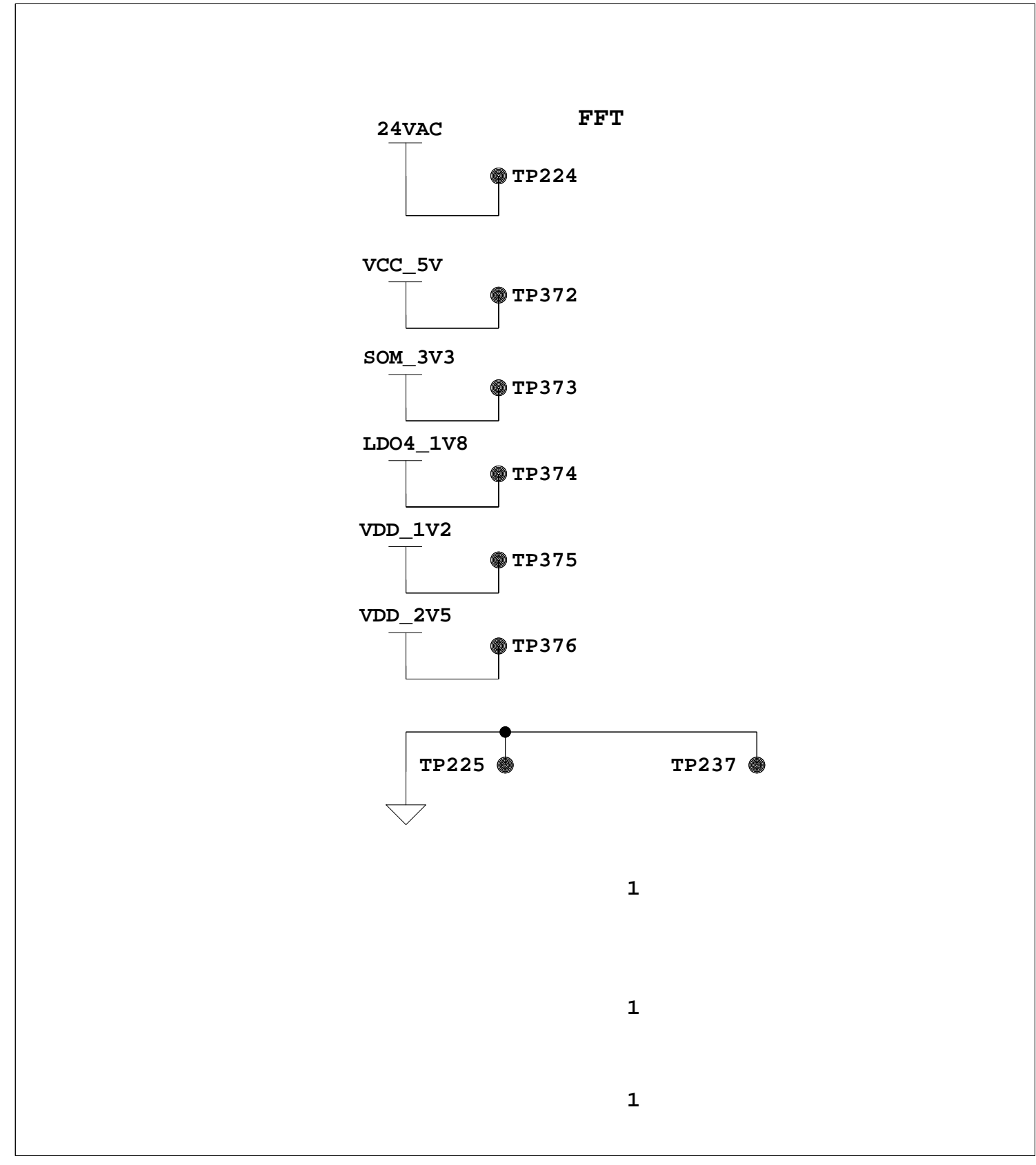
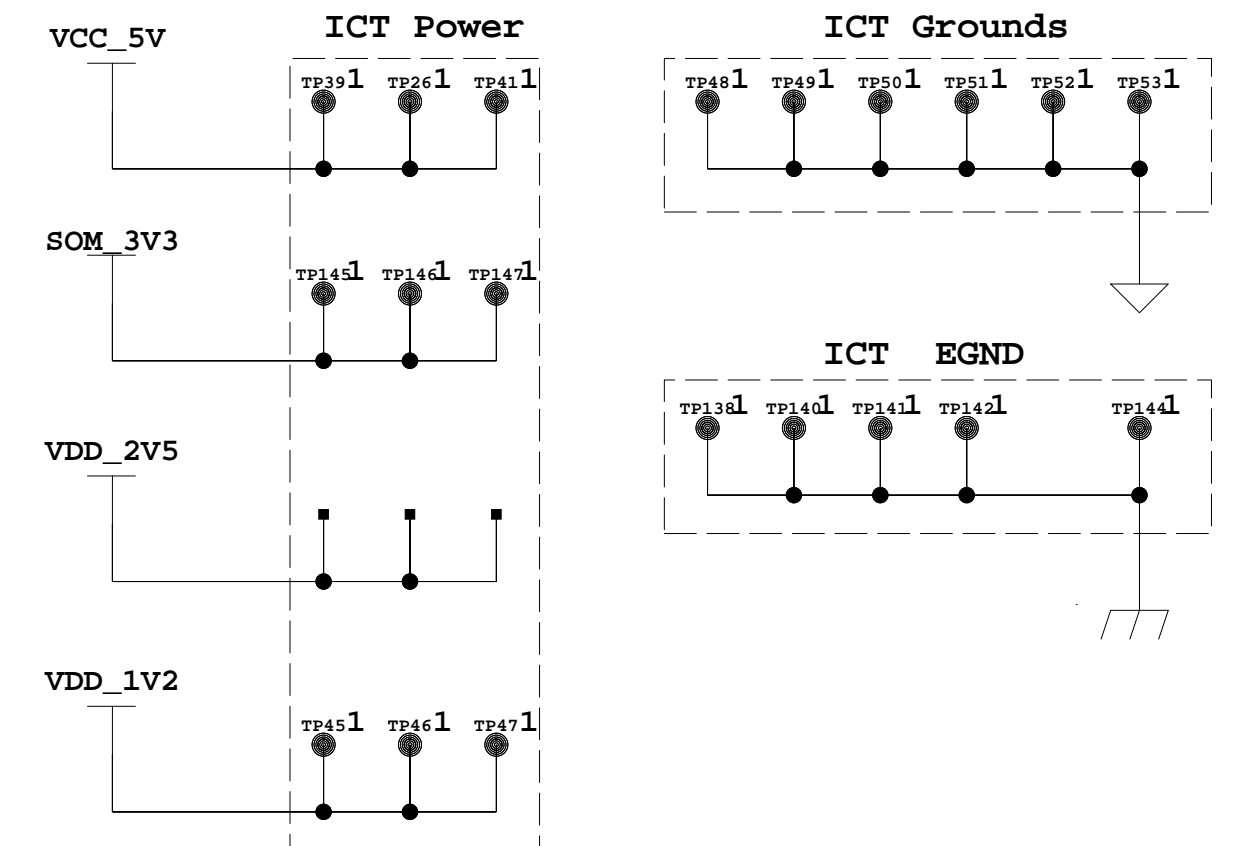
Power-bus and Honey-bus interface



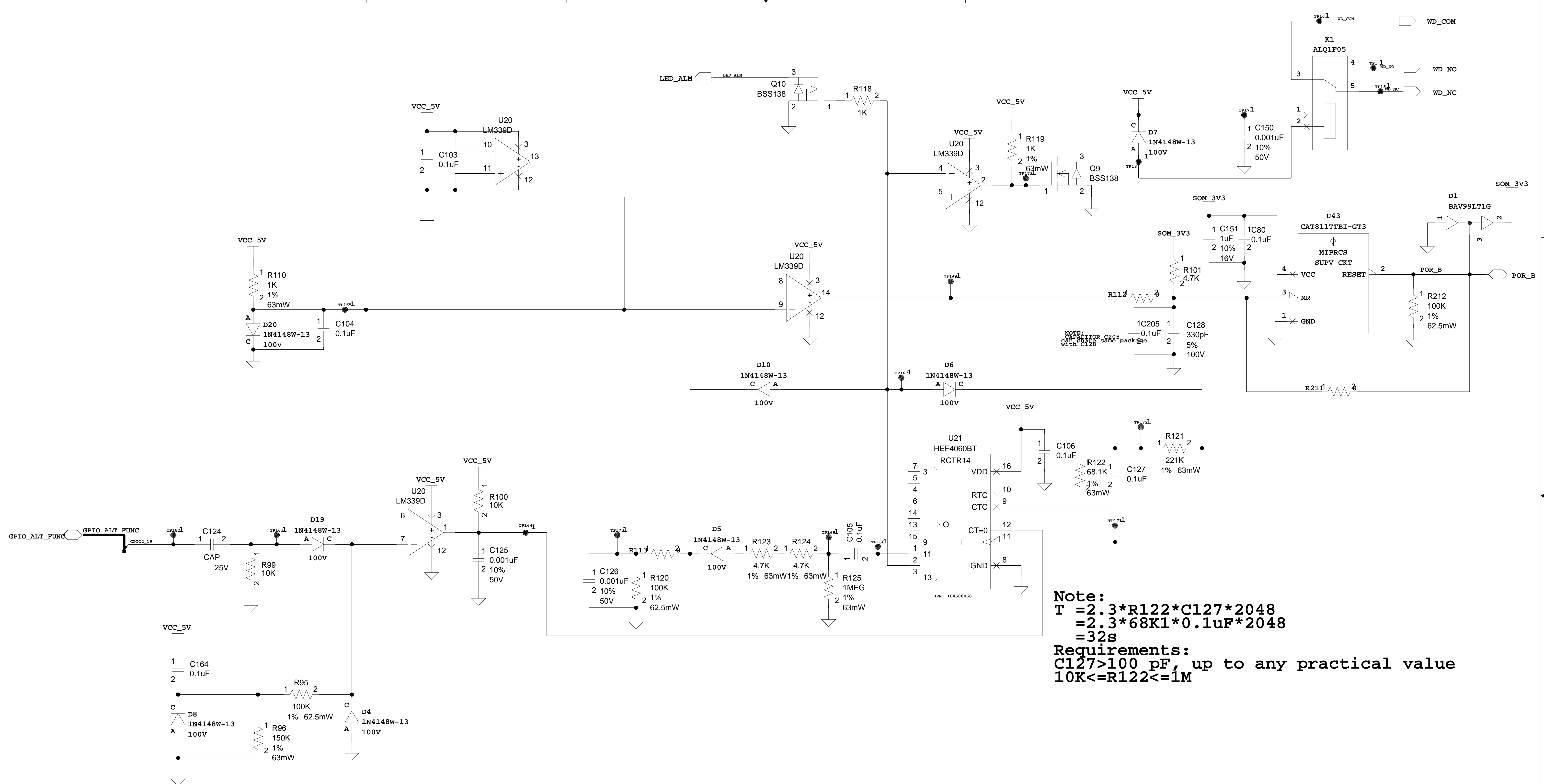
6 PIN ORDER
 24V AC
 GND
 FGND
 48V GND
 48V+
 5+



TOP connector



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		SCALE: NONE	REV A



Note:
 $T = 2.3 * R122 * C127 * 2048$
 $= 2.3 * 68K1 * 0.1uF * 2048$
 $= 32s$
Requirements:
 $C127 > 100 \text{ pF}$, up to any practical value
 $10K \leq R122 \leq 1M$

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		SCALE: NONE	REV A