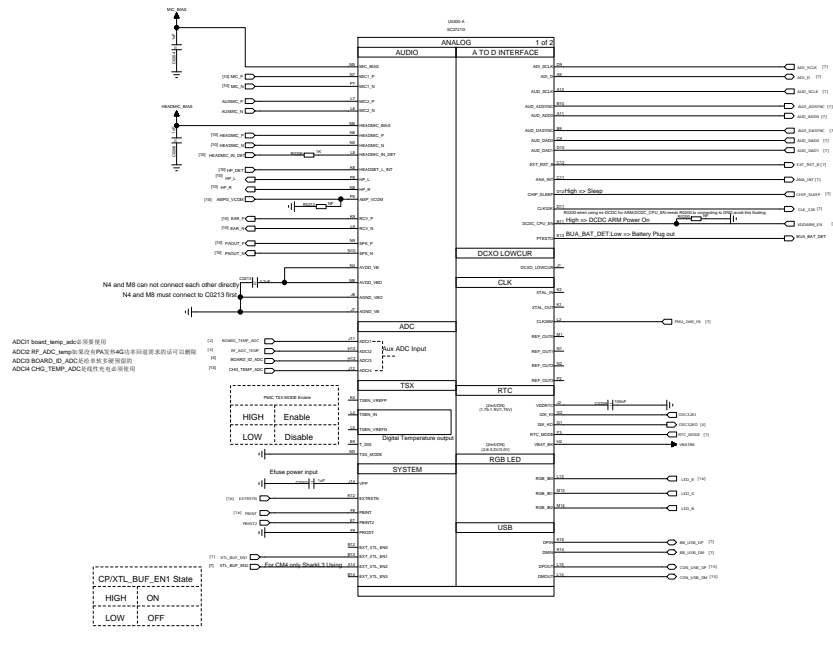


REVISED RECORD			
DATE	REV. NO.	DESCRIPTION	DATE

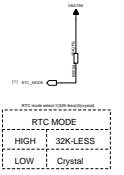
PMU_ANALOG



BKBT



RTC



RTC Mode	Type	R0202	X0200	C0201	C0202	R0203	R0204	R0617	R0205
32K Crystal	Option	OR	Crystal	8.2pF	8.2pF	OR	NF	NF	NF
32K-less	Default	NF	NF	NF	NF	NF	10K	OR	OR

Note: 32K-less only use in DCXO&TCXO mode and TSX

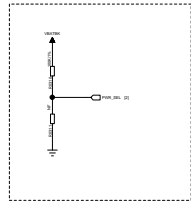
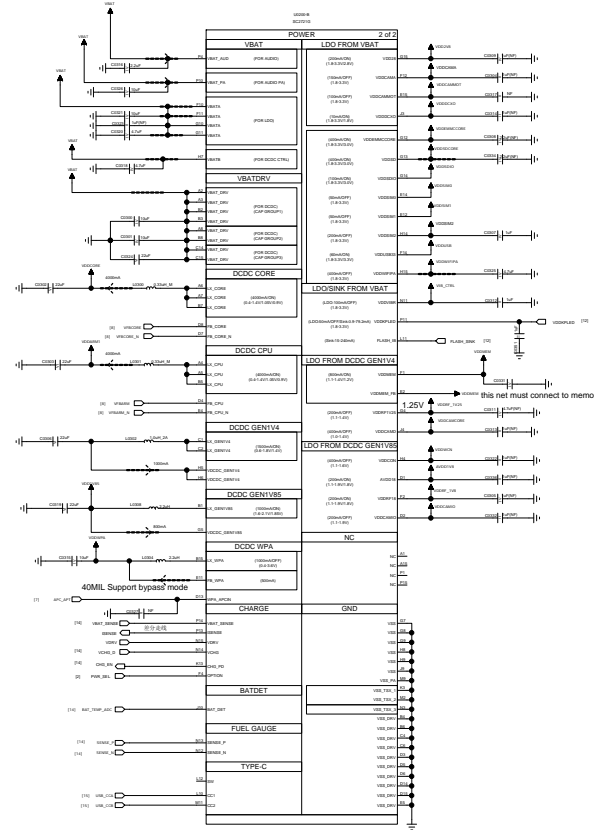
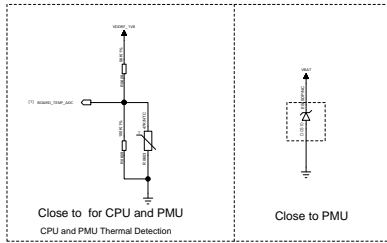
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EQUIPMENT NO.		
DESIGNER	DATE	DEPARTMENT
		Hardware DEPT.
EDA	DATE	COMPANY
		Spreadtrum communications, Inc.
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REV	DATE	APPROVAL	DATE

PMU_POWER

INPUT	Description
VBAT_AUD	VBAT power input for audio
VBAT_PA	VBAT power input for audio speaker PA
VBATA	VBAT power input for LDO
VBATR	VBAT power input for KP_LED_VIB_VBATBK_Flash_LED
VBATC	VBAT power input for LDO
VBAT_DRV	VBAT power input for DCDC

Default: VBAT R0300-SMT
 Option 1: VBAT_PA R0316/R0307-SMT



PMU_SEL	Platform	R0310	R0311	VDDARM	VDDCORE
HIGH	SharkL3	100K	NF	0.9V	0.9V/0.7V
LOW	SharkL2	NF	0ohm	1.05V	1.05V/0.8V

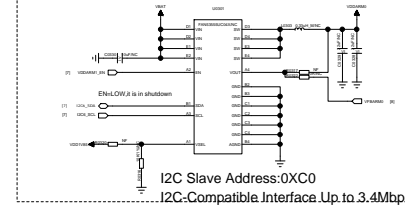
SC2721 DCDC output

Input Power	Power Name	Output Voltage (V)	Output Current	Default Voltage	Default
VBAT	DCDCCPU	0.4-1.4/1.05/0.9	400mA	0.9V	ON
	DCDCCORE	0.4-1.4/1.05/0.9	400mA	0.9V	ON
	DCDCMEM	1.1-1.4	800mA	1.2V	ON
	DCDCGEN1V85	1.6-2.1	1000mA	1.85V	ON
	DCDCWPA	0.4-3.6	1000mA		OFF

SC2721 LDO output

Input Power	Power Name	Output Voltage (V)	Output Current	Default Voltage	Default
LDO from VBAT	VDDCAMA	1.8-3.3	150mA	2.8V	OFF
	VDDCAMMOT	1.8-3.3	100mA	2.8V	OFF
	VDDSIM0	1.8-3.3	50mA	1.8V	OFF
	VDDSIM1	1.8-3.3	50mA	1.8V	OFF
	VDDSIM2	1.8-3.3	200mA	1.8V	OFF
	VDD28	1.8-3.3	200mA	2.8V	ON
	VDDMEMCCORE	1.8-3.3	400mA	3.0V	ON
	VDDSDCORE	1.8-3.3	400mA	3.0V	ON
	VDDSDIO	1.8-3.3	100mA	3.0V	ON
	VBATBK	2.6-3.2	2mA	3.0V	ON
	VDDVIB	1.8-3.3	100mA	3.3V	OFF
	VDDKPLED	1.8-3.3	LDO 50mA/Sink 0.9-29.2mA		
	VDDWIFIPA	1.8-3.3	400mA	3.3V	OFF
	VDDDCXO	1.8-3.3	10mA	1.8V	ON
	VDDUSB33	1.8-3.3	60mA	3.3V	ON
LDO from DCDCGEN	VDDCAMD	1.0-1.4	400mA		OFF
	VDD_CON	1.1-1.6	400mA		OFF
	VDD_MEM	1.1-1.4	800mA	1.2V	ON
	VDDCAMIO	1.1-1.9	200mA		OFF
	AVDD18	1.1-1.9	200mA	1.8V	ON
VDDRF18	1.1-1.9	200mA	1.8V	ON	
VDDRF1V25	1.1-1.4	200mA		OFF	

EXT DCDC ARM



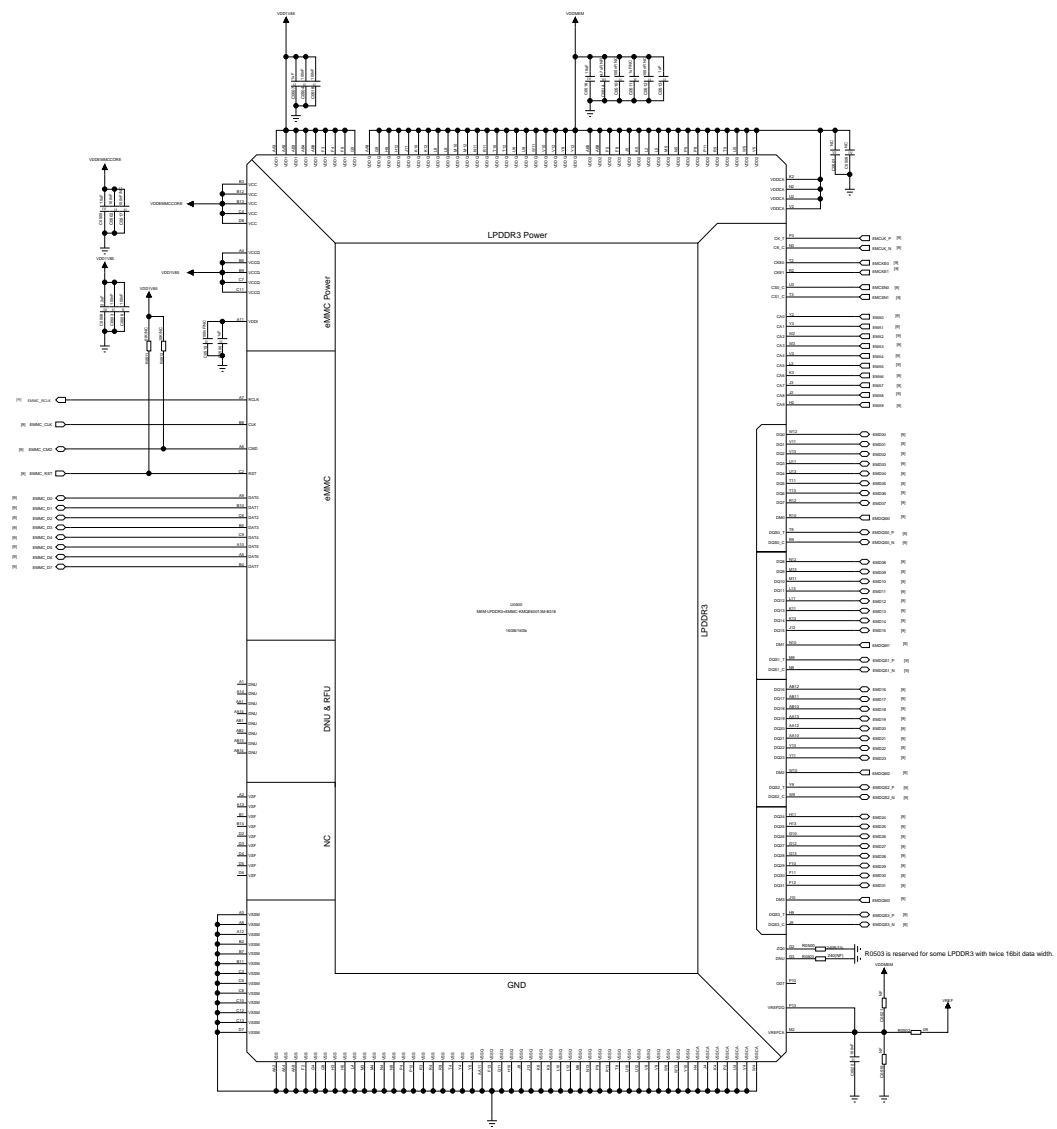
SC1893A(VDDARM) C0328-22uF C0328-22uF U0301-FANES1850-C04X C0320-10uF R0316-10K1% L0303-0.33uH M R0322-HR
 SC1893E(VDDARM) C0328-22uF C0328-22uF U0301-HC C0320-10uF R0316-10K1% L0303-0.33uH M R0322-HC

REV	DATE	DESCRIPTION

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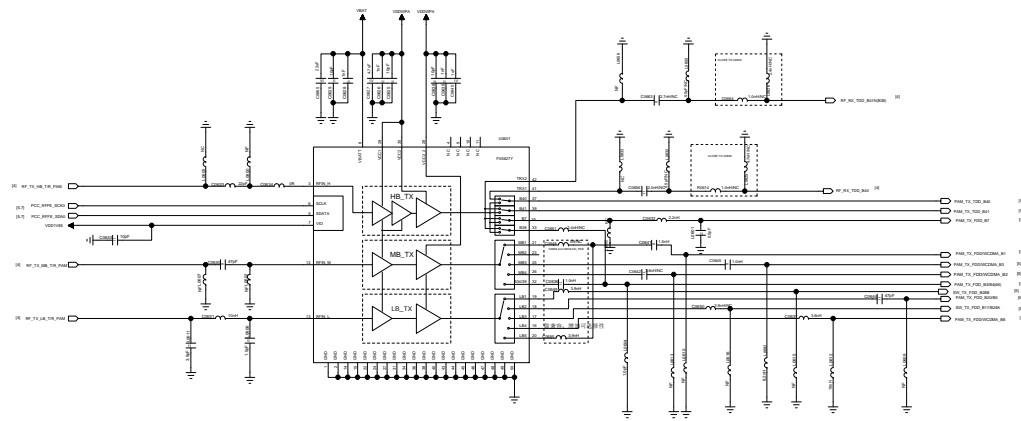
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DATE	DESCRIPTION	APPROVED BY	DATE

eMMC+LPDDR3

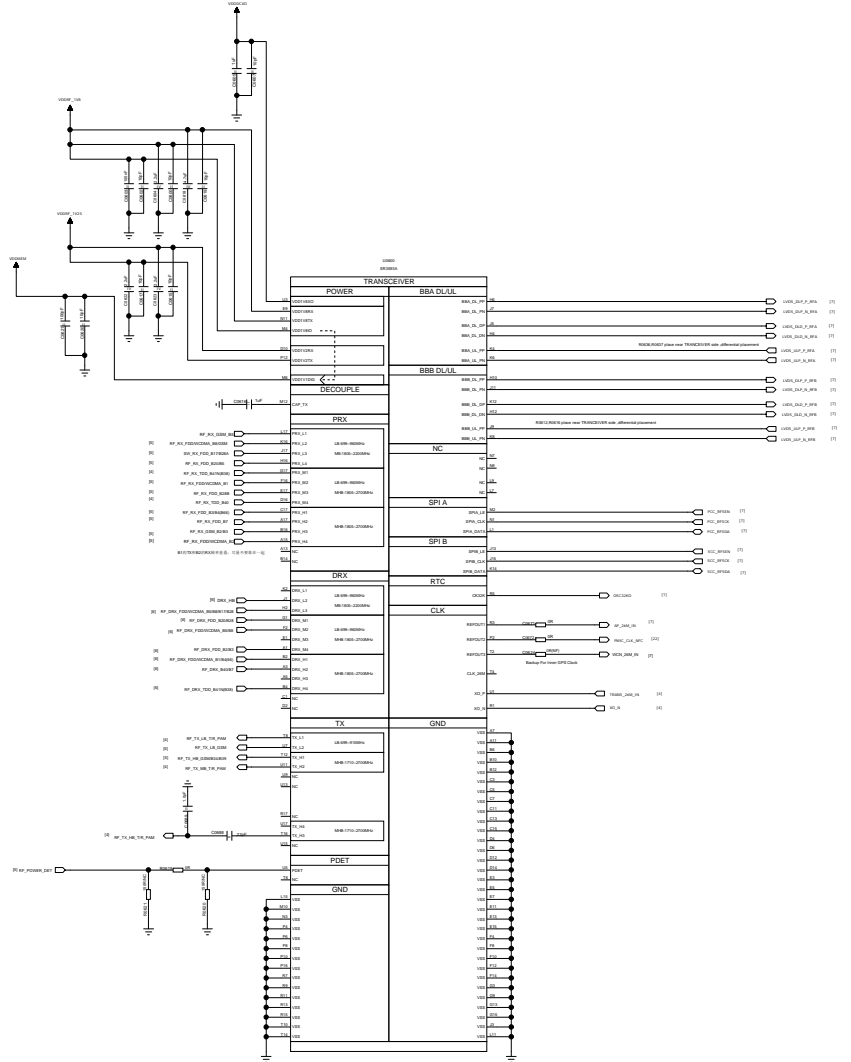
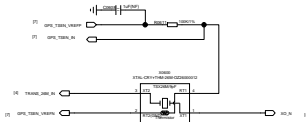
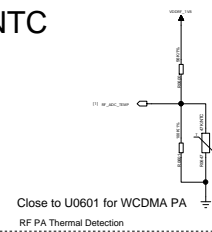


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DRAWN		DATE	APPROVED BY
CHECKED		DATE	APPROVED BY
APPROVED		DATE	APPROVED BY
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LTE/WCDMA PAM



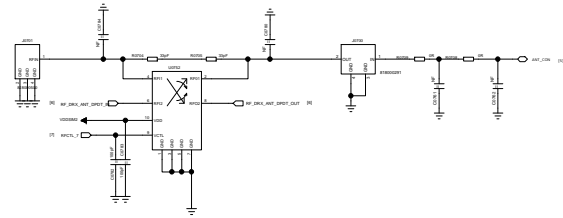
NTC



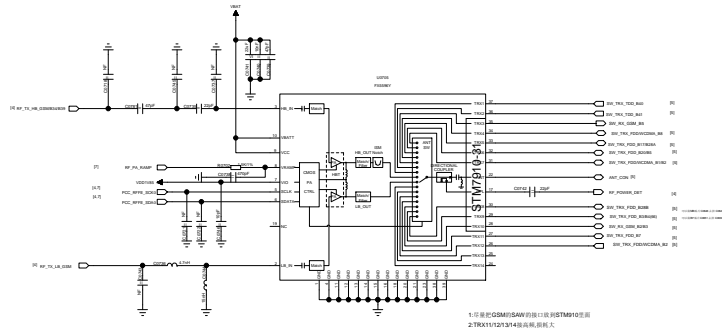
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REV.	REASON	APPROVAL	DATE

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DESIGNER	DATE	DESIGN NO.	Hardware DEPT.
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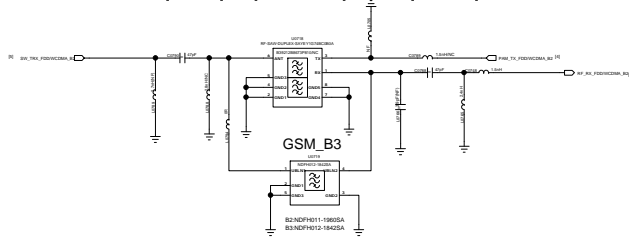
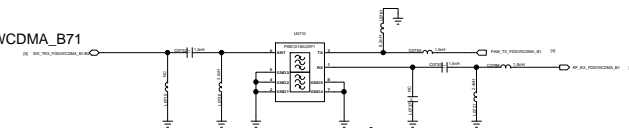
Primary LMB Antenna



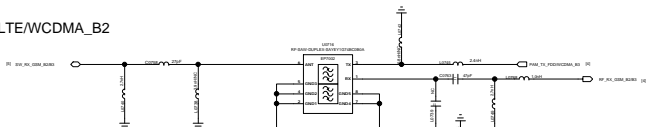
TDD B34/B39/GSM PA + Switch



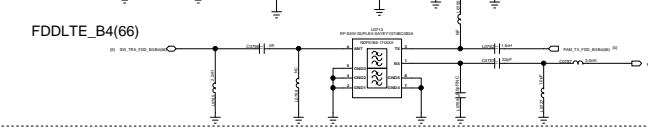
FDDLTE/WCDMA_B71



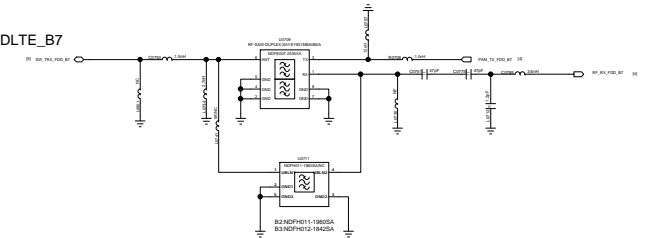
FDDLTE/WCDMA_B2



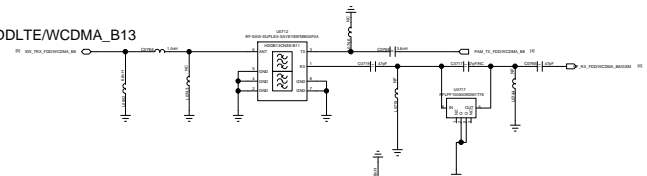
FDDLTE_B4(66)



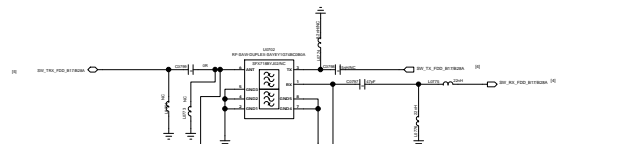
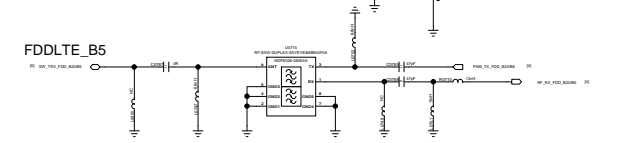
FDDLTE_B7



FDDLTE/WCDMA_B13

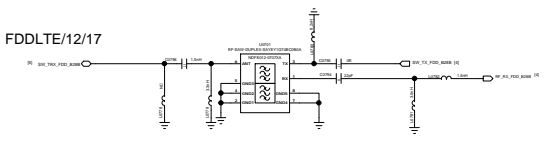


FDDLTE_B5

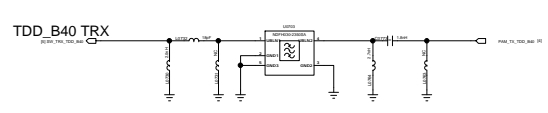


GSM_B8

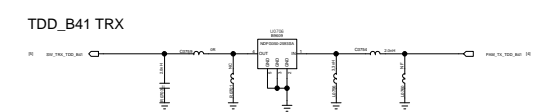
FDDLTE/12/17



TDD_B40 TRX



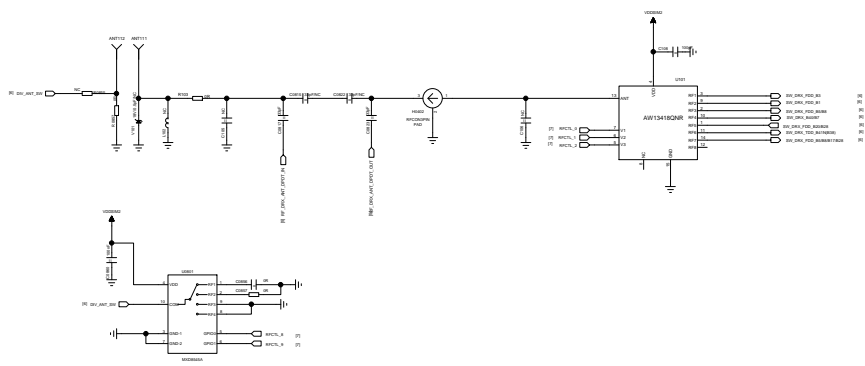
TDD_B41 TRX



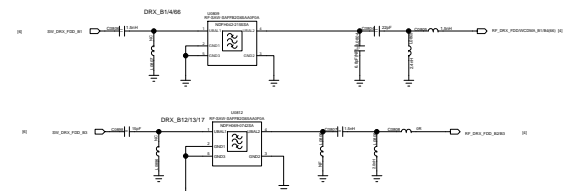
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DESCRIPTION			
DESIGNER	DATE	DEPT	Hardware DEPT.
CHK	DATE	COMPANY	Spreadtrum communications, Inc.
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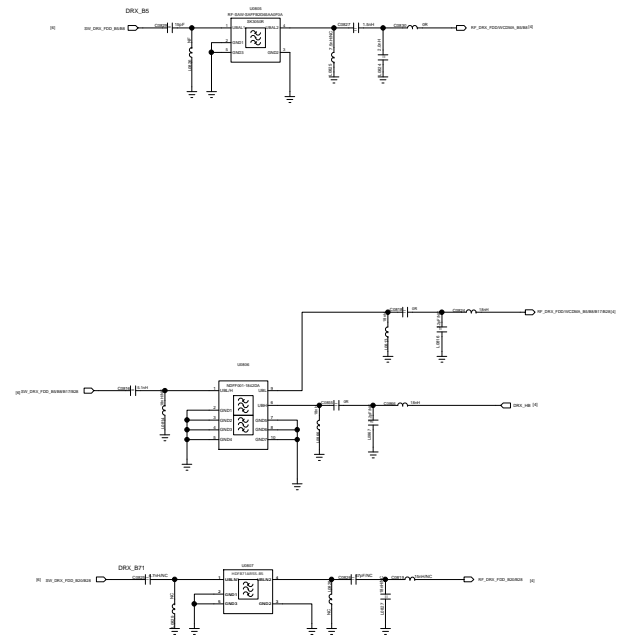
Diversity LTE LMB Path



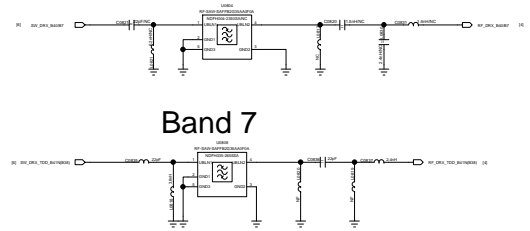
M Band Diversity RX Path



L Band Diversity RX Path



H Band Diversity RX Path

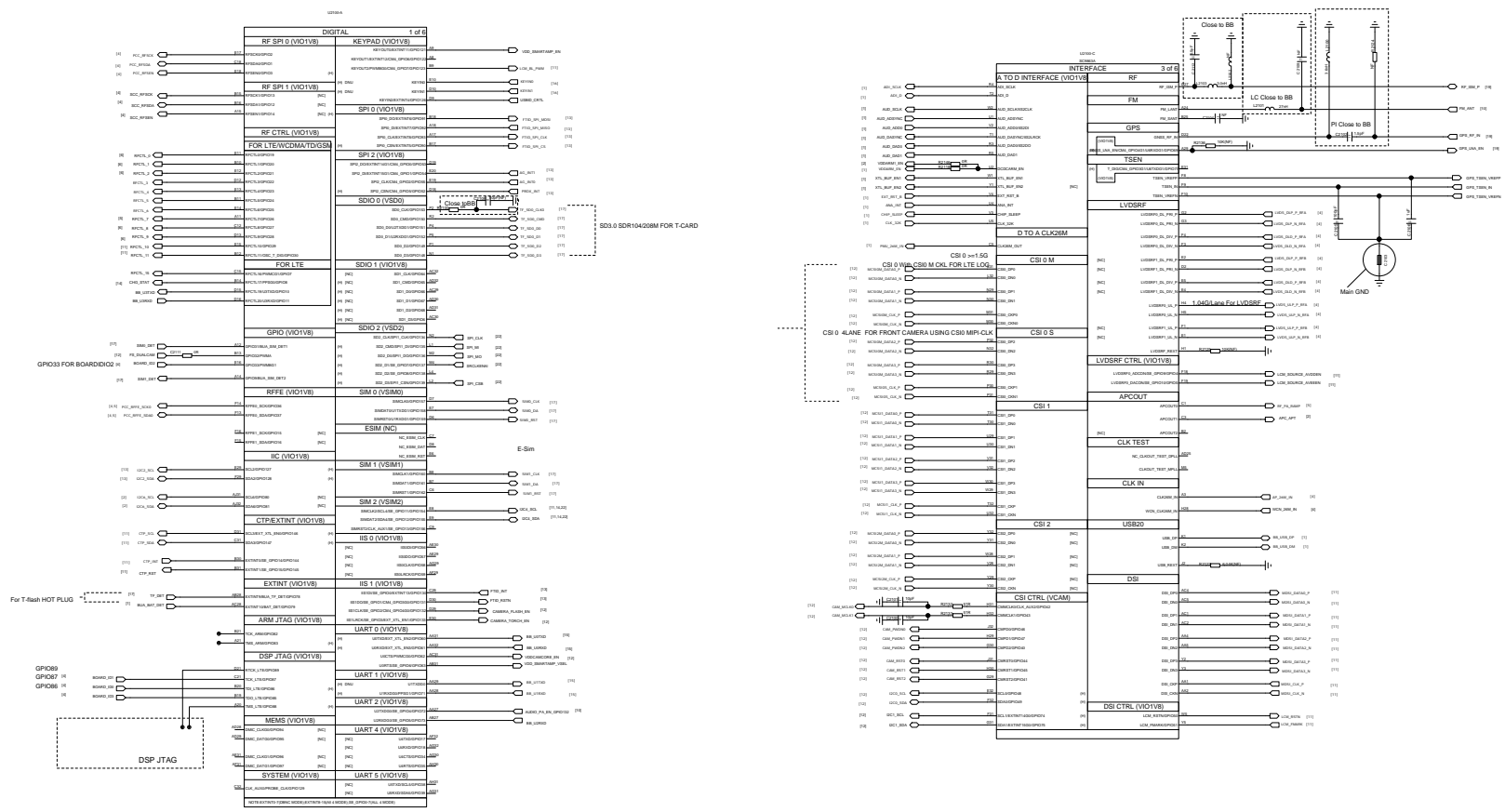


Band 7

TITLE & REV			
DESCRIPTION REV			
DESIGNER	DATE	DESIGN NAME	Hardware DEPT.
EDA	DATE	COMPANY	Spreadtrum communications, Inc.
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REV	REVNO	APPNO	DATE

DIGITAL

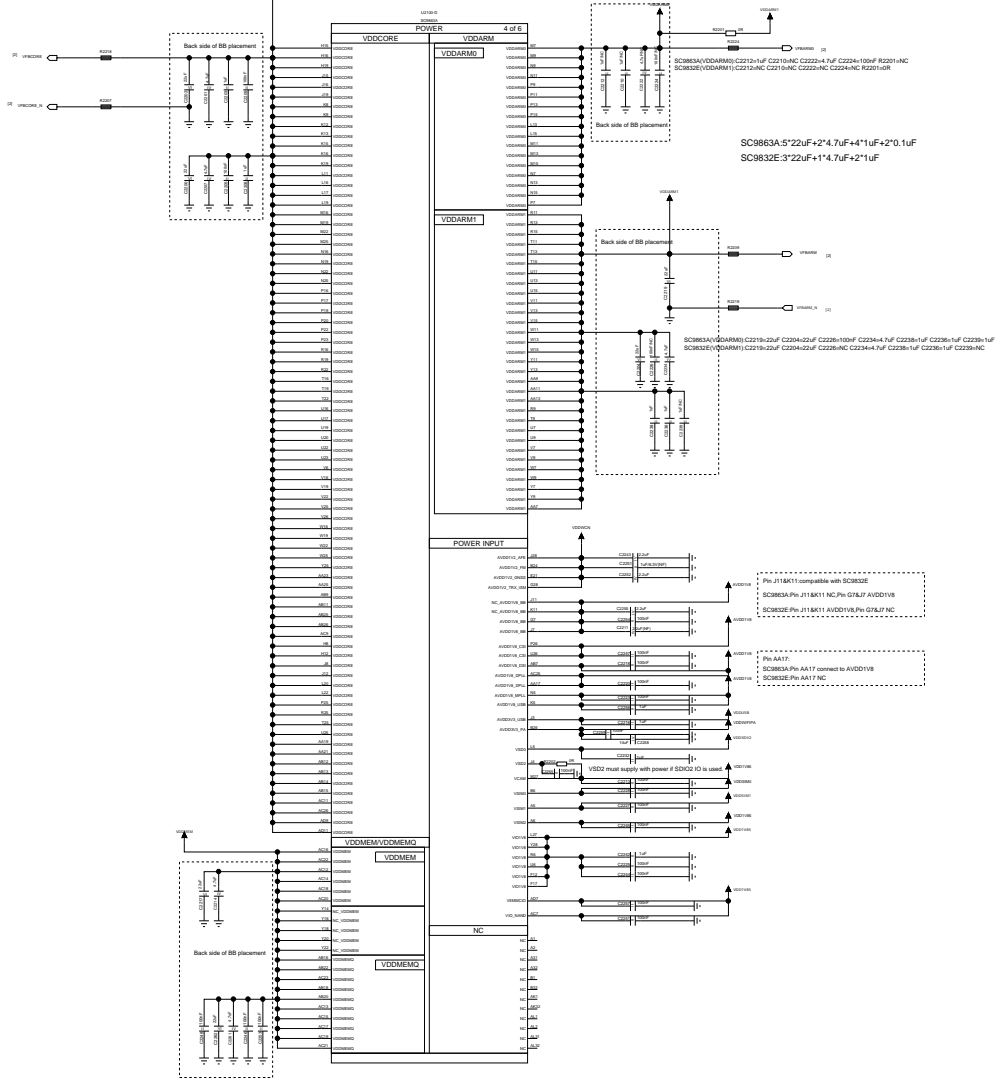


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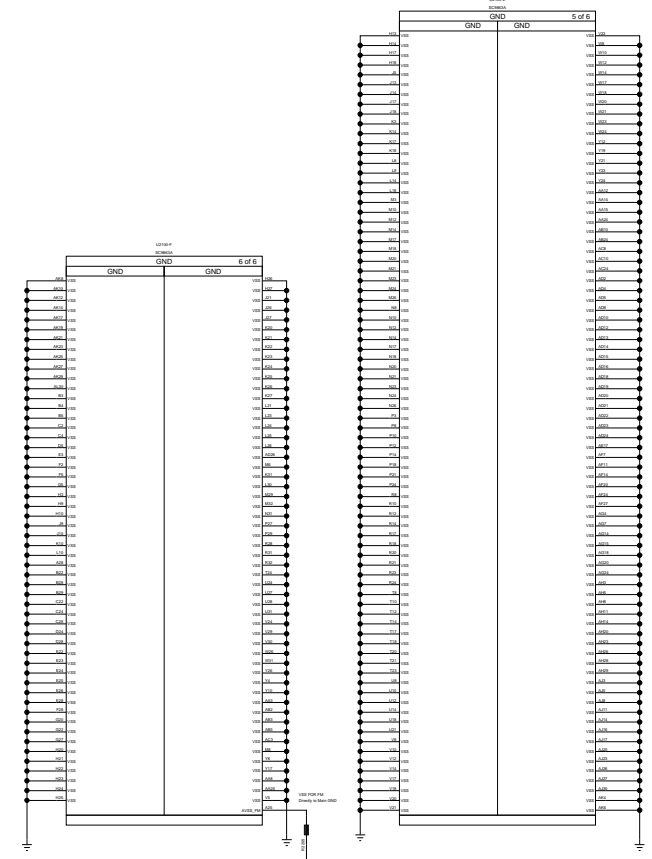
Hardware DEPT.
Spreadtrum communications, Inc.

REVISION HISTORY			
DATE	BY	DESCRIPTION	DATE

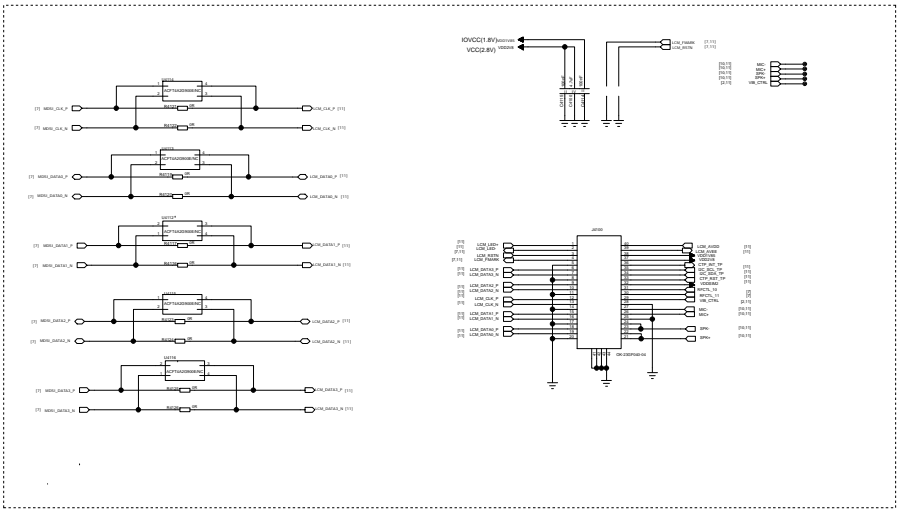
POWER



GND

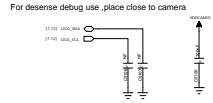
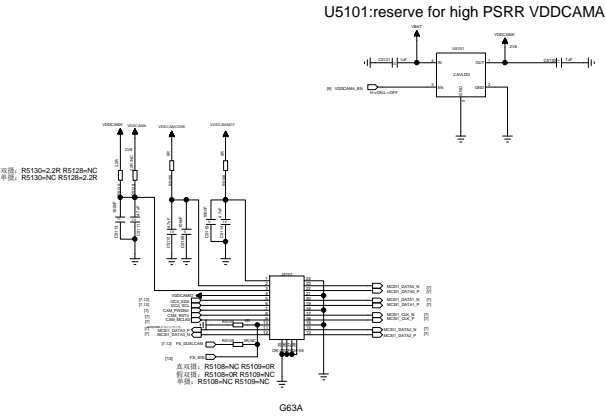


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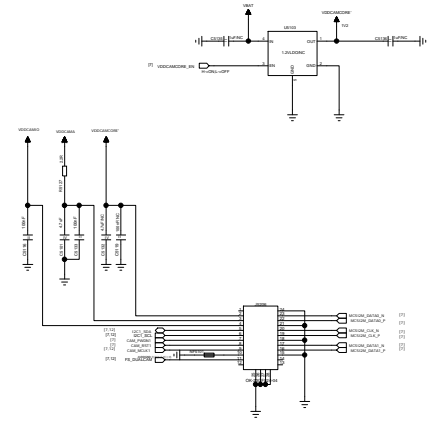


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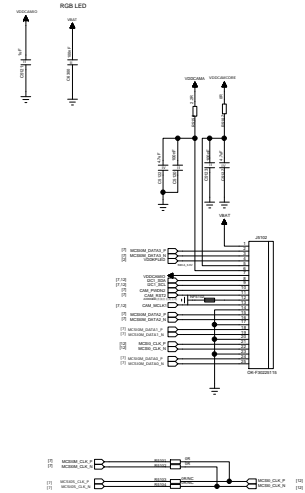
Rear Dual Camera 0:13M



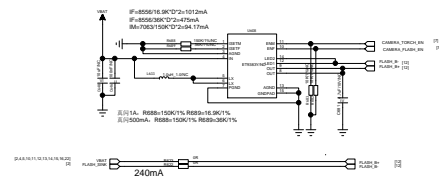
Rear Daul Camera



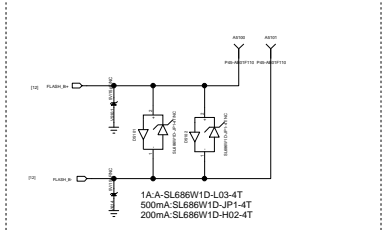
Front Camera 2:16M



FLASH LED_BACK

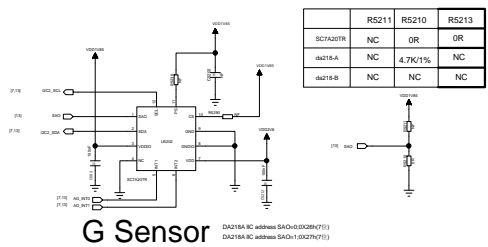


BACK LED

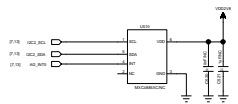


Front LED

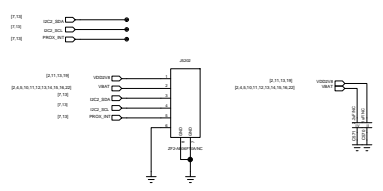
Accelerometer



G Sensor

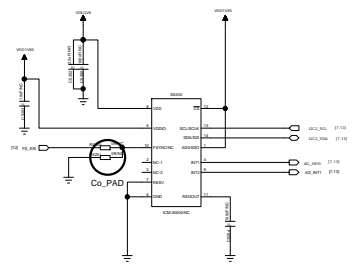


ALS & PROX

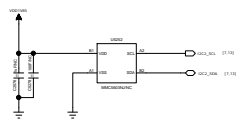


	LTR-553ALS-WA
SIZE	3.94 x 2.38 x 1.35
1	SDA
2	INT
3	LDR
4	LED K
5	LED A
6	GND
7	SCL
8	VDD
9	VDD

Accelerometer&GYRO: ICM-20600



Magnetic Sensor:AK09911C

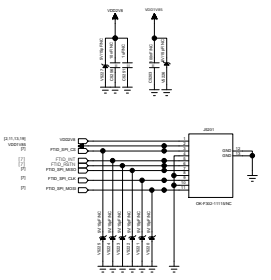


IIC address: 0x30 (7位)

Pin	Definition
VDD	2.4V - 3.6V
VID	1.65V - VDD
CAD	Address select Note : connect to VDD,not VID

FingerPrint ID

NOTE:FPC=LAYOUT LINE<10MM
(BACKUP)



I2C ADDRESS

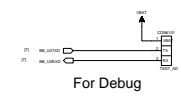
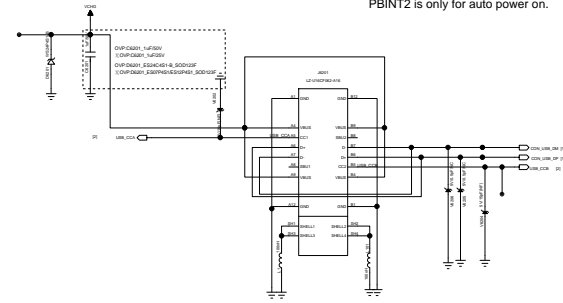
	Manufacturer	MPN	Address
A sensor	BOSONH	BM4255	0b0011001 (SDCA=1)
M sensor	ASAHIKASEI	AK09911	0b0001101 (CAD=1)
ALS & PROX	LITEON	LTR-553ALS-WA	0b100011
A&G Sensor	InvenSense	ICM-20600	SA0=0.0b11010000 SA1=0.0b11010001
M sensor	AKM	AK09918C	0b0001100 (R-W)

TITLE & REV.		
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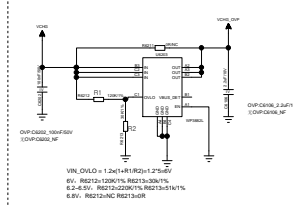
Revision History			
CR	Rev No.	Entered	By

5pin Micro USB

USB BOOT CONTROL
 NBOOT = Float---->NAND BOOT
 NBOOT = 0 ---->USB BOOT
 PBINT2 is only for auto power on.



OVP



UART POINT



MARK POINT

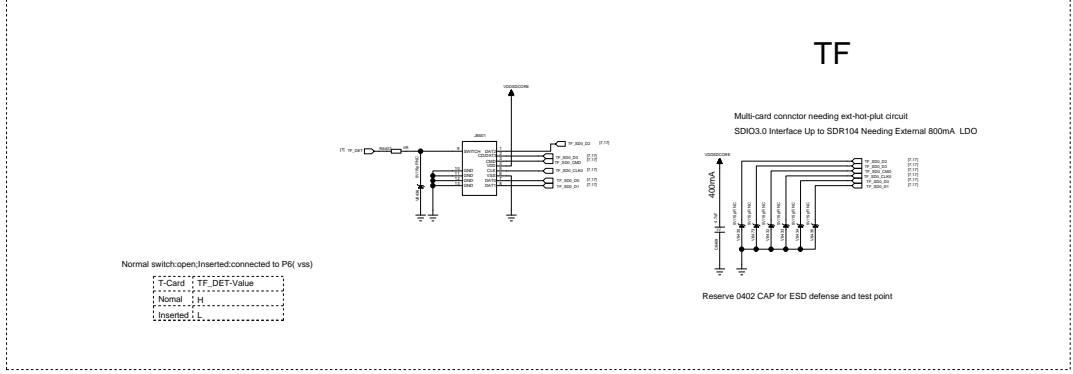
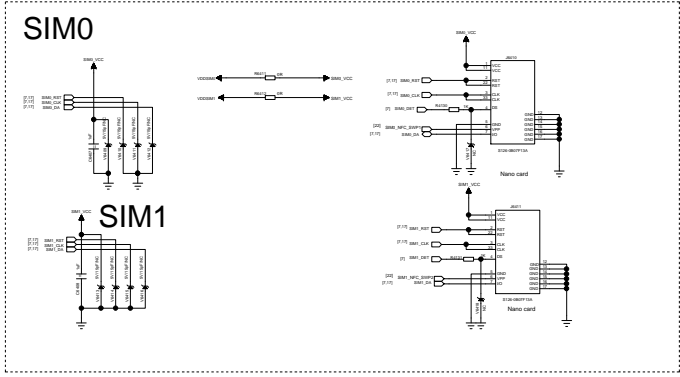


SharkLE strapping pin

Ball name	Signal name in boot code	Value	Description	Default value
U1TXD	USB_DOWNLOAD_EN	0	USB download enable (time out)	1(=1,wp0)
AUD_DAD1	ARM_BOOT_MD0	000	Reserved	
		001	TIC/NAND Toggle	
AUD_DADD	ARM_BOOT_MD1	010	MLC/SLC NAND Flash(ON)	11(=1,wp0)
		011	SLC boot (no time out)	
		100	MLC/SLC NAND Flash(Toggle)	(MSB=02)
		101	no NAND/Flash/ROM/EEPROM	(LSB=03)
AD1_SCLK	ARM_BOOT_MD2	110	Reserved	
		111	MMC boot	

Title & Rev.		
Description		
DESIGNER	DATE	DEPARTMENT
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Revision History			
CR	REV	DESCRIPTION	DATE



Title & Rev			
Equipment No.			
DESIGNER	DATE	APPROVED	Hardware DEPT.
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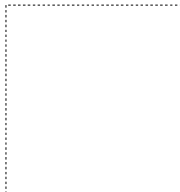
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REVISION RECORD			
DATE	DESCRIPTION	APPROVED BY	DATE



D

D

C

C

B

B

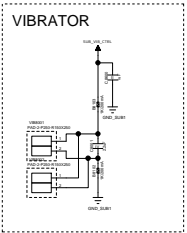
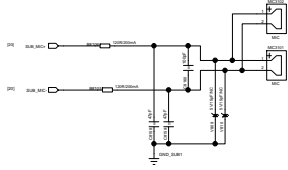
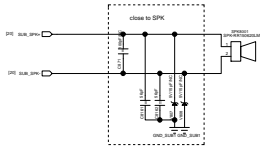
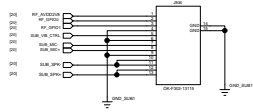
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A

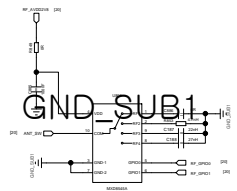
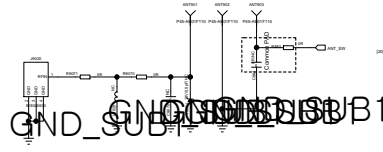
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DESIGNED BY:	DATE:	APPROVED BY:	DATE:
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		Spreadtrum communications, Inc.	
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CHK	DATE	APPROVED BY	DATE

Audio_SUB



ANT_SUB

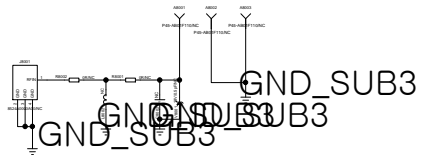


DESIGNER		DATE		APPROVED BY		DATE	

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DESIGNER	DATE	APPROVED BY	DATE
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Spreadtrum communications, Inc.			
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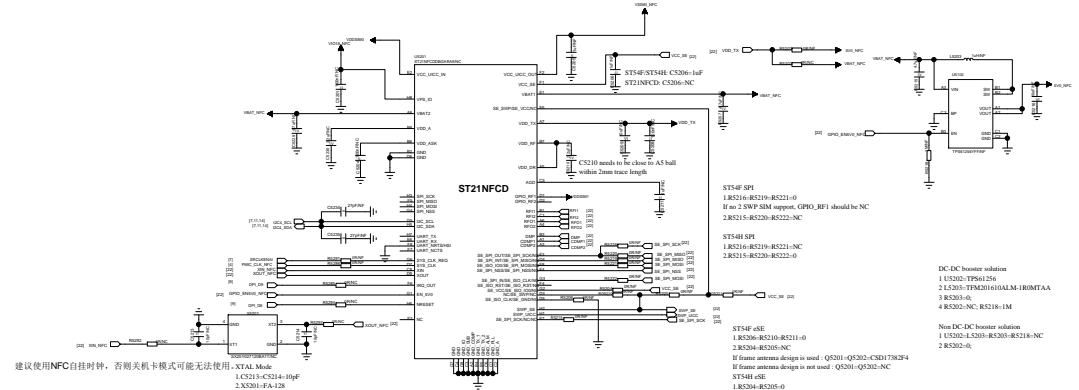
REVISION RECORD			
LINE	DESCRIPTION	DATE	BY

ANT_SUB



DATE:		DATE:		DATE:		DATE:		DATE:	
DESIGNED:		DATE:		CODE:		REV:		DRAWING NO.	
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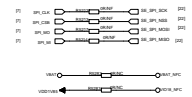
REVISION HISTORY			
LINE	REV. NO.	APPROVED	DATE



建议使用NFC自挂时钟，否则关机卡模式可能无法使用。ATX14. Mode: 1 CS213-CS214-10uF 2 X5201-FA128 3 R5206-R5201-NC

As for co-lock mode, if customers need to pass CT NFC certification, recommended to increase NFC antenna size > 150mm² to ensure enough PCB distance margin.

Co-Check Mode: 1 CS213-CS214-X5201-NC 2 R5206-R5201-0 ohm



SE ball name definition for ST54F, ST54H, and ST21NFC, respectively

Ball	ST21NFC	ST54F	ST54H
D3	NC	SE_SWP	NC
D4	NC	SE_SPI_MISO	SE_SPI_INT
D5	NC	SE_GND	SE_ISO_CLK
E3	NC	SE_SPI_SCK	SE_SPI_OUT(MISO)
E4	NC	SE_SPI_NSS	SE_SPI_NSS
E5	NC	SE_VCC	SE_SWP
E7	NC	NC	SE_SPI_SCK
E8	NC	SE_SPI_MOSI	SE_ISO_IO0
F4	NC	SE_ISO_RST	SE_ISO_RST
Q2	NC	SE_ISO_IO0	SE_VCC
Q3	NC	SE_ISO_CLK	SE_SPI_IN(MOSI)

ST54F SPI
1 R5216-R5219-R5221-0
If use 2 SWP SIM support, QW03_BF1 should be NC
2 R5215-R5220-R5222-NC

ST54H SPI
1 R5216-R5219-R5221-NC
2 R5215-R5220-R5222-0

DC-DC booster solution
1 U3202-TPS61256
2 L3203-TPM21016(0ALM1R0MTAA)
3 R5201-0
4 R5202-NC; R5218-1M

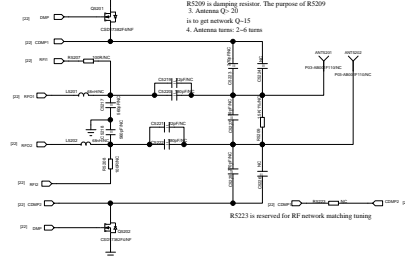
Non DC-DC booster solution
1 U3202-L3209-R5201-R5218-NC
2 R5202-0

ST54F eSE
1 R5206-R5210-R5211-0
2 R5204-R5205-NC
If frame antenna design is used - Q5201-Q5202-CSD1782F4
If frame antenna design is not used - Q5201-Q5202-NC

ST54H eSE
1 R5204-R5205-0
2 R5206-R5210-R5211-NC

ST21NFC
1 R5204-R5205-R5206-R5210-R5211-NC

Recommended NFC antenna spec, below
1. L @ 13.56MHz is 0.2uH ± 0.6uH
2. Freq. ant > 10MHz
R5209 is damping resistor. The purpose of R5209 is to get network Q=15
3. Antenna Q=20
4. Antenna turns 2-6 turns



- 1. ST21NFC - 1 SWP SIM Only
- 1 R5212-R5223-0 ohm
- 2 Q5201-Q5202-Q5203-NC
- 3 R5201-R5202-R5203-R5204-R5205-R5206-R5221-NC
- 2. ST21NFC - 2 SWP SIM
- 1 Q5201-CSD1782F4-Q5202-Q5203-CSD1782F4
- 2 R5204-R5205-1M; R5206-1K; R5201-R5202-R5203-R5221-R5222-0 ohm
- 3. ST54F - 1 SWP SIM + 1 SWP eSE
- 1 R5212-R5223-0 ohm
- 2 R5201-R5202-R5203-R5204-R5205-R5206-R5221-NC; Q5201-Q5202-Q5203-NC

