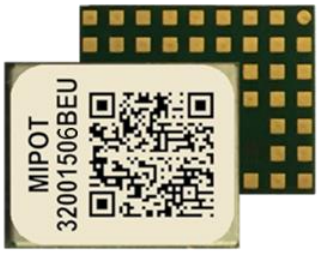
Wireless Protocol Modules MiP Series 32001552xUS Family

Stand Alone LoRa™ Modem with MCU

Datasheet



Overview

The 32001552xUS is a family of transceivers operating in the 915 MHz SRD Band optimized for very long range, low power applications, suitable for LPWA networks. Based on LoRa® RF Technology, it provides ultra-long range spread spectrum communication and high interference immunity.

Thanks to its small LGA form factor (11.3 x 8.9 mm only) and its low current consumption, this module allows the implementation of highly integrated low power (battery operated) solutions for Internet of Things (IoT) applications, security systems, sensor networks, metering, smart buildings, agriculture, supply chain.

The 32001552xUS family features a dual core microcontroller in which one is dedicated to the radio stack and the ARM Cortex M4 is free for the customer application firmware.

It also includes a Secure Element chip to store root of trust, sensitive data, keys, certificates …

The available radio stacks support a wide range of applications as the wM-Bus standard (32001552AUS), or accelerating the development of a LoRaWAN application (32001552BUS) using the LoRa modulation, or performing a local star network using the LoRa Mipot stack (32001552CUS). Using the LoRa Modem stack (32001552DUS), it is easy to create point-to-point applications or build a more complex custom stack. The 32001552FUS contains all the forementioned stack allowing to switch between them at runtime.

Contents

1. Product Features

Mechanical highlights:

- ✓ Extremely compact dimensions
- ✓ LGA pattern

Low power characteristics:

- ✓ Sleep current consumption 2.2 µA
- ✓ 11 mA in RX mode

Memories:

- ✓ 196 kB Flash memory
- ✓ 32 kB RAM
- ✓ 512 B OTP (One Time Programmable) memory

RF performances:

- ✓ -135 dBm Sensitivity @LoRa®
- ✓ +20 dBm Output power

Additional features:

- ✓ ARM Cortex-M4 CPU
- ✓ Preloaded radio library
- ✓ Internal communication channel with the radio peripheral
- ✓ Based on STM32WL55J

Multiple Stacks available:

- ✓ wM-Bus (32001552AUS)
- ✓ LoRaWAN (32001552BUS)
- ✓ LoRa Mipot (32001552CUS)
- ✓ LoRa Modem (32001552DUS)
- ✓ LoRa Multistack (32001552FUS)

Emission designator:

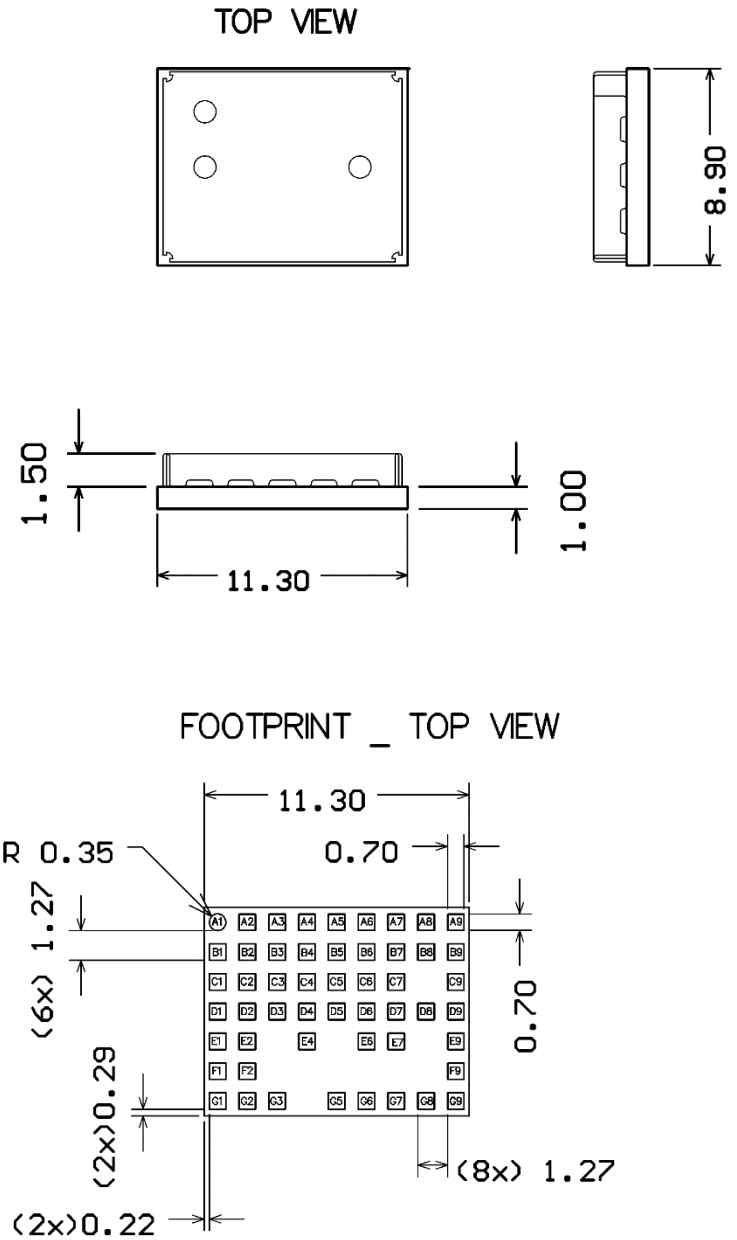
LoRa® DTS: 500KF1D

LoRa® FHSS: 125KFXD

Regulatory compliance:

- ✓ USA FCC Rules and Regulations CFR 47, Part 15, Subpart B (10-1-20 Edition)
- ✓ USA FCC Part 15.247 (10-1-20 Edition): Operation within the bands 902 - 928 MHz, 2400 -2483.5 MHz, and 5725 - 5850 MHz.
- ✓ USA FCC Part 15.209 (10-1-20 Edition): Radiated emission limits; general requirements.
- ✓ USA FCC 47 CFR Part 2.1091 Radiofrequency radiation exposure evaluation: mobile devices.
- ✓ ANSI C63.10-2013: American National Standard for Testing Unlicensed Wireless Devices.
- ✓ CANADA ICES-003 Issue 7 (October 2020)
- ✓ CANADA RSS-247 Issue 2 (February 2017).
- ✓ CANADA RSS-Gen Issue 5 amendment 1 (March 2019).
- ✓ CANADA ISED RSS-102 Issue 5 (2015-03) – Radio Frequency Exposure Compliance of Radiocommunication Apparatus (All Frequency Bands)

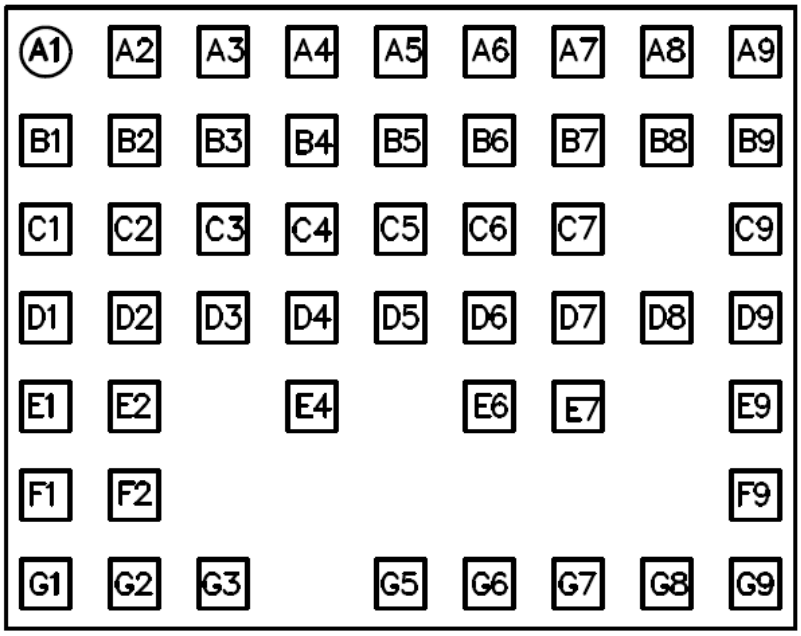
2. Mechanical Dimensions



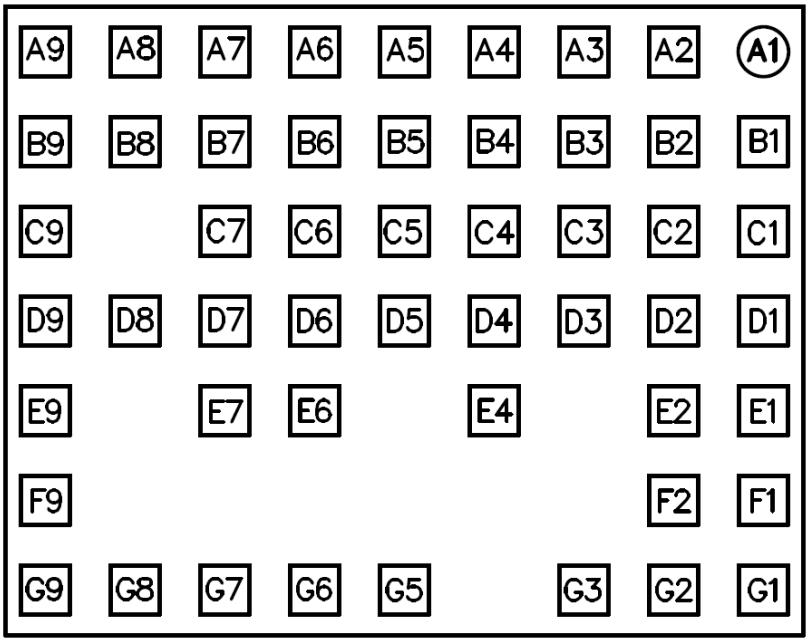
Note: Dimension in mm. General tolerance ±0.1mm. The tolerance is not cumulative.

3. Pin Definition

Top View



Bottom View



32001552DUS LGA PAD	STM32WL BGA BALL
A1	PA6
A2	PA5
A3	PA4
A4	PC0
A5	PC1
A6	PB5
A7	PB8
A8	PB9
A9	VDD
B1	PA7
B2	PC6
B3	PA2
B4	PA3
B5	PB6
B6	PB7
B7	PA15
B8	VDDA
B9	VDD
C1	PH3-BOOT0
C2	PA8
C3	PA1
C4	GND
C5	PA0
C6	PB4
C7	VREF+
C9	GND

32001552DUS LGA PAD	STM32WL BGA BALL
D1	GND
D2	PB10
D3	PB11
D4	GND
D5	PB14
D6	PA10
D7	VBAT
D8	PB13
D9	PC2
E1	GND
E2	GND
E4	PB1
E6	PB2
E7	PA12
E9	PC3
F1	ANT
F2	GND
F9	PB12
G1	GND
G2	GND
G3	GND
G5	NRST
G6	SWDIO
G7	SWCLK
G8	SWO
G9	PA9

4. Firmware development

4.1. Overview

The 32001552xUS family module is based on the STM32WL55J and embeds the necessary circuitry for the RF subsystem in the 868 MHz band. The MCU employs an asymmetrical dual core CPU comprised of an ARM Cortex-M4 and an ARM Cortex-M0+.

The Cortex-M0+ core is reserved for the RF stack while the user code runs on the Cortex-M4. The communication between the cores is done using the Inter-Processor Communication Controller (IPCC).

The RF stack is preloaded in the module and uses the same set of commands of the host based version.

For details about the MCU, please refer to STM32WL55J data sheet (DS13293) and reference manual (RM0453).

4.2. Memory organization

The memory available for the user code depend on the model because of different memory requirements of the different stacks, and is shown in the following tables.

4.2.1. Available memory for 32001552AUS

Start address	End Address	Length	Description
0x0800 0000	0x08031FFF	204800	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

4.2.2. Available memory for 32001552BUS

Start address	End Address	Length	Description
0x0800 0000	0x08029FFF	172032	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

4.2.3. Available memory for 32001552CUS

Start address	End Address	Length	Description
0x0800 0000	0x0802C7FF	182272	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

4.2.4. Available memory for 32001552DUS

Start address	End Address	Length	Description
0x0800 0000	0x0802 FFFF	196608	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

4.2.5. Available memory for 32001552FUS

Start address	End Address	Length	Description
0x0800 0000	0x08021FFF	139264	User Flash Memory
0x2000 0000	0x2000 7FFF	32768	User RAM
0x2000 8000	0x2000 83FF	1024	IPCC RAM
0x1FFF 7200	0x1FFF 73FF	512	User OTP Memory

4.3. Reserved Pins

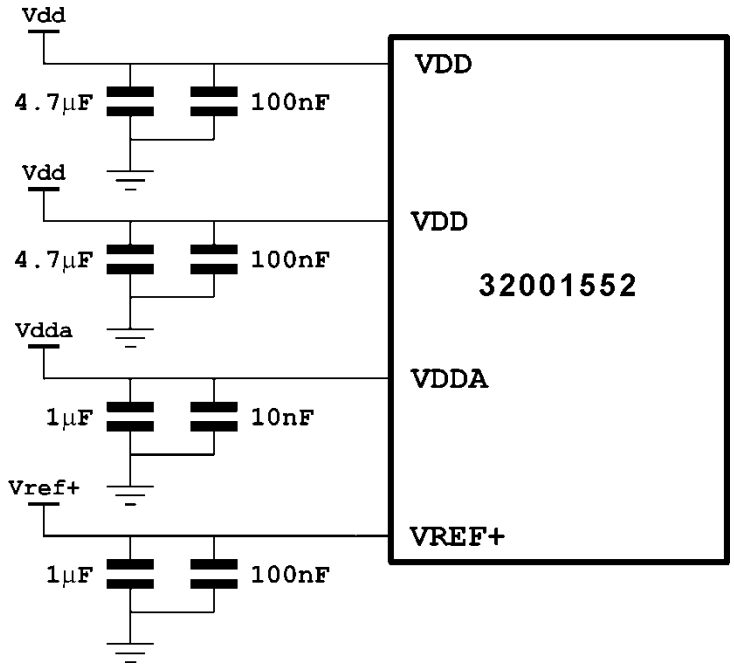
Some Pins of the STM32WL55J are reserved for internal use, so those are not available for the user application and must be not modified in any way.

- PA11
- PB0
- PC4
- PC5
- PC13
- PC15

5. Hardware integration

5.1. Decoupling capacitors

Each power supply pin must be decoupled with capacitors with the values suggested in the figure.



5.2. Layout guidelines

For better noise rejection, put the decoupling capacitors as close as possible to the power pins of the module, giving precedence to the low value ones.

The trace connecting to the RF pin must have an impedance of 50 Ω. For better performance, connect the GND pads around the RF pin without thermals.

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Parameter	Max.	Unit
Supply Voltage (VDD)	3.9	V
Radio Frequency Input Level, pin F1	0	dBm
Voltage Standing Wave Radio (VSWR) at RF Input, ANT, pad F1	10:1	
I/O Pin voltage	VDD + 0.3	V
Storage Temperature	-40 ÷ 100	°C
Operating Temperature	-40 ÷ 85	°C

6.2. Operating Condition

Note: All RF parameters measured with input (pad F1, ANT) connected to a 50 Ω impedance signal source or load.

6.2.1. GENERAL ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
Supply Voltage (VDD)	1.9	3.0	3.6	V	
VDDA	0	-	3.6	V	
VBAT	1.55	-	3.6	V	
VIN	-0.3	-	VDD+0.3	V	
Sleep DC Current	-	2.2	3.0	µA	
Data Rate 2-FSK	-	-	48	kbit/s	
Data Rate LoRa®	0.98	-	21.9	kbit/s	

6.2.2. RECEIVER ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
DC Current Drain	-	-	11	mA	6
Operating Frequency	902.0	-	928.0	MHz	
Channel Frequency Precision	-	±15	-	kHz	
Sensitivity, 2-FSK	-	-115	-	dBm	2,3,5
Sensitivity, LoRa®	-	-135	-	dBm	2,4,5
Spurious radiated level	-	-	-57	dBm	
Output Logic Low	GND	-	0.05	V	
Output Logic High	VDD - 0.2	-	VDD	V	

6.2.3. TRANSMITTER ELECTRICAL CHARACTERISTICS @ 25 °C

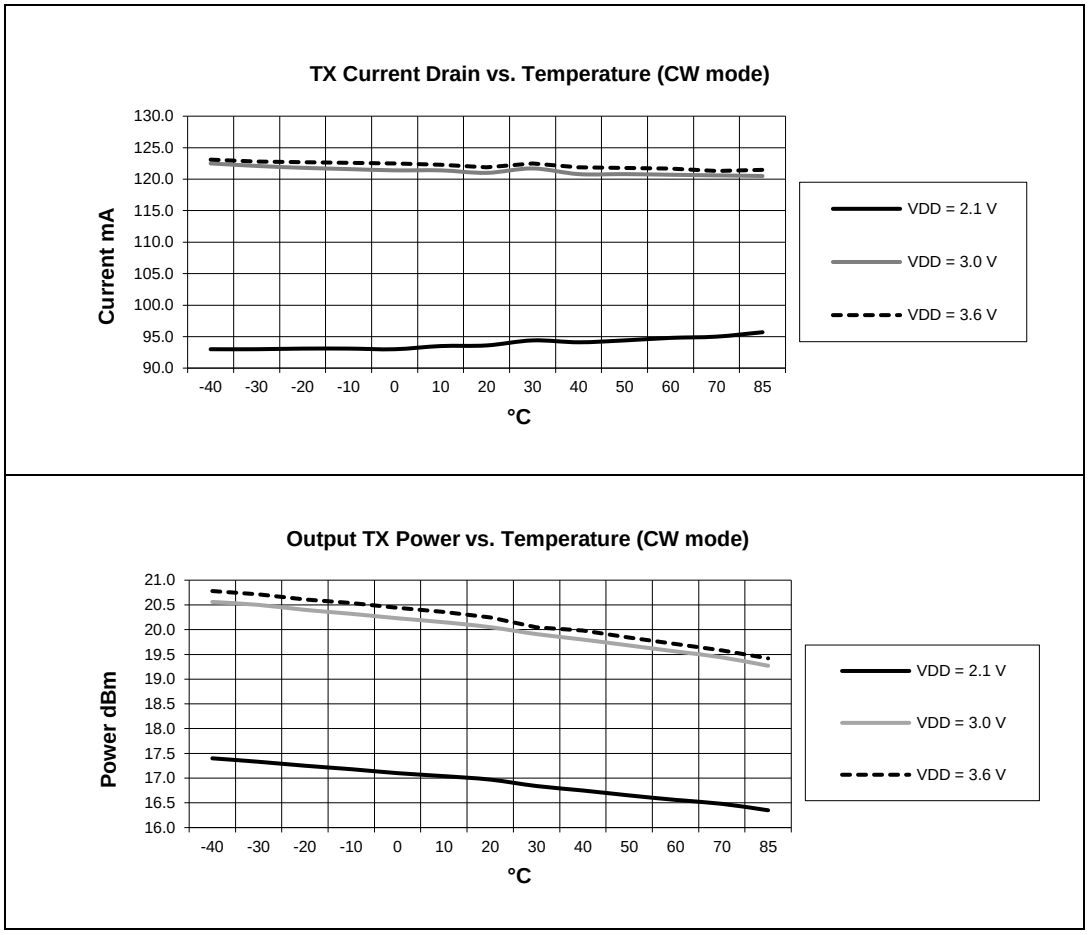
Parameter	Min.	Typ.	Max.	Unit	Notes
Current Drain (CW @20 dBm)	-	138	-	mA	1,2
Operating frequency	902.0	-	928.0	MHz	
Occupied Bandwidth LoRa® DTS	500	-	-	kHz	
Occupied Bandwidth LoRa® FHSS	-	125	-	kHz	8
Operating Channel Width LoRa®	-	600	-	kHz	
Operating Channel Width LoRa® FHSS	-	200	-	kHz	8
Maximum Output power (50 Ω load)	-	20	-	dBm	1,2,7
RF Output Impedance	-	50	-	Ω	
Input Logic Low	GND	-	0.05	V	
Input Logic High	VDD - 0.2	-	VDD	V	

Notes:

1) VDD = 3.6 V.
2) All RF parameters measured with input (pin F1, ANT) connected to 50 Ω impedance signal source or load.
3) Pseudo random code NRZ, 2-FSK BER (bit error rate) = 0.1 % or better, 2-level FSK modulation without pre-filtering, Bit Rate = 4.8 kbit/s, frequency deviation = 5 kHz, filter bandwidth = 20 kHz.
4) LoRa® PER (packet error rate) = 1 %, packet of 64 bytes, preamble of 8 bytes, error correction code CR = 4/5, CRC on payload enabled, no reduced encoding, no implicit header.
5) Sensitivities given using highest LNA gain step.
6) Power consumption measured with -140 dBm signal and AGC ON.
7) In order not to exceed the maximum power permitted by the FCC PART 15 regulation, choose an appropriate antenna system and power supply.
8) Single hop OBW and OCW.

7. Temperature Range Curves

Note: All RF parameters measured with input (pad F1) connected to a 50 Ω impedance signal source or load.



8. Exposure assessment

A conservative evaluation distance of 20 cm has been used to perform the assessment.

The Maximum Gain to meet FCC Radiofrequency radiation exposure limits is:

Technology/Mode	Band	Frequency (MHz)	Distance (cm)	FCC General Population Limit (mW/cm^2)	Maximum Gain to comply with RF Exposure Limits (dBi)
LoRa	ISM (USA)	902 - 928	20	0.60	16.10

9. Antenna details

To perform the assessments the following antenna has been used as reference:

Antenna model	2J0B15 – C885G		
Parameters	868/915 MHz ISM Antenna		
Standards	ZigBee, ISM, SIGFOX, LoRa		
Band (MHz)	868		915
Frequency (MHz)	863 - 870		902 – 928
Return Loss (dB)	~-7.8		-8.0
VSWR	2.4:1		2.4:1
Efficiency (%)	66.1		75.2
Peak Gain (dBi)	2.7		3.3
Average Gain (dB)	-1.8		-1.2
Impedance (Ω)		50	
Polarization		Linear	
Radiation Pattern		Omni-Directional	
Max. Input Power (W)		25	

10. Supporting documentation

Title	Description	Doc
Command Reference Manual	Description of commands for the wM-Bus stack	32001552AUS_Com_Ref
Command Reference Manual	Description of commands for the LoRaWAN stack	32001552BUS_Com_Ref
Command Reference Manual	Description of commands for the LoRa Mipot stack	32001552CUS_Com_Ref
Command Reference Manual	Description of commands for the LoRa Modem stack	32001552DUS_Com_Ref
Command Reference Manual	Description of commands for the multi-stack module	32001552FUS_Com_Ref
Manufacturing Process Information for LGA MiP Series Modules	Packaging information, Tape& Reel Specification, Reflow soldering information	AN_MNF002
STM32WL55J data sheet	Overview of the MCU and its peripherals	DS13293 (from ST)
STM32WL55J reference manual	Detailed description of the MCU and its peripherals	RM0453 (from ST)

11. Ordering Information

Title	Description	DoC
32001552AUS	MiP-Wm-2C256S-US	United States
32001552BUS	MiP-Lw-2C256S-US	United States
32001552CUS	MiP-LoMi-2C256S-US	United States
32001552DUS	MiP-LoMo-2C256S-US	United States
32001552FUS	MiP-LwMo-2C256S-US	United States

12. Regulatory Approvals

Models: 32001552AUS, 32001552BUS, 32001552CUS, 32001552DUS, 32001552FUS

U.S.

FCC ID: 2AQJP-MIP

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

CANADA

IC: 28566-MIP

HVIN: 32M01514

PMN:	32001552AUS, 32001552BUS, 32001552CUS, 32001552DUS, 32001552FUS	HVIN:	32M01514
HMN:	-	FVIN:	-

Doc	Title	Description
DoI	32001505BUS_DoI	Declaration of Identity

13. Revision History

Revision	Date	Description
0.0	07.06.2023	First emission
1.0	03.11.2023	Added regulatory approvals labels, exposure assessment and antenna details