2.4G Module

DKL 1908_V.1

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Applications

- RF Remote Control
- Interactive Wireless Toy and Game
- Wireless Audio/Video
- Wireless Consumer Electronics
- Wireless Keyboard Mouse
- Wireless Lighting Control

Introduction

The DKL 1908_V.1 is a 2.4 GHz Direct Sequence Spread Spectrum (DSSS) / Minimum-Shift Keying (MSK) RF transceiver with integrated baseband and MAC in a single chip. Targeting for the low cost and low power applications, the DKL 1908_V.1 is very suitable for toys, games, remote controller, wireless lighting control, PC peripherals and varieties of wireless consumer electronics.

The DKL 1908_V.1 supports multiple data rates of 125kbps DSSS, 250kbps DSSS, 1Mbps MSK, and 2Mbps MSK for flexible system design. With the integrated medium access controller (MAC), DKL 1908_V.1 can largely reduce the loading of the host MCU and also reduce the development effort and time, especially for the wireless applications having more complicated network topology and large network nodes. The DKL 1908_V.1 is packaged in 3x3 mm^2 leadless 16-pin QFN package.

Features

RF/Analog

- Worldwide 2.4GHz ISM band operation
- Meet RF spurious emission requirements for all markets in the world at maximum TX power
- RF receiver and transmitter share the same pin(s) for easily connecting to an external antenna
- Support both differential and single-end RF interface allow customers to select the best performance or the lowest external parts count
- Fully integrated PLL, VCO and loop filter
- Automatic RF frequency calibration for each channel to maximize frequency stability and accuracy due to process, temperature and supply voltage variation
- Integrated programmable load capacitors for crystal oscillator
- Digital frequency tuning to allow low cost/quality crystal to precisely tune the transmitted RF frequency
- TX ramping up/down minimizing RF spurious for each TX burst
- 16 or 12 pin QFN package, or 8 pin SSOP package (TBD)
- Support 125/250 Kbps date rate based on O/QPSK and DSS modulation
- Support 1/2 Mbps data rate based on MSK modulation
- -97 /-93dBm sensitivity @ 125K/250K (OQPSK-DSSS)
- -83/-80dBm sensitivity @ 1M/2M (MSK)
- 5 dBm maximum input level
- 11 dBm typical output power
- 11 to -3 dBm TX power control range in 2 dB step.
- -14 to -29 dBm TX power control range in 5 dB step.
- Typical 1% TX EVM for all RF power output
- 24 mA RX and 50 mA 11dBm output power TX mode.
- 1 uA at deep sleep mode
- 0.1 uA at power down mode

MAC/Baseband

- Automatic ACK with 2 byte programmable information
- **6 data pipes for 1:6 star networks**
- Trigger TX FIFO automatically after register wakeup
- Automatic FCS generation and FCS check
- Innovative and patented on-fly multi-rate detection
- 38-byte TX FIFO (Length: 1 byte, MAC header:5 bytes, payload:32 bytes)
- 40-byte RX FIFOs(Length: 1 byte, MAC header:5 bytes, payload:32 bytes, CRC:2 bytes)
- Various power saving modes
- 3-wire/4-wire SPI interface
- Support 4 Group ID
- Mixed network operation between 125 kbps and 1 Mbps date rates
- Mixed network operation between 250 kbps and 2 Mbps date rate

Table of Content

Abbreviations

ACK	Acknowledgement
ADC	Analog to Digital Converter
CCM	Counter Channel Mode
CRC	Cyclic Redundancy Check
DSSS	Direct Sequence Spread Spectrum
EMI	Electro Magnetic Interference
ESD	Electronic Static Discharge
EVM	Error Vector Magnitude
FCF	Frame Control Field
FCS	Frame Check Sequence
FIFO	First In First Out
INT	Interrupt
ISM	Industrial Scientific and Medical
ITU-T	International Telecommunication Union - Telecommunication
I/O	Input / Output
I/Q	In-phase / Quadrature-phase
Kbps	Kilo bit per second
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit / Byte
MSB	Most Significant Bit / Byte
MAC	Medium Access Control
NA	Not Available
NC	Not Connected
O-QPSK	Offset-Quadrature Phase Shift Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Locked Loop
QFN	Quad Flat No-lead Package
RF	Radio Frequency
RX	Receive
SPI	Serial Peripheral Interface
SFD	Start-of-Frame Delimiter
TBD	To Be Defined
TX	Transmit
VCO	Voltage Control Oscillator

Format Representations of Registers and Their Bits

1. REG0xnn[m] or REG0xnn[p:m]
   REG: register
   0xnn: register number
   nn: can be numerical numbers (for example:1, 2, or 3, etc) or alphabetical words (for example: A, B, or C, etc)
   [m]: the bit number
   [p:m]: bit m to bit p (for example: bit[7:5] means bit 7, bit 6, and bit 5)

1. Pin Configuration

1.1. Device Pin Assignments

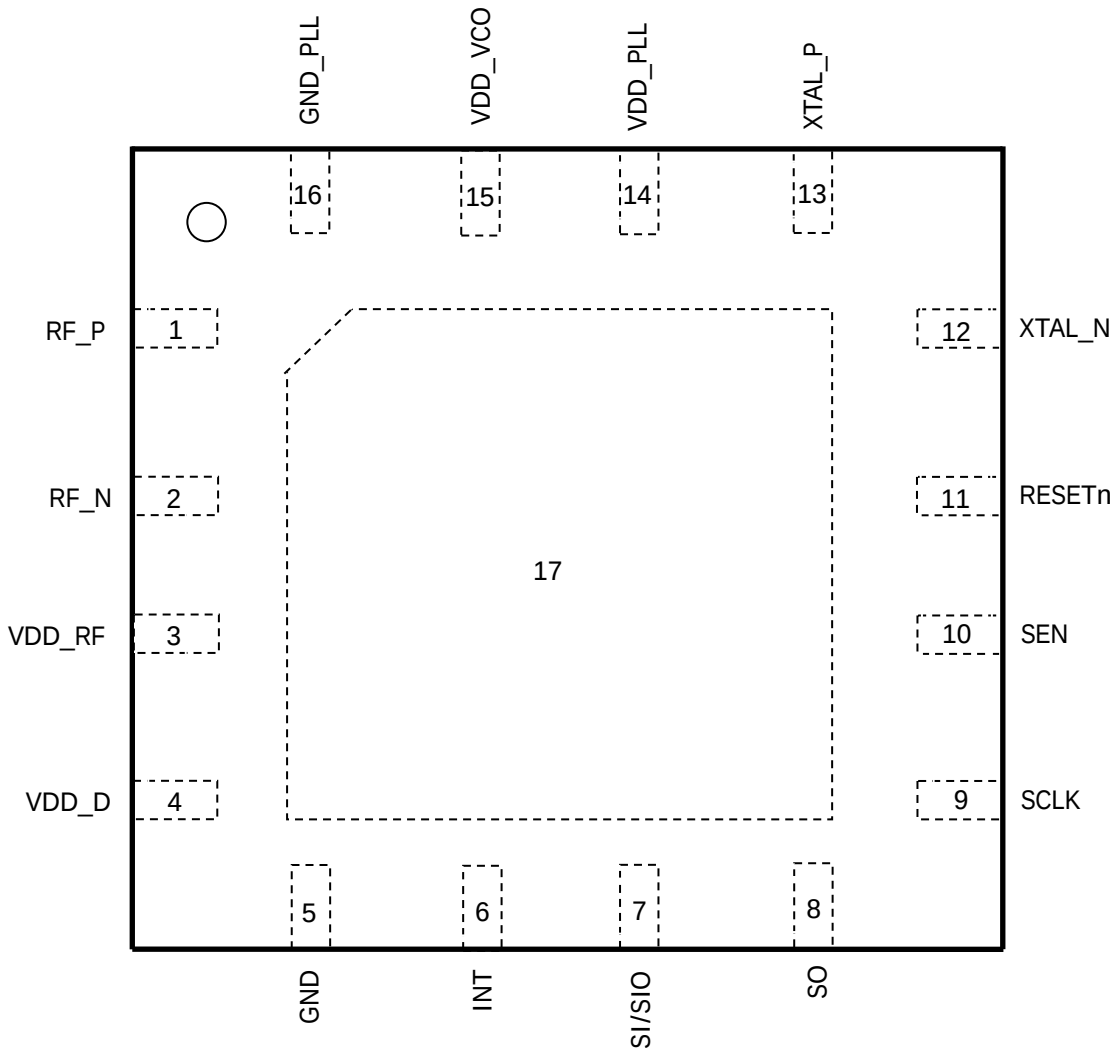


Figure 1. Pin Assignments (Top View)

1.2. Device Pin Descriptions

Pin type abbreviation: A = Analog, D = Digital, P = Power, I = Input, O = Output

Pin	Symbol	Type	Description
1	RF_P	AIO	Differential RF input/output (+)
2	RF_N	AIO	Differential RF input/output (-)
3	VDD_RF	PI	RF power supply (1)
4	VDD_D	PI	Digital circuit power supply
5	GND	Ground	Ground
6	INT	DO	Interrupt pin to the micro-processor
7	SI/SIO	DI/DIO	Serial interface data input (SI: 4 wire SPI mode, SIO: 3-wire SPI mode)
8	SO	DO	Serial interface data output
9	SCLK	DI	Serial interface Clock
10	SEN	DI	Serial interface enable
11	RESETn	DI	Global hardware reset pin, active low
12	XTAL_N	AI	16 MHz Crystal (-)
13	XTAL_P	AI	16 MHz Crystal (+) (input for an external clock if needed)
14	VDD_PLL	PI	RF power supply (1)
15	VDD_VCO	PI	VCO power supply
16	GND_PLL	Ground	Ground
17	IC Ground Pad	Ground	Backside ground plane. Must be connected to the ground.

Table 1. Pin Descriptions

* ***Caution***: ESD sensitive. Please refer to Section 2.5 for more information.

Note 1: Connecting bypass capacitor(s) to the pin as close as possible.

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameters	Min	Max	Unit
Storage temperature	-40	+120	℃
Supply voltage VDD pin to the ground	-0.5	+3.6	V
Voltage applied to inputs	-0.5	VDD+0.5	V
Short circuit duration, to GND, or VDD		5	sec

Table 2. Absolute Maximum Ratings

2.2. Recommended Operating Conditions

Test conditions: VDD = 3 V

Parameters	Min	Typ	Max	Units
Ambient Operating Temperature	-20		+85	℃
Supply Voltage for VDD	2.1	3		V
Logical high input voltage (for DI type pins)	0.85 x VDD			V
Logical low input voltage (for DI type pins)			0.2 x VDD	V

Table 3. Recommended Operating Conditions

2.3. DC Characteristics

Test conditions: T_A = 25°C, VDD = 3 V

Parameter	Test Conditions	Min	Typ	Max	Unit
ACTIVE: TX	At 11 dBm output power		50		mA
ACTIVE: RX	125K/1Mbps Mode		23		mA
	250K/2Mbps Modes		24		mA
STANDBY	Sleep clock remains active, RF/MAC/BB, system clock shutdown.		2		uA
DEEP SLEEP	Registers and FIFOs remain active. All the other powers are shutdown.		1		uA
POWER DOWN	Wake-up circuit remains active. All powers are shutdown. Register and FIFO data are not retained.		0.1		uA

2.4. ESD Characteristics

Human-body mode → All pins pass 2KV
Machine mode → All pins pass 200V

2.5. AC Characteristics

2.5.1. Receiver

Test conditions: TA = 25℃, VDD_IO = 3 V, LO frequency=2.445 GHz

Parameters	Test Conditions		Min	Typ	Max	Unit
RF frequency range	ISM band		2400		2483.5	MHz
	Recommended operating frequency range for band-edge limitation (for example: FCC/CE regulation)		2408		2475	MHz
RF sensitivity	At antenna input signal PER≦1% (for 20 bytes paodload)	125Kbps		-97		dBm
		250Kbps		-93		dBm
		1Mbps		-83		dBm
		2Mbps		-80		dBm
Maximum RF input	@250Kbps			5		dBm
Adjacent channel rejection	@+/-5 MHz, 250Kbps			20		dBc
Alternative channel rejection	@+/-10 MHz, 250Kbps			40		dBc

2.5.2. Transmitter

Test conditions: T_A = 25℃, VDD_IO = 3 V, LO frequency=2.445 GHz, 250 Kbps

Parameters	Test Conditions	Min	Typ	Max	Unit
RF frequency range	ISM band	2400		2483.5	MHz
	Recommended operating frequency range for band-edge limitation (for example: FCC/CE regulation)	2408		2475	MHz
Maximum RF output power			11		dBm
Programmable output power range 1	In 2 dB step	-3		11	dB
Programmable output power range 2	In 5 dB step	-29		-14	dB
TX EVM for O-QPSK 125 / 250 Kbps modes			1		%

2.5.3. Synthesizer

Test conditions: T_A = 25℃, VDD = 3 V, LO frequency=2.445 GHz, 250 Kbps

Parameters	Test Conditions	Min	Typ	Max	Unit
PLL reference clock frequency			16		MHz
RF channel resolution			1		MHz
PLL settling time			40		us

2.6. Power-on and External Reset Characteristics

The DKL 1908_V.1 has built-in power-on reset (POR) circuit which automatically resets all digital registers when the power is turned on. For stabilization of the complete circuit after the power-on reset, it is highly recommended to wait at least 3ms before starting the normal operation of the DKL 1908_V.1.

For external hardware reset (warm start), external reset pin RESETn is internally pulled high. The DKL 1908_V.1 will hold in reset state for around 20 us after RESETn is released from the low state.

2.7. Crystal Parameter Specifications

The requirements of the crystal used by the 16 MHz crystal oscillator of DKL 1908_V.1 are listed in the table below.

Parameter	Min	Typ	Max	Unit
Crystal Frequency		16		MHz
Frequency Error	-40		40	ppm
*Integrated Crystal Load Capacitance REG0x17[7:6]		16	24	pF
*Crystal stable Time		1.6		msec

Table 4. Requirements for 16 MHz Crystal

*Notes: Different crystal vendor have different load capacitance requirement. DKL 1908_V.1 integrates those two capacitors which are programmable in three values: 16, 20 and 24 pF. If larger capacitor than 24 pF is needed, the extra capacitors (Figure 17-1 and Figure 17-2) can soldered to the crystal connection pins(PIN12 and PIN13). A bigger capacitor value results a bigger crystal oscillator's stable time. The stable time is the time from the crystal oscillator is applied the supply voltage to the time which the receiver is able to receive a packet or the transmitter is able to transmit a packet.

3. Functional Description

The DKL 1908_V.1 is composed of the following five blocks:

- PHY
- MAC
- Memory
- Power Management
- Interface

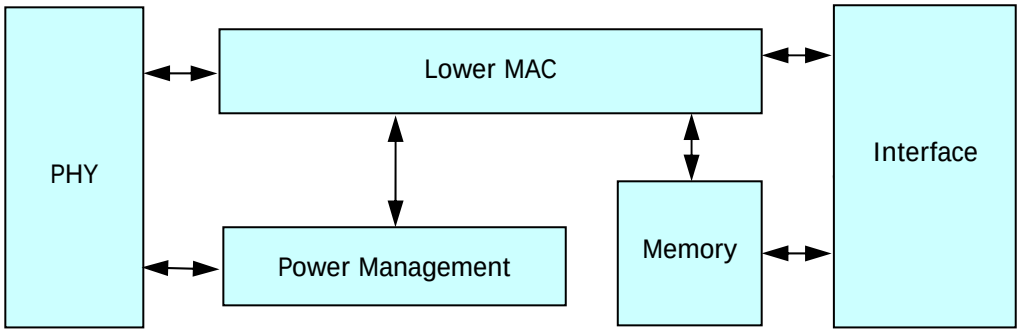


Figure 2. Block Diagram of DKL 1908_V.1

3.1. PHY

The architecture of PHY is shown in Figure 3.

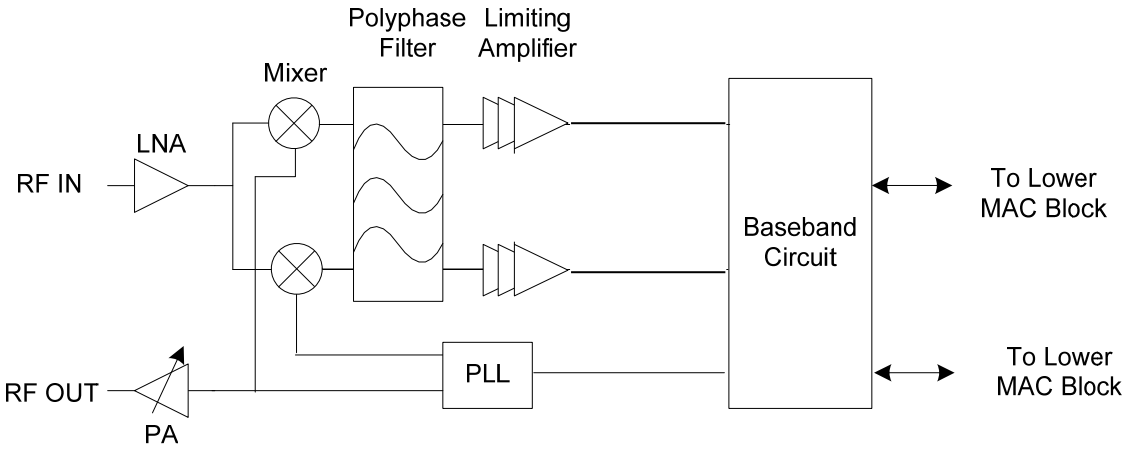


Figure 3. PHY Architecture

The key features of the DKL 1908_V.1 PHY are:

- RF frequency ranges from 2400 to 2483.5 MHz with 1MHz programmable resolution.
- Offset QPSK (O-QPSK) modulation with DSSS : 125kbps and 250kbps.
- Minimum-Shift Keying (MSK) : 1Mbps, and 2 Mbps
- Innovative and patented on-fly multi-rate detection

For all MSK modes, 4:32 spreading codes of DSSS are used for PHY header including preamble, SFD and Frame Length (FL) but no spreading codes are used for the PHY payload data. The transmission rate of the un-spreading PHY payload data bits is 8 times of PHY header. Thus the data rate of MSK modes is 8 times than OQPSK-DSSS modes.

The 125Kbps OQPSK-DSSS mode and the 1Mbps MSK mode have the same chip rate 1Mcps and occupy an RF channel bandwidth of 1MHz.The 250kbps OQPSK-DSSS mode and the 2Mbps MSK mode have the same chip rate 2Mcps and occupy an RF channel bandwidth of 2MHz.
The DKL 1908_V.1 PHY provides on-fly multi-rate detection function. The DKL 1908_V.1 PHY provides on-fly multi-rate detection function to permit multi-rate transmission and on fly detection of transmission rate. The DKL 1908_V.1 PHY comprises the transmitter configured to set a predetermined bit in the PHY header of the transmission frame to indicate whether the transmission frame is encoded by OQPSK-DSSS encoding mode or by MSK encoding mode and the receiver configured to decode the received transmission frame according to whether the predetermined bit in the PHR of the received transmission frame indicates the received transmission frame is encoded by OQPSK-DSSS encoding mode or by MSK encoding mode. The 8th digit bit of the frame length is used to identify which modulation is used in PHY payload data. By detecting whether the 8th digit bit of the frame length is a 0 or a 1 on the fly, the receiver distinguishes between the OQPSK-DSSS mode and the MSK mode and determines whether 4:32 spreading codes of DSSS is being used without predefining which mode is used.

The packet includes a 6-byte PHY header and a 8-39-byte PHY payload. The 6-byte PHY header includes 4 bytes of preamble, 1 byte of SFD, and 1 byte of frame length. Preamble and SFD are used for receiver packet detection and synchronization. The FL field specifies the length of the PHY payload. The length is valid from 6 to 31 bytes. The 8th bit of FL field is used for indicating OQPSK-DSSS mode when the 8th bit is a 0, and MSK mode when the 8th bit is a 1. The frame format is as below:

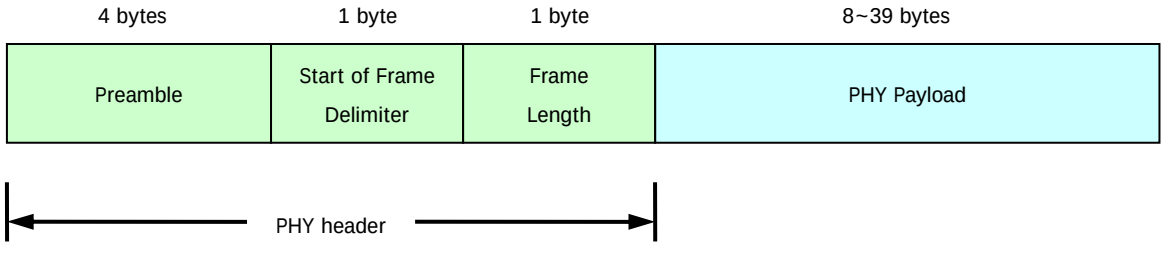
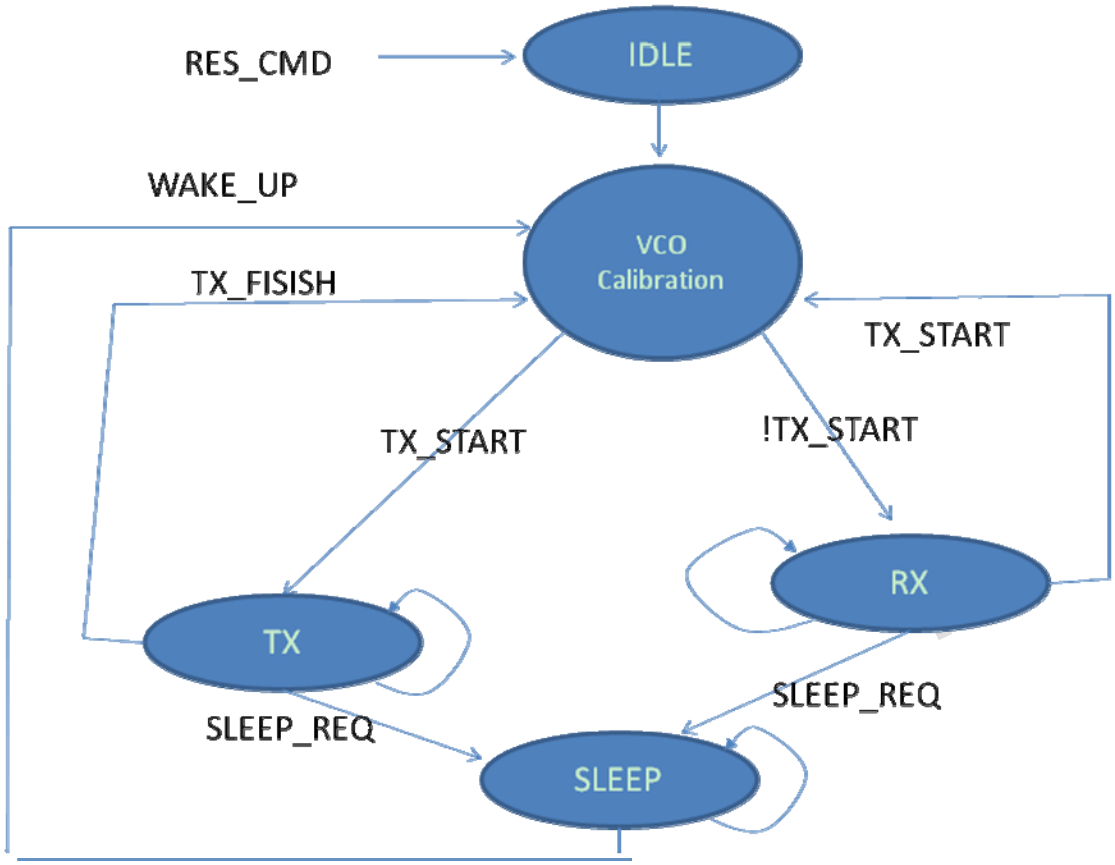


Figure 4. PHY Layer Frame Format

3.1.1. State Machine Control



Radio state diagram

RES_CMD: External reset pin or SW reset (REG0x34[0]) or REG0x36[2]
TX_START: TXFIFO trigger REG0x1B[0]
SLEEP_REQ: REG0x35[7]
WAKE_UP: External pin wake-up or timed wake-up or wake-up by register REG0x22[6]

DKL 1908_V.1 has five radio states designated IDLE, VCO calibration, TX, RX and SLEEP as above Figure. The response times between theses states are listed in the table below. In IDLE state, RF circuit is shutdown. MAC/BB, system clock and the sleep clock remain active. External reset pin or SW reset (REG0x34[0]) or REG0x36[2] can force DKL 1908_V.1 to IDLE state. After the initialization, DKL 1908_V.1 will enter RX state. The host processor can set the TX_START commands over the SPI interface to go to TX state. In TX state, DKL 1908_V.1 transmits the packet in TX FIFO. After transmission of the packet, DKL 1908_V.1 enters VCO calibration state and then RX state. The host processor can set the SLEEP_REQ command to let DKL 1908_V.1 in SLEEP state. In SLEEP state, DKL 1908_V.1 can be power saving mode STANBY, DEEP_SLEEP and POWER_DOWN. Detailed descriptions are available in Section 3.4.3.

Chip Mode	Response Time to		Unit
	RX	TX	
TX	144	N / A	u sec
RX	N / A	192	u sec
STANDBY	1600	*	u sec
DEEP SLEEP	1600	*	u sec
POWER DOWN	1600 + Initialization Time	*	u sec

* DKL 1908_V.1 will enter RX mode after wake up from each SLEEP modes.

3.2. MAC

The DKL 1908_V.1 MAC provides plenty of hardware-assisted features to relieve the loadings of the host MCU. Not only providing the reliable wireless packet communication between two nodes, it also handles data and command transfer between the network layer and the physical layer automatically.

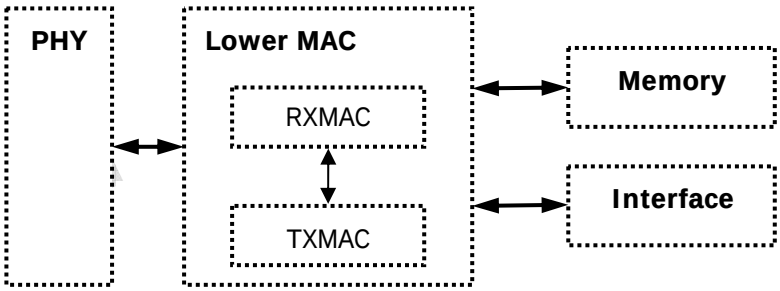


Figure 5. MAC Block Diagram

3.2.1. MAC Frame Format

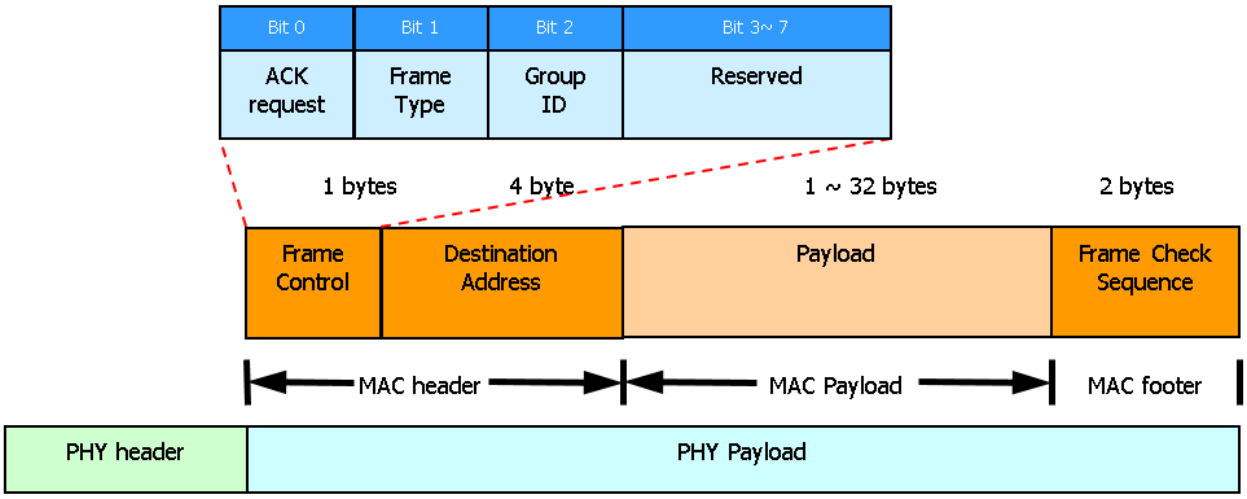


Figure 6. MAC Frame Format

The MAC frame format is composed of a frame control field (FC), a destination address field, a payload field and a frame check sequence field. The frame control field (FC) is one byte in length and contains ACK request (bit0), frame type (bit1) and group ID (bit2). The bit 0 of frame control (FC) field is used for Ack-Request which specifies whether an acknowledgement is required from the recipient device. If the bit is '1', the recipient device shall send an acknowledgement frame back after determining that the received frame is valid. The bit 1 of FC field is '0' for data frame. The bit 2 of frame control (FC) field is used for group ID. If the bit is '1', the recipient device shall check whether the MSB byte (bit 32~ bit 25) of destination address field is matched to group ID or not. There are four group IDs supported in REG0x1c, REG0x1d, REG0x1e and REG0x1f. The matched status of group ID is reported to REG0x30[3:0]. For example, if the bit 2 of frame control (FC) field is '1'. And the MSB byte (bit 32~ bit 25) of destination address field is matched to group 0 ID (REG0x1c). The bit 0 of RX status register (REG0x30) shall be reported to '1'. The destination address field contains the broadcast address (0xffff-ffff) or destination address. The length of payload field is variable from 1 to 32 bytes. The frame check sequence (FCS) is calculated over the address field, FC field and the payload. The polynomial is degree 16:

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1$$

Acknowledgement Frame

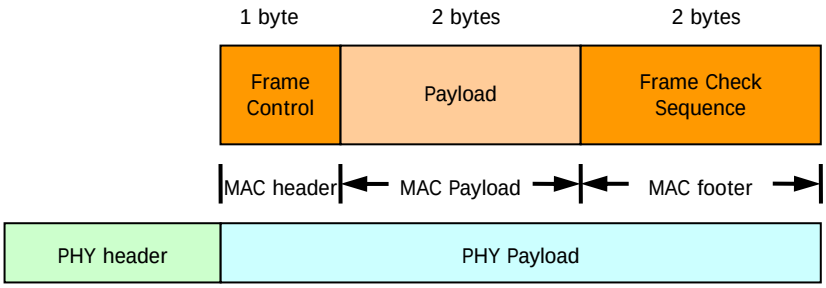


Figure 7. Acknowledgement Frame Format

The length of acknowledgement frame is always 5 bytes. Bit 1 of FC field is '1' for ACK frame. The payload field, containing user information of acknowledgement frame, can be configured by REG0x03 and REG0x04. The FCS is calculated over the FCS of the received packet, FC field and the payload field. The polynomial is degree 16:

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1$$

3.2.2. Destination address

The destination address is 4-byte address for the receiver. An address ensures that the packet is detected by the target receiver. The RX device can open up to six data pipes to support up to six TX devices with unique addresses. All six TX device addresses are searched simultaneously. In RX side, the data pipes are enabled with the bits in the PIPEN(REG0x01) register.

By default only data pipe 0 and 1 are enabled. Each pipe can have up to 4 bytes configurable address. Data pipe 0 has a unique 4 byte address. Data pipes 1-5 share the 3 most significant address bytes. The LSB byte must be unique for all 6 pipes.

3.2.3. TXMAC

When the TXFIFO is triggered, the TXMAC gets the data from TXFIFO to generate a 16-bit FCS and sends the packet to the PHY layer of the TX immediately. TXMAC can also handle the retransmission when the acknowledgement packet is not received. The block diagram of the TXMAC is shown in Figure 8 below.

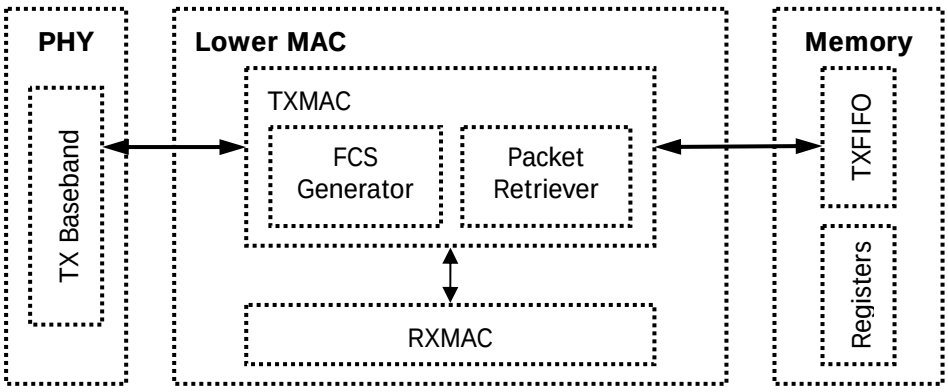


Figure 8. TXMAC Block Diagram

3.2.4. RXMAC

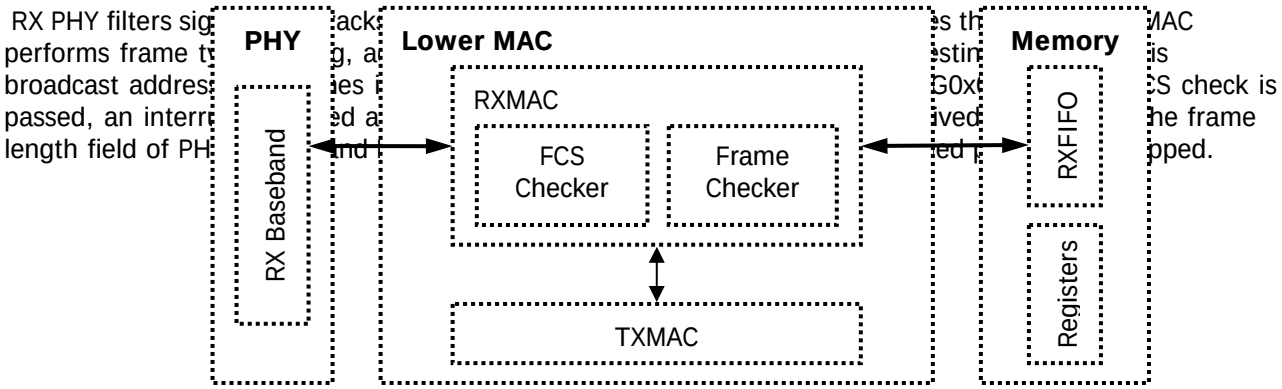


Figure 9. RXMAC Block Diagram

The contents of the RXFIFO can be flushed only by the following four ways: (1) the MCU host reads length field of RXFIFO and the last byte of the packet, (2) the host issues an RX flush, (3) the lifetime of the packet reaches the limitation of RX FIFO time-to-live (TTL) and (4) the software reset by REG0x34[0]. Note that RXFIFO is ready to receive next packet and all the data in RFIFO will be overwritten after RXFIFO flushed.

DKL 1908_V.1 provides the function of RX FIFO time-to-live (TTL). If the packet has been in RX FIFO too long time and more than the duration of some slow clock cycles specified in REG0x2B[7:6], the packet should be discarded and RXFIFO is flushed, too.

3.2.5. Auto Acknowledgement

The RXMAC supports automatically acknowledgement. If and only if the packet is successfully received and an Ack-Request bit, Bit 0, in the FC field of the received packet is set, RXMAC informs TXMAC to send an acknowledgement packet automatically. User should write the FC field correctly into the TX FIFO.

If an acknowledgement is requested and the replied ACK frame is not received, the transmitter automatically resends the packet until the maximum retransmission times, specified in REG0x1B[7:4], are reached. To utilize the function properly, the corresponding registers of both transmitting and receiving sides need to be set correctly.

Auto-retransmission on TX Side

To automatically retransmit a packet when an ACK is not received, REG0x1B[2] is required to be set to '1'.

Auto-acknowledgement on RX Side

To automatically reply an ACK packet when Ack-Request bit is set to '1', REG0x00[5] should be set to '0'.

3.3. Memory

The memory block of the DKL 1908_V.1 is implemented by the SRAM. It is composed of registers and FIFOs, which can be accessed by the SPI interfaces.

Figure 10. Memory Space Diagram

- Registers: 0x00~0x3F (support R/W during sleep)
- TXFIFO: page0 : 0x41~0x67 (support R/W during sleep)
- RXFIFO: page1 : 0x40~0x68

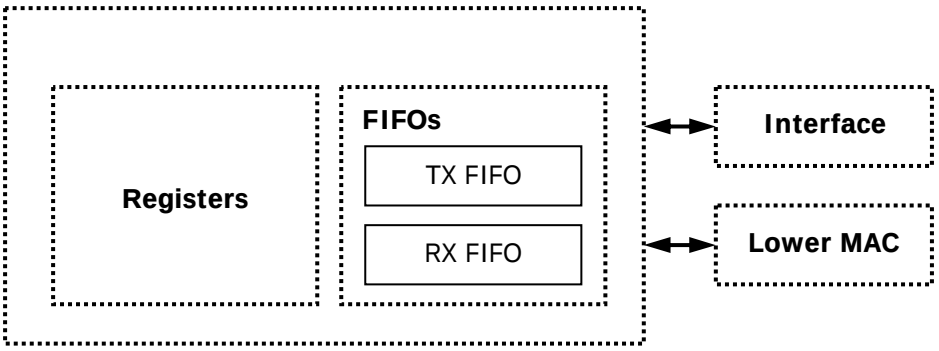


Figure 11. Memory Block Diagram

3.3.1. Registers

Registers provide control bits and status flags for the DKL 1908_V.1 operations, including transmission, reception, interrupt control, MAC/baseband/RF parameter settings ...etc.

3.3.2. FIFOs

TXFIFO

The TXMAC gets the to-be transmitted data from the 38-byte TXFIFO. The memory space of TXFIFO is from '0x041' to '0x67' of page 0 and contains a FL field, address field, FC field and payload field. The FL field indicat0xes the length of the address field, FC field and the payload field. The valid value of frame length is from 6 to 37 bytes. The value of the FL field of PHY header is calculated by adding the above mentioned value and the length of FCS field of MAC frame, i.e. 2, up. Below figure shows the TXFIFO format.

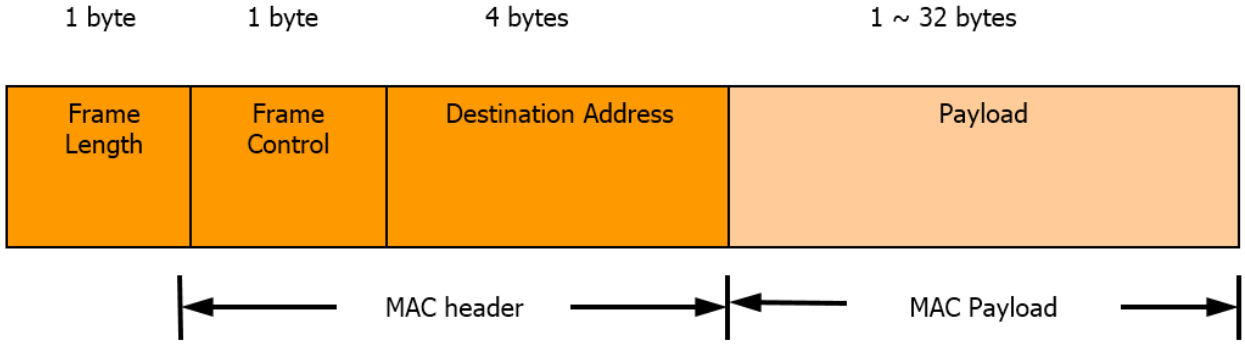


Figure 12. TXFIFO Format

RXFIFO

A RXFIFO is composed of a 40-byte FIFO to store the incoming packet. Each of them is designed to store one packet at a time. RXFIFO contains a FL field, address field, FC field, payload field and FCS field. The memory space of RXFIFO is from '0x40' to '0x68' of page 1. The FL field, which is extracted from the PHY header, indicates the length of the address field, FC field, the payload field and FCS field. The valid value of frame length is from 8 to 39 bytes. Figure 13 shows the RXFIFO format.

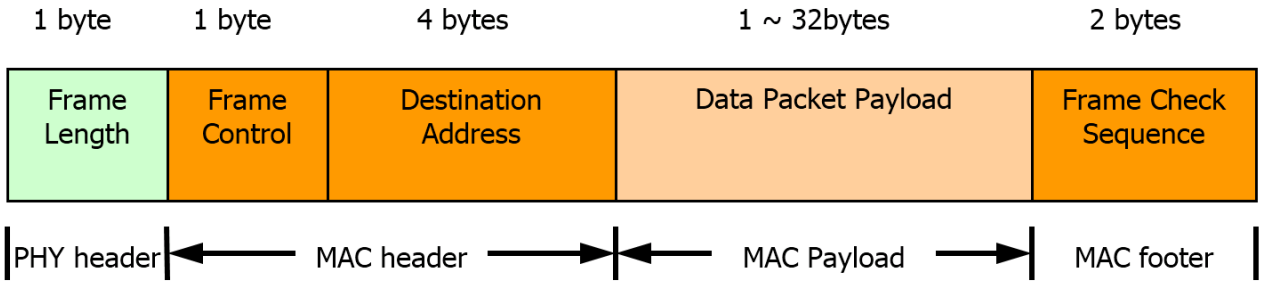


Figure 13. RXFIFO Format

3.4. Power Management

Almost all wireless sensor network applications require low-power consumption to lengthen battery life. Typical battery-powered device is required to be operated over years without replacing its battery. The DKL 1908_V.1 achieves low active current consumption of both the digital and the RF/analog circuits by controlling the supply voltage and using low-power architecture.

The DKL 1908_V.1 has four power saving modes that will be further described in Section 3.4.4. For ultra low-power operation, power-down mode is available which consumes around 1uA. All data stored in registers and FIFOs will be lost under power-down mode. In this mode, The DKL 1908_V.1 is able to wake up by an external reset (RESETn Pin11) signal. Except power-down mode, the data in the registers/FIFOs are retained during the other power saving modes.

3.4.1. Power Supply Scheme

The table below lists the recommended values of the external bypass capacitors for each power pin of the DKL 1908_V.1. For pin 3 and pin 4, an extra bypass capacitor is needed for the decoupling purpose while the rest of the power pins require only one bypass capacitor. The path length between the bypass capacitors to each pin should be as short as possible.

Pin	Symbol	Bypass Capacitor
3	VDD_RF	0.1 uF
4	VDD_D	

Table 5. Recommended External Bypass Capacitors

3.4.2. Power Saving Modes

Four power saving modes are supported by DKL 1908_V.1:

- STANDBY: RF/MAC/BB shutdown with the sleep clock and 16MHz clock remain active.
- DEEP_SLEEP: All powers are shutdown except the power to the digital circuits and register and FIFO data are retained.
- POWER_DOWN: All powers are shutdown. Register and FIFO data are not retained. An external reset signal is needed to wake up DKL 1908_V.1.

The difference between STANDBY mode and DEEP SLEEP mode is the power status of the sleep clock. To wake up DKL 1908_V.1, the host MCU has to control the time of sleep process.

The power management control is used for the low power operation of MAC and baseband modules. It manages to turn on and off the 16 MHz clock when the IC goes into power saving mode. By turning off the 16 MHz clock, the MAC and baseband circuits become inactive regardless whether their power supplies exist or not. All the digital modules are clock-gated automatically. That means only when a module is functioning, its clock would then be turned on. This approach efficiently decreases certain amount of the current consumption.

3.5. Interface

3.5.1. SPI

The slave SPI is supported for host MCU to read/write the control registers and FIFO of the DKL 1908_V.1. The features are as below:

- A simple 3-wire slave SPI (SIO, SCLK and SEN).
- A simple 4-wire slave SPI (SO, SI, SCLK and SEN)
- Most significant bit (MSB) of all addresses and data transfers on the SPI is done first.

SPI Addressing Format

Bit 0 is a one-bit read/write indicator. The other bits, from bit 7 to bit 1, indicate the SPI address.

Addressing Format	Bit 7 ~ 1	Bit 0
	0x00 ~ 0x7F	Read: 0 Write: 1

Figure 14. SPI Addressing Format

3-wire slave SPI

REG0x23[7] can enable 3-wire slave SPI mode. If REG0x23[7] is '1', Pin 7 is SIO for data input and output. Figure 16 shows the timing diagram of 3-wire slave SPI.

SPI Characteristics

Parameter	Symbol	Min	Max	Units	Conditions
SCLK, clock frequency	F_{SCLK}		5	MHz	
SCLK low pulse duration	t_{CL}	100		ns	The minimum time SCLK must be low.
SCLK high pulse duration	t_{CH}	100		ns	The minimum time SCLK must be high.
SEN setup time	t_{SP}	100		ns	The minimum time SEN must be low before the first positive edge of SCLK.
SEN hold time	t_{NS}	100		ns	The minimum time SEN must be held low after the last negative edge of SCLK.
SI setup	t_{SD}	25		ns	The minimum time data must be ready at SI, before the positive edge of SCLK
SI hold time	t_{HD}	25		ns	The minimum time data must be held at SI, after the positive edge of SCLK.
Rise time	t_{RISE}		25	ns	The maximum rise time for SCLK and SEN.
Fall time	t_{FALL}		25	ns	The maximum fall time for SCLK and SEN.

Table 6. SPI Characteristics

SPI Time Diagrams

Figure 15 and 16 shows the timing diagram for 4-wire slave SPI and 3-wire slave SPI respectively. SPI master will initiate a read or write operation by asserting SEN to low, toggling SCLK and sent the address field by SI. The SEN should be high when a transaction is completed.

The SPI burst mode is provided for the access on a continuous basis. If SEN does not go high after the 8-bit write data and the SCLK continuously toggles, the followed 8-bit write data is written to next address field. Same for the read access, the data of the next address will be read.

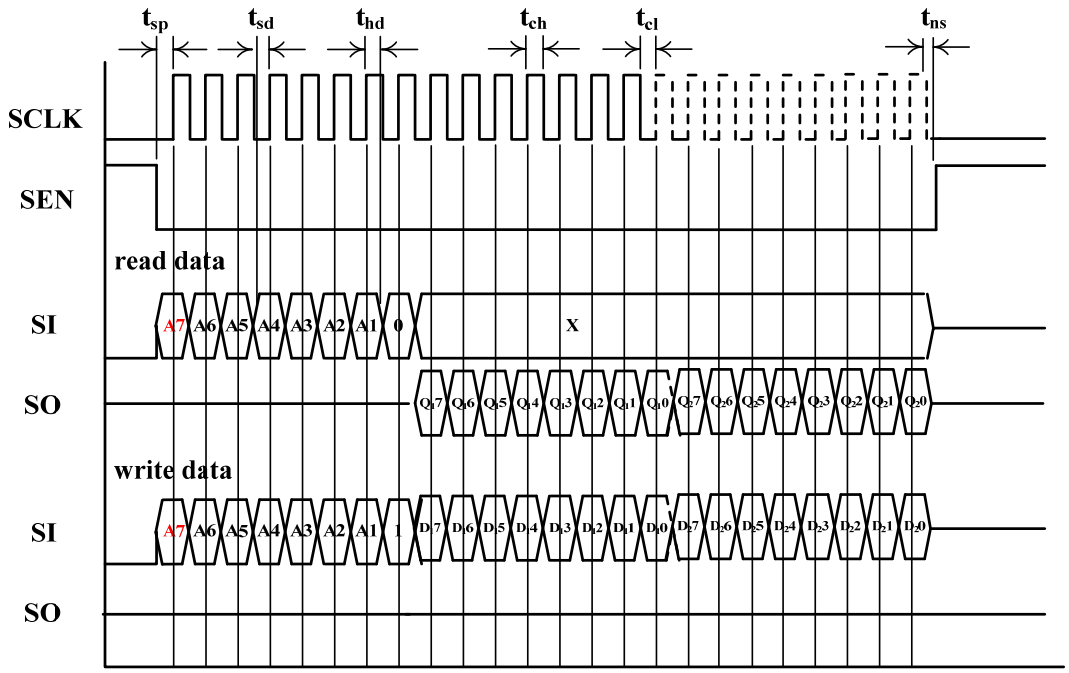


Figure 15. Timing Diagram of 4-wire slave SPI

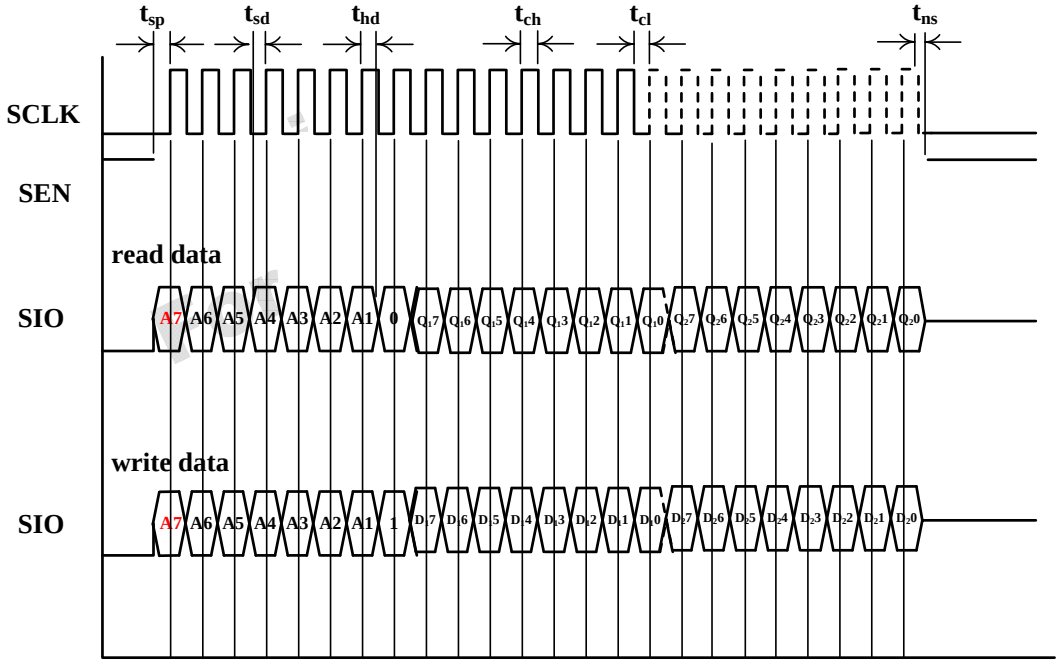


Figure 16. Timing Diagram of 3-wire slave SPI

3.5.2. Interrupt Signal

The DKL 1908_V.1 provides an output interrupt pin (pin 6, INT) with selectable polarity. The DKL 1908_V.1 issues interrupts to the host MCU on three possible events. For each event, the DKL 1908_V.1 sets the corresponding status bit in REG0x31. If the corresponding interrupt mask in REG0x32 is clear (i.e. equals '0'), an interrupt will be issued on pin 6. If it is set to '1' (masked), no interrupt will be issued, but the status is still present. Whenever REG0x31 is read, the interrupt and the status are cleared. The three interrupt events are described as below:

Wake-up alert interrupt (WAKEIF)

Every time a wake-up event happens, the DKL 1908_V.1 issues the interrupt event.

Packet received interrupt (RXIF)

This interrupt is issued when an available packet is received in the RXFIFO. An available packet means that it passes an RXMAC filter, which includes frame type identifying, address filtering and FCS check.

TX FIFO release interrupt (TXNIF)

This interrupt can be issued in two possible conditions. The conditions are when a packet in TXFIFO is triggered and sent successfully, or when a packet is triggered and the retransmission is timed out.

4. Application Guide

4.1. Initialization

After DKL 1908_V.1 is powered on, some registers need to be configured before the data transmitting or reception. The procedure is described as below.

DKL 1908_V.1 Initialization (4-wire SPI)*		
Register	Note	
do{Uz2472WriteReg(0x05,0x5c);} while((Uz2472ReadReg(0x05) & 0x5c) != 0x5c);	Wait power on stable.	
REG0x34=0x0F	Software reset for BB, MAC and register	
REG0x10=0x0A	Channel Setting for calibration (Initial setting Channel_2410 MHz)	
REG0x13=0x8C	VCO Settling Time	
REG0x14=0x02	VCO Settling Time	
REG0x16=0xFF	Power setting	Max. output power
REG0x37=0x02	RF setting	
REG0x38=0x82	Data Rate Select	250Kbps
REG0x14=0x06	RF optimized control	
REG0x36=0x20	RF optimized control	
REG0x37=0x12	RF optimized control	
	Wait 2mS	
REG0x12=0x6A	RF optimized control	
	Wait 8mS	
REG0x12=0x68	RF optimized control	
REG0x37=0x02	RF optimized control	
REG0x36=0x00	RF optimized control	
REG0x14=0x02	RF optimized control	
REG0x32=0x00	REG0x32=0x09 → Polling process for TX/RX REG0x32=0x00 → Interrupt process for TX/RX	

Initialization Option Items	
Register	Notes
REG0x0D=0x02	Disable TX trigger after register wakeup
REG0x00=0x40	MAC header format consistence with DKL 1908_V.1
REG0x17=0x01	Sleep mode is Deep Sleep mode

Different data rate setting as following table:

	Data rate			
Register	125K	1M	250K	2M
REG0x38	0x80	0x81	0x82	0x83
If change data rate after initialization, it must do following calibration procedure.				
REG0x14	0x06			
REG0x36	0x20			
REG0x37	0x12			
Wait 2mS				
REG0x12	0x6A			
Wait 8mS				
REG0x12	0x68			
REG0x37	0x02			
REG0x36	0x00			
REG0x14	0x02			

4.2. Change Channel

Set RF operation channel by configuring REG0x10. DKL 1908_V.1 will go to RX state after 192us.

4.3. RF Channel Fine Tuning

If precise channel frequency is required, DKL 1908_V.1 provides a digital frequency tuning which can achieve a frequency error less than 500 Hz via Register REG0x19[7:0]. The 8 bit register will changes both TX and RX RF frequency. Please note that the large the register value is, the less RF frequency becomes. If one wants to increase RF frequency with this feature, one can reduce the crystal load capacitor so that the RF frequency is greater than the desired one, and then, use this digital frequency tuning to reduce the RF frequency to the desired one.

4.4. Interrupt

The DKL 1908_V.1 issues a hardware interrupt at pin 6 to the host MCU. There are two related registers that need to be set correctly. All the interrupts are masked (disabled) by default. The interrupt mask should be removed by setting REG0x32 in advance. By default, the interrupt signal is sent to the host MCU as a falling edge after mask removed. The polarity can be configured by REG0x33[4]. The interrupt status can be read from REG0x31 when it is triggered.

4.5. TX

For TX operation, the TXMAC of DKL 1908_V.1 automatically generates the preamble, Start-of-Frame delimiter and the FCS. The host MCU needs to write all other frame fields into TXFIFO. To send a packet in TX FIFO, there are several steps to follow:

Step 1.
Fill necessary data in TXFIFO. The format of TXFIFO is as follows:

Step 2.
Set Ackreq by REG0x1B[2], if an acknowledgement / retransmission is required. The DKL 1908_V.1 automatically retransmits the packet till the number of the Max trial times specified in SREG1B[7:4] is reached, if there is no acknowledgement received.

Step 3.
By triggering REG0x1B[0], the TXMAC will send the packet immediately. This bit will be automatically cleared.

Step 4.
Wait for the interrupt status shown in REG0x31[0]. If retransmission is not required, REG0x31[0] indicates the packet is successfully transmitted.

Step 5.
Check REG0x24[0] to see if transmission is successful. REG0x24[0]=0 means transmission successful and the ACK was received. The number of times of the retransmission can be read at REG0x24[7:4]. REG0x24[0]=1 means transmission failed and ACK was not received.

4.6. RX

When a valid packet is received, an interrupt is issued at REG0x31[3]. The MCU host can read the whole packet inside the RXFIFO. The RXFIFO is flushed when the frame length field and the last byte of RXFIFO are read, or when the host triggers a RX flush by REG0x0D[0].

4.7. Power Saving

Standby, Deep-Sleep and Power-Down modes are designed for DKL 1908_V.1. It is only allowed to switch between power saving modes and active mode. The following settings are effective in active mode only.

STANDBY Mode:

Shutdown RF/MAC/BB, while the voltage regulator, partial 16 MHz clock and sleep clock remains active.

- Set REG0x17[1:0] to '00' to select for Standby mode

DEEP SLEEP Mode:

All power is shutdown except the power to the digital circuits and sleep clock. Register and FIFO are retained.

- Set REG0x17[1:0] to '01' to select for Deep Sleep mode

POWER DOWN Mode:

All power is shutdown. Register and FIFO data are not retained. Initialization is needed after DKL 1908_V.1 back to active mode. Set REG0x17[1:0] to '11' to select for Power Down mode

After the necessary settings mentioned above are configured, user can set REG0x35[7]=1 to place DKL 1908_V.1 to power saving mode. After set REG0x35[7]=1, the SEN Pin need to set to low (ground).

4.8. Wake-up

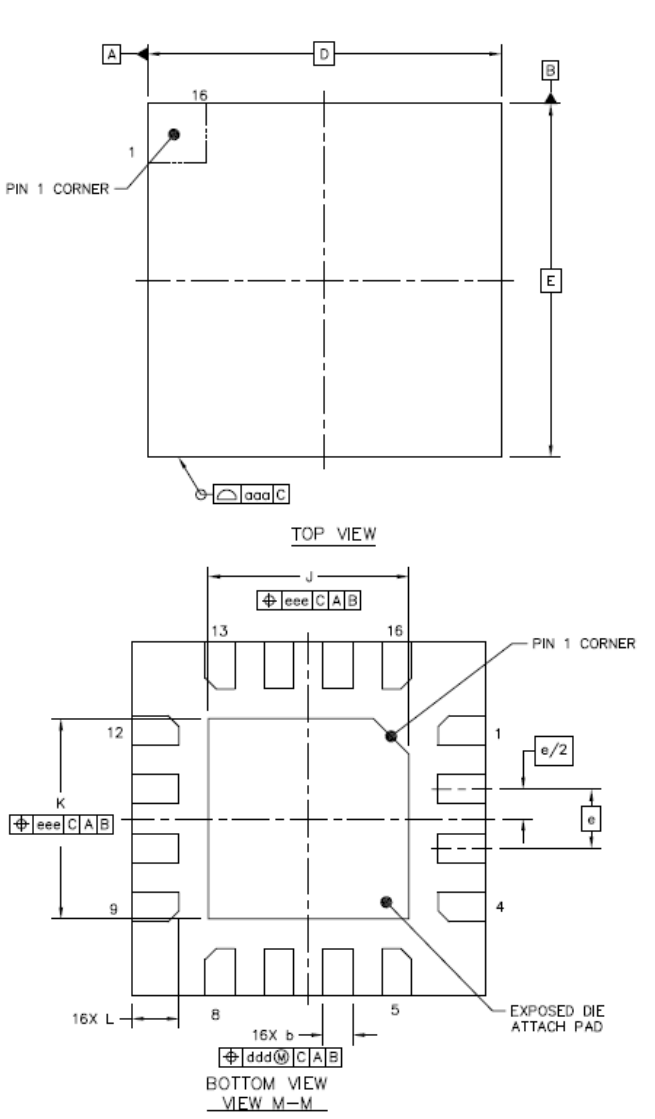
After entering into power saving mode, DKL 1908_V.1 could be waked up from STANDBY and DEEP_SLEEP modes by simply setting REG0x22[6]='1'. DKL 1908_V.1 will issue wake-up interrupt REG0x31[6] after wakeup operation completion. For POWER_DOWN mode, DKL 1908_V.1 can be waked up by using external reset pin (PIN11:RESETn).

5. Package Information

5.1. Package Drawing

The QFN-16 package outline is given below.

QFN-16, 3x3mm²



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	1.6	1.7	1.8
	Y	K	1.6	1.7	1.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

5.2. Package Soldering

5.2.1. Background

The DKL 1908_V.1 is housed in a small 16-pin lead-free QFN 3x3 mm^2 package. DKL 1908_V.1 can also be packaged as 12 pin or 8 pin SOP package. The packaged part passes the Level 3 pre-condition testing.

5.2.2. Reference Reflow Temperature Profile

Figure 18 is the reference temperature profile for the SMD IR reflow. Different equipments may have different optimized reflow conditions for maximum yield.

Pb-free SMD Package IR Reflow Profile

Step#	Profile Feature	Condition / Duration
Step 1	Ramp-up rate	1.5-3℃ /sec
Step 2	Preheat : 150~ 200℃ (Ta-Tb)	t1-t2: 60~80 sec
Step 3	Ramp-up rate (T_L to T_P)	1.5-3℃ /sec
	Temperature maintained above 220℃ (T_L)	t_L : 80~150 sec
Step 4	Peak temperature (T_P)	260+0/-5℃
	Time within 5℃ of actual peak temperature	30±10 sec
Step 5	Ramp-down rate	6℃/sec. Max.
Note1: Time 25℃ to peak temperature: 8 minutes max. Note2: The time between reflows shall be 5 minutes minimum and 60 minutes maximum.		

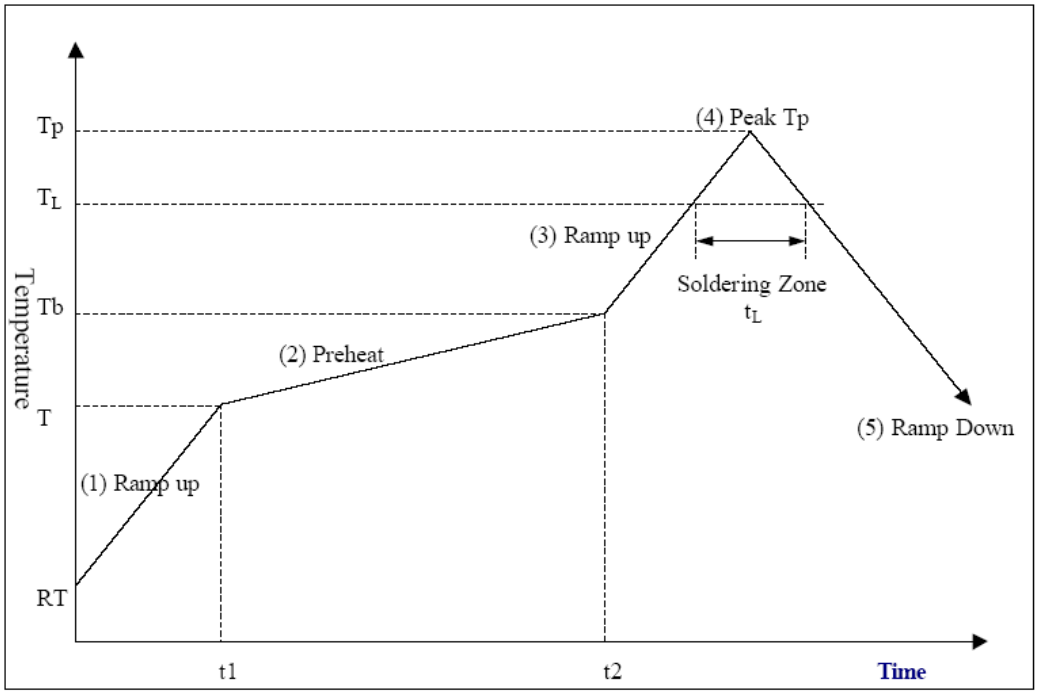


Figure 18. Reference SMD Package IR Reflow Profile

Appendix A. TX Power Configuration

Default output power is 11 dBm. Different output power settings are listed in the table below.
(TBD)

REG0x16	Reference Power
0xFF	Default Power
0xD7	Default Power – 2dBm
0xDD	Default Power – 4dBm
0xE3	Default Power – 6dBm
0xF9	Default Power – 8dBm
0xD9	Default Power – 10dBm
0xC9	Default Power – 12dBm
0xC1	Default Power – 14dBm
0xD6	Default Power – 25dBm
0xD4	Default Power – 30dBm
0xE0	Default Power – 35dBm
0xC8	Default Power – 40dBm

Appendix B. Register Descriptions

Register Types

Register Type	Description
R/W	Read/Write register
WT	Write 1 to trigger register, automatically cleared by hardware
RC	Read to clear register
R	Read-only register
R/W1C	Read/Write '1' to clear register

B.1 Registers (REG0x00~REG0x38)

REG0x00:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	MHF	NOACKRSP	r	AACKSET	ENACKBF	r	r
R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R-0	R-0

Bit 7 **Reserved**: Maintain as '0b0'

Bit 6 **MHF**: MAC header format

0: MAC header format = 1-byte frame control field then 4-byte address field

1: MAC header format = 4-byte address field then 1-byte frame control field (compliance with UM2471)

Bit 5 **NOACKRSP**: Automatic Acknowledgement Response

0: (default) Enables automatic acknowledgement response

1: Disables automatic acknowledgement response

Bit 4 **Reserved**: Maintain as '0b0'

Bit 3 **AACKSET**: ACK request bit of frame control field set automatically

0: (default) disable

1: ACK request bit of frame control field controlled by REG0x1b[2]

Bit 2 **ENACKBF**: ACK response when broadcast frame received

0: Disable ACK response when broadcast frame received

1: Enable ACK response when broadcast frame received

Bit 1-0 **Reserved**: Maintain as '0b00'

REG0x01:

PIPE ENABLE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	PIPEN6	PIPEN5	PIPEN4	PIPEN3	PIPEN2	PIPEN1	PIPEN0
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1

Bit 7 **Reserved**: Maintain as '0b0'
Bit 6 **PIPEN6**: Broadcasting frame enable
Bit 5 **PIPEN5**: Pipe5 enable
Bit 4 **PIPEN4**: Pipe4 enable
Bit 3 **PIPEN3**: Pipe3 enable
Bit 2 **PIPEN2**: Pipe2 enable
Bit 1 **PIPEN1**: Pipe1 enable
Bit 0 **PIPEN0**: Pipe0 enable

REG0x02:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	PIPE6	PIPEN5	PIPE4	PIPE3	PIPE2	PIPE1	PIPE0
R-0	R	R	R	R	R	R	R

Bit 7 **Reserved**: Maintain as '0b0'
Bit 6 **PIPE6**:
1: Broadcasting frame matched
0: not Broadcasting frame matched
Bit 5 **PIPE5**:
1: pipe5 address matched
0: pipe5 address not matched
Bit 4 **PIPE4**:
1: pipe4 address matched
0: pipe4 address not matched
Bit 3 **PIPE3**:
1: pipe3 address matched
0: pipe3 address not matched
Bit 2 **PIPE2**:
1: pipe2 address matched
0: pipe2 address not matched
Bit 1 **PIPE1**:
1: pipe1 address matched
0: pipe1 address not matched
Bit 0 **PIPE0**:
1: pipe0 address matched
0: pipe0 address not matched

REG0x03:

ACKNOWLEDGEMENT USER INFORMATION LOW BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
AUINF7	AUINF6	AUINF5	AUINF4	AUINF3	AUINF2	AUINF1	AUINF0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **AUINF[7:0]**: 16-bit User Information of Acknowledgement frame, Low Byte

REG0x04:

ACKNOWLEDGEMENT USER INFORMATION HIGH BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
AUINF15	AUINF14	AUINF13	AUINF12	AUINF11	AUINF10	AUINF9	AUINF8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **AUINF[15:8]**: 16-bit User Information of Acknowledgement frame, High Byte

REG0x05:

PIPE0 ADDRESS 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P0ADDR7	P0ADDR6	P0ADDR5	P0ADDR4	P0ADDR3	P0ADDR2	P0ADDR1	P0ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P0ADDR[7:0]**: Pipe0 address[7:0]

REG0x06:

PIPE0 ADDRESS 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P0ADDR15	P0ADDR14	P0ADDR13	P0ADDR12	P0ADDR11	P0ADDR10	P0ADDR9	P0ADDR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P0ADDR[15:8]**: Pipe0 address[15:8]

REG0x07:

PIPE0 ADDRESS 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P0ADDR23	P0ADDR22	P0ADDR21	P0ADDR20	P0ADDR19	P0ADDR18	P0ADDR17	P0ADDR16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P0ADDR[23:16]**: Pipe0 address[23:16]

REG0x08:

PIPE0 ADDRESS 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P0ADDR31	P0ADDR30	P0ADDR29	P0ADDR28	P0ADDR27	P0ADDR26	P0ADDR25	P0ADDR24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P0ADDR[31:24]**: Pipe0 address[31:24]

REG0x09:

PIPE1 ADDRESS 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P1ADDR7	P1ADDR6	P1ADDR5	P1ADDR4	P1ADDR3	P1ADDR2	P1ADDR1	P1ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P1ADDR[7:0]**: Pipe1 address[7:0]

REG0x0a:

PIPE1 ADDRESS 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P1ADDR15	P1ADDR14	P1ADDR13	P1ADDR12	P1ADDR11	P1ADDR10	P1ADDR9	P1ADDR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P1ADDR[15:8]**: Pipe1 address[15:8]

REG0x0b:

PIPE1 ADDRESS 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P1ADDR23	P1ADDR22	P1ADDR21	P1ADDR20	P1ADDR19	P1ADDR18	P1ADDR17	P1ADDR16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P1ADDR[23:16]**: Pipe1 address[23:16]

REG0x0c:

PIPE1 ADDRESS 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P1ADDR31	P1ADDR30	P1ADDR29	P1ADDR28	P1ADDR27	P1ADDR26	P1ADDR25	P1ADDR24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P1ADDR[31:24]**: Pipe1 address[31:24]

REG0x0D:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	DISTXW	RXFLUSH
R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	WT-0

Bit 7 **Reserved**: Maintain as '0b000000'

Bit 1 **DISTXW**: Disable the function of TX trigger after register wakeup

1: Disable the function of TX trigger after register wakeup

0: Enable the function of TX trigger after register wakeup

Bit 0 **RXFLUSH**: Flush the RX FIFO

1: Flush RX FIFO. RX FIFO data is not modified. If Ping-pong FIFO is enabled (REG0x34[0]=1), both FIFOs are flushed at the same time. Bit is automatically cleared to '0' by hardware.

REG0x10:

RF CHANNEL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	1MFRCH6	1MCSCH5	1MCSCH4	1MCSCH3	1MCSCH2	1MCSCH1	1MCSCH0
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0

Bit 7 **Reserved**: Maintain as '0b0'

Bit 6-0 **1MCSCH**: 1 MHz Channel Spacing Channel Number

0000000: 2400 MHz	0100100: 2436 MHz	1001000: 2472 MHz
0000001: 2401 MHz	0100101: 2437 MHz	1001001: 2473 MHz
0000010: 2402 MHz	0100110: 2438 MHz	1001010: 2474 MHz
0000011: 2403 MHz	0100111: 2439 MHz	1001011: 2475 MHz
0000100: 2404 MHz	0101000: 2440 MHz	1001100: 2476 MHz
0000101: 2405 MHz	0101001: 2441 MHz	1001101: 2477 MHz
0000110: 2406 MHz	0101010: 2442 MHz	1001110: 2478 MHz
0000111: 2407 MHz	0101011: 2443 MHz	1001111: 2479 MHz
0001000: 2408 MHz	0101100: 2444 MHz	1010000: 2480 MHz
0001001: 2409 MHz	0101101: 2445 MHz	1010001: 2481 MHz
0001010: 2410 MHz	0101110: 2446 MHz	1010010: 2482 MHz
0001011: 2411 MHz	0101111: 2447 MHz	1010011: 2483 MHz
0001100: 2412 MHz	0110000: 2448 MHz	1010100: 2484 MHz
0001101: 2413 MHz	0110001: 2449 MHz	1010101: 2485 MHz
0001110: 2414 MHz	0110010: 2450 MHz	1010110: 2486 MHz
0001111: 2415 MHz	0110011: 2451 MHz	1010111: 2487 MHz
0010000: 2416 MHz	0110100: 2452 MHz	1011000: 2488 MHz
0010001: 2417 MHz	0110101: 2453 MHz	1011001: 2489 MHz
0010010: 2418 MHz	0110110: 2454 MHz	1011010: 2490 MHz
0010011: 2419 MHz	0110111: 2455 MHz	1011011: 2491 MHz
0010100: 2420 MHz	0111000: 2456 MHz	1011100: 2492 MHz
0010101: 2421 MHz	0111001: 2457 MHz	1011101: 2493 MHz
0010110: 2422 MHz	0111010: 2458 MHz	1011110: 2494 MHz
0010111: 2423 MHz	0111011: 2459 MHz	1011111: 2495 MHz
0011000: 2424 MHz	0111100: 2460 MHz	1100000: Undefined
0011001: 2425 MHz	0111101: 2461 MHz	...
0011010: 2426 MHz	0111110: 2462 MHz	1111111: Undefined
0011011: 2427 MHz	0111111: 2463 MHz	
0011100: 2428 MHz	1000000: 2464 MHz	
0011101: 2429 MHz	1000001: 2465 MHz	
0011110: 2430 MHz	1000010: 2466 MHz	
0011111: 2431 MHz	1000011: 2467 MHz	
0100000: 2432 MHz	1000100: 2468 MHz	
0100001: 2433 MHz	1000101: 2469 MHz	
0100010: 2434 MHz	1000110: 2470 MHz	
0100011: 2435 MHz	1000111: 2471 MHz	

REG0x11:

VCO							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CALWT1	CALWT0	VCOSB4	VCOSB3	VCOSB2	VCOSB1	VCOSB0	ICTLPA0
R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0

Bit 7-6 **CALWT[1:0]**: VCO calibration wait time
00: 1.25u S
01: 2.5u S
10: 5u S
11: 10u S (default)

Bit 5-1 **VCOSB[4:0]**: VCO sub-band number with manual selection
00000: highest frequency band
.....
10010: (default)
.....
11111: lowest frequency band

Bit 0 **MVCO**: VCO sub-band manual selection
0: Auto selection (default)
1: Manual selection

REG0x12:

FDEV							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
FDEVM5	FDEVM4	FDEVM3	FDEVM2	FDEVM1	FDEVM0	FDEVCS	FDEVMS
R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

Bit 7-2 **FDEVM[5:0]**: Manual frequency deviation value
000000: No frequency deviation
.....
011010: (default)
.....
111111: Maximum frequency deviation

Bit 1 **FDEVCS**: Frequency Deviation Calibration start signal
Set to 1 to start frequency deviation calibration and set to 0 to stop the calibration. 0-1-0 transaction completes a full calibration cycle. This cycle must be greater than 4 ms

Bit 0 **FDEVMS**: Manual frequency deviation selection
0: Auto (default)
1: Manual

REG0x13:

PLL_1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
LOCKEN	FILTERV1	FILTERV0	LF3R1	LF3R0	LF2R2	LF2R1	LF2R0
R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

Bit 7 **LOCKEN**: Lock detector enable
0: Disable
1: Enable (default)

Bit 6-5 **FILTERV[1:0]**: Filter voltage option
00: 0.875 V (default)
01: 0.9 V
10: 0.925 V
11: 0.95 V

Bit 4-3 **LF3R[1:0]**: PLL loop filter R3 parameter
00: 40K ohm
01: 60K ohm (default)
10: 80K ohm
11: 100K ohm

Bit 2-0 **LF2R[2:0]**: PLL loop filter R3 parameter
000: 60K ohm (default)
001: 70K ohm
010: 80K ohm
011: 90K ohm
100: 100K ohm
101: 110K ohm
110: 120K ohm
111: 130K ohm

REG0x14:

PLL_2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	FILTERI1	FILTERI0	CPI	CPVCO	PRSI1	PRSI0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5-4 **FILTERI[1:0]**: Filter current option

00: 12.5u A (default)

01: 25u A

10: 37.5u A

11: 50u A

Bit 3 **CPI**: Charge pump current option

0: 50u A

1: 100u A (default)

Bit 2 **CPVCO**: Charge pump disable for VCO

0: Enable (default)

1: Disable

Bit 1-0 **PRSI[1:0]**: Prescaler current option

00: 30u A

01: 35u A

10: 40u A (default)

11: 50u A

REG0x15:

PLL_3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
VCORX1	VCORX0	VCOTX1	VCOTX0	LOBRX1	LOBRX0	LOBTX1	LOBTX0
R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1

Bit 7-6 **VCORX[1:0]**: VCO current option for RX
- 00: 2.25m A
- 01: 2.475m A (default)
- 10: 2.7m A
- 11: 2.925m A

Bit 5-4 **VCOTX[1:0]**: VCO current option for TX
- 00: 2.25m A
- 01: 2.475m A (default)
- 10: 2.7m A
- 11: 2.925m A

Bit 3-2 **LOBRX[1:0]**: LO buffer current option for RX
- 00: 1.25m A (default)
- 01: 1.5m A
- 10: 1.75m A
- 11: 2m A

Bit 1-0 **LOBTX[1:0]**: LO buffer current option for TX
- 00: 1.25m A
- 01: 1.5m A
- 10: 1.75m A
- 11: 2m A (default)

REG0x16:

PA							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
DIV2TX1	DIV2TX0	PAI2	PAI1	PAI0	PABUF1	PABUF0	PAMODE
R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0

Bit 7-6 **DIV2TX[1:0]**: Divide-by-2 current option for TX
- 00: 1.25m A (default)
- 01: 1.5m A
- 10: 1.75m A
- 11: 2m A

Bit 5-3 **PAI[2:0]**: PA reference current Iref option
- 000: 50u A
- 001: 75u A
- 010: 100u A
- 011: 125u A
- 100: 150u A
- 101: 175u A
- 110: 200u A
- 111: 225u A (default)

Bit 2-1 **PABUF[1:0]**: PA buffer current option
- 00: 1.65m A
- 01: 2.1m A
- 10: 3m A
- 11: 5.1m A (default)

Bit 0 **PAMODE**: PA power mode
- 0: very low power (default)
- 1: normal power

REG0x17:

WAKE UP							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
XTALC1	XTALC0	WAKEC2	WAKEC1	WAKEC0	LDOSM	SLEEPM1	SLEEPM0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	WT-0

Bit 7-6 **XTALC[1:0]**: Crystal load capacitor control
00: 16p F (default)
01: 20p F
10: 20p F
11: 24p F

Bit 5-3 **WAKEC[2:0]**: Number of slow clock cycles to wake digital circuit up
000: 5 (default)
001: 6
010: 7
.....

Bit 2 **LDOSM:** Digital LDO sleep mode control
0: Deep sleep and standby mode (default)
1: power down mode

Bit 1-0 **SLEEPM[1:0]:** Sleep mode selection
00: Standby mode
01: Deep sleep mode
10: Forbidden (default)
11: Power down mode

REG0x18:

SLEEP MODE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLEEPVM1	SLEEPVM0	SLEEPVMC	BTMEN	LOOPV1	LOOPV0	LDOD	LDODB
R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	WT-0

Bit 7-6 **SLEEPVM[1:0]**: Manual voltage supply in sleep mode
00: 1.8~2.3 V
01: 2.3~2.8 V
10: 2.8~3.2 V (default)
11: 3.2~3.6 V

Bit 5 **SLEEPVMC**: Digital circuit voltage supply in sleep mode
0: Automatically set by battery monitor (default)
1: Controlled by REG0x18[7:6]

Bit 4 **BTMEN:** Battery monitor control
0: Disable
1: Enable (default)

Bit 3-2 **LOOPV[1:0]**: Loop filter pre-charge voltage option
00: 0.9 V (default)
01: 1 V
10: 1.1 V
11: 1.2 V

Bit 1 **LDOD**: Digital regulator output voltage
0: 1.8 V (default)
1: 1.65 V

Bit 0 **LDODB:** Digital regulator bypass control
0: Digital regulator normal operation (default)
1: Digital LDO bypass

REG0x19:

FREQUENCY DIGITAL TUNE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
FDTUNE7	FDTUNE 6	FDTUNE 5	FDTUNE 4	FDTUNE 3	FDTUNE 2	FDTUNE 1	FDTUNE 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	WT-0

Bit 7-0 **FDTUNE[7:0]**: RF digital frequency tuning
1 LSB reduces the RF frequency by 977 Hz

REG0x1A:

SLEEP MODE_2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
MIXERV1	MIXERV0	RAMPUD	CAPADJ1	CAPADJ0	r	LOCKC1	LOCKC0
R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R-1	R/W-1	WT-1

Bit 7-6 **MIXERV[1:0]**: Mixer voltage option
00: 1.25 V
01: 1.275 V
10: 1.3 V
11: 1.325 V (default)

Bit 5 **RAMPUD**: Ramp up/down time
0: 16u S
1: 8u S (default)

Bit 4-3 **CAPADJ[1:0]**: Frequency deviation Cap number adjustment
00: +0 calibrated value
01: +1 (default)
10: -2
11: -1

Bit 2 **Reserved**: Maintain as ‘0b1’

Bit 1-0 **LOCKC[1:0]:** 16MHz crystal oscillator current option
00: 200u A
01: 300u A
10: 500u A
11: 600u A (default)

REG0x1B:

TRANSMIT FIFO CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXRTYN3	TXRTYN2	TXRTYN1	TXRTYN0	r	TXACKREQ	r	TXTRIG
R/W-0	R/W-0	R/W-1	R/W-1	R-0	R/W-0	R-0	WT-0

Bit 7-4 **TXRTYN**: Maximum TX Retry Times
0000: 0
...
0011: 3 (default)
...
1111: 15

Bit 3 **Reserved**: Maintain as '0b0'

Bit 2 **TXACKREQ:** TX FIFO Acknowledgement Request bit
Transmit a packet with Acknowledgement request. If Acknowledgement is not received, the DKL 1908_V.1 retransmits up to **TXRTYN** times.
0: (default) No Acknowledgement packet requested
1: Acknowledgement packet requested

Bit 1 **Reserved**: Maintain as '0b0'

Bit 0 **TXTRIG:** Transmit Frame in TX FIFO bit
1: Transmit the frame in the TX FIFO. Bit is automatically cleared to '0' by hardware.

REG0x1C:

Group0 ID							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
G0ID7	G0ID6	G0ID5	G0ID4	G0ID3	G0ID2	G0ID1	G0ID0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 G0ID**[7:0]**: Group0 ID [7:0]

REG0x1D:

Group1 ID							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
G1ID7	G1ID6	G1ID5	G1ID4	G1ID3	G1ID2	G1ID1	G1ID0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 G1ID**[7:0]**: Group1 ID [7:0]

REG0x1E:

Group2 ID							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
G2ID7	G2ID6	G2ID5	G2ID4	G2ID3	G2ID2	G2ID1	G2ID0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 G2ID**[7:0]**: Group2 ID [7:0]

REG0x1F:

Group3 ID							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
G3ID7	G3ID6	G3ID5	G3ID4	G3ID3	G3ID2	G3ID1	G3ID0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 G3ID**[7:0]**: Group3 ID [7:0]

REG0x22:

WAKE CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	REGWAKE	r	r	r	r	r	R
R-1	WT-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7 **Reserved**: Maintain as '0b1'

Bit 6 **REGWAKE**: Register Triggered Wake-up Signal

1: To wake DKL 1908_V.1 up. Bit is automatically cleared to '0' by

Bit 5-0 hardware. **Reserved**: Maintain as '0b000000'

REG0x23:

ACKNOWLEDGEMENT TIMEOUT							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
3SPI	MATOP6	MATOP5	MATOP4	MATOP3	MATOP2	MATOP1	MATOP0
R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **3SPI**:

1: enable 3-wire SPI

0: disable 3-wire SPI

Bit 6-0 **MATOP[6:0]**: Maximum Acknowledgement Timeout Period

0000000: 0

...

1000000: 40(default)

...

1111111: 127

REG0x24:

TX STATUS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXRETRY3	TXRETRY2	TXRETRY1	TXRETRY0	r	r	TXLERR	TXNS
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-4 **TXRETRY[3:0]**: TXFIFO Retry Times
Maximum number of retries of the most recent TXFIFO transmission.
0000: 0 (default)
...
1111: 15

Bit 3-1 **Reserved**: Maintain as '0b000'

Bit 1 **TXLERR**: TX FIFO length error
0: (default) Succeeded
1: The frame length in TXFIFO is zero

Bit 0 **TXNS**: TX FIFO Release Status
0: (default) Succeeded
1: Fail, retry count exceed

REG0x2A:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	r	PAGE
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R/W-0

Bit 7-1 **Reserved**: Maintain as '0b0000000'

Bit 5-0 **PAGE**:
0 : Memory 0x40~0x68 is TXFIFO
1 : Memory 0x40~0x68 is RXFIFO

REG0x2B:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RXTTL1	RXTTL0	r	r	r	r	r	r
R/W-1	R/W-1	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-6 **RXTTL[1:0]**: RX FIFO time-to-live
00 : 1024 slow clock cycles
01 : 2048 slow clock cycles
10 : 4096 slow clock cycles
11 : 8192 slow clock cycles

Bit 5-0 **Reserved**: Maintain as '0b000000'

REG0x2C:

PIPE2 ADDRESS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P2ADDR7	P2ADDR6	P2ADDR5	P2ADDR4	P2ADDR3	P2ADDR2	P2ADDR1	P2ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P2ADDR[7:0]**: Pipe2 address[7:0]

REG0x2D:

PIPE3 ADDRESS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P3ADDR7	P3ADDR6	P3ADDR5	P3ADDR4	P3ADDR3	P3ADDR2	P3ADDR1	P3ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P3ADDR[7:0]**: Pipe3 address[7:0]

REG0x2E:

PIPE4 ADDRESS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P4ADDR7	P4ADDR6	P4ADDR5	P4ADDR4	P4ADDR3	P4ADDR2	P4ADDR1	P4ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P4ADDR[7:0]**: Pipe4 address[7:0]

REG0x2F:

PIPE5 ADDRESS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
P5ADDR7	P5ADDR6	P5ADDR5	P5ADDR4	P5ADDR3	P5ADDR2	P5ADDR1	P5ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P5ADDR[7:0]**: Pipe5 address[7:0]

REG0x30:

RX MAC STATUS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	RXFFOVFL	RXCRCERR	GroupID3	GroupID2	GroupID1	GroupID0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5 **RXFFOVFL**: RX FIFO Overflow

0: (default) Not overflow

1: Overflow

Bit 4 **RXCRCERR**: RX CRC Error

0: (default) RX CRC correct

1: RX CRC error

Bit 3 **GroupID3**:

1: Group ID 3 matched

0: Group ID 3 not matched

Bit 2 **GroupID2**:

1: Group ID 2 matched

0: Group ID 2 not matched

Bit 1 **GroupID1**:

1: Group ID 1 matched

0: Group ID 1 not matched

Bit 0 **GroupID0**:

1: Group ID 0 matched

0: Group ID 0 not matched

REG0x31:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	RXIF	r	WAKEIF	TXNIF
R-0	R-0	R-0	R-0	RC-0	R-0	RC-0	RC-0

Bit 7-4 **Reserved**: Maintain as '0b0000'

Bit 3 **RXIF**: RX FIFO Reception Interrupt (1)

0: (default) No RX FIFO reception interrupt occurred

1: An RX FIFO reception interrupt occurred

Bit 2 **Reserved**: Maintain as '0b0'

Bit 1 **WAKEIF**: Wake-up Alert Interrupt (1)

0: (default) No wake-up alert interrupt occurred

1: A wake-up interrupt occurred

Bit 0 **TXNIF**: TX FIFO Transmission Interrupt (1)

0: (default) No TX FIFO transmission interrupt occurred

1: TX FIFO transmission interrupt occurred

Note 1: Interrupt bits are cleared to '0b0' when the register is read.

REG0x32:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	RXMSK	r	WAKEMSK	TXNMSK
R-0	R-0	R-0	R-0	R/W-1	R-0	R/W-1	R/W-1

Bit 7-4 **Reserved**: Maintain as '0b0000'

Bit 3 **RXMSK**: RXFIFO Reception Interrupt Mask

0: Enable the RXFIFO reception interrupt

1: (default) Disable the RXFIFO reception interrupt

Bit 2 **Reserved**: Maintain as '0b0'

Bit 1 **WAKEMSK**: Wake-up Alert Interrupt Mask

0: Enable the wake-up alert interrupt

1: (default) Disable the wake-up alert interrupt

Bit 0 **TXNMSK**: TXFIFO Transmission Interrupt Mask

0: Enable the TXFIFO transmission interrupt

1: (default) Disable the TXFIFO transmission interrupt

REG0x33:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	IRQPOL	r	r	r	r
R-0	R-0	R-0	R/W-1	R-0	R-0	R-0	R-0

Bit 7-5 **Reserved**: Maintain as '0b000'

Bit 4 **IRQPOL**: Interrupt Edge Polarity

0: (default) Falling edge

1: Rising edge

Bit 3-0 **Reserved**: Maintain as '0b0000'

REG0x34:

SOFTWARE RESET							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	RSTTRX	RSTPWR	RSTBB	RSTMAC
R-0	R-0	R-0	R-0	WT-0	WT-0	WT-0	WT-0

Bit 7-4 **Reserved**: Maintain as '0b0000'

Bit 3 **RSTTRX**: MAC TX/RX Reset

1: Reset MAC TX/RX circuitry. Initialization is not needed after **RSTTRX** reset. Bit is automatically cleared to '0' by hardware.

Bit 2 **RSTPWR**: Power management Reset

1: Reset Power management circuitry. Initialization is not needed after **RSTPWR** reset. Bit is automatically cleared to '0' by hardware.

Bit 1 **RSTBB**: Baseband Reset

1: Reset baseband circuitry. Initialization is not needed after **RSTBB** reset. Bit is automatically cleared to '0' by hardware.

Bit 0 **RSTMAC**: MAC and Registers Reset

1: Reset MAC circuitry and Registers. Initialization is needed after **RSTMAC** reset. Bit is automatically cleared to '0' by hardware.

REG0x35:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0
WT-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **SLPACK**: Sleep Acknowledgement
Place the DKL 1908_V.1 to Power Saving Mode. Bit is automatically cleared to '0' by
Bit 6-0 hardware. **WAKECNT[6:0]**: System Clock Recovery Time
WAKECNT is a 15-bit value. The WAKECNT[14:7] bits are located in REG0x37
0000000: (default)

REG0x36:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	VCOCTL	r	r	RFRST	r	R
R-0	R-0	R/W-0	R-0	R-0	R/W-0	R-0	R -0

Bit 7-6 **Reserved**: Maintain as '0b00'
Bit 5 **VCOCTL**: VCO manual control enable
Bit 4-3 **Reserved**: Maintain as '0b00'
Bit 2 **RFRST**: RF State Machine Reset (1)

0: (default) Normal operation of RF state machine
1: Hold RF state machine in Reset
Bit 1-0 **Reserved**: Maintain as '0b00'
allow RF circuitry to calibrate.
Note 1: Perform RF reset by setting RFRST = 1 and then RFRST = 0. Delay at least 192 us after performing to

REG0x37:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	VCO	r	r	SPISYNCE	SPISYNC
R-0	R-0	R-0	R/W-0	R-0	R-0	R/W-0	R/W-0

Bit 7-5 **Reserved**: Maintain as '0b000'
Bit 4 **VCO**: VCO manual control
Bit 3 **Reserved**: Maintain as '0b0'
Bit 1 **SPISYNCE**: Sync SPI enable function controlled by
1 : SPISYNC
0 : MAC (enable during active, sleep during sleep)
Bit 0 **SPISYNC:** Sync SPI interface to prevent glitch

REG0x38

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	CONT_TX	BBMODE2	BBMODE 1	BBMODE 0
R -1	R-0	R-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0

Bit 7-3 **Reserved**: Maintain as '0b00000'

Bit 2-0 **BBMODE [2:0]**: Turbo Mode Select

000: 125kbps DSSS-OQPSK

001: 1Mbps MSK

010: 250kbps DSSS-OQPSK (default)

011: 2Mbps MSK

100~111 : Undefined

Specification

Operation frequency:2408MHz~2475MHz

Maximum power: 6.94dBm(EIRP)

Statement

1. The device complies with RF specifications when the device used at 0mm form your body.
2. This product is a category 1 receiver device.
3. The operating temperature of the EUT can't exceed 55°C and shouldn't be lower than -20°C.
4. This product can be used across EU member states.

CE

Revision History

Revision	Date	Description of Change
0.0	2018/05/08	Initial preliminary version.

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DISCLAIMER

FCC Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-- Reorient or relocate the receiving antenna.

-- Increase the separation between the equipment and receiver.

-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-- Consult the dealer or an experienced radio/TV technician for help.

§15.19 Labeling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

§15.21 Information to user.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

RF exposure

This equipment complies with FCC and ISED radiation exposure limits set forth for an uncontrolled environment. The RF exposure compliance of the distance of 0 mm between the radiator and your body. Antenna gain must be below 0.4dBi.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093.

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

Labelling Requirements for the Host device

The host device shall be properly labeled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and ISED of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Model: 2.4G module

Contains FCC ID：2APYU-DKL1908

The host OEM user manual must also contain clear instructions on how end users canfind and/or access the module and the FCC ID and ISED.

Model: 2.4G module

Contains FCC ID：2APYU-DKL1908

The transmitter module may not be co-located with any other transmitter or antenna. Module Antenna Type: Integral Antenna,ANT Gain: 0.4dBi

OEM Statement

a. The module manufacturer must show how compliance can be demonstrated only for specific host or hosts

b. The module manufacturer must limit the applicable operating conditions in which t transmitter will be used, and

c. The module manufacturer must disclose that only the module grantee can make the te evaluation that the module is compliant in the host. When the module grantee either refuses to make this evaluation, or does not think it is necessary, the module certification is rendered invalid for use in the host, and the host manufacturer has no choice other than to use a different module, or take responsibility (§ 2.929) and obtain a new FCC ID for the product.

d. The module manufacturer must provide the host manufacturer with the follow requirements:

e. The host manufacturer is responsible for additional testing to verify compliance as composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions).

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. In such cases, please involve a FCC certification specialist in order to determine if a Permissive Class II Change or new Certification is required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). The end-product may need Verification testing, Declaration of Conformity testing, a Permissive Class II Change or new Certification. Please involve a FCC certification specialist in order to determine what will be exactly applicable for the end-product.

KDB Ref Sect	Requirements of KDB 996369 D03	Description
2.2	List of applicable FCC rules	This product compliance with FCC Part 15C section 15.249, section 15.203,section 15.207,section 15.209, section 15.215.
2.3	Summarize the specific operational use conditions	This product has an Integral antenna
2.4	Limited module procedures	This product is a limited module
2.5	Trace antenna designs	This product without trace antenna designs
2.6	RF exposure considerations	race antenna designs compliance RF exposure limits
2.7	Antennas	This product has an Integral antenna
2.8	Label and compliance information	The host system using this module , should label in a visible area indicated the following texts: "Contains FCC ID : 2APYU-DKL1908"
2.9	Information on test modes and additional testing requirements	Data transfer module demo can control the EUT works in RF test mode and specified channel
2.10	Additional testing, Part 15 Subpart B disclaimer	The module without unintentional-radiator digital circuit, so the module does not require an evaluation by FCC part 15 Subpart B. The host should be evaluated by FCC part 15 Subpart B