

# DK7050

## Bluetooth® Low Energy Module

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Version 0.5BETA Formal Release

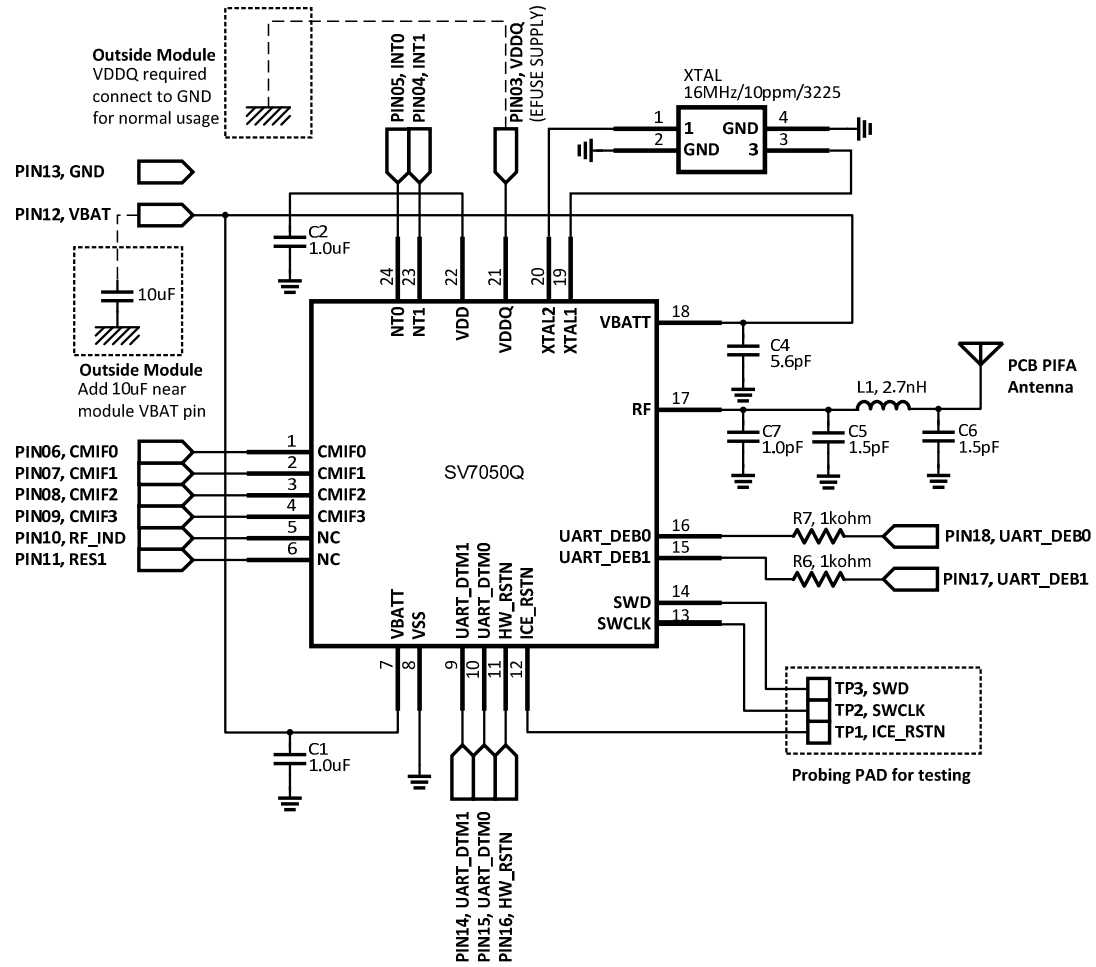
### ■ INTRODUCTION

DK7050 is a Bluetooth® Low Energy wireless module to provide BLE connectivity to MCU or hosted systems. It consists of a fully integrated 2.4GHz radio transceiver, modem, and baseband processor for Bluetooth® Low Energy system. DK7050 runs autonomously, automatically advertising, scanning and maintaining connection with minimal host effort. DK7050 supports “iCMD”, a light-weight command set with BLE GAP and GATT Server function. SPI & UART interface are supported. Typical code usage on the system host for the DK7050 setup is 4kB to 8kB and SRAM usage of 200 to 500 bytes depending on application complexity.

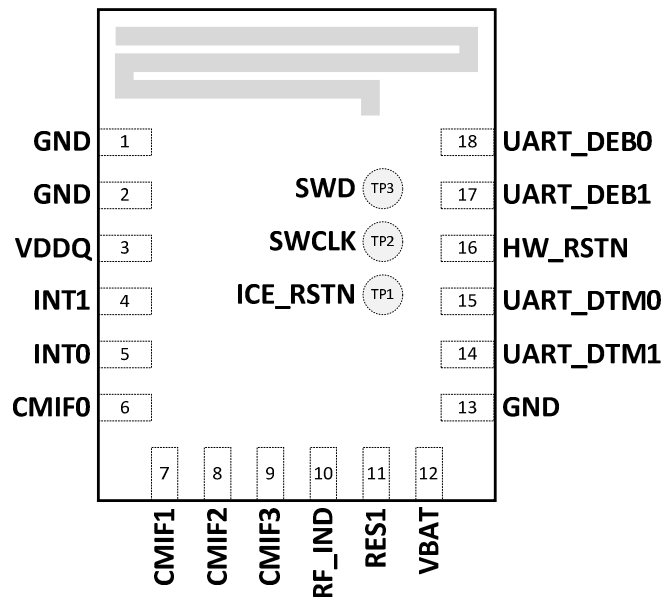
### ■ FEATURES

- Bluetooth® Core Spec v4.2 compliant
- GAP roles supported: Broadcaster, Observer, & Peripheral
- GATT features: GATT server; up to 22 bytes for each Characteristic, expandable to 512 bytes; up to 38 Characteristics
- Radio Certification
  - MIC Japan (Certification no. TBD)
  - FCC (FCC ID: TBD)
  - RED (R&TTE ID: TBD)
- Bluetooth® Qualification (End Product, QDID: D033798)
- Battery Supply Voltage 1.9V to 3.6V
- Operational Temperature -20°C to +85°C
- Current Consumptions
  - Hibernate (Idle, XTAL off) Mode 3.5uA (Typ.)
  - On State (Idle) Mode 7.5mA (Typ.)
  - TX Mode (2dBm) 31mA (Typ.)
  - RX Mode 28mA (Typ.)
- Dimension 12.0mm(W) x 13.0mm(L) x 1.8mm(H)
- Pb Free, RoHS Compliant

## ■ SCHEMATICS



## ■ PIN ASSIGNMENTS (TOP VIEW)



## ■ PIN DEFINITIONS

#	Pin Name	I/O	Ana/Dig	I/O Type	Function
1	GND	-	GND	GND	GND
2	GND	-	GND	GND	GND
3	VDDQ	-	ANA	-	E-Fuse programming power input pin Required connect to GND for normal usage.
4	INT1	IN	DIG	CMOS	Interrupt input to DK7050 (WAKELOCK)
5	INT0	OUT	DIG	CMOS	Interrupt to external MCU, active-low
6	CMIF0	INOUT	DIG	CMOS	iCMD interface, set to SPI SCLK by strapping CMIF2
7	CMIF1	INOUT	DIG	CMOS	iCMD interface, set to SPI CSN by strapping CMIF2 or UART RXD
8	CMIF2	INOUT	DIG	CMOS	iCMD interface, set to SPI MISO by strapping CMIF2 or UART TXD
9	CMIF3	INOUT	DIG	CMOS	iCMD interface, set to SPI MOSI by strapping CMIF2
10	RF_IND	OUT	DIG	CMOS	Indicating RF (TX or RX) is on, Configurable active polarity
11	RES1	OUT	DIG	CMOS	Reserved test pins, NC for normal operation
12	VBAT	-	PWR	VCC	Power Supply, 1.9V to 3.6V
13	GND	-	GND	GND	GND
14	UART_DTM1	INOUT	DIG	CMOS	UART DTX for DTM tests, default tri-state Enable by iCMD Keep floating for normal operation
15	UART_DTM0	INOUT	DIG	CMOS	UART DRX for DTM tests, default tri-state Enable by iCMD Keep floating for normal operation
16	HW_RSTN	IN	DIG	CMOS	Hardware reset pin (active low)
17	UART_DEB1	INOUT	DIG	CMOS	Debugging UART DTX (protocol debug) Keep floating for normal operation
18	UART_DEB0	INOUT	DIG	CMOS	Debugging UART DRX (protocol debug) Keep floating for normal operation
TP0	ICE_RSTN	IN	DIG	CMOS	ICE reset pin (active low), debugging purpose
TP1	SWCLK	INOUT	DIG	CMOS	ICE SWCLK pin, debugging purpose
TP2	SWD	INOUT	DIG	CMOS	ICE SWD pin, debugging purpose

## ■ SYSTEM OVERVIEW

### ● Power States

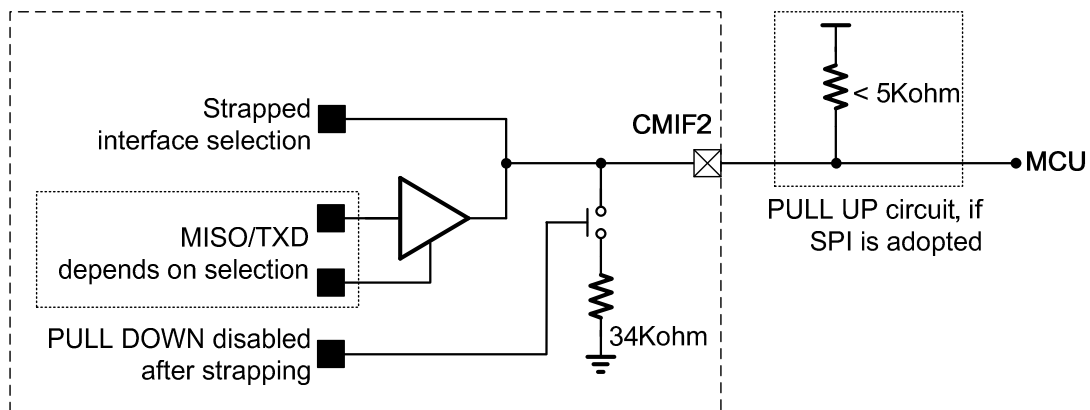
DK7050 consists of 2 power states: hibernate and active. The different power states have different level of current consumption and activities.

Mode Name	Function
Hibernate	32k RC as RTC
Active	System on, set up protocol parameters and databases, running BLE protocol and RF activities. The 32k RC clock is calibrated with the RF crystal during active state, ensuring frequency accuracy during hibernate state.

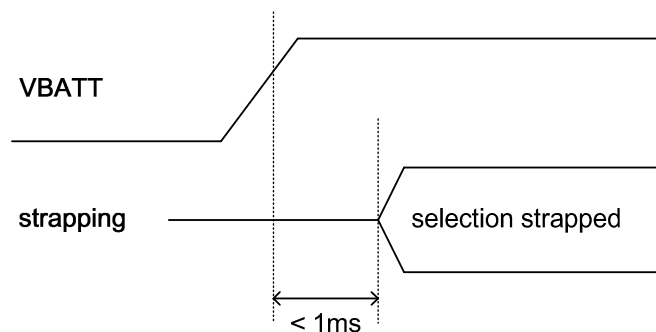
### ● Boot Strapping

DK7050 iCMD interface supports UART and SPI (SPI MODE0) interfaces. The choice is set by boot strapping pin CMIF2 during POR.

- For choosing SPI interface requires adding external pull-up resistor (< 5kohm) on CMIF2 pin.
- For using UART interface there is no any additional action required.



The timing chart about strapping related to VBATT power sequence is shown below. After VBATT power settled interface mode would be strapped in 1ms.



The mapping table for SPI or UART is shown below.

#	Pin Name	SPI definition	UART definition	Notes
6	CMIF0	SCLK	-	
7	CMIF1	CSN	RXD	
8	CMIF2	MISO	TXD	Strapping pin pull high for SPI, leave open for UART
9	CMIF3	MOSI	-	

DK7050 UART and SPI specification are shown below.

Mode Name	Max Speed	Notes
UART	9600bps	8 data bits, no polarity bit used, 1 stop bit used
SPI	4MHz	Only support SPI MODE0

● **IRQ/WAKELOCK**

#	Pin Name	I/O	definition	Notes
5	INT0	OUT	IRQ	Event interrupt, active low
4	INT1	IN	WAKELOCK	Prevent DK7050 into idle mode, active high

● **Hardware Reset**

#	Pin Name	I/O	definition	Notes
16	HW_RSTN	IN	RSTN	Weakly pull-high, Active low

● **UART\_DTM**

UART\_DTM1 and UART\_DTM0 pins are used for SIG DTM tests. A special iCMD command enables the UART function for DTM test; system host should have a test mode procedure to set DK7050 to DTM mode.

#	Pin Name	I/O	definition	Notes
15	UART_DTM0	INOUT	DRX	Default Tri-State, Enable by iCMD Keep floating for normal operation
14	UART_DTM1	INOUT	DTX	Default Tri-State, Enable by iCMD Keep floating for normal operation

● **UART\_DEB**

UART\_DEB1 and UART\_DEB0 pins provide debugging log for the BLE protocol. Leave the pins open; tying the pins to logic 0 or 1 will cause malfunction.

#	Pin Name	I/O	definition	Notes
18	UART_DEB0	INOUT	DRX	Protocol debugging purpose keep floating for normal operation
17	UART_DEB1	INOUT	DTX	Protocol debugging purpose keep floating for normal operation

■ **ELECTRICAL CHARACTERISTICS**

● **Absolute Maximum Ratings**

Symbol	Description	Note	Min.	Typ.	Max.	Unit
V <sub>PIN</sub>	Limiting voltage on pin		-0.1		VBATT	V
T <sub>Store</sub>	Storage temperature		-50		150	°C
T <sub>VRISE</sub>	Power supply rise time		5		100	msec.
V <sub>BATT_L</sub>	Supply voltage limit		-0.1		3.6	V
ESD <sub>HBM</sub>	ESD, human body mode				4000	V
ESD <sub>MM</sub>	ESD, machine mode				125	V
ESD <sub>CDM</sub>	ESD, charged device mode				1000	V

● **Operating Conditions**

Parameter	Description	Note	Min.	Typ.	Max.	Unit
V <sub>BATT</sub>	Supply Voltage		1.9		3.6	V
V <sub>DDQ</sub>	E-fuse programming voltage		2.4	2.5	2.6	V
V <sub>IO</sub>	I/O Voltage		0		VBATT	V
T	Operational Temperature		-20		+85	°C

● **Power Consumptions**

Parameter	Description	Note	Min.	Typ.	Max.	Unit
I <sub>HIB</sub>	Hibernate mode current			3.5		uA
I <sub>ON</sub>	On state (Idle) mode current			7.5		uA
I <sub>TX2DBM</sub>	TX mode current			31		mA
I <sub>RX</sub>	RX mode current			28		mA

● **TX Characteristics**

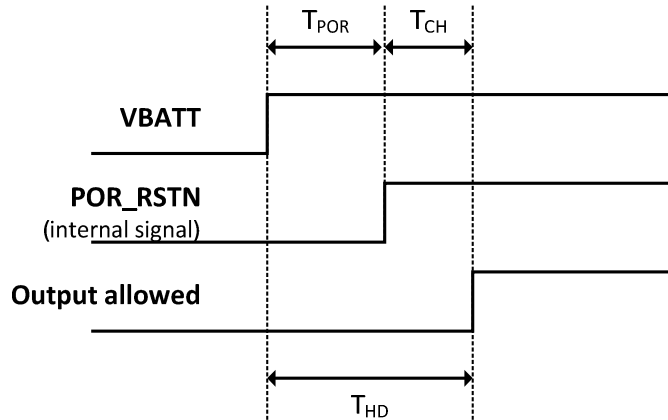
Parameter	Description	Note	Min.	Typ.	Max.	Unit
F <sub>RANGE</sub>	Operational frequency range		2400		2483	MHz
F <sub>DEV</sub>	Frequency deviation		225	250	275	kHz
P <sub>RF_MAX</sub>	Maximum output power*			8		dBm
P <sub>RF_TYP</sub>	Typical output power			2		dBm
P <sub>RF_RANGE</sub>	output power range			30		dB
P <sub>RF_LP</sub>	Quiet mode output power			-40		dBm
P <sub>RF_OFFSET2M</sub>	Spurious @ 2MHz offset				-54	dBm
P <sub>RF_OFFSET3M</sub>	Spurious @ 3MHz offset				-58	dBm
P <sub>RF_HD2</sub>	2 <sup>nd</sup> harmonic power			-53	-49	dBm
P <sub>RF_HD3</sub>	3 <sup>rd</sup> harmonic power			-44	-42	dBm

\*Not support radio certification in +8dBm TX output case.

● **RX Characteristics**

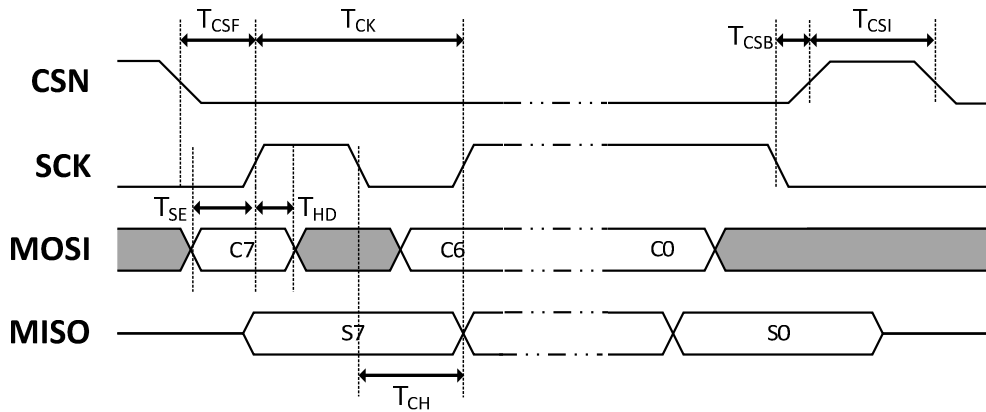
Parameter	Description	Note	Min.	Typ.	Max.	Unit
P <sub>RX_MAX</sub>	Maximum received power			2		dBm
P <sub>RX_MIN_IDEAL</sub>	Minimum received power, ideal			-93.5		dBm
P <sub>RX_MIN_DIRTY</sub>	Minimum received power, dirty			-92		dBm
C <sub>RX_I_CO</sub>				8		dB
C <sub>RX_I_1ST</sub>				1		dB
C <sub>RX_I_2ND</sub>				-28		dB
C <sub>RX_I_3+N</sub>				-38		dB
C <sub>RX_I_IMG</sub>				-21		dB
C <sub>RX_I_IMG1</sub>				-23		dB
P <sub>RX_IMD</sub>			-38	-35		dBm
P <sub>RX_OOB1</sub>	Out-of-band blocker, 2GHz~2.399GHz			-16		dBm
P <sub>RX_OOB2</sub>	Out-of-band blocker, < 2GHz			-5		dBm
P <sub>RX_OOB3</sub>	Out-of-band blocker, 2.484GHz~6GHz			-15		dBm

● Power On Reset



Parameter	Description	Note	Min.	Typ.	Max.	Unit
T <sub>POR</sub>	Time from power ready to POR		2			msec
T <sub>CH</sub>	Time from POR to strap latched		1			msec
T <sub>HD</sub>	T <sub>HD</sub> = T <sub>POR</sub> +T <sub>CH</sub>		3			msec

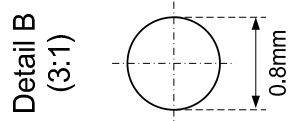
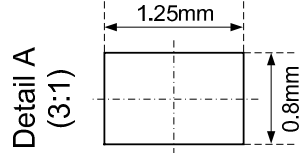
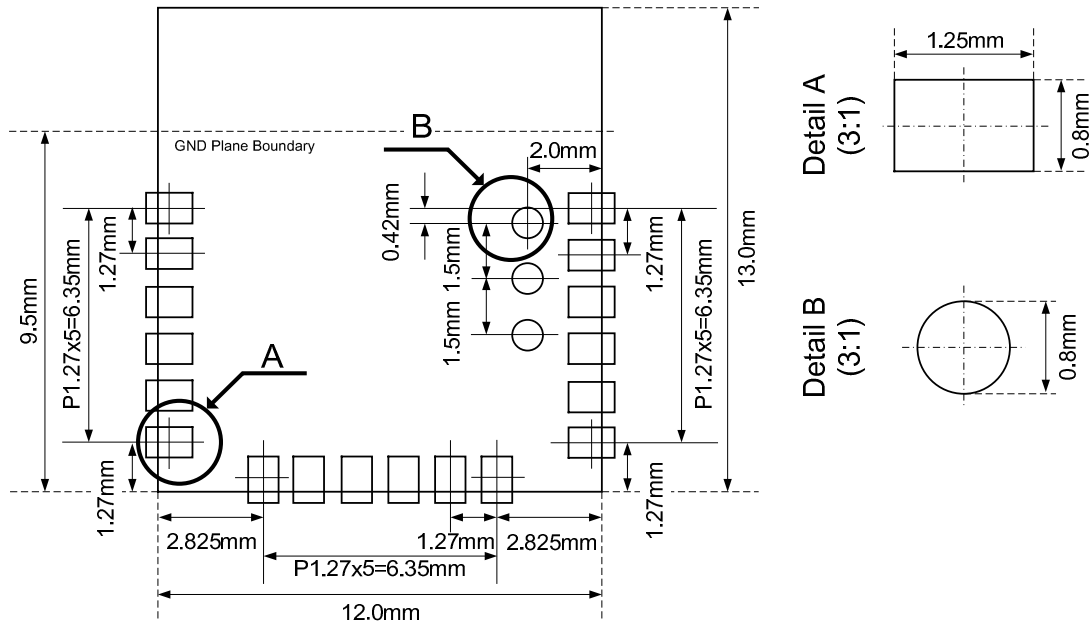
● SPI Specification



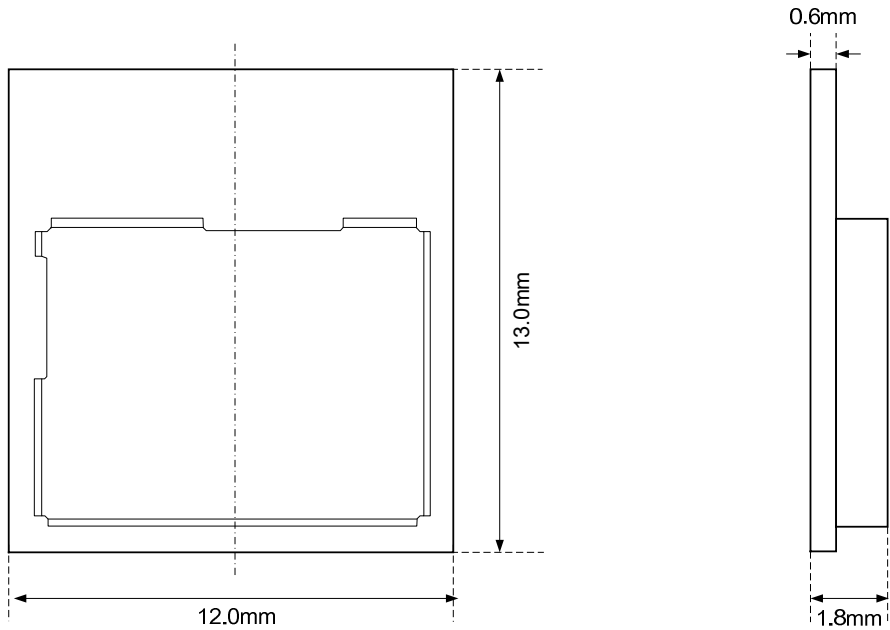
Parameter	Description	Note	Min.	Typ.	Max.	Unit
T <sub>CSF</sub>	CSN to SCK positive edge		1000			nsec
T <sub>CSB</sub>	SCK negative edge to CSN time		1000			nsec
T <sub>CSI</sub>	CSN inactive time		1000			nsec
T <sub>CK</sub>	SCK period time		250			nsec
T <sub>SE</sub>	MOSI data input setup time		5			nsec
T <sub>HD</sub>	MOSI data input hold time		5			nsec
T <sub>CH</sub>	MISO data output change time		15			nsec



## MODULE DIMENTIONS

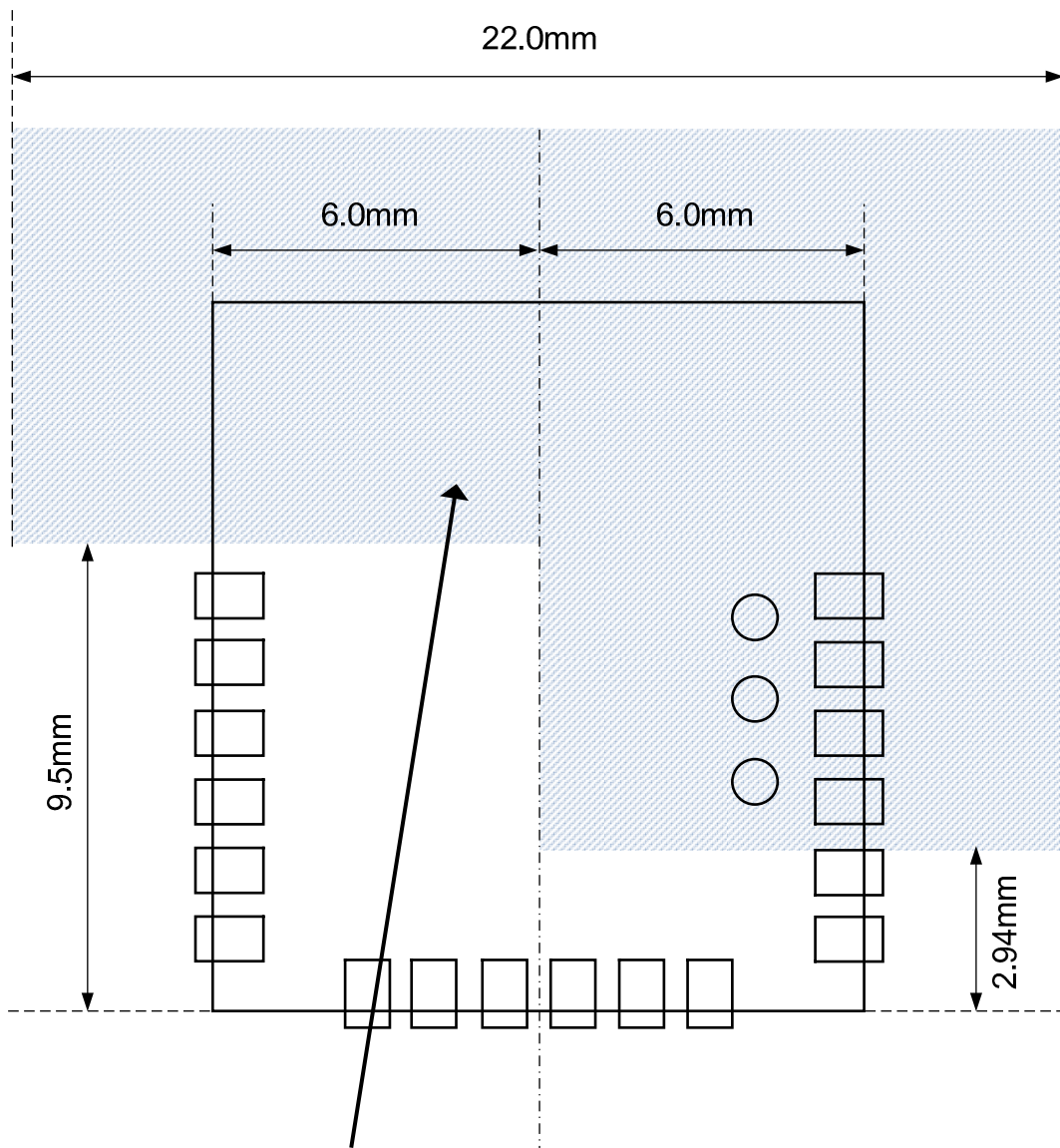


Top View



Top View

## ■ REFERENCE PCB LAYOUT/METAL KEEP-OUT AREA



Metal exclusion zone to edge of board  
No metal, no any layer, except mechanical LGA pad  
(Top View)

**Important notes to third party user for transceiver module:**

The transceiver Module complies with Part15 of the FCC rules and regulations. Compliance with the labeling requirements, FCC notices and antenna usage guidelines is required. To fulfill FCC Certification, the third party user must comply with the following regulations:

1. The third party user must ensure that the text on the external label provided with this device is placed on the outside of the final product. Contains FCC ID: 2APYU-DK7050. The enclosed device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
2. The transceiver Module may only be used with the onboard PCB antenna (internal, integral antenna) that have been tested and approved for use with this module.
3. The transceiver Module have been certified by the FCC for use with other products without any further certification. Modifications not approved by DAKAI could void the user's authority to operate the equipment.
4. This device and its antenna must not be co-located or operating in conjunction with any other antenna or transmitter.
5. Third party users must test final product to comply with unintentional radiators before declaring compliance of their final product to Part 15 of the FCC Rules.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

**FCC Statement**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.