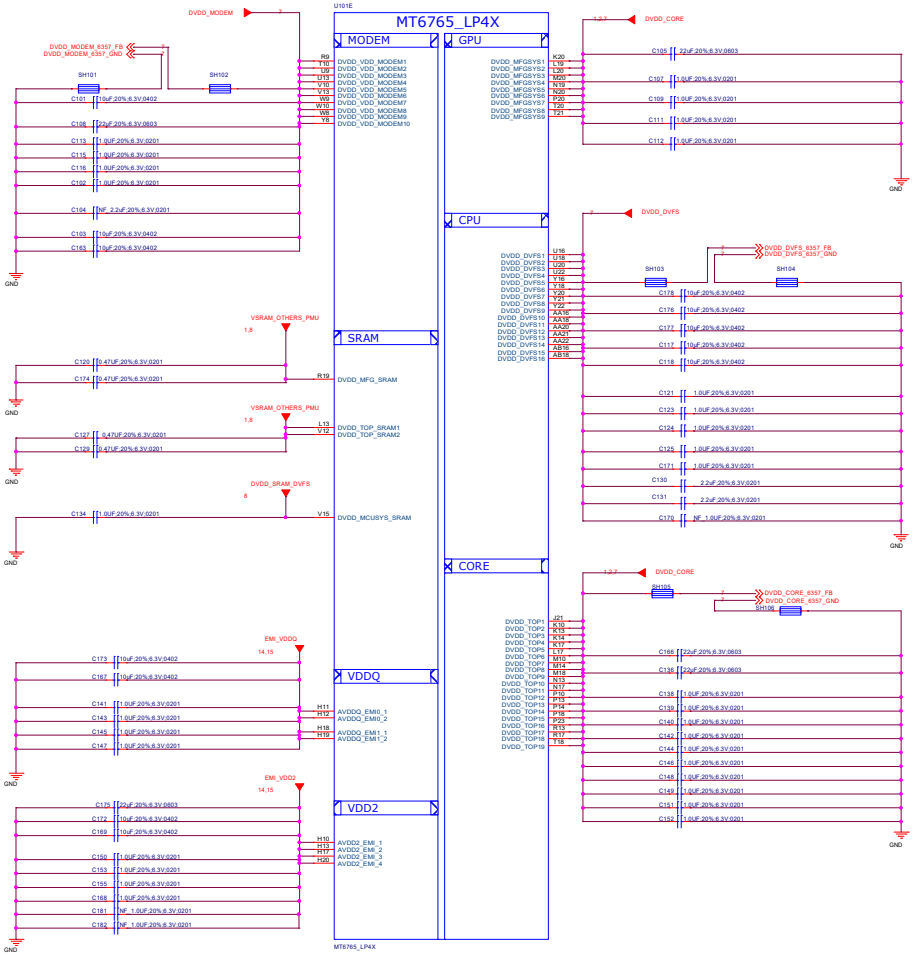
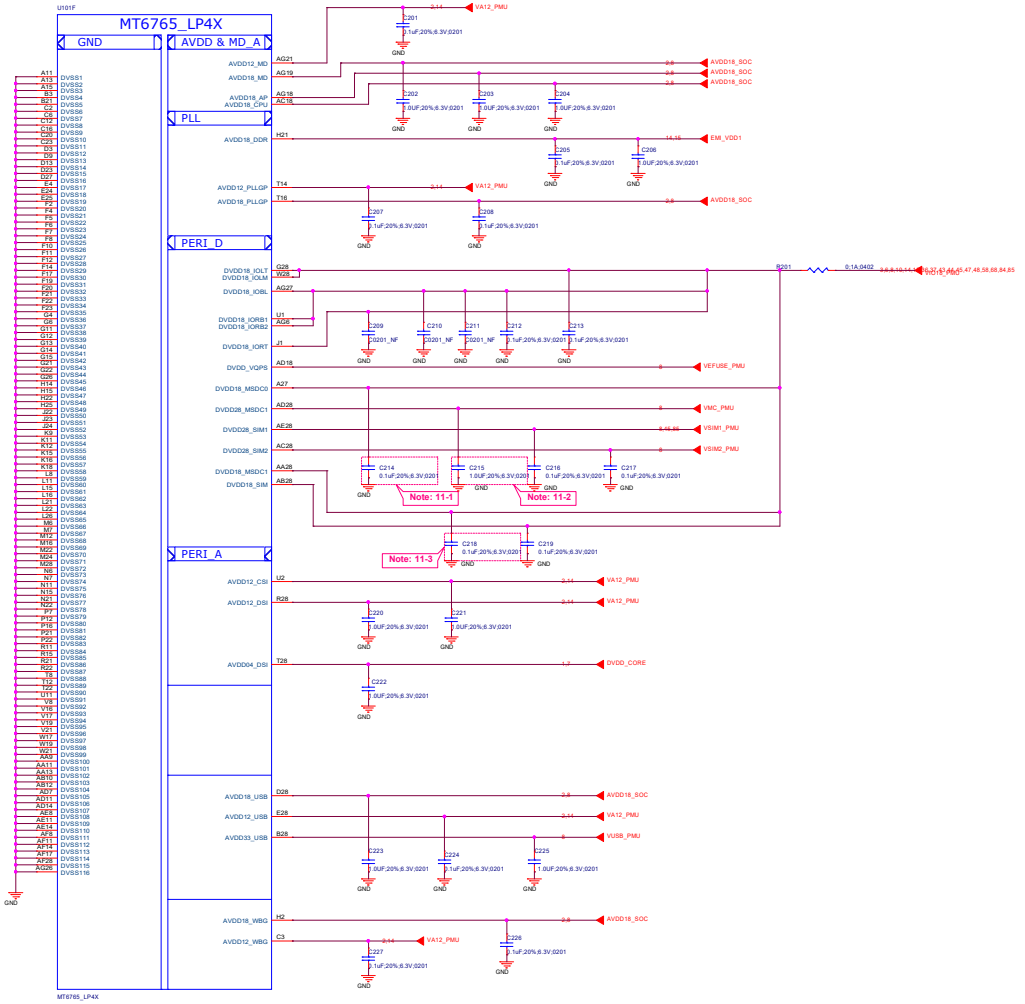


Title	02_BB_POWER_IO	REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 1 of 48



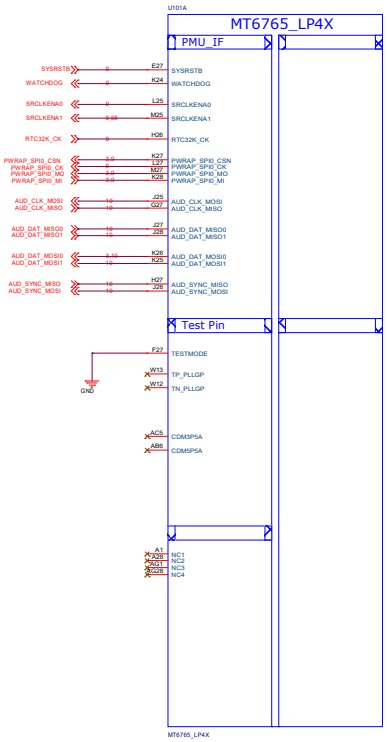
Schematic design notice of "11_BB_POWER_IO" page.

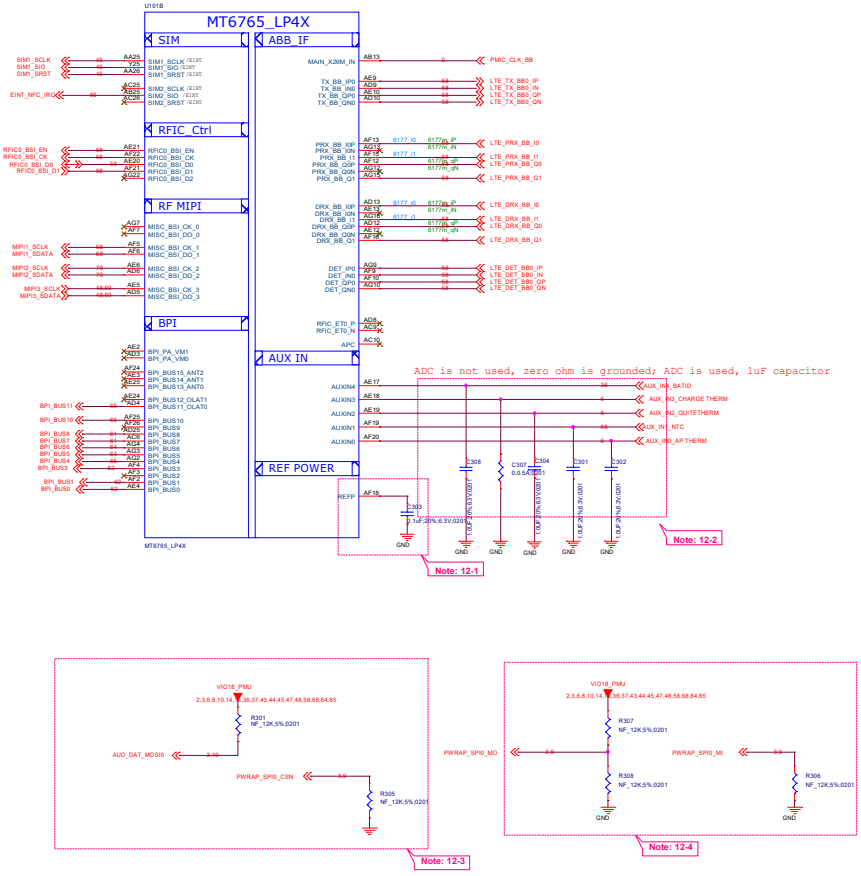
Note 11-1: C214 closed DVDD18_MSDC0 150mil

Note 11-2: C215 closed DVDD28_MSDC1 150mil

Note 11-3: C218 closed DVDD18_MSDC1 150mil

Title	02_BB_POWER_IO	REV: V10
DOCUMENT NO.:	Design Name	Size: D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 2 of 48





Schematic design notice of "12_BB_1" page.

Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-3: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pin to select which interface will be the JTAG pin out.

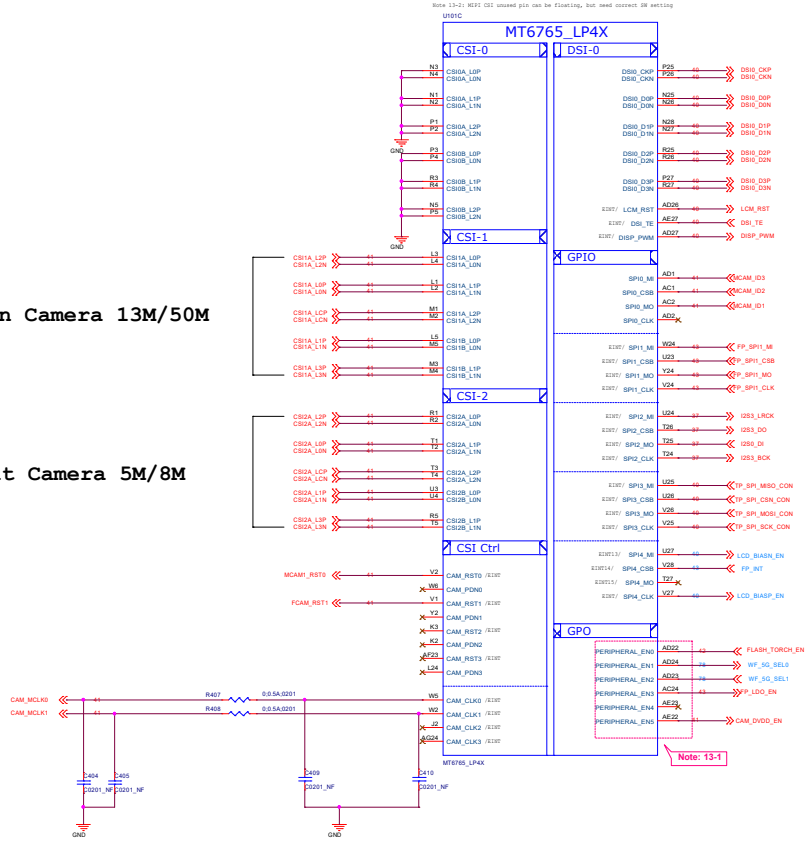
PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by ext. PU)	SPI0+EINT8	SPI1+SPI3
LO (by ext. PD)	LO	SPI0+EINT8	N/A
LO (by ext. PD)	HI (by ext. PU)	MSDC1	N/A

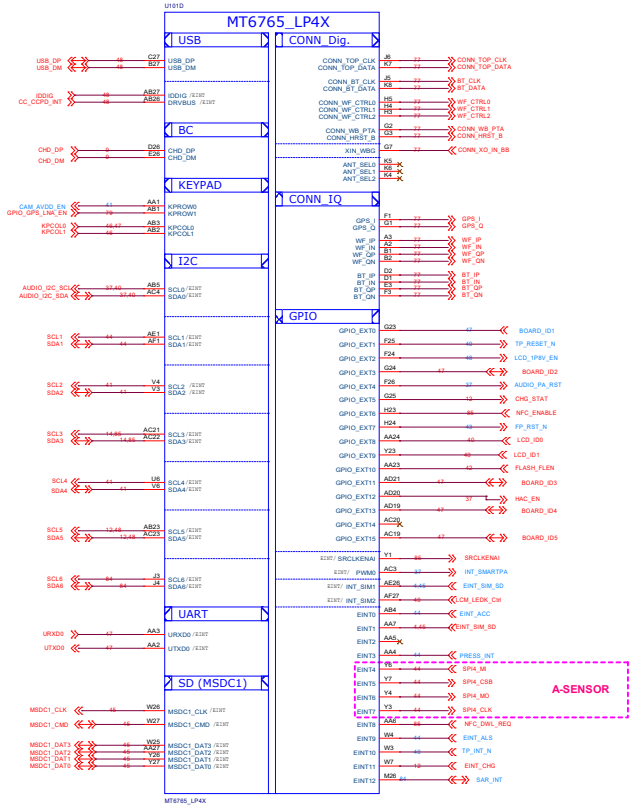
Note 12-4: PWRAP_SPI0_MI / PWRAP_SPI0_MO is DDR type feature in bootstrap

PWRAP_SPI0_MI	PWRAP_SPI0_MO	Booting interface	
default=PU	default=PD	DDR	MSDC0 pin mux
LO (by ext. PD)	LO	LPDDR3	follow LPDDR3 Ref SCH.
LO (by ext. PD)	HI (by ext. PU)	N/A	N/A
HI	LO	LPDDR4X	follow LP4X/LP4 Ref SCH.
HI	HI (by ext. PU)	LPDDR4	follow LP4X/LP4 Ref SCH.

Note 12-5: Please set unused IQ pins in NC

Title: 03_BB_1_RF&SIM_IF			REV: V10
DOCUMENT NO.: Design Name			Size: D
DEPARTMENT: WINGTECH-SH		DESIGNER: YL	
Date: Friday, February 11, 2022	Sheet 3 of 48		

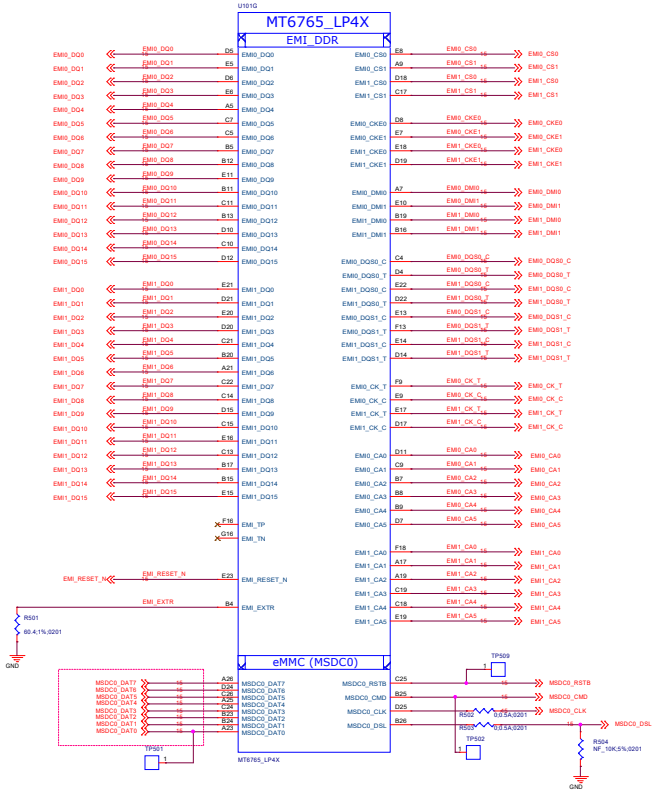




Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5]
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

Title:	04_BB_2_MIPI&GPIO		REV: V10
DOCUMENT NO.:	Design Name		Size: D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Thursday, March 31, 2022	Sheet 4 of 48	



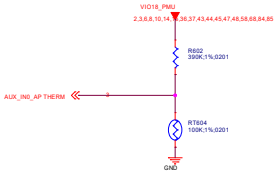
Schematic design notice of "14_BB_3" page.

Note 14-1: R501 please select 34.8 ohm (1%) resistor

Note 14-2: Please check eMCP LP3 and eMCP LP4X pin mux

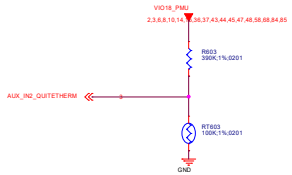
Title	05_BB_3_EMMC	REV:	V10
DOCUMENT NO.:	Design Name	Size	D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Friday, February 11, 2022	Sheet	5 of 48

The pull up ressister need to be 1% accuracy
NTC=100K



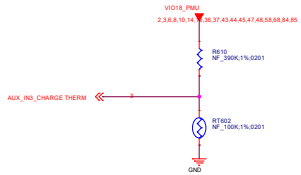
Thermistor to sense AP temperature

1. RT604must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.



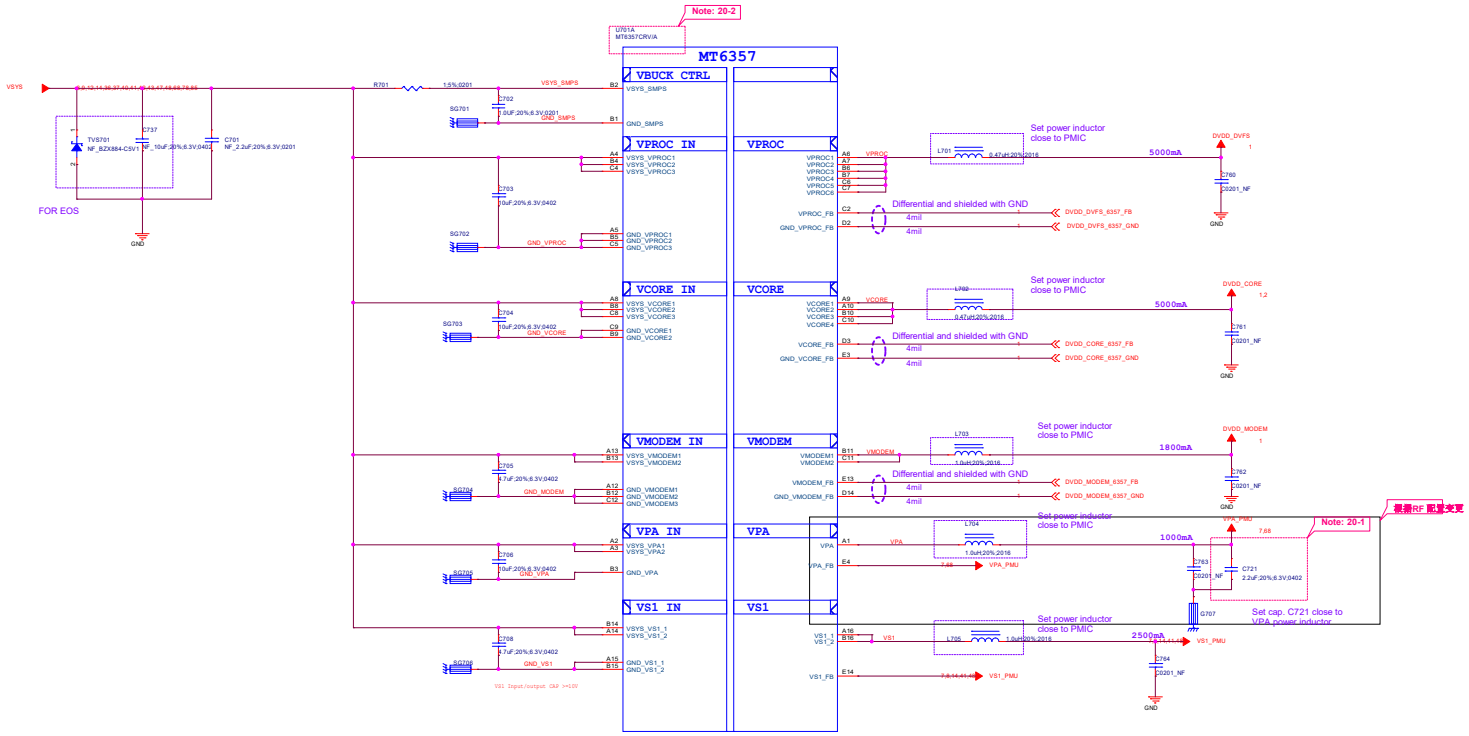
Quite thermistor

Thermistor to sense BORAD temperature



Thermistor to sense CHARGE temperature

Title	06_BB_AUXADC_Thermal	REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 6 of 48

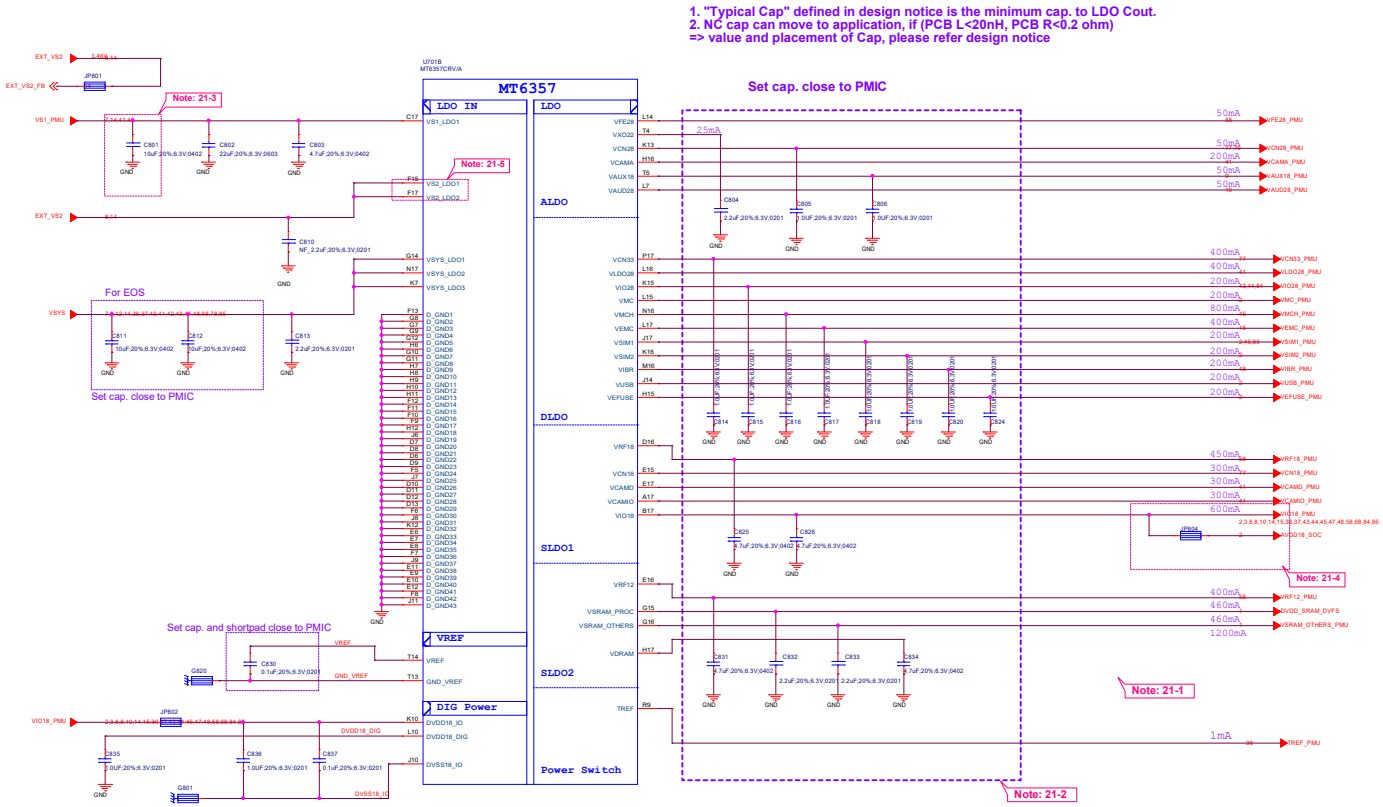


Schematic design notice of "20_POWER_MT6357_Buck"

Note 20-1: C707, please choose 0402 size

Note 20-2: For MT6765/62/61 platform, please only use MT6357CRV

Title	07_POWER_MT6357_Buck	REV:	V10
DOCUMENT NO.:	Design Name	Size	D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Friday, February 11, 2022	Sheet	7 of 48



Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

Note 21-3: Ext Buck BOM option

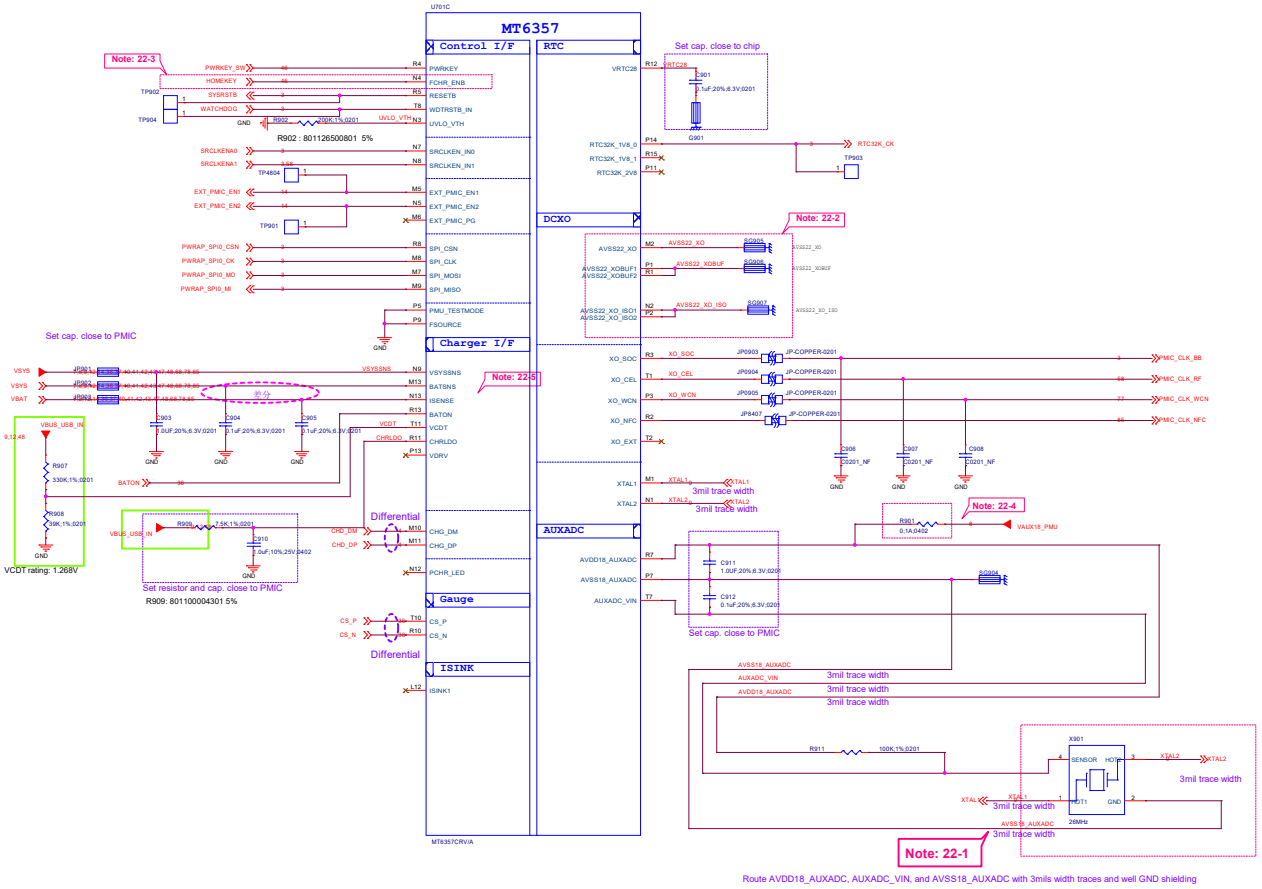
	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C801	10uF	22uF

Note 21-4: Please set R803 and R803 close to C826, making star connection among VIO18_PMU, AVDD18_SOC, and EMI_VDD1 near to LDO cap. C826

Please also refer to MT6357 design notice for further detail design information

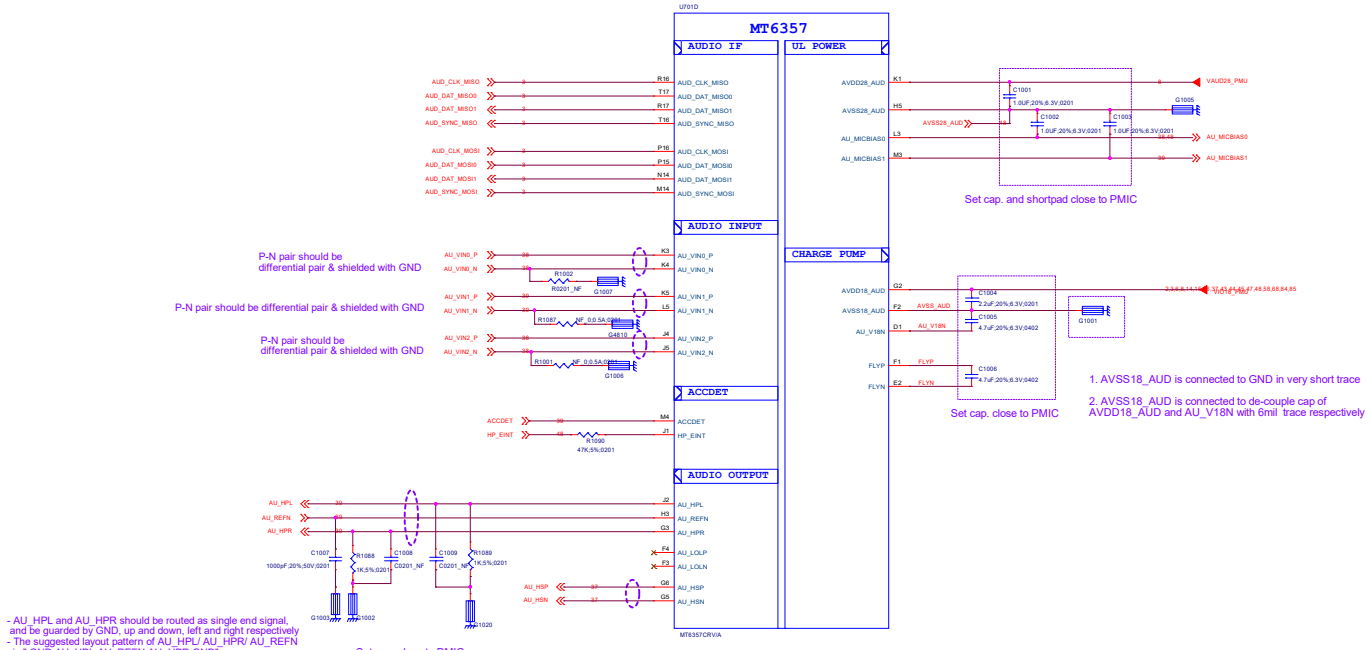
Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V

Title	08_POWER_MT6357_LDO		REV: V10
DOCUMENT NO.:	Design Name		Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Thursday, June 30, 2022	Sheet 8	of 48



Schematic design notice of "22_POWER_MT6357-IF"	
Note 22-1:	Please implement 2520 & 2016 Size TMS PCB co-layout. Please refer to MT6762_MT6357 Co-Clock Design Notice for co-layout guide
Note 22-2:	1. Please Connect P1 and R1 ball first and then to GND 2. Please Connect P2 and N2 ball first and then to GND 3. Please connect DCXO GND to main GND by independent L1-2 GND via.; DO NOT connect it through L1 GND
Note 22-3:	Let floating if disable HOMEKEY function
Note 22-4:	Please follow MT6762_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD. Please route VAUX18_PMU with well-ground sheilding if using 0 ohm to replace BEAD for AVDD18_AUXADC
Note 22-5:	Please connect to battery connector

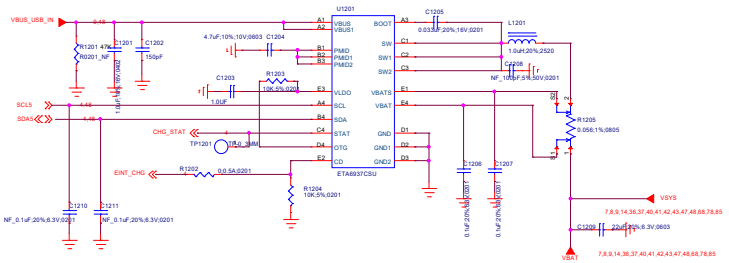
Title	09_POWER_MT6357_IF	REV:	V10
DOCUMENT NO.:	Design Name	Size	D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Friday, February 11, 2022	Sheet	9 of 48



Title	10_POWER_MT6357_Audio	REV:	V10
DOCUMENT NO.:	Design Name	Size	D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Friday, February 11, 2022	Sheet	10 of 48

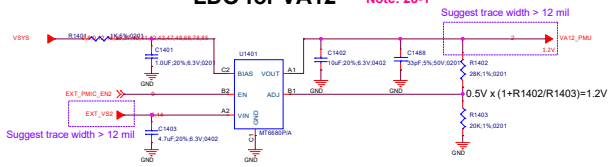
I2C Address 0x6AH
WRITE 0xD4
READ 0xD5

USB CHARGE 5V/1A

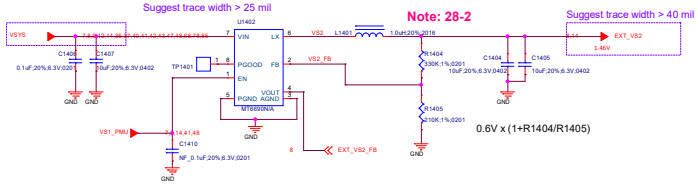


Title: 12_POWER_SubPMIC-Charger + PP			REV: V1.0
DOCUMENT NO.: Design Name			Size: D
DEPARTMENT: WINGTECH-SH		DESIGNER: YL	
WINGTECH			
Date: Wednesday, June 29, 2022	Sheet 12	of 48	

LDO for VA12 Note: 28-1

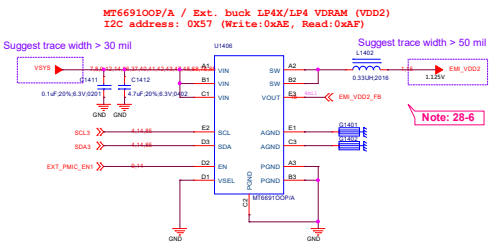


Ext. Bulk for VS2

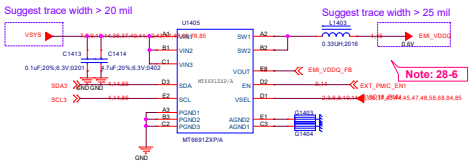


NOTE: Do not use VCAMD 1.3/1.5/1.8 when VS2 BUCK applied

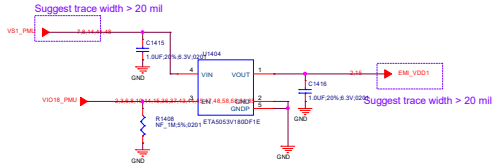
Ext. buck LPDDR4X/LPDDR4 VDRAM Note: 28-4



Ext. buck LPDDR4X VDDQ Note: 28-4

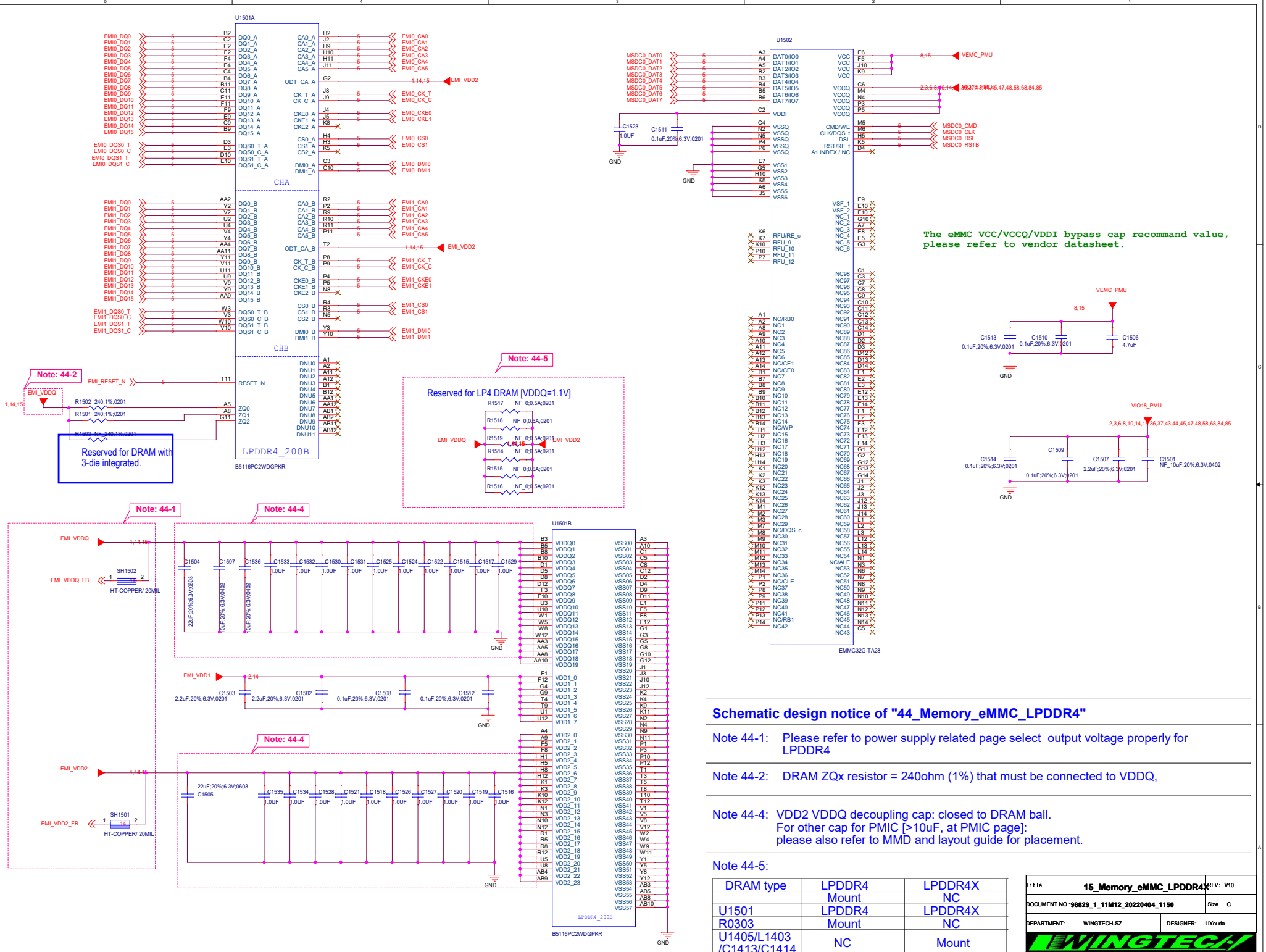


LPDDR4X/LPDDR4 VDD1 1.8V LDO Note: 28-5



Schematic design notice of "28_POWER_ThirdParty-Power"	
Note 28-1:	VA12 Layout placement please close to AP
Note 28-2:	VS2 Buck Layout placement please close to PMIC MT6357
Note 28-3:	VCN33 LDO Layout placement please close to MT6631
Note 28-4:	1.MT6691OOP/A Buck Layout Placement please close to LP4X/LP4 2.MT6691ZXP/A Buck Layout Placement please close to LP4X 3.If DRAM Application is LPDDR4 , MT6691ZXP/A NC
Note 28-5:	U2810 LDO Layout Placement Please close to LPDDR4X/LPDDR4 VDD1 power ball
Note 28-6:	For EMI_VDD2_FB and EMI_VDDQ_FB, please follow MMD rule

Title:	14_POWER_ThirdParty_Powers	REV:	V10
DOCUMENT NO.:	Design Name	Size	D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Friday, February 11, 2022	Sheet	14 of 48



Schematic design notice of "44_Memory_eMMC_LPDDR4"

Note 44-1: Please refer to power supply related page select output voltage properly for LPDDR4

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

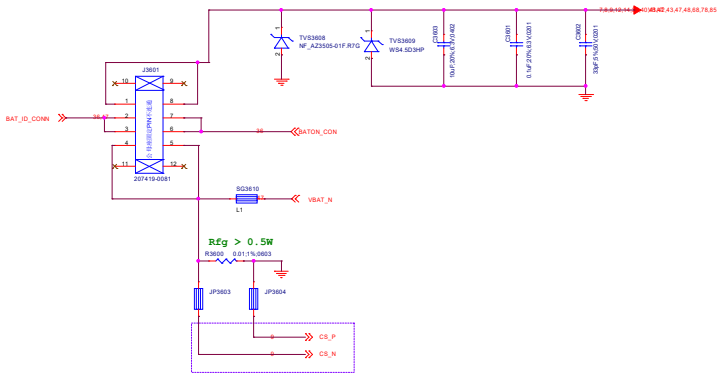
Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

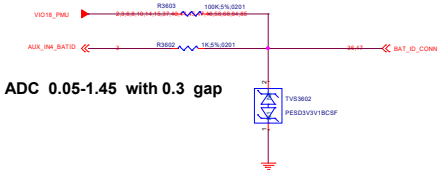
Note 44-5:

DRAM type	LPDDR4	LPDDR4X
	Mount	NC
U1501	LPDDR4	LPDDR4X
R0303	Mount	NC
U1405/L1403 /C1413/C1414	NC	Mount

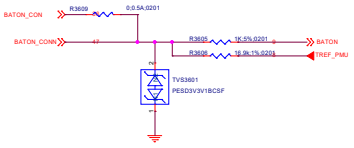
Title	15_Memory_eMMC_LPDDR4X	REV:	V10
DOCUMENT NO.:	98829_1_11M12_20220404_1150	Size	C
DEPARTMENT:	WINGTECH-SZ	DESIGNER:	LiYouda
Date:	Friday, February 11, 2022	Sheet	15 of 48

Battery Connector





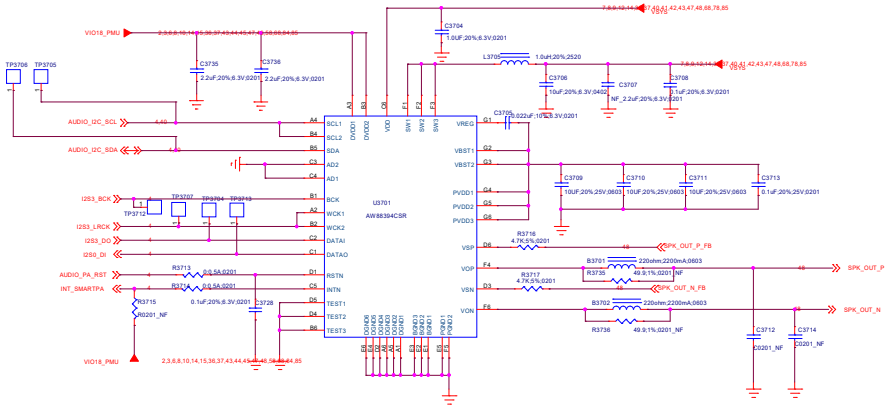
ADC 0.05-1.45 with 0.3 gap



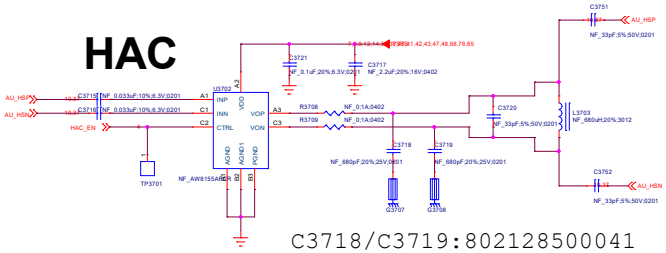
Battery pack is considered not present if BAT_ON is above 0.944*TREF

Title	36_Battery/USB IF	REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 36 of 48

Audio PA

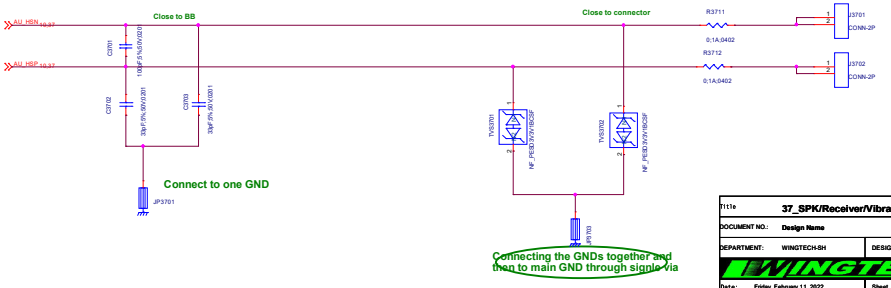


HAC



C3718/C3719:802128500041

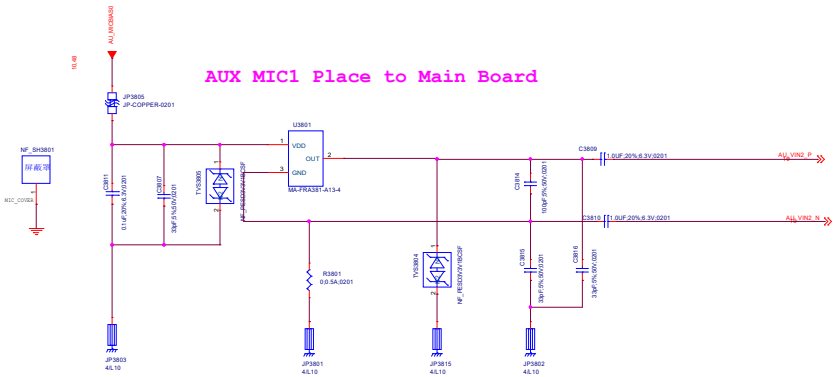
Receiver



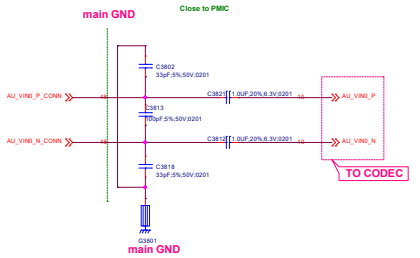
Title	37_SPK/Receiver/Vibrator	REV: V10
DOCUMENT NO.:	Design Name	Size: D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 37 of 48

WINGTECH

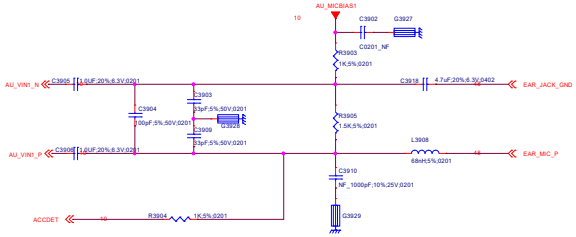
AUX MIC



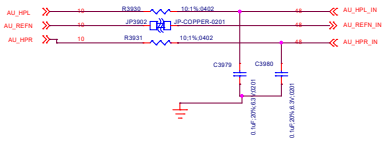
MAIN MIC



Title	38_MIC	REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 38 of 48



Earphone



Title	39_Earphone		REV: V10
DOCUMENT NO.:	Design Name		Size: D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
	WINGTECH		
Date:	Friday, February 11, 2022	Sheet	39 of 48

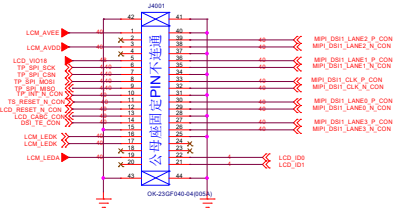
Note 62-1: Part # of BEAD6202, BEAD6203, BEAD6204 and BEAD6205 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

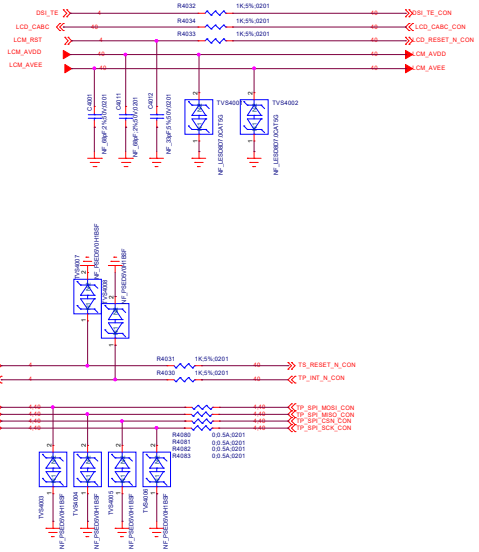
Note 62-2: Reserved Cap for CS/RS test, please double check multi-key function when used

Note 62-3:

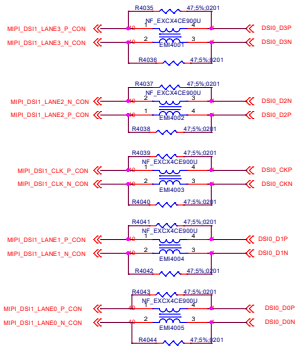
	Earphone Jack @ Main board	Earphone Jack @ Sub board
R6513	0 ohm	100nF

Note 62-4: Please Select ACC Mode for Operator Project to Pass Electrical MOS Test;

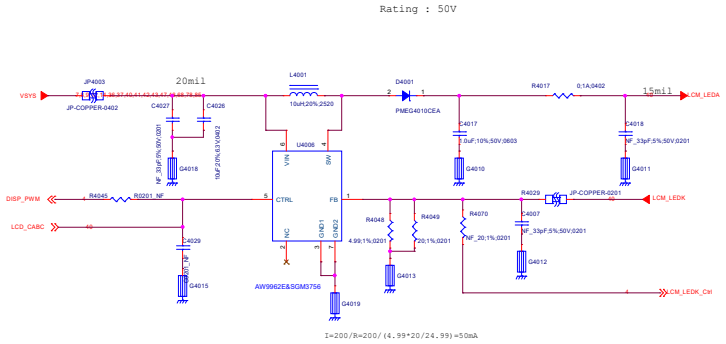




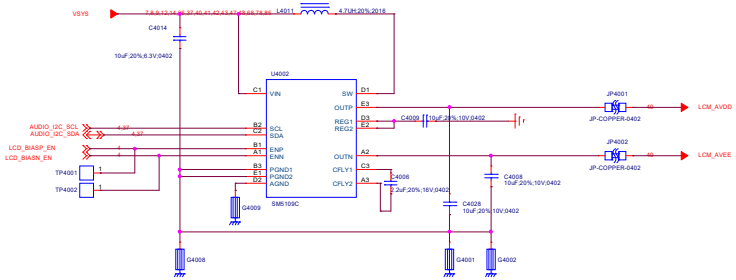
Common Mode Filter



LCD Backlight LED Driver

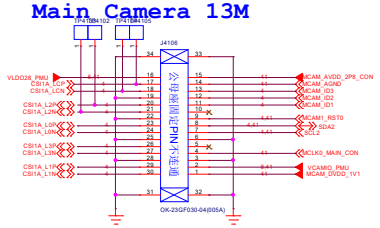


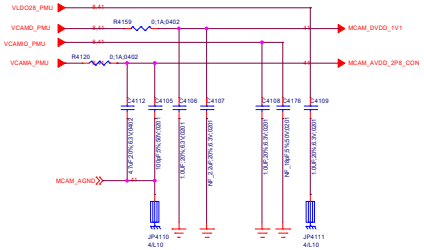
LCD Gate Drive

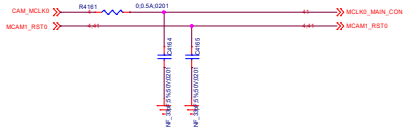


Title	40_LCD/CTP IF		REV: V1.0
DOCUMENT NO.:	Design Name		Size: D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Monday, April 04, 2022	Sheet	40 of 48

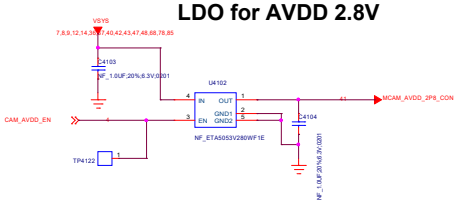
Main Camera 13M



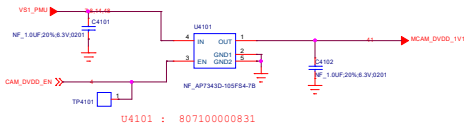


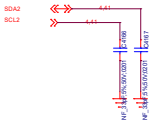


LDO for AVDD 2.8V

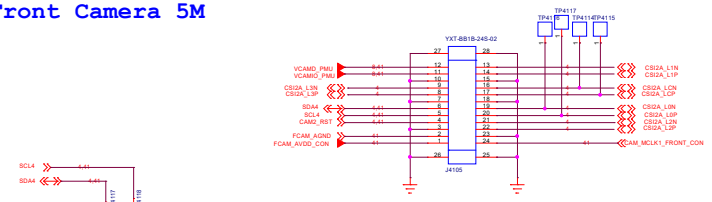


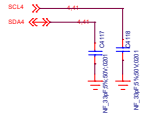
LDO for DVDD 1.1V

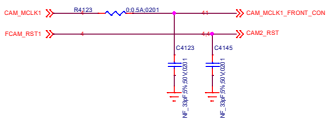


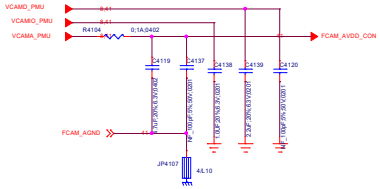


Front Camera 5M

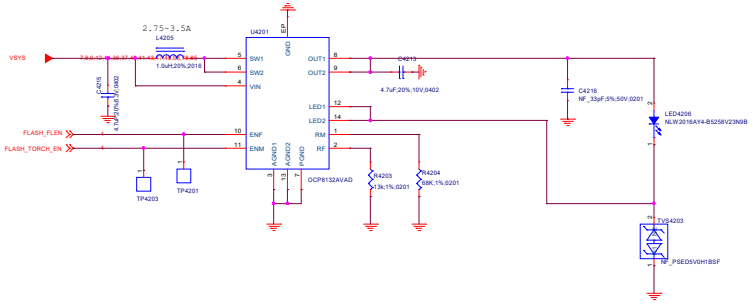






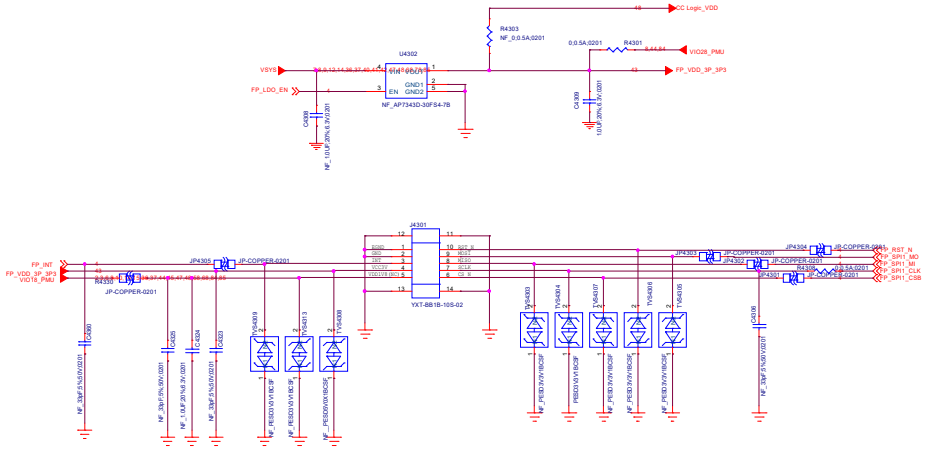


Title	41_Camera IF	REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Thursday, March 10, 2022	Sheet 41 of 48



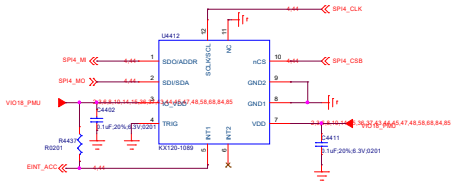
Title	42_Flash/RGB	REV: V1.0
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Wednesday, March 30, 2022	Sheet 42 of 48

Fingerprint

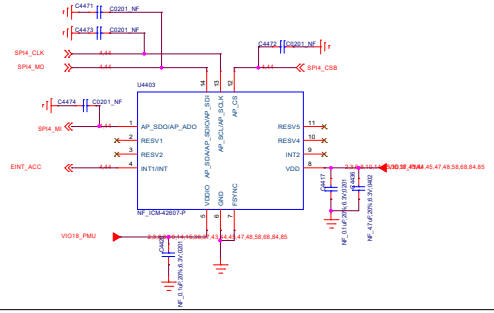


Title	43.Fingerprint	REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 43 of 48

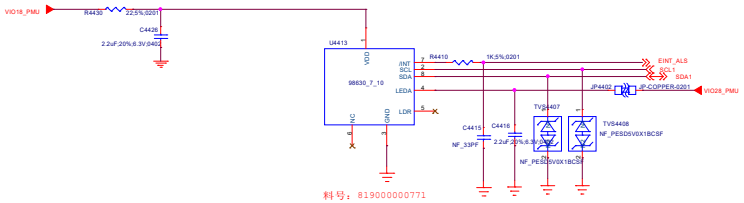
A Sensor



ACCELEROMETER Keep on but Gyro Cut up

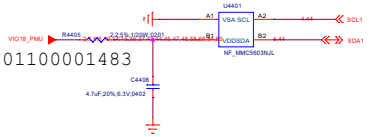


ALS+Proximity -Sensor

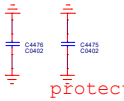


Vendor	Manufacture PN	Slave Address (7-bit)	I2C Address(8-bit)	Remark
Sensortek	STK33562	0X46	Read:0X8C Write:0X8D	

Compass



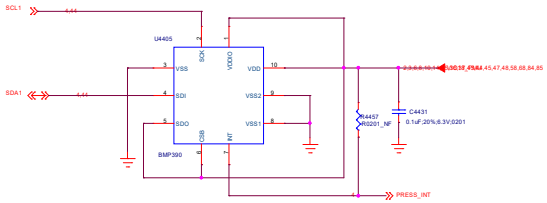
5% 801100001483



protect compass

AKM09918C	
I2C	0x19(R) 0x18(W)
MMC5603NJL	
I2C	0x61(R) 0x60(W)

Barometer Sensor

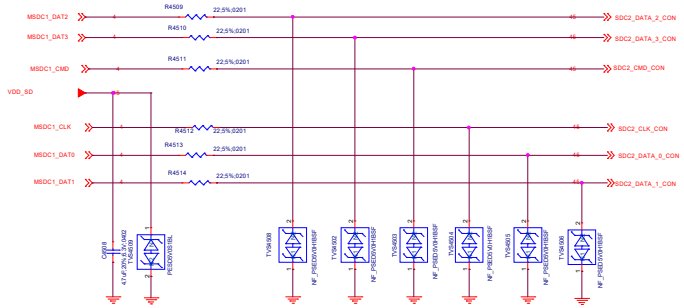


BMP390		
I2C	0x77(R) 0x76(W)	SDO--GND
ICP-10101		
I2C	0xC7(R) 0xC6(W)	
LPS22HH		
I2C	0x5D(R) 0x5C(W)	

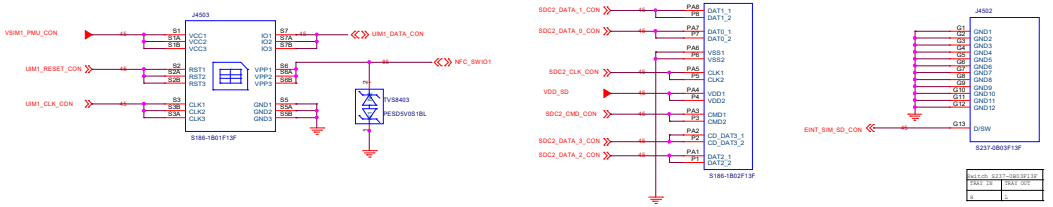
Title	44_Sensor		REV: V10
DOCUMENT NO.:	Design Name		Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Friday, February 11, 2022	Sheet	44 of 48

SIM/TF IF

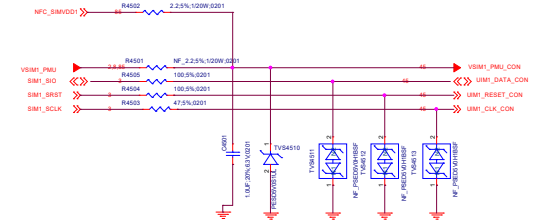
TF CARD

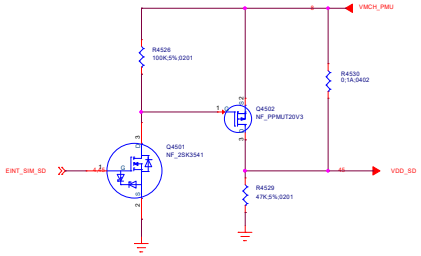


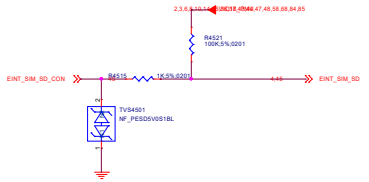
TF+SIM1 CARD



USIM1



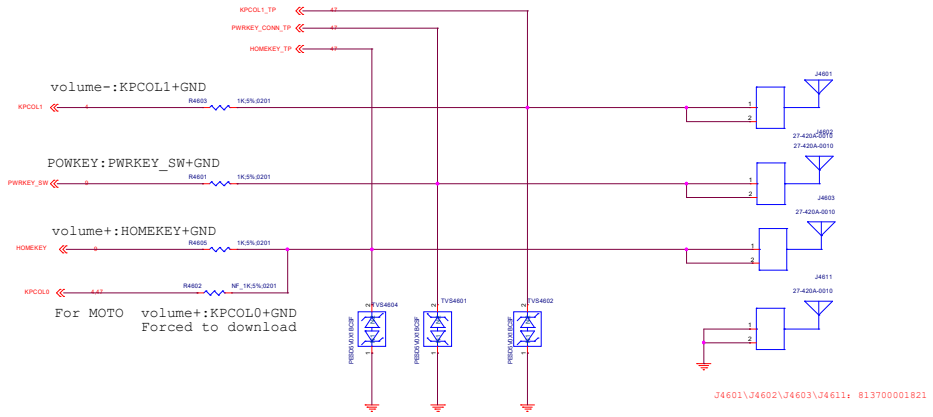




Title	45_SIM/TF IF		REV: V1.0
DOCUMENT NO.:	Design Name		Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Friday, February 11, 2022	Sheet	45 of 48

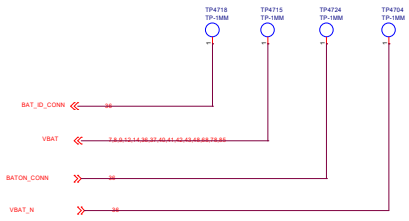
Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY

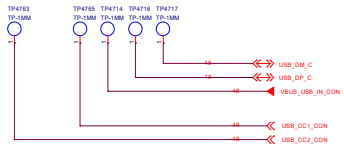


Title	46_Sidekey	REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 46 of 48

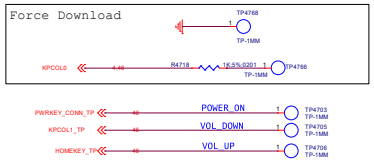
BATTERY



USB

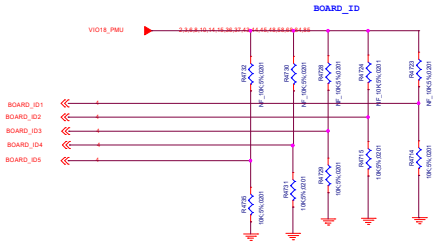


KEYS

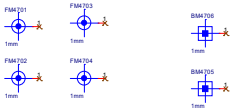


UART

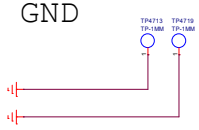
BOARD ID



MARK Waterproof



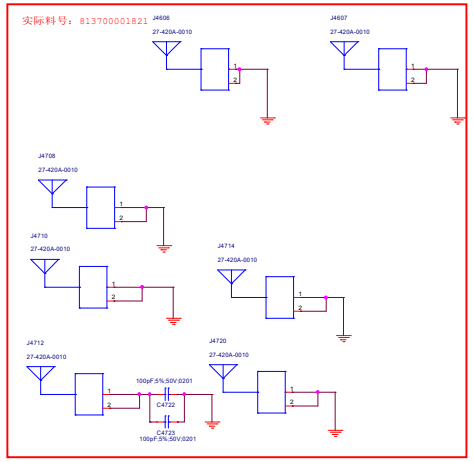
GND

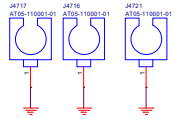


MIC LABLE

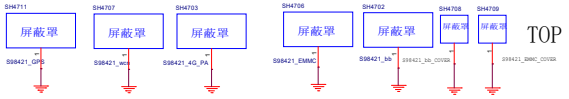
SN Label

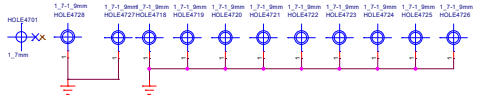
GND SHRAPNEL





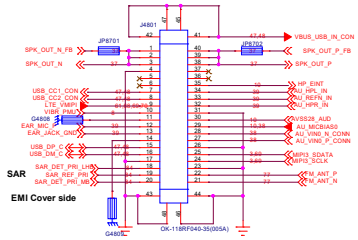
SHIELDING



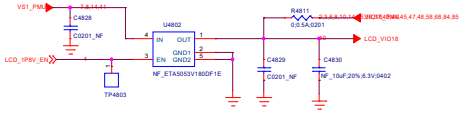


Title	47_Testpoint/Shielding/GND	REV:	V10
DOCUMENT NO.:	Design Name	Size	D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Friday, February 11, 2022	Sheet	47 of 48

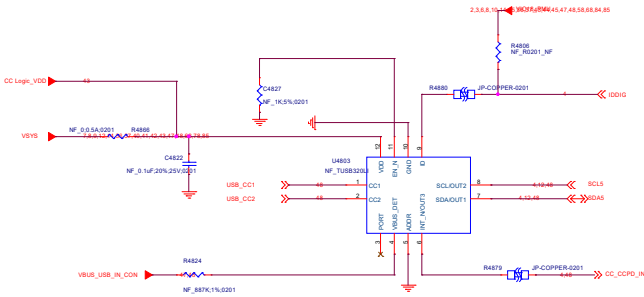
SUB CONNECTOR



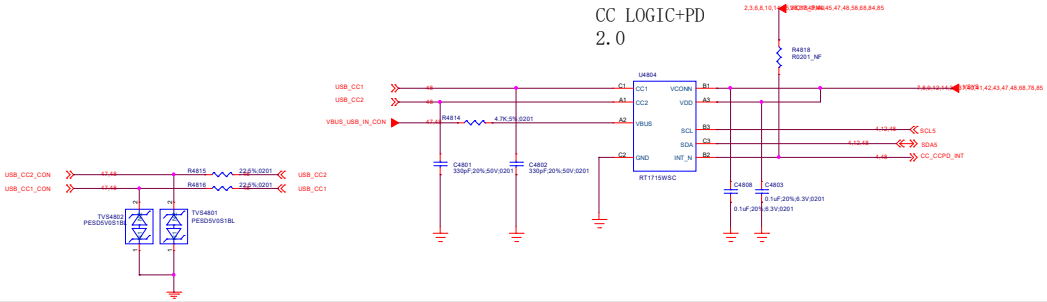
Reserve for ESD



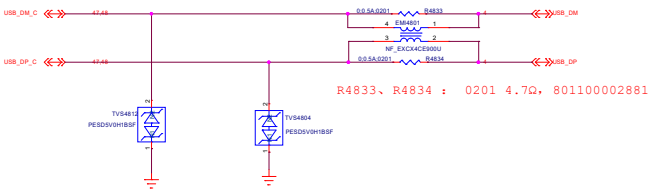
CC LOGIC



CC LOGIC+PD 2.0

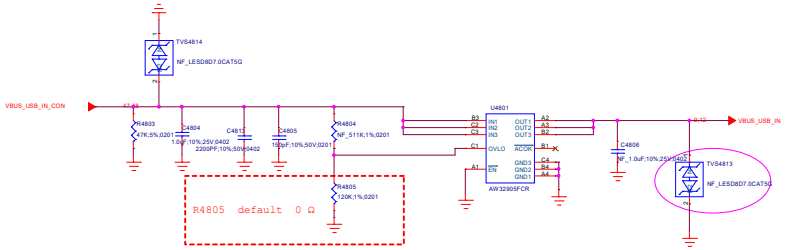


USB_DP DM



R4833、R4834 ： 0201 4.7Ω, 801100002881

OVP



R4805 default 0 Ω

Title	48_Sub PCB IF	REV: V1.0
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Friday, February 11, 2022	Sheet 48 of 48

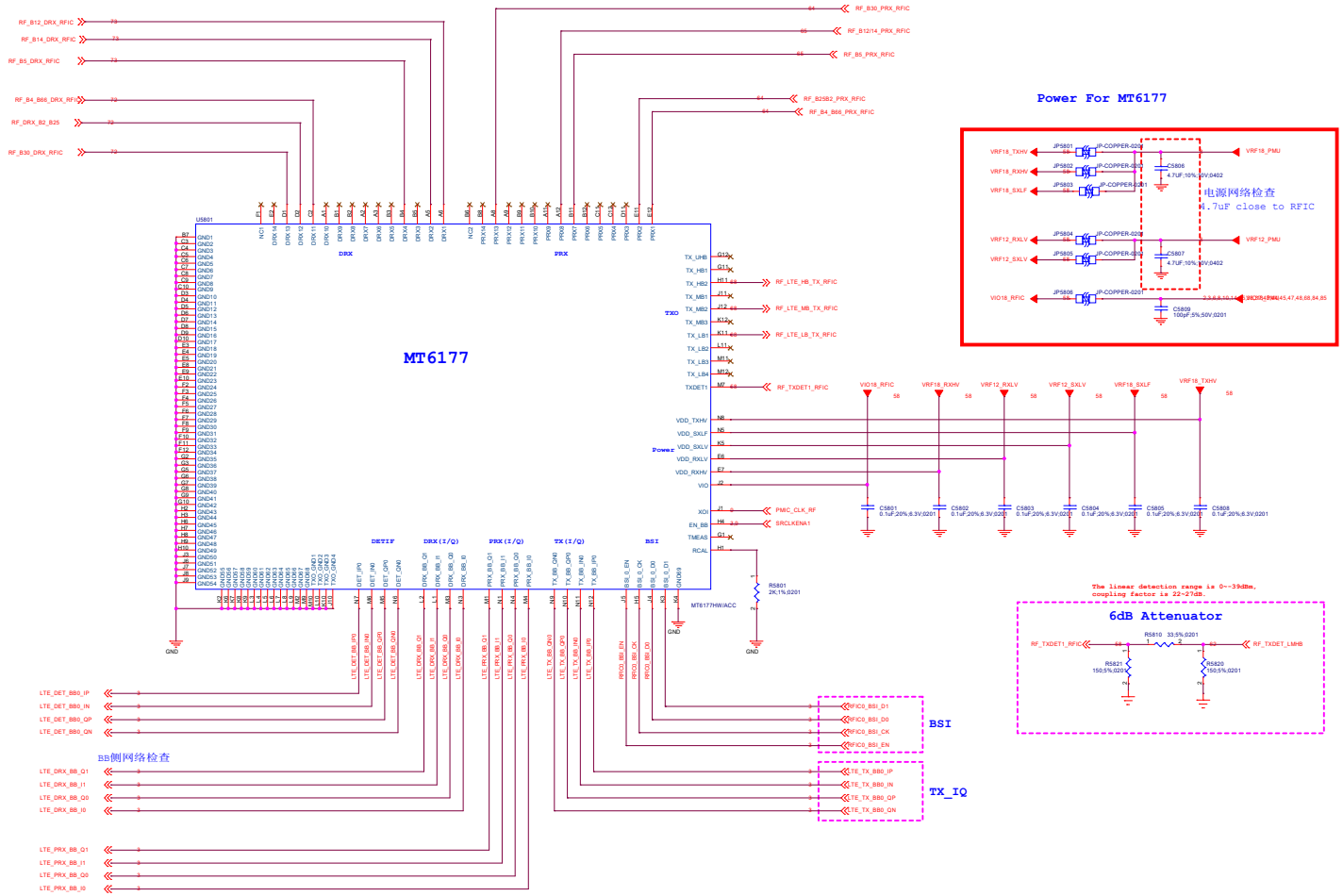
WINGTECH

RX PORTMAPPING

								HB/UHB		MB/HB(2)		MB/HB(1)		LB/MB(4)		LB/MB(3)		LB/MB(2)		LB/MB(1)	
Area(SKU)	2G	3G	4G	4G Roaming	UL intra-band CA	DL intra-band CA	DL inter-band CA	PRX14	PRX13	PRX12	PRX11	PRX10	PRX9	PRX8	PRX7	PRX6	PRX5	PRX4	PRX3	PRX2	PRX1
Ellis RF1	B2/B3/B5/B8	B1/B2/B4/B5/B8	B2/B4/B5/B12/B13/B14/B30/B66		-	-	-	-	30	1	4(66)	-	-	3	2	-	13	5	14	8	12(13)
Ellis RF2	B2/B3/B5/B8	B1/B2/B4/B5/B8	B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B25/B26/B30/B41(full)/B66/B71		CA_41C	CA_2C.CA_2A-2A.CA_4A-4A.CA_5B. CA_7C.CA_7A-7A.CA_12B. CA_25A-25A. CA_39C.CA_41C.CA_41A-41A. CA_66B.CA_66C.CA_66A-66A	CA_2A-5A.CA_5A-7A.CA_7A-12A. CA_25A-26A.CA_26A-41A. CA_2A-7A.CA_25A-41A need compatible design	-	7	1	4(66)	-	41	3	2(25)	-	13	5(26)	71	8	12(17/13)
Tanga RF1	B2/B3/B5/B8	B1/B2/B4/B5/B8	B2/B4/B5/B12/B13/B14/B30/B66		-	CA_2C.CA_2A-2A.CA_4A-4A.CA_5B. CA_66B.CA_66C.CA_66A-66A. Cricket/ATT disable 2C4 by SE	CA_2A-5A.CA_13A-2A	-	30	1	4(66)	-	-	3	2	-	13	5	14	8	12
Tanga RF2	B2/B3/B5/B8	B1/B2/B4/B5/B8	B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B25/B26/B30/B41(full)/B66/B71		CA_41C	CA_2C.CA_2A-2A.CA_4A-4A.CA_5B. CA_7C.CA_7A-7A.CA_12B. CA_25A-25A. CA_39C.CA_41C.CA_41A-41A. CA_66B.CA_66C.CA_66A-66A	CA_2A-5A.CA_5A-7A.CA_7A-12A. CA_25A-26A.CA_26A-41A. CA_2A-7A.CA_25A-41A need compatible design	-	7	1	4(66)	-	41	3	2(25)	-	13	5(26)	71	8	12(17)

								HB/UHB		MB/HB(2)		MB/HB(1)		LB/MB(4)		LB/MB(3)		LB/MB(2)		LB/MB(1)	
Area(SKU)	2G	3G	4G	4G Roaming	UL intra-band CA	DL intra-band CA	DL inter-band CA	DRX14	DRX13	DRX12	DRX11	DRX10	DRX9	DRX8	DRX7	DRX6	DRX5	DRX4	DRX3	DRX2	DRX1
Ellis RF1	B2/B3/B5/B8	B1/B2/B4/B5/B8	B2/B4/B5/B12/B13/B14/B30/B66		-	-	-	-	30	-	1(4/66)	-	-	3	2	-	-	5	14	8	12(13)
Ellis RF2	B2/B3/B5/B8	B1/B2/B4/B5/B8	B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B25/B26/B30/B41(full)/B66/B71		CA_41C	CA_2C.CA_2A-2A.CA_4A-4A.CA_5B. CA_7C.CA_7A-7A.CA_12B. CA_25A-25A. CA_39C.CA_41C.CA_41A-41A. CA_66B.CA_66C.CA_66A-66A	CA_2A-5A.CA_5A-7A.CA_7A-12A. CA_25A-26A.CA_26A-41A. CA_2A-7A.CA_25A-41A need compatible design	-	7	-	1(4/66)	-	41	3	2(25)	-	-	5(26)	71	8	12(17/13)
Tanga RF1	B2/B3/B5/B8	B1/B2/B4/B5/B8	B2/B4/B5/B12/B13/B14/B30/B66		-	CA_2C.CA_2A-2A.CA_4A-4A.CA_5B. CA_66B.CA_66C.CA_66A-66A. Cricket/ATT disable 2C4 by SE	CA_2A-5A.CA_13A-2A	-	30	-	1(4/66)	-	-	3	2	-	-	5	14	8	12(13)
Tanga RF2	B2/B3/B5/B8	B1/B2/B4/B5/B8	B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B25/B26/B30/B41(full)/B66/B71		CA_41C	CA_2C.CA_2A-2A.CA_4A-4A.CA_5B. CA_7C.CA_7A-7A.CA_12B. CA_25A-25A. CA_39C.CA_41C.CA_41A-41A. CA_66B.CA_66C.CA_66A-66A	CA_2A-5A.CA_5A-7A.CA_7A-12A. CA_25A-26A.CA_26A-41A. CA_2A-7A.CA_25A-41A need compatible design	-	7	-	1(4/66)	-	41	3	2(25)	-	-	5(26)	71	8	12(17/13)

Title: SDM653+WTR3925 with CA平台规格图	REV: V10
DOCUMENT NO.: WINGTECH-SH-HW-SCH001	Size: D
DEPARTMENT: ShangHai-Hardware	DESIGNER: WHF+HBQ
Date: 2018-03-15	Sheet: of



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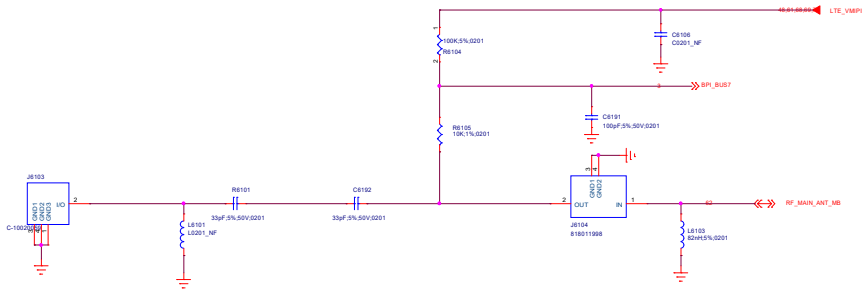
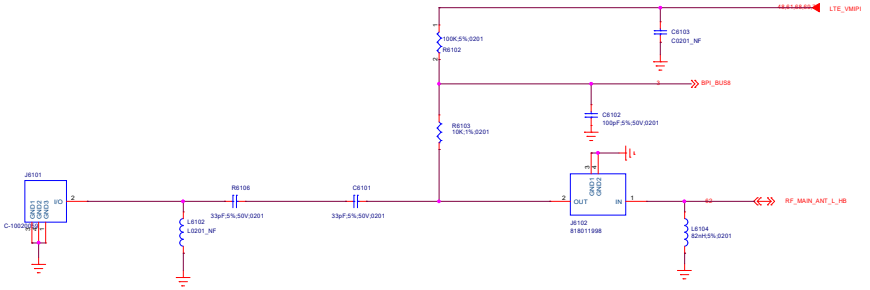
DEPARTMENT:	DEPARTMENT = WINGTECH SDESIGNER: DESIGNER = PENGLIZHONG
Date:	Page Modify Date = Friday, February 11, 2022 Sheet 58 of 48





Title	SDM653+WTR3925 witch CA平台层级图	REV: V10
DOCUMENT NO.:	WINGTECH-SH-HW-SCH001	Size D
DEPARTMENT:	ShangHai-Hardware	DESIGNER: WHF+HBQ
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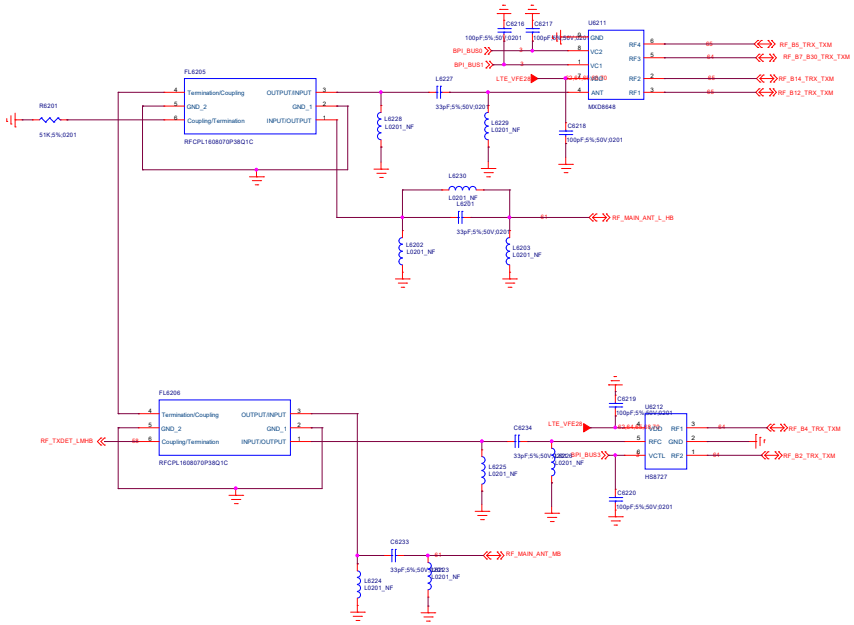

Title	SDM653+WTR3925 witch CA平台采样图	REV: V10
DOCUMENT NO.:	WINGTECH-SH-HW-SCH001	Size D
DEPARTMENT:	ShangHai-Hardware	DESIGNER: WHF+HBQ
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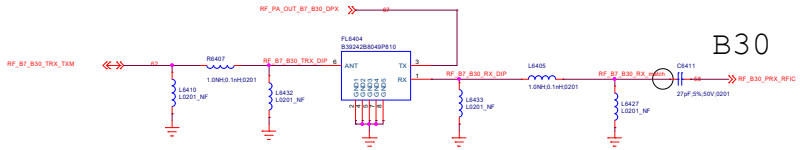

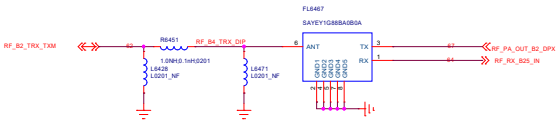

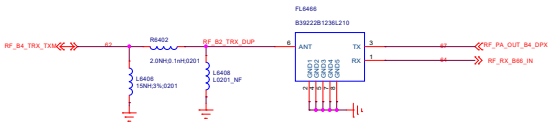

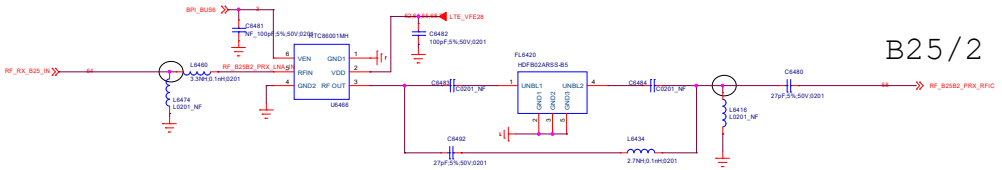

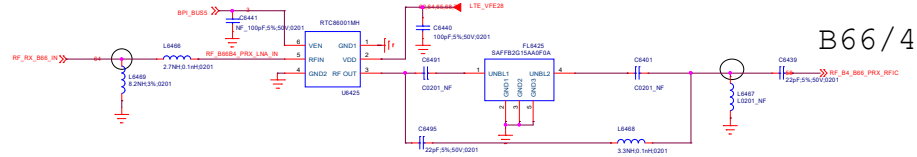

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DOCUMENT NO.:	WINGTECH-SH-HW-SCH001	Size D
DEPARTMENT:	ShangHai-Hardware	DESIGNER: WHF+HBQ
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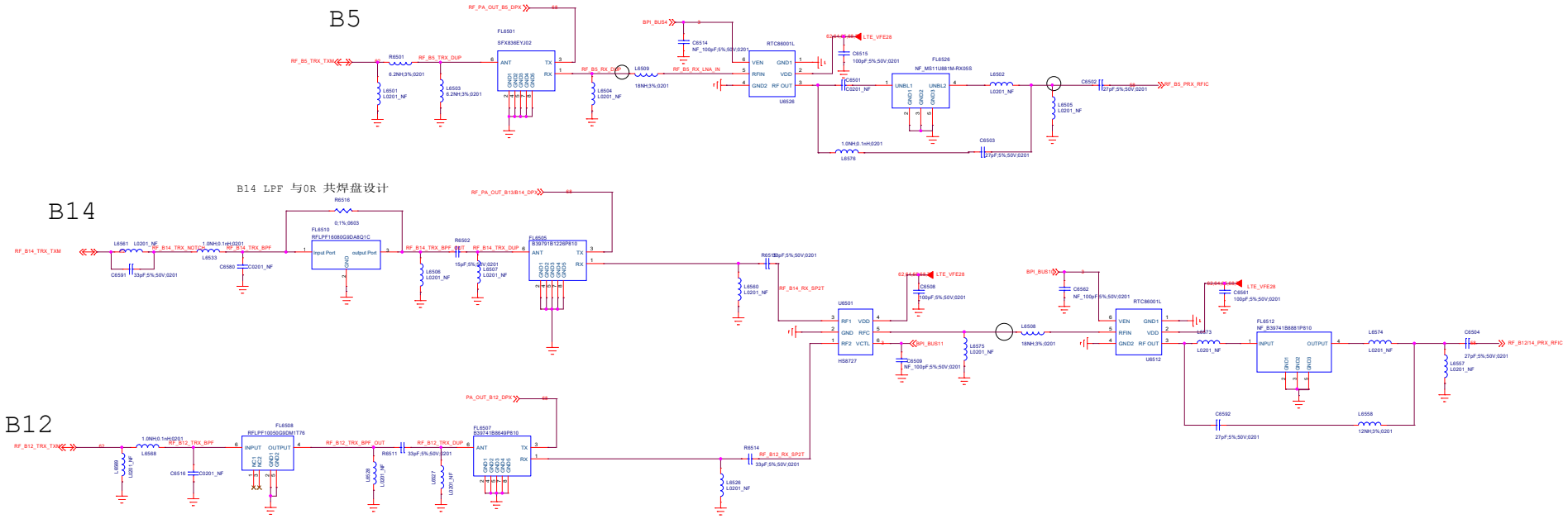

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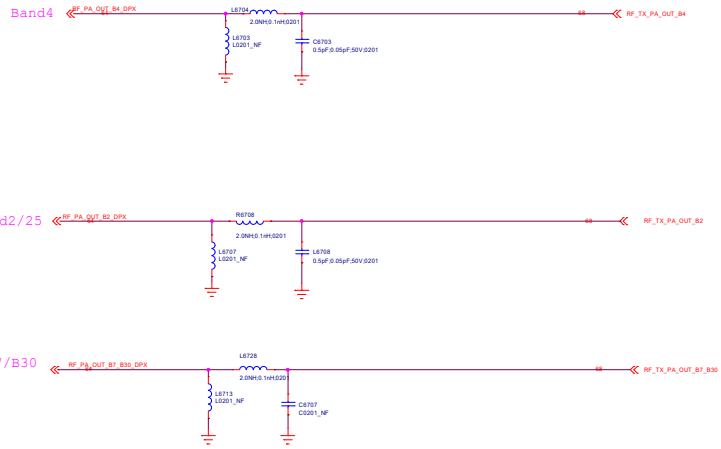
DOCUMENT NO.:	WINGTECH-SH-HW-SCH001	Size D
DEPARTMENT:	ShangHai-Hardware	DESIGNER: WHF+HBQ
WINGTECH		
Date:	2018-03-15	Sheet of



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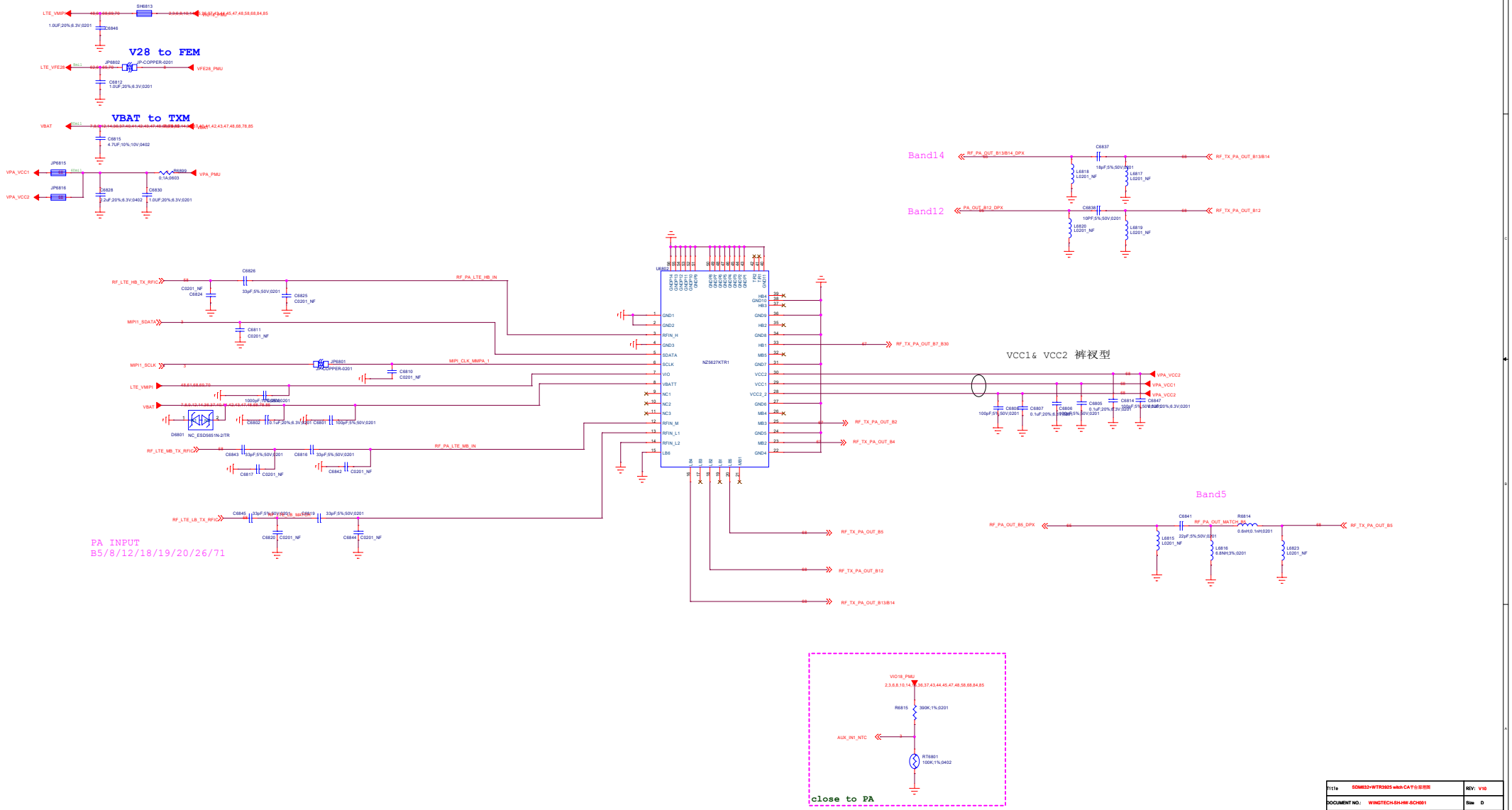
DEPARTMENT: ShangHai-Hardware	DESIGNER: WHF+HBQ	
WINGTECH		
Date: 2018-03-15	Sheet: of	

Power Net Connection



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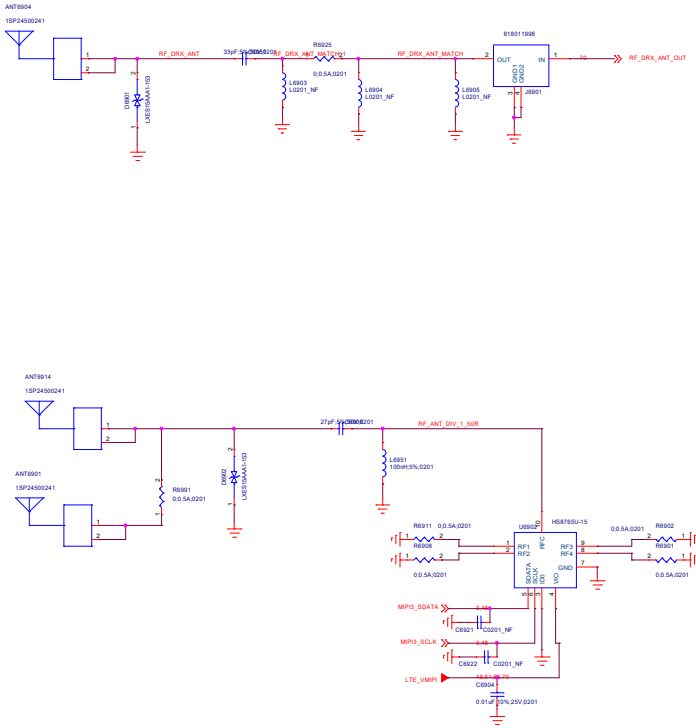
DESIGNER:	WHF+HBQ
Date:	2018-03-15
Sheet	of



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DOCUMENT NO.:	WINGTECH-SH-HW-SCH001	Size D
DEPARTMENT:	ShangHai-Hardware	DESIGNER: WHF+HBQ
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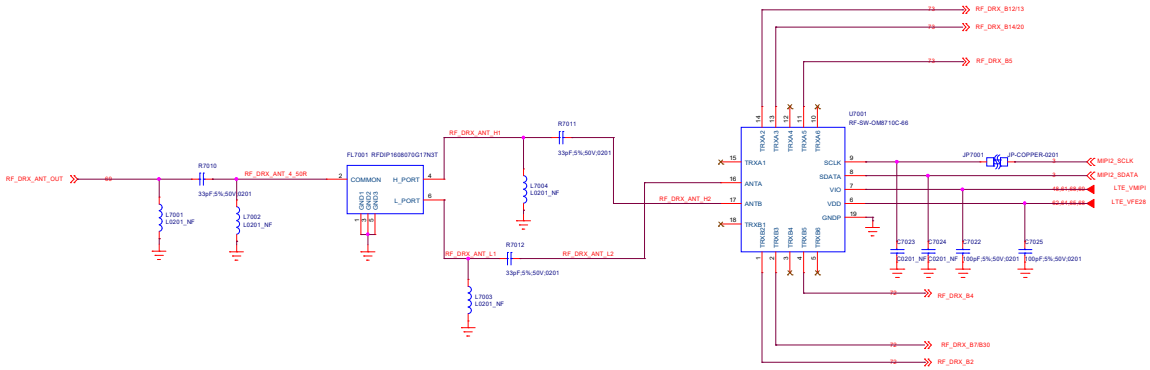
Date: 2018-03-15		Sheet of



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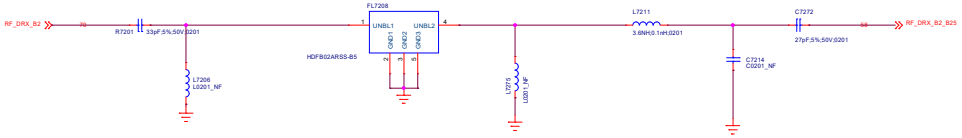
B66/4

B25/2



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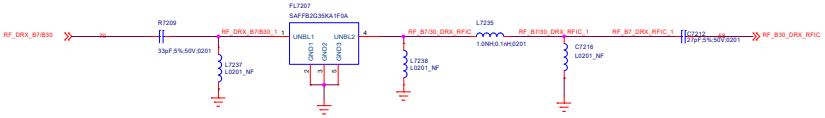

Title	SDM653+WTR3925 witch CA平台层级图	REV: V10
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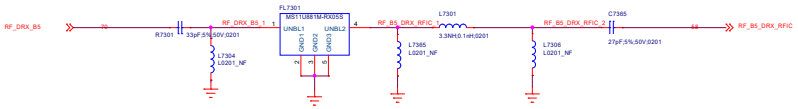
DEPARTMENT:	ShangHai-Hardware	DESIGNER: WHF+HBQ
Date:	2018-03-15	Sheet of

B5



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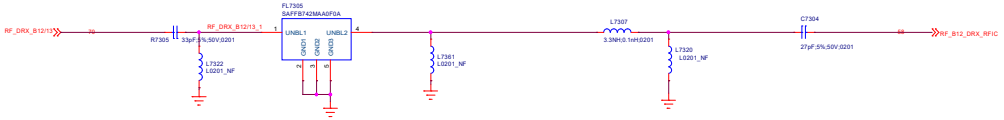

B14/B20

Title	SDM653+WTR3925 witch CA平台采用图	REV: V10
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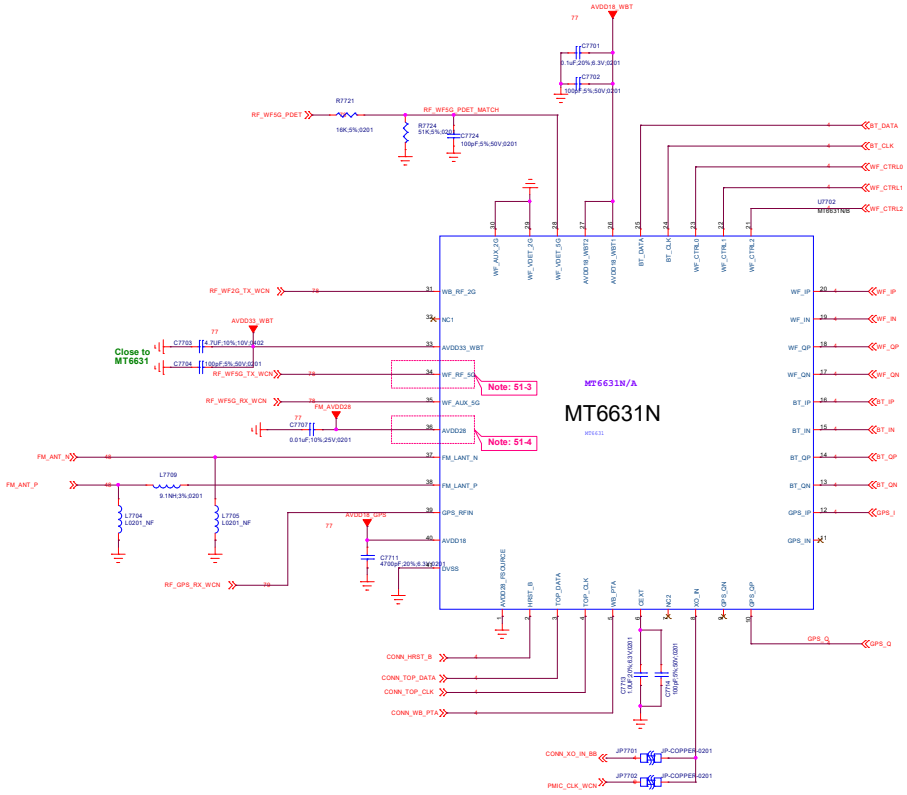
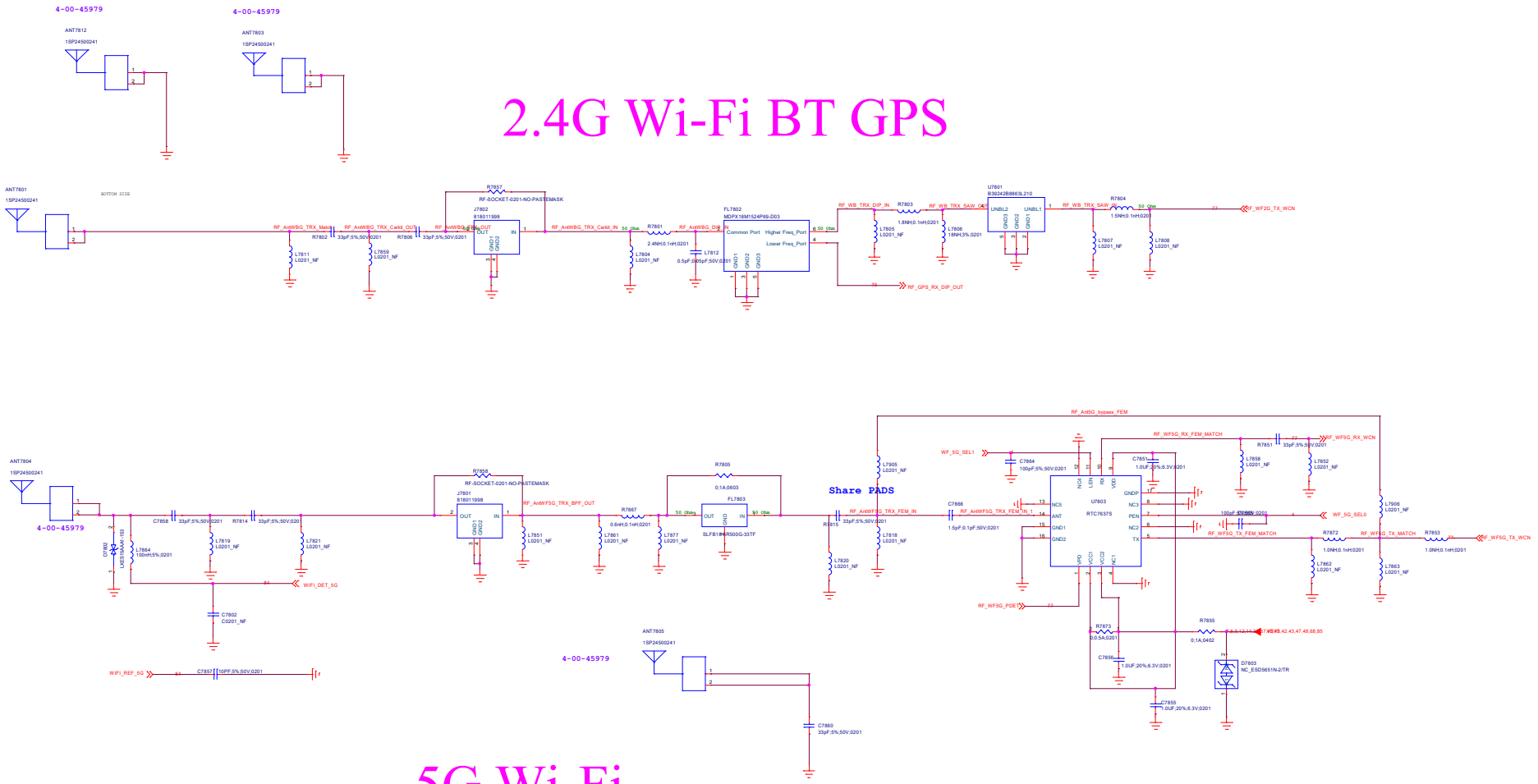
Date:	2018-03-15	Sheet of



Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"	
Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6762 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support
Note 51-5:	If WiFi 5G were no need, VCN33 could be chosen from PMIC output (VCN33_PMU)

Title:	Page Name = 77_WCN_MT6631	REV: V10
DOCUMENT NO.:	Design Name = 96829_1_119812_20220401_0959	
DEPARTMENT:	DEPARTMENT = WINGTECH-SZ	DESIGNER: DESIGNER = PENGLIZHONG
Date:	Page Modify Date = Friday, February 11, 2022	Sheet 77 of 48



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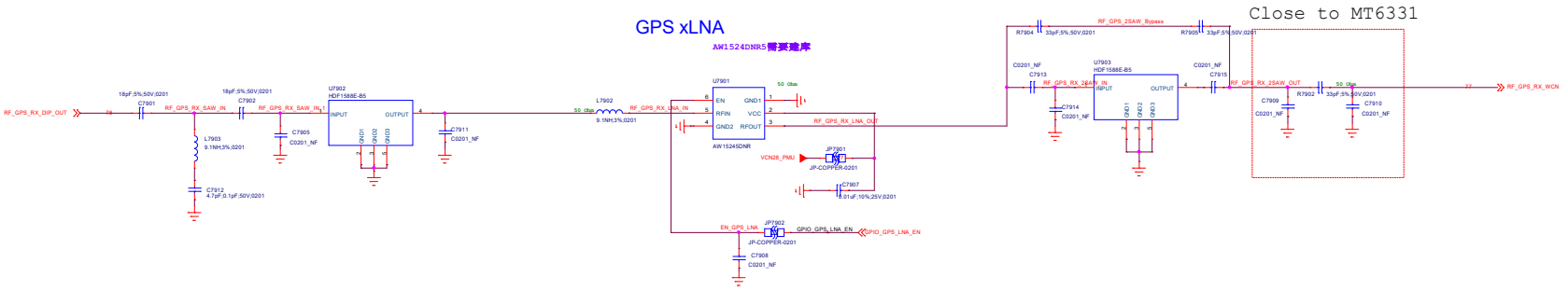
DOCUMENT NO.: Design Name		Size: D
DEPARTMENT: WINGTECH-SH	DESIGNER: PENGLIZHONG	
WINGTECH		
Date: Saturday, July 02, 2022	Sheet 78 of 48	



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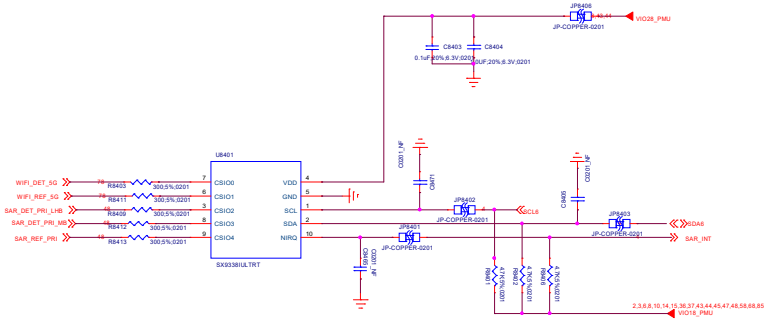
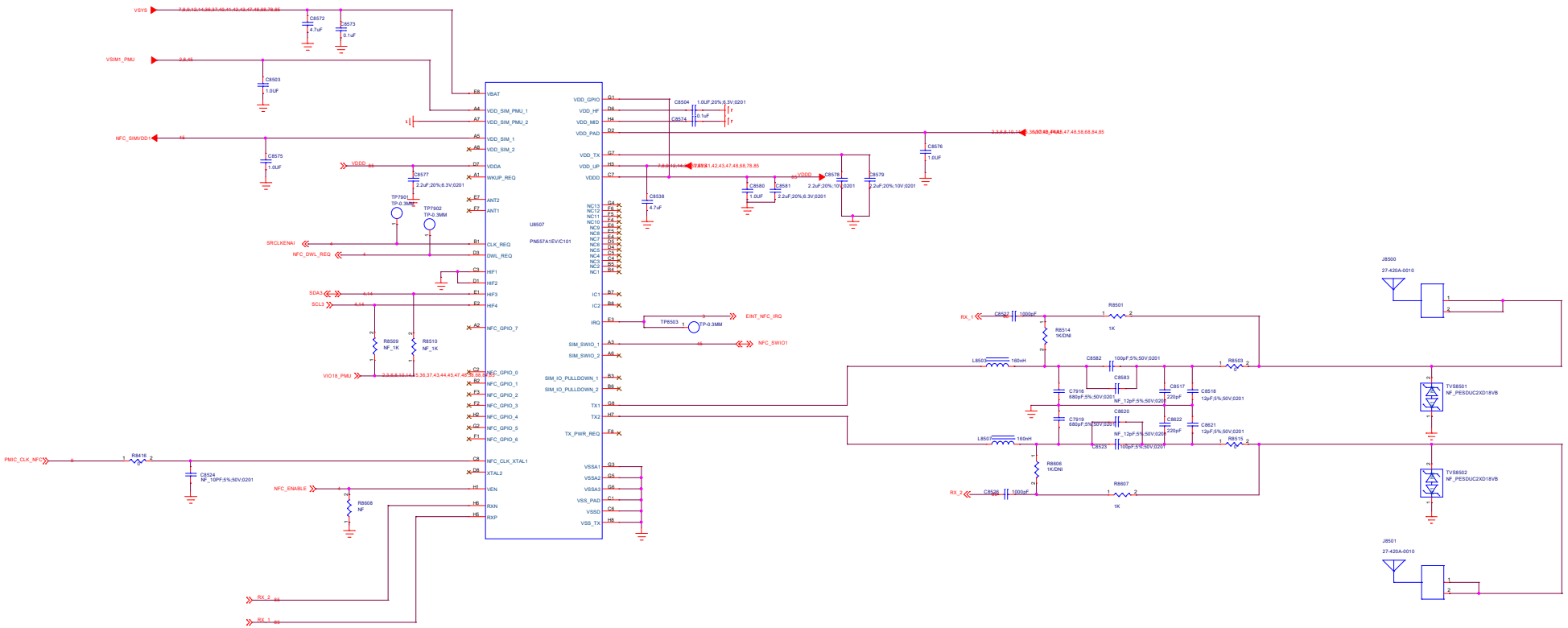
WINGTECH		
Date: Friday, February 11, 2022	Sheet 79 of 48	



Title	48_Sub PCB IF	REV: V1.0
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT: WINGTECH-SH		DESIGNER: YL
Data: Tuesday, June 28, 2022	Sheet 84 of 48	

85.NFC_PN557


VSYS
VSIM1_PMU
NFC_SIMVDD1
VDDD_85
SRCLKENA1
NFC_DWL_REQ
SDA1
SCL1
VIO18_PMU
PMIC_CLK_NFC
NFC_ENABLE
RX_2
RX_1
U8507
PN557A1EV/C101
VBAT
VDD_SIM_PMU_1
VDD_SIM_PMU_2
VDD_SIM_1
VDD_SIM_2
VDDA
WKUP_REQ
ANT2
ANT1
CLK_REQ
DWL_REQ
HIF1
HIF2
HIF3
HIF4
NFC_GPIO_7
NFC_GPIO_0
NFC_GPIO_1
NFC_GPIO_2
NFC_GPIO_3
NFC_GPIO_4
NFC_GPIO_5
NFC_GPIO_6
NFC_CLK_XTAL1
XTAL2
VEN
RXN
RXP
VDD_GPIO
VDD_HF
VDD_MID
VDD_PAD
VDD_TX
VDD_UP
VDDD
IC1
IC2
IRQ
SIM_SWIO_1
SIM_SWIO_2
SIM_IO_PULLDOWN_1
SIM_IO_PULLDOWN_2
TX1
TX2
TX_PWR_REQ
VSSA1
VSSA2
VSSA3
VSS_PAD
VSSD
VSS_TX
EINT_NFC_IRQ
NFC_SWIO1
J8500
J8501
TVS8501
TVS8502
NF_PESDUC2XD18VB
27-420A-0010
Title 85_NFC
REV: V1.0
DOCUMENT NO.: Design Name
Size D
DEPARTMENT: WINGTECH-SH
DESIGNER: YL
Date: Friday, February 11, 2022
Sheet 85 of 48