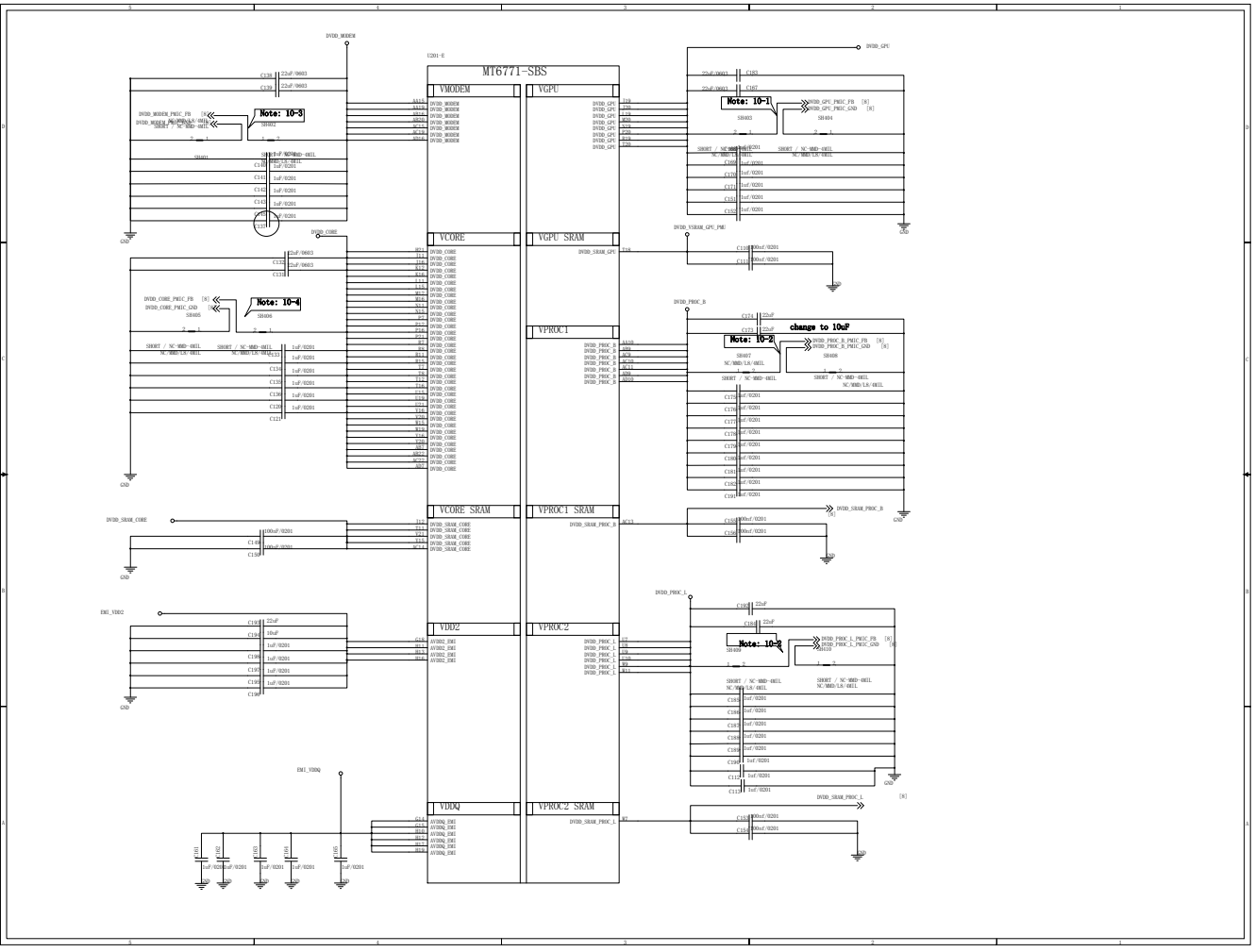
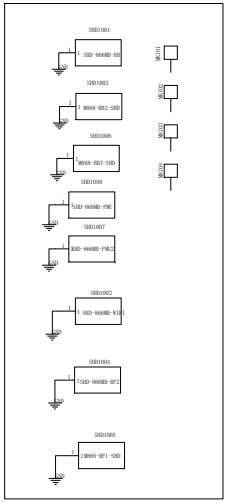
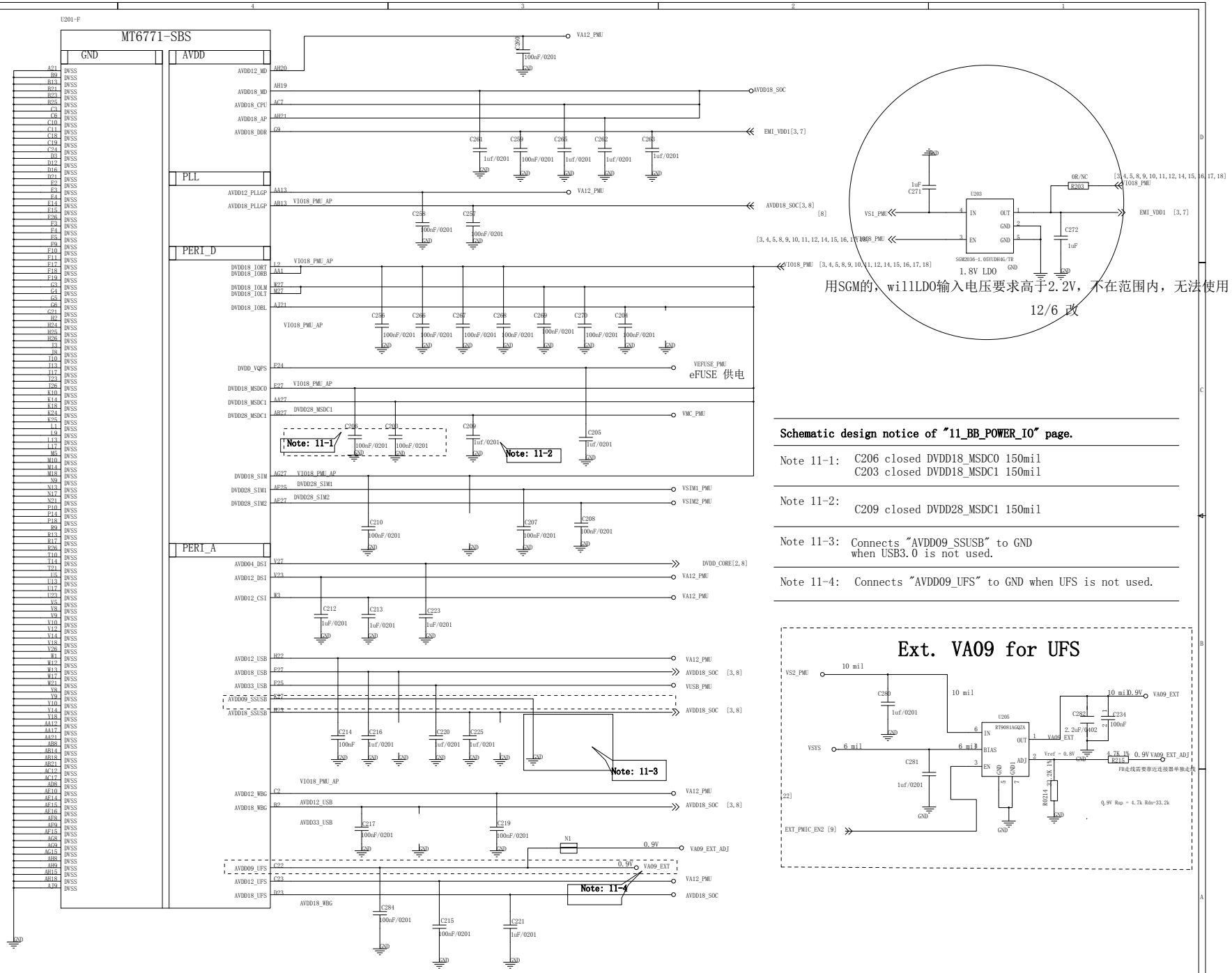


Schematic design notice of "10_BB_POWER_PDN" page.

Note 10-1:	Differential pair of DVDD_GPU remote sense Remote sense trace with GND shielding to PMIC (Differential) must be close to BB's ball.
Note 10-2:	Differential pair of DVDD_PROC remote sense Remote sense trace with GND shielding to PMIC (Differential) must be close to BB's ball
Note 10-3:	Remote sense trace with GND shielding to PMIC (Differential) Differential pair of DVDD_MODEM remote sense must be close to BB's ball.
Note 10-4:	Remote sense trace with GND shielding to PMIC (Differential) Differential pair of DVDD_CORE remote sense must be close to BB's ball.





用SGM的，willLDO输入电压要求高于2.2V，不在范围内，无法使用

12/6 改

Schematic design notice of "11_BB_POWER_IO" page.

Note 11-1:	C206 closed DVDD18_MSDC0 150mil C203 closed DVDD18_MSDC1 150mil
Note 11-2:	C209 closed DVDD28_MSDC1 150mil
Note 11-3:	Connects "AVDD09_SSUSB" to GND when USB3.0 is not used.
Note 11-4:	Connects "AVDD09_UFS" to GND when UFS is not used.

Schematic design notice of "12_BB_1" page.

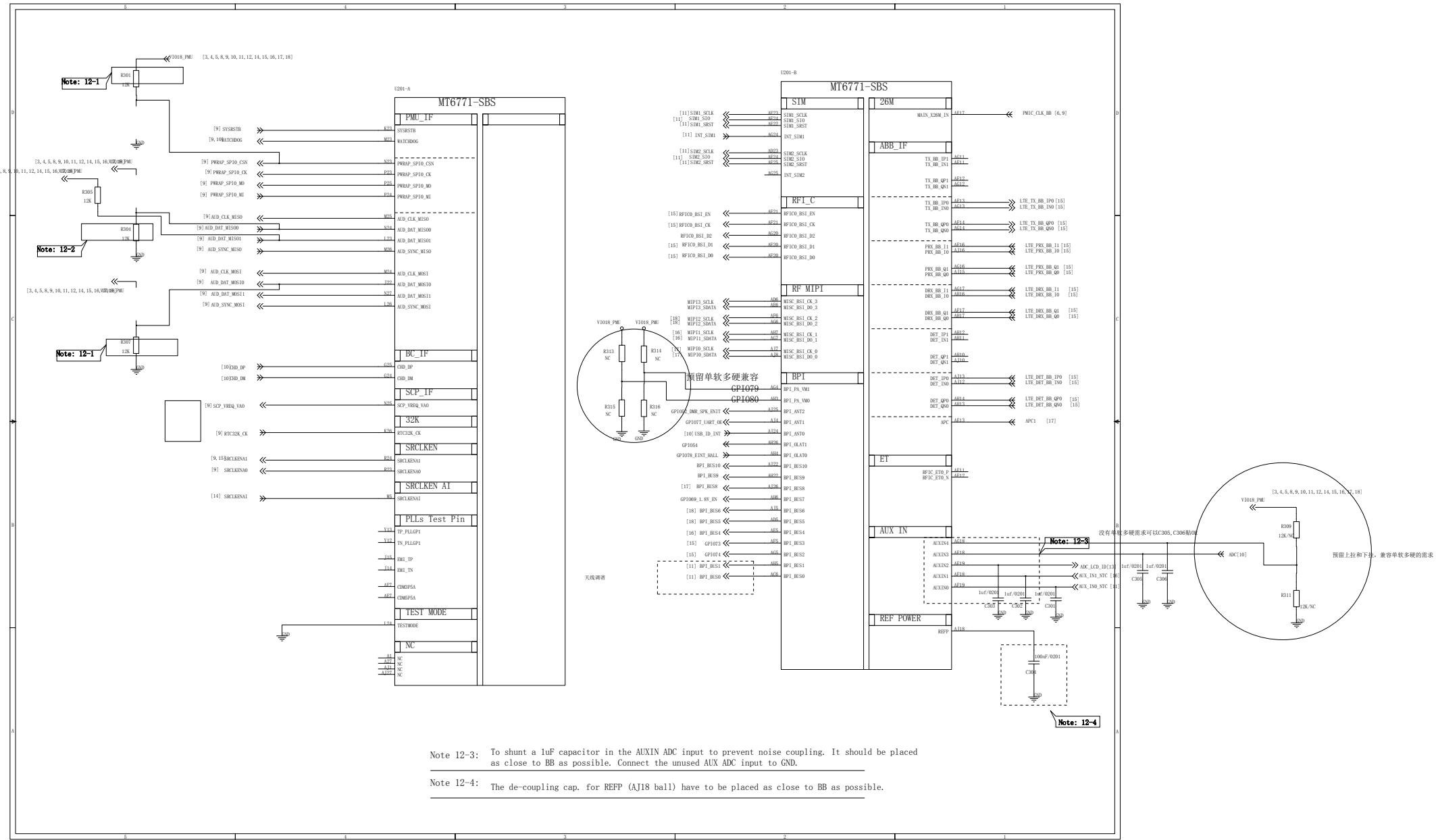
Note 12-1: "PWRAP_SPIO_CSN" and "AUD_DAT_MOSIO" are bootstrap pin to slect which interface will be the JTAG pin out.

PWRAP_SPIO_CSN	AUD_DAT_MOSIO	Which interface will be the JTAG pin out	
		AP_JTAG	IO_JTAG
HI	LO	N/A	N/A
HI	HI	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI / EINT8	DPI_11/DPI_HSYNC/DPI_VSYNC /DPI_DE/DPI_CK/DPI_D8/DPI_D9
LO	LO	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI / EINT8	N/A
LO	HI	MSDC1_CLK/CMD/ DAT0/DAT1/DAT2	N/A

Note 12-2: "AUD_DAT_MISO0" is bootstrap pin to enable serial JTAG output over USB2.0 interface or not.
When "AUD_DAT_MISO0" is pulled to high in system start up and then USB2.0 interface will be switched into serial JTAG mode.

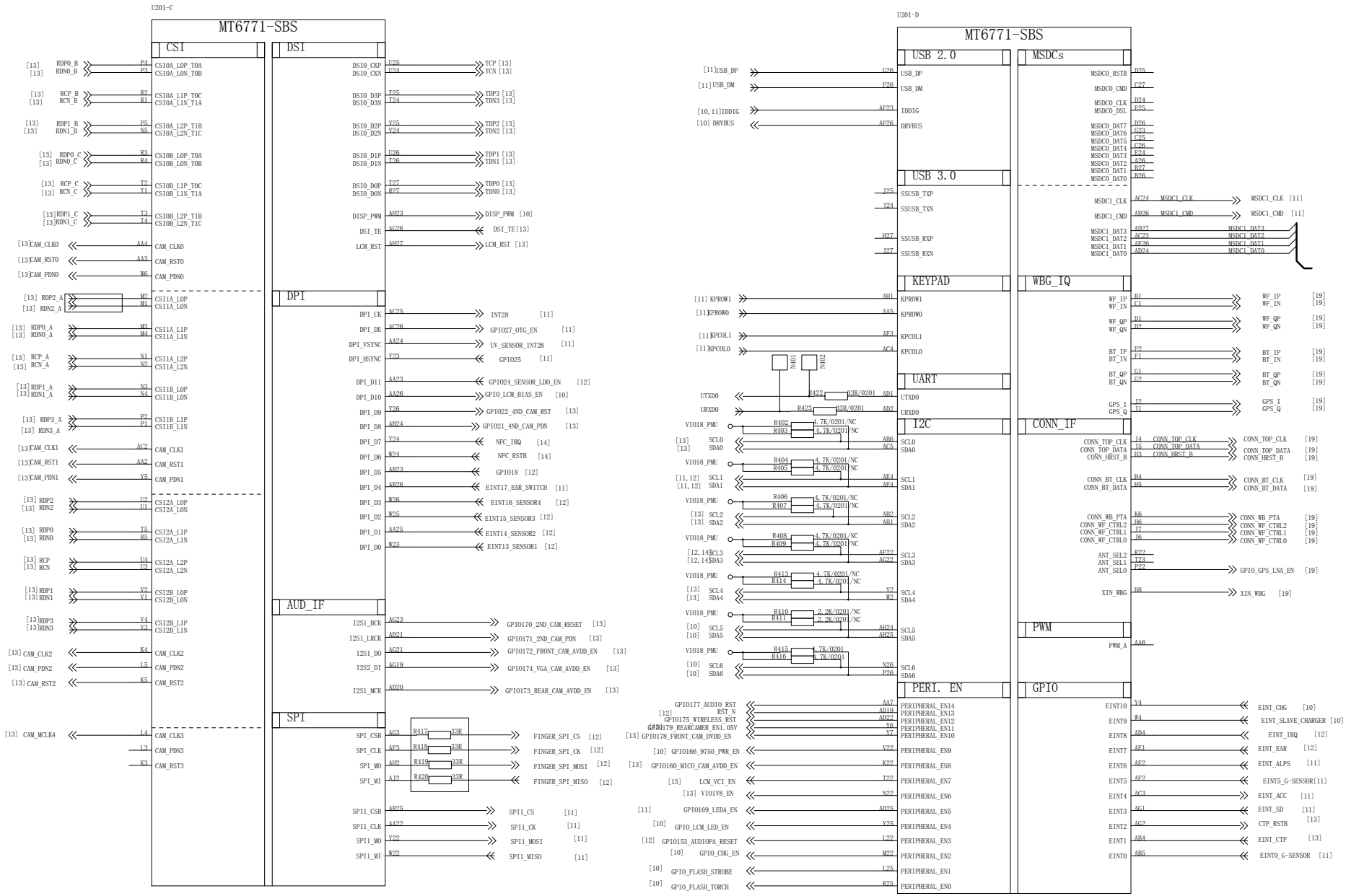
"AUD_DAT_MISO1" is bootstrap pin to select system booting up from eMMC or UFS device.

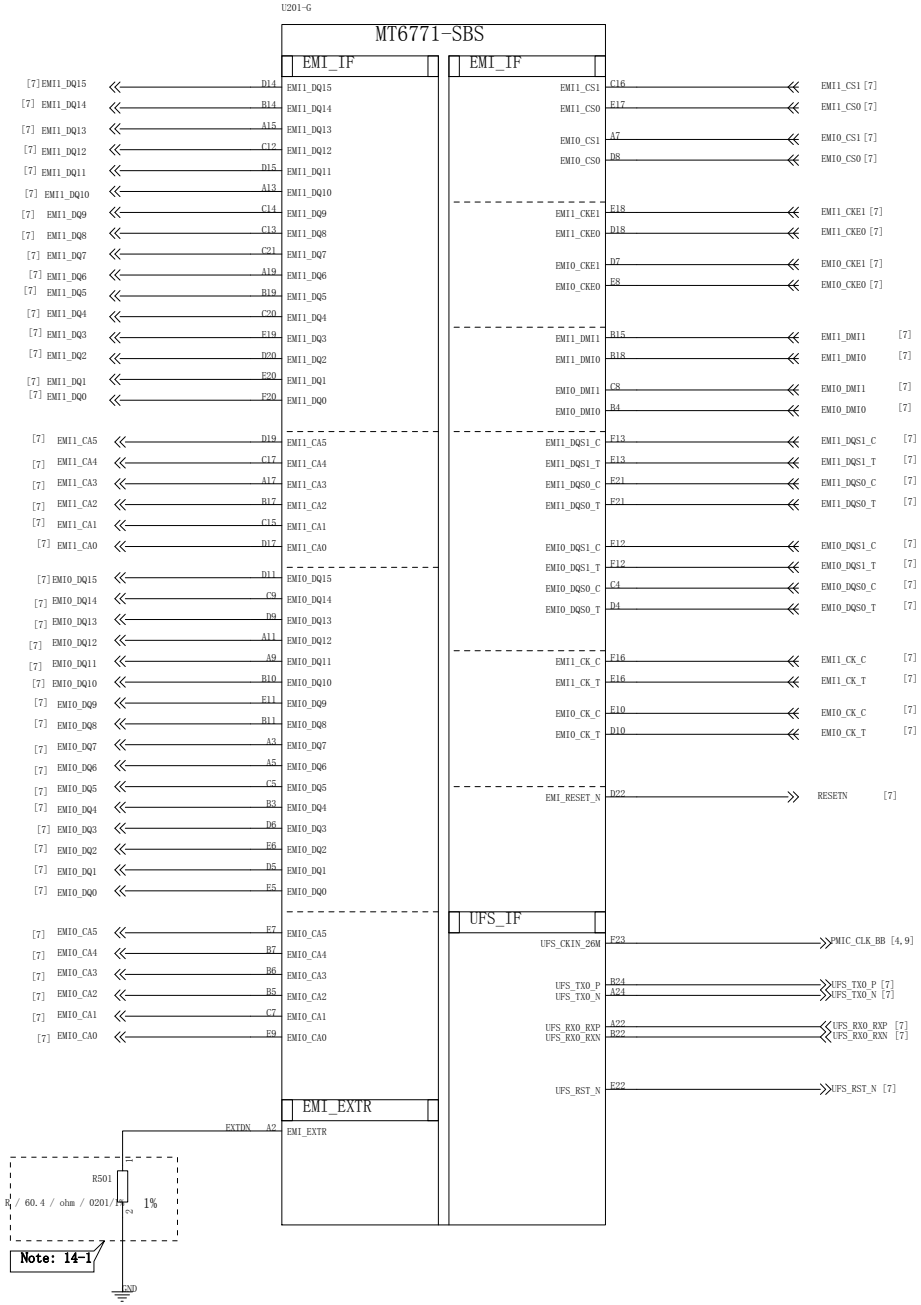
AUD_DAT_MISO1	Booting device
LO	eMMC
HI	UFS



Note 12-3: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

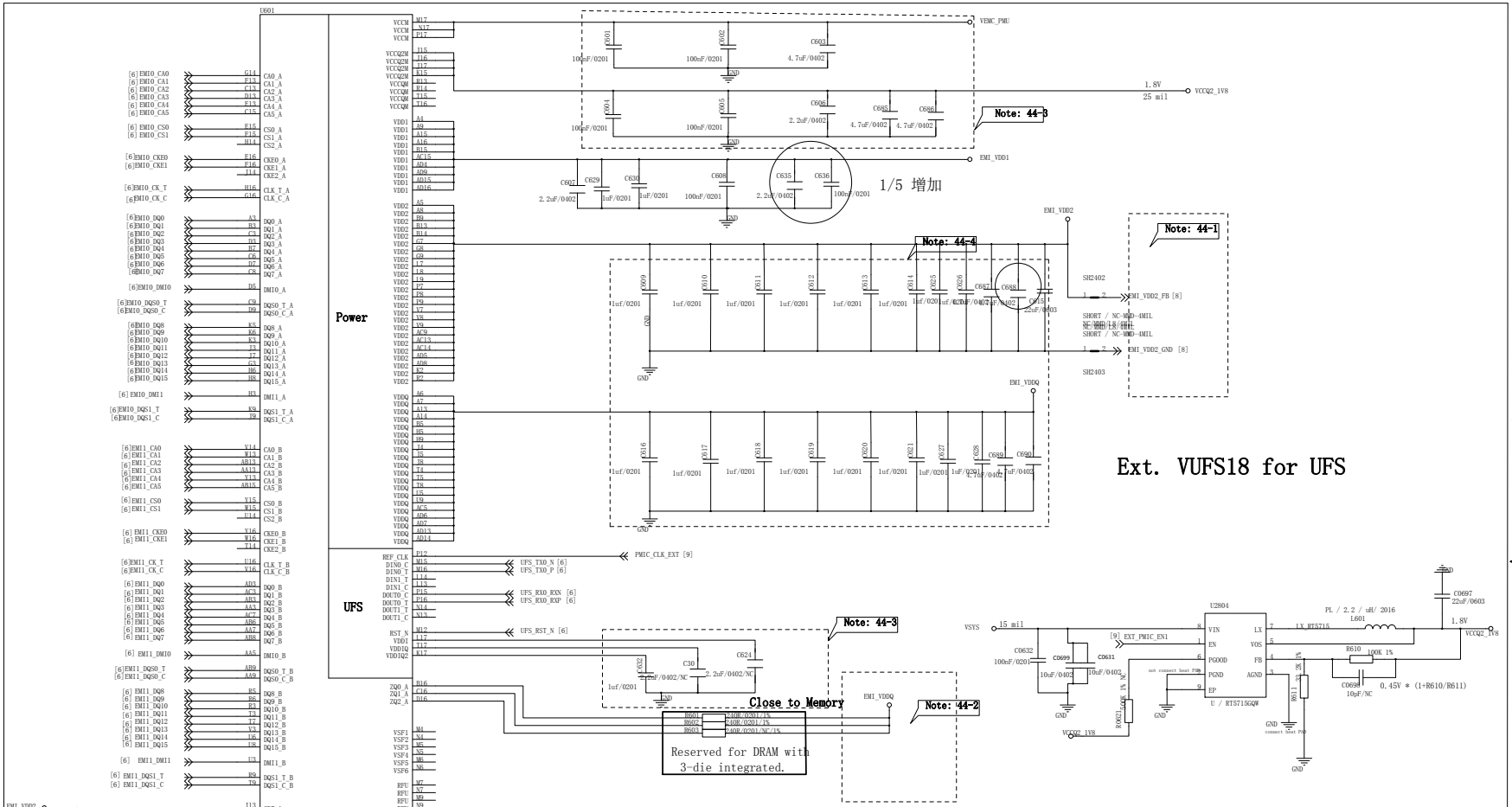
Note 12-4: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.


U201-C
MT6771-SBS
CSI
DSI
DPI
AUD_IF
SPI
U201-D
USB 2.0
USB 3.0
KEYPAD
UART
I2C
PERI. EN
MSDCs
WBG_IQ
CONN_IF
PWM
GPIO



Schematic design notice of "14_BB_3" page.

Note 14-1: The resistor of EMI_EXTR for DRAM has to be placed near to BB as close as possible
R501, please select 60.4 ohm 1% resistor



Schematic design notice of "44_Memory_eMMC_LPDDR4X"

Note 44-1:

Please refer to power supply related page select VDRAM 2 / VDRAM1 output voltage properly for LPDDR4X

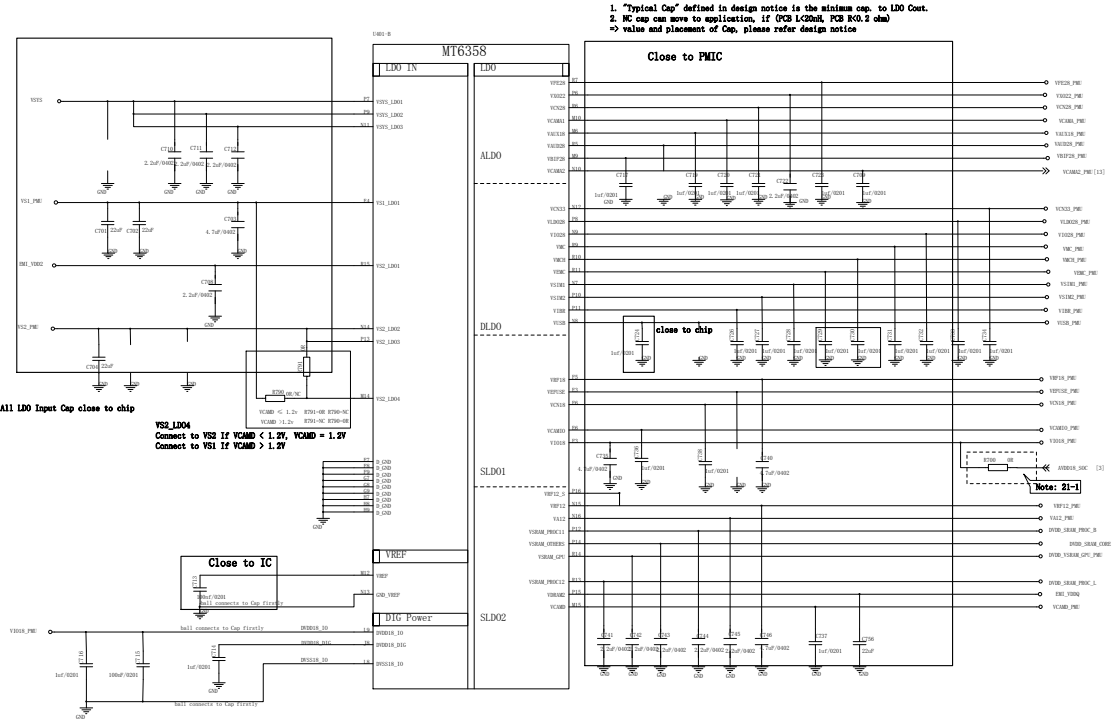
Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ.

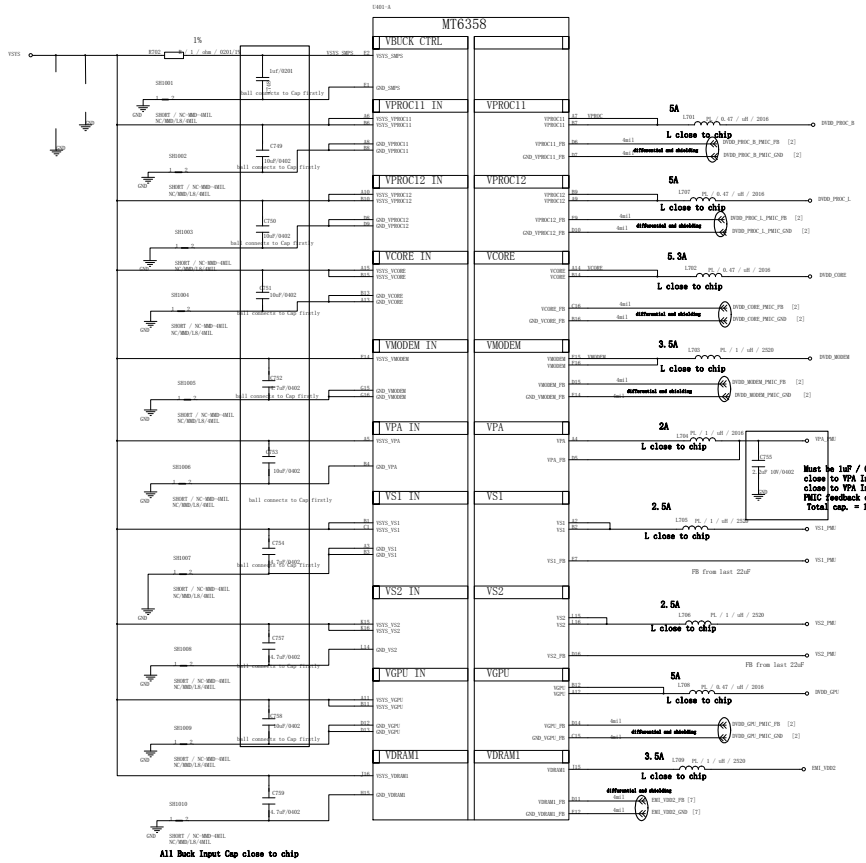
Note 44-3:

Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4:

VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.





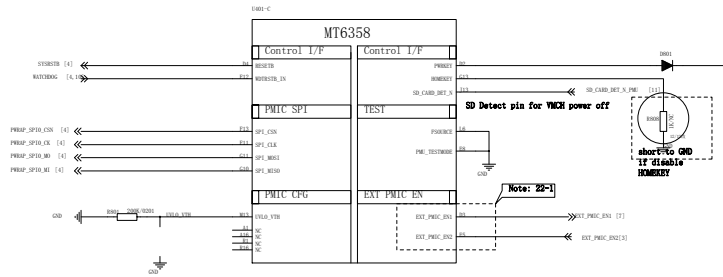
Schematic design notice of "21_POWER_MT6358-LDO" page.

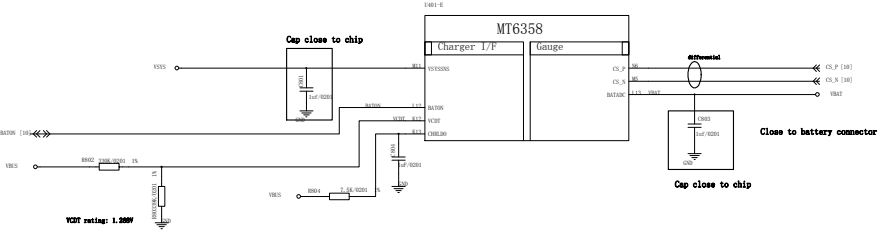
Note 21-1: Please set SH2101 close to C735, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
Please also refer to MT6358 design notice for further detail design information

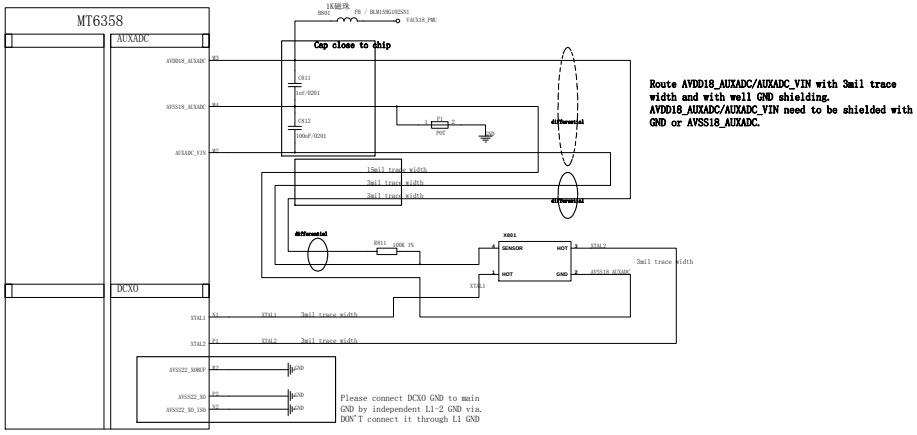
Schematic design notice of "23_POWER_MT6358-Audio"

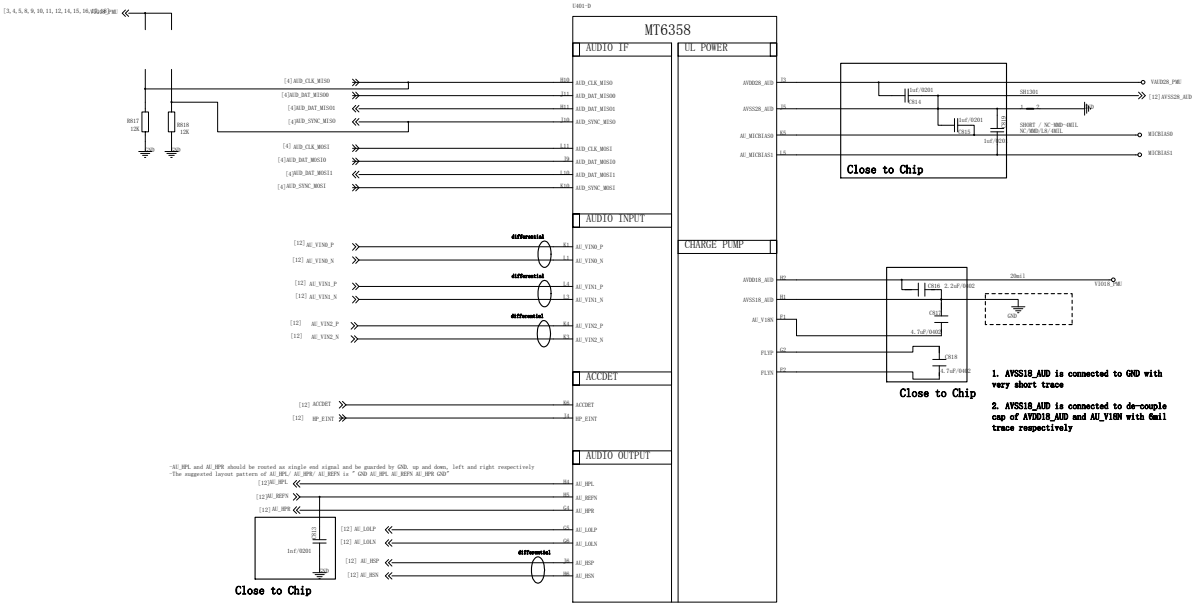
Note 23-1: VDRAM 2 / VDRAM1 output voltage vs. trap pin.

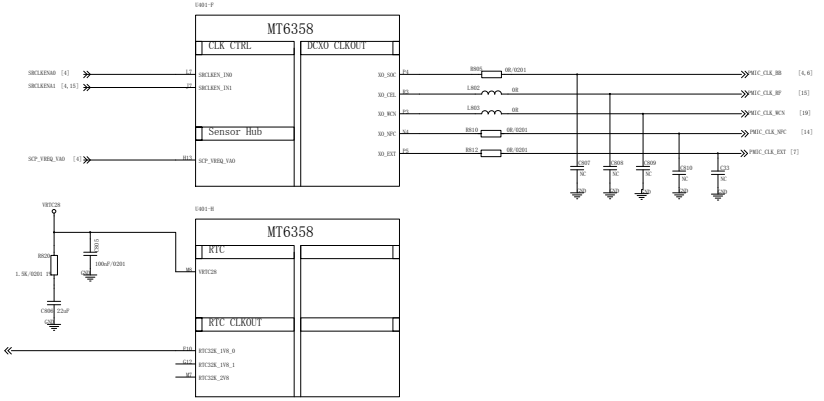
HW GPIO configuration		Trapping Option		DRAM type	VDRAM2 Power source (VS2 LDO1 ball)
AUD_SYNC_MISO	AUD_CLK_MISO	VDRAM1	VDRAM2		
0	0	1.125V	0.6V	LP4X	VDRAM1
0	1	OFF	1.8V	LP4X (Ext x 2 EN)	VS1
1	0	1.225V	OFF	LP3	VDRAM1
1	1	1.125V	1.8V	LP4X (Ext x 1 EN)	VS1









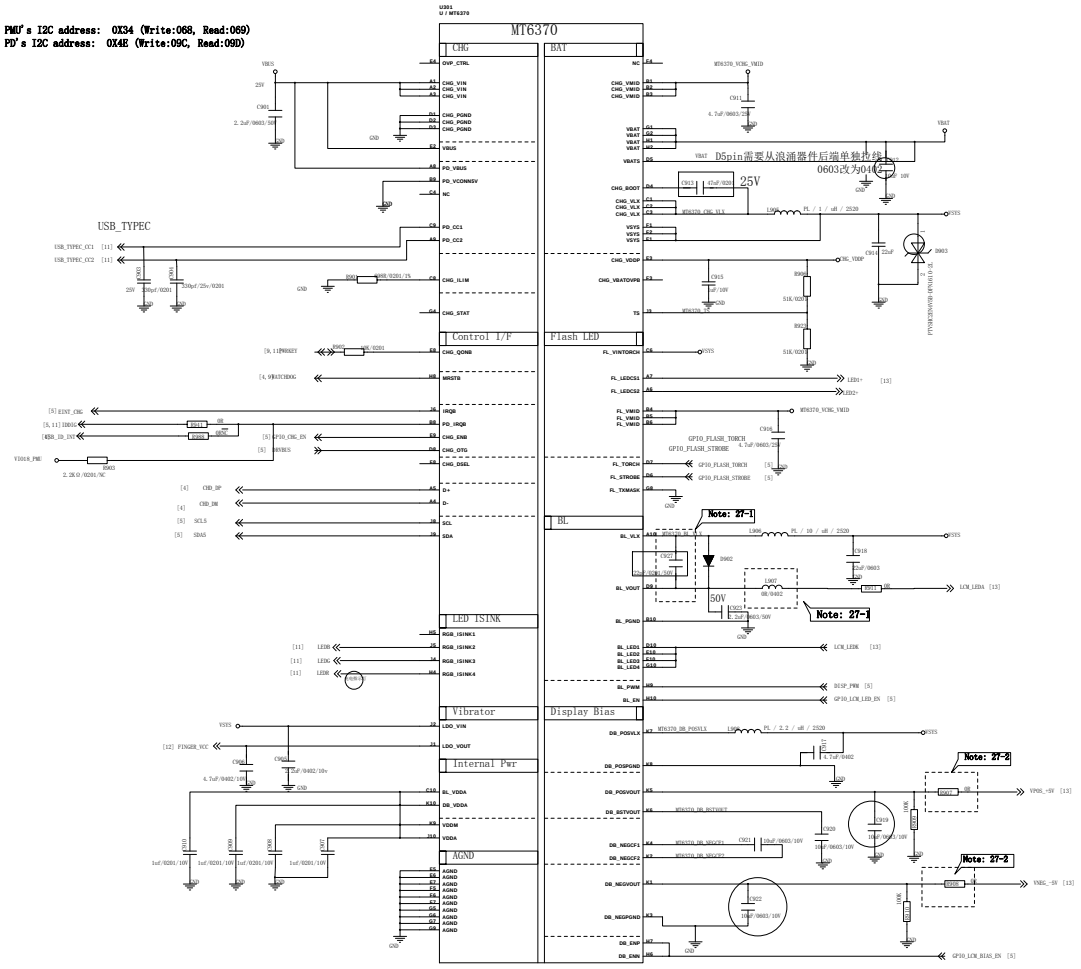


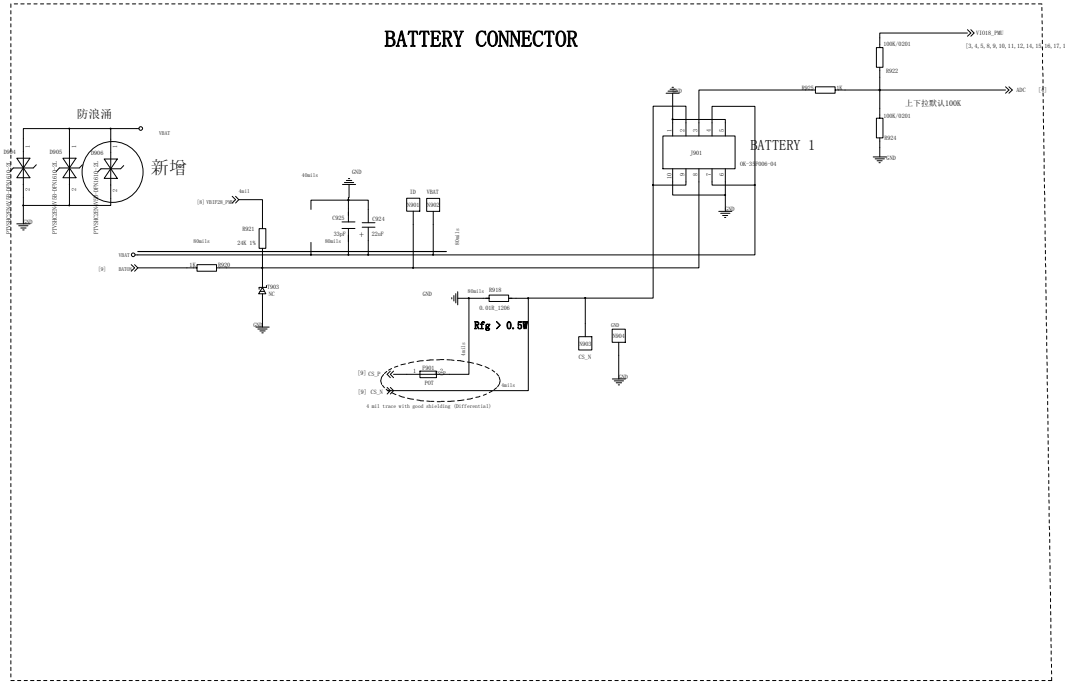
Schematic design notice of "22_POWER_MT6358-General"

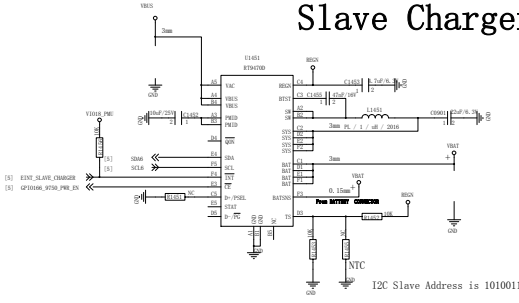
Note 22-1: EXT_PMIC_EN1 : For UFS_1V8, and keep floating if it is not used

EXT_PMIC_EN2 : For VA09 of SSUSB/UFS, and keep floating if it is not used

MT6370 PMU's I2C address: 0X34 (Write:068, Read:069)
MT6370 PD's I2C address: 0X4E (Write:09C, Read:09D)





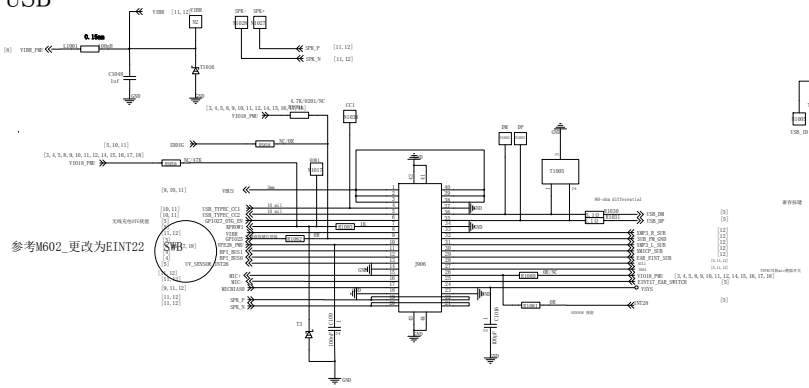


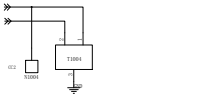
Schematic design notice of "27_POWER_SubPMIC-HV powers" page.

Note 27-1: It is recommended to reserve 0-ohm and cap. for BOM fine tune to minimize RF de-sense.

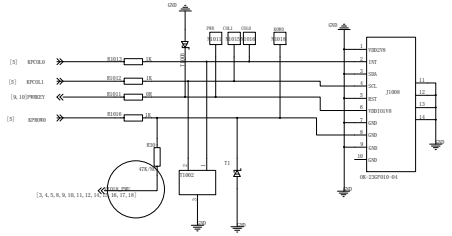
Note 27-2: It is recommended to reserve 0-ohm for BOM fine tune to minimize RF de-sense.

USB

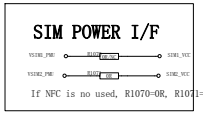


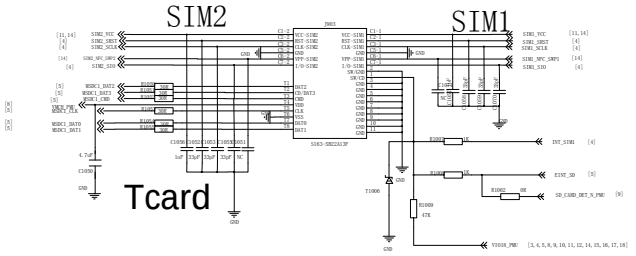


SIDE KEY

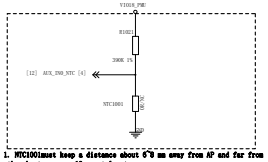


Nano sim1+ sim2&Tcard



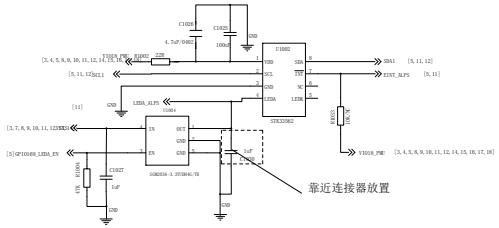


Thermistor / To sense board level temperature

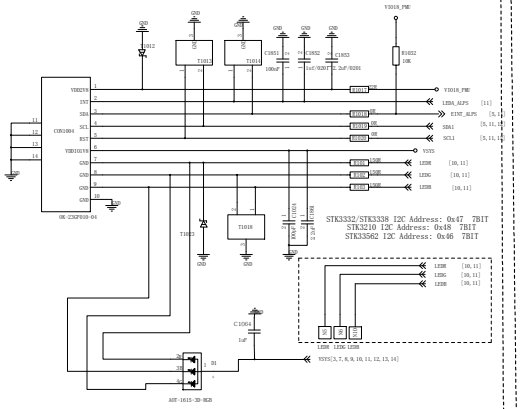


Sensor

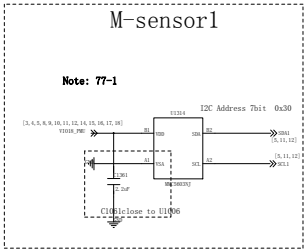
ALS & PS Sensor



ALS & PS Sensor



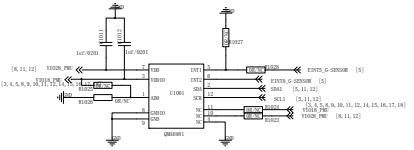
M-sensor1



G-sensor

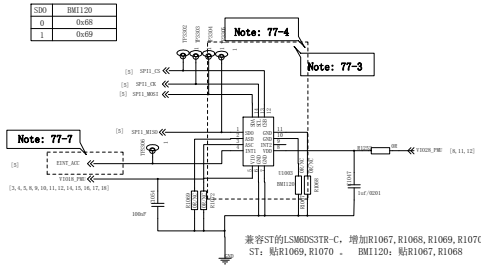
ADO	QMA6981
0	0x12
1	0x13

ADO	STK8BA53
This:	0x18

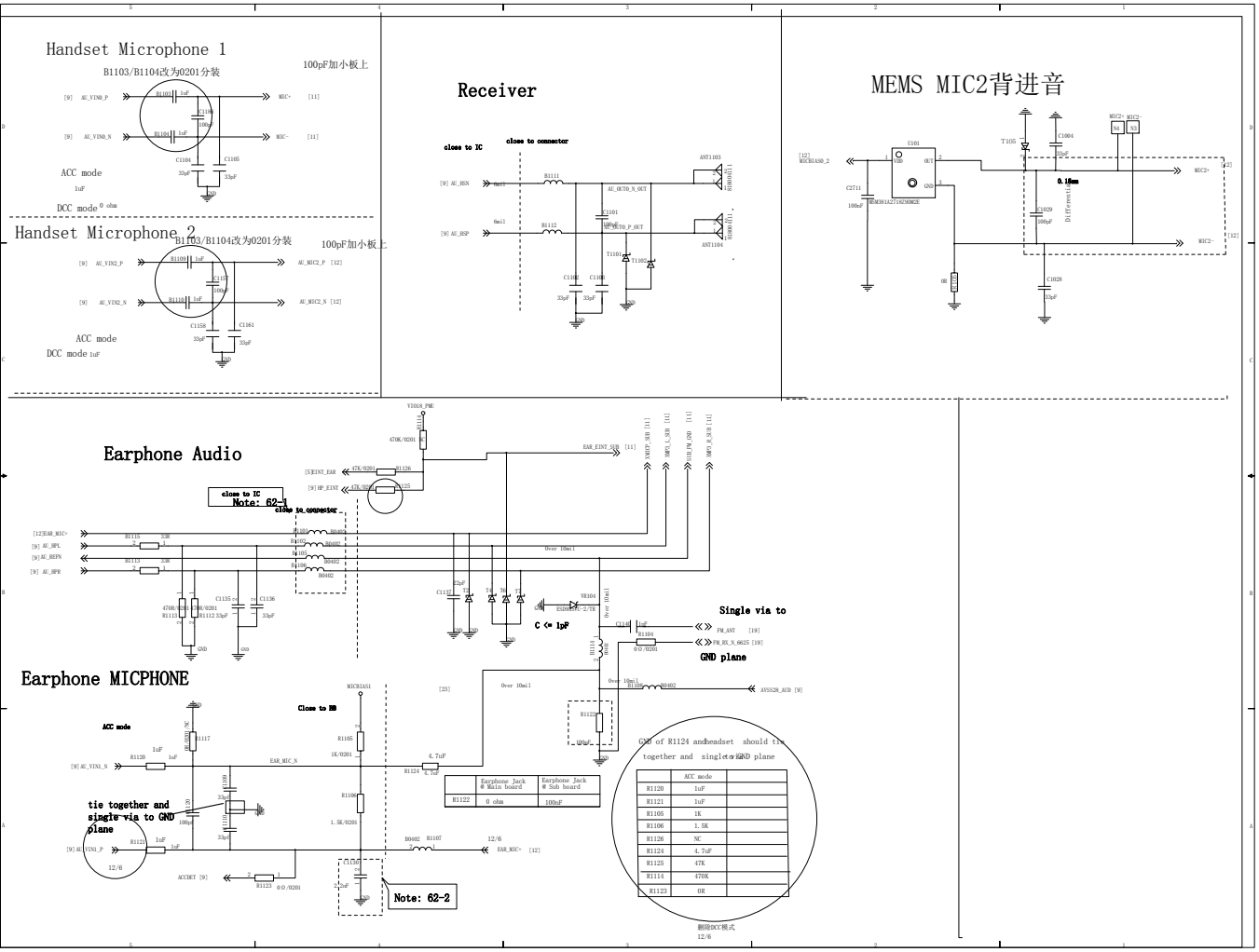


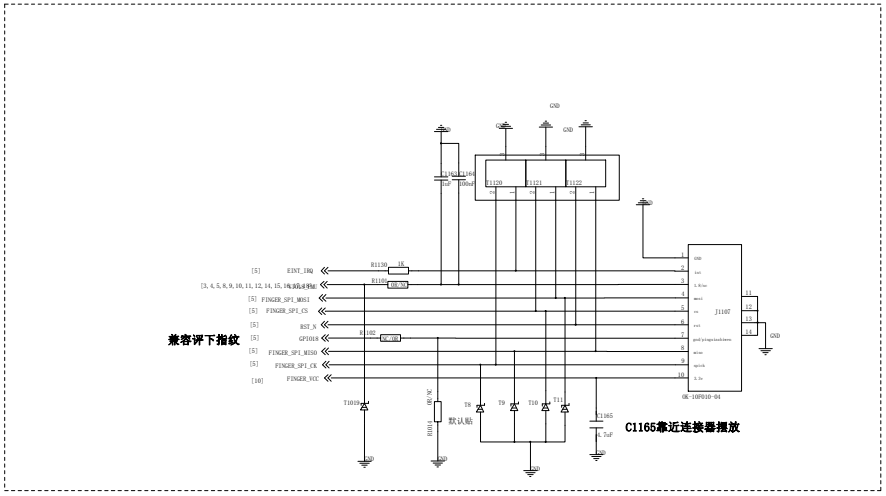
G+Gyro sensor

SDO	BMI120
0	0x68
1	0x69



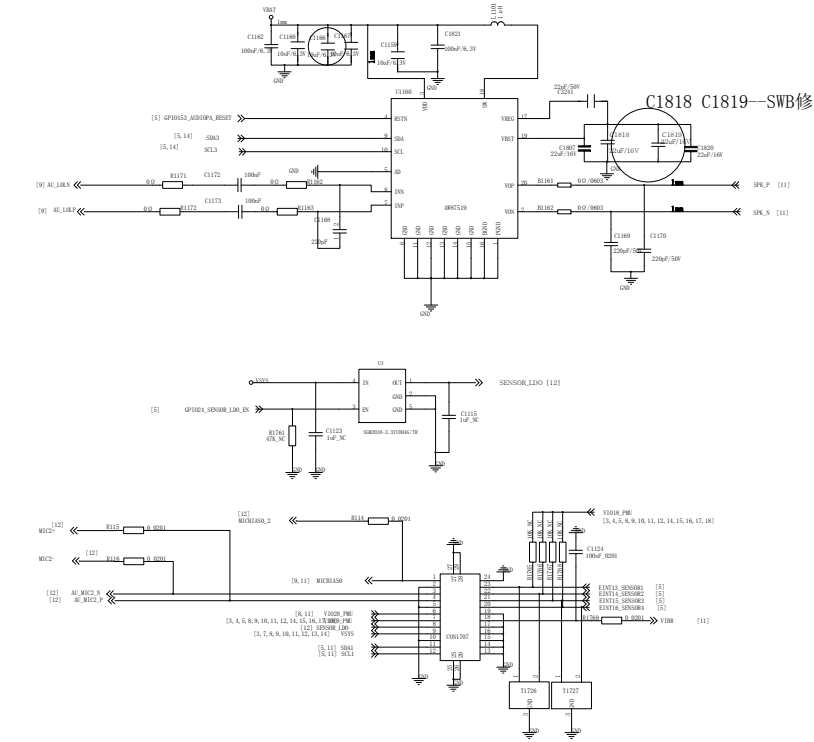
Schematic design notice of "77_PERI_SENSORS_MEMs_ALS/PS" page.
Note 77-1: [M sensor] Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail
Note 77-2: [A+G] For optmized GPS performance, please check HW design notice for Sensor selection guide
Note 77-3: [A+G] MUST use SPI for optmized sensor hub performance **DO NOT USE i2C**
Note 77-4: [A+G] Suggest choose sensor support FIFO watermark interrupt otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse.
Note 77-5: [Baro] Reserve Baro sensor for LPPe feautre (Must for North America Operator / NA SKU)
Note 77-6: DO NOT share Sensor hub i2C to other non-SCP device
Note 77-7: Interrupt pin of MEMS sensor must be assign to ball EINT[12:0]





Smart Audio Amplifier

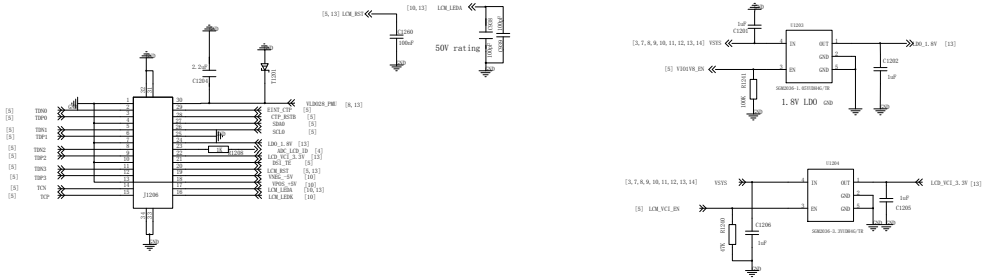
AW87519CSR: 0x58 (0xB0(W),0xB1(R))



Schematic design notice of "62_PERI_AUDIO_IO" page.	
Note 62-1:	Part of BEAD6202, BEAD6203, BEAD6204 and BEAD6205 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .
Note 62-2:	Reserved Cap for CS/RS test, please double check multi-key function when used
Note 62-3:	For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

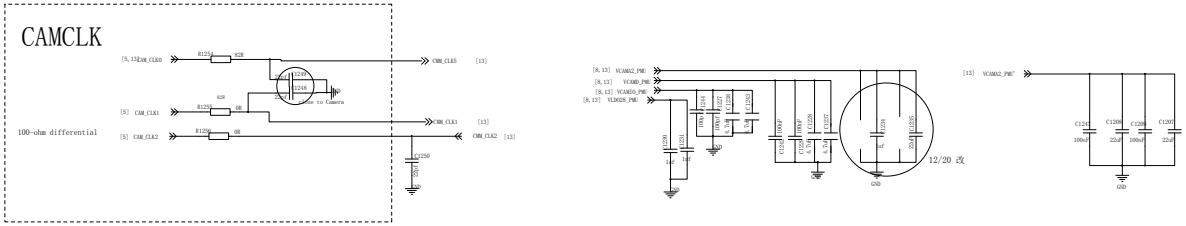
Note 62-4:

LCD

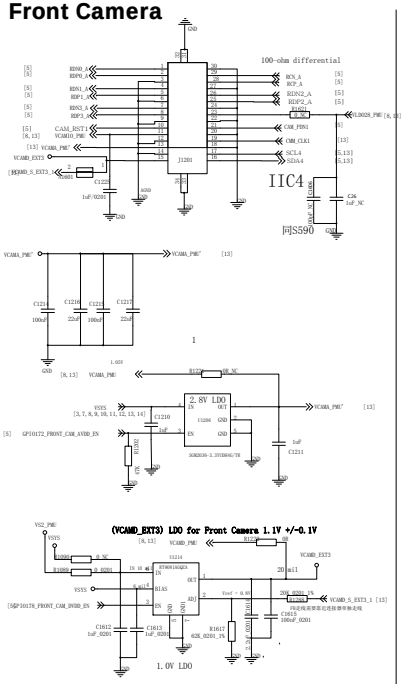


CAMCLK

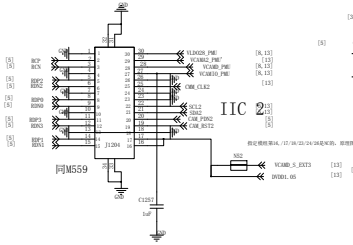
100-ohm differential

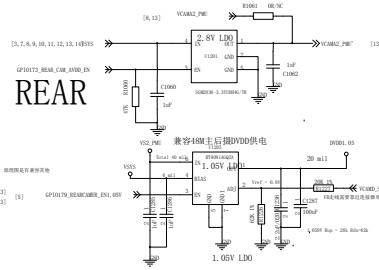


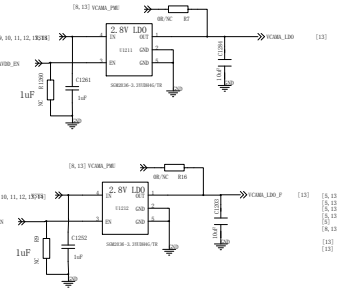
Front Camera



Rear Camera

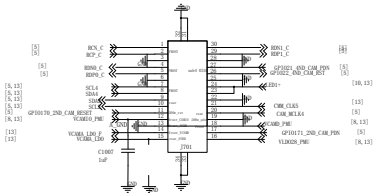


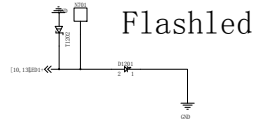




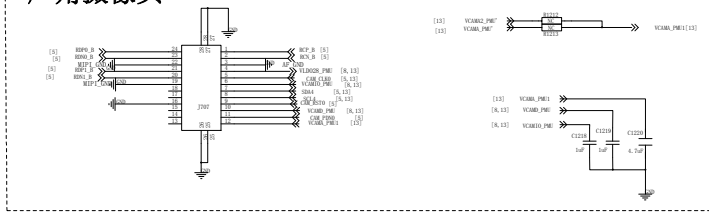
副后摄/微距摄像头/闪光灯

2&3&4 SUB*3 Camera
2&4 SUB*2 Rear Camera
GC 0310 W-42A H-43A
SP0A08 W-7A H-7B



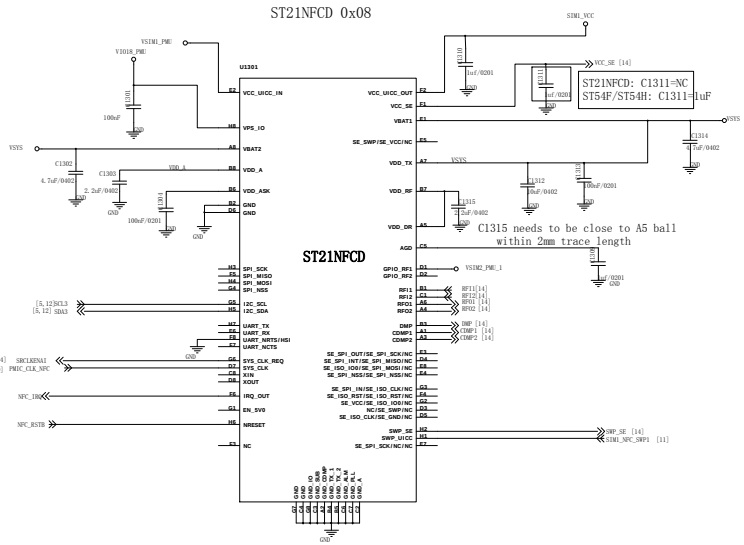


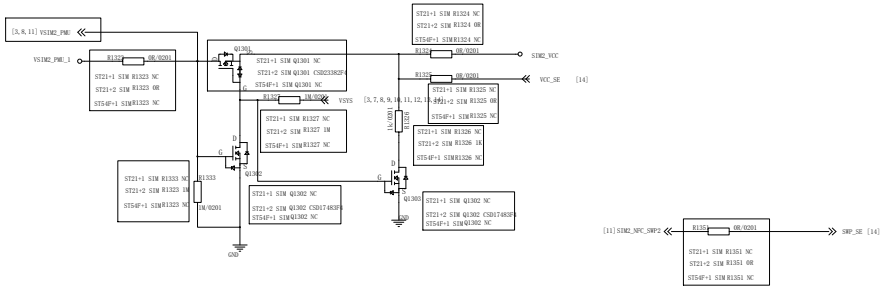
广角摄像头



ST21NFCD, ST54F and ST54H PCB footprint are the same.
ST21NFCD is NFC controller only; ST54F and ST54H are NFC controller with embeeded SE

ST21 PIN ST54F,CAN NOT SUPPORT ST54H

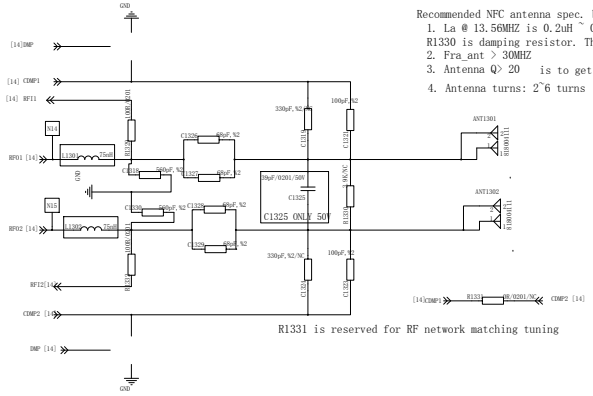




1. ST21NFCD + 1 SWP SIM Only
(1)R1352=R1353=0 ohm
(2)Q1301=Q1302=Q1303=NC
(3)R1323=R1325=R1324=R1327=R1333=R1326=R1351=NC

2. ST21NFCD+2 SWP SIM
(1)Q1301=CSD23382F4 ; Q1302=Q1303=CSD17483F4
(2)R1327=R1333=1M; R1325=R1324=R1323=R1351=R1352=R1353=0 ohm
(3)R1326=1k

3. ST54F/54H+1 SWP SIM + 1 SWP eSE
(1)R1352=R1353=0 ohm
(2)R1323=R1325=R1324=R1327=R1333=R1326=R1351=NC
(3)Q1301=Q1302=Q1303=NC

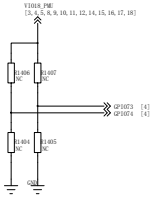


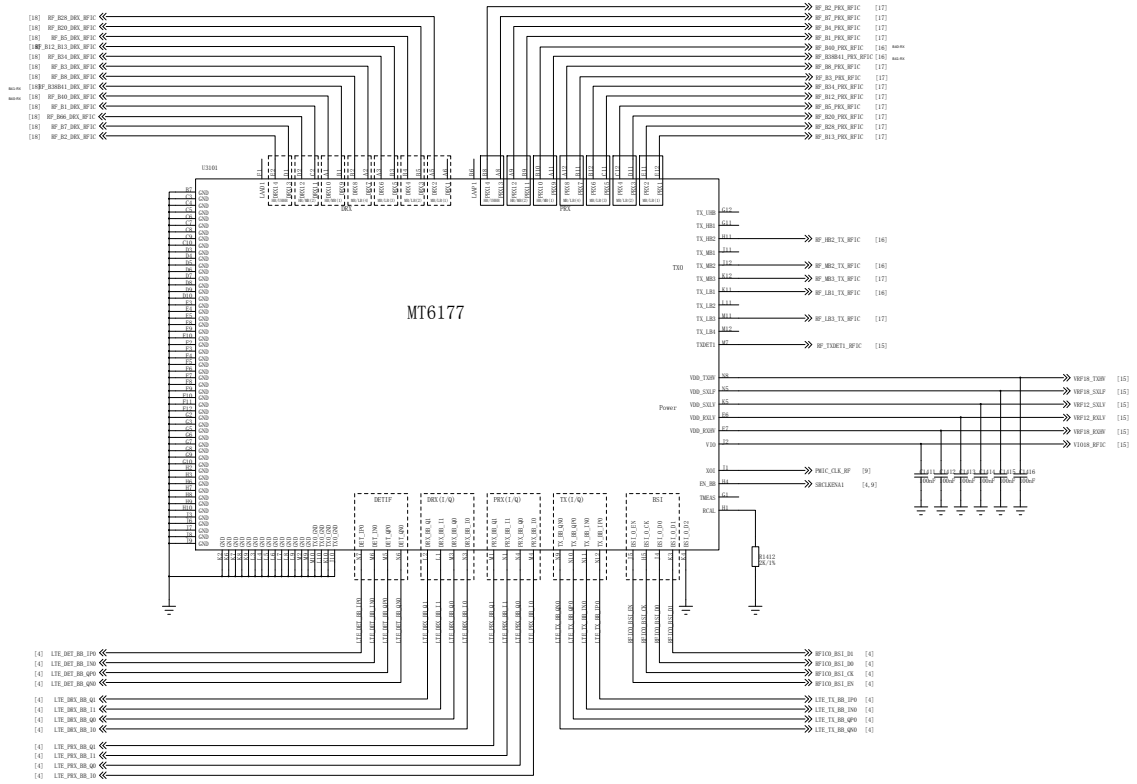
SE ball name definition for ST54F, ST54H, and ST21NFCD, respectively

Ball	ST21NFCD	ST54F	ST54H
D3	NC	SE_SWP	NC
D4	NC	SE_SPI_MISO	SE_SPI_INT
D5	NC	SE_GND	SE_ISO_CLK
E3	NC	SE_SPI_SCK	SE_SPI_OUT(MISO)
E4	NC	SE_SPI_NSS	SE_SPI_NSS
E5	NC	SE_VCC	SE_SWP
E7	NC	NC	SE_SPI_SCK
E8	NC	SE_SPI_MOSI	SE_ISO_IO0
F4	NC	SE_ISO_RST	SE_ISO_RST
G2	NC	SE_ISO_IO0	SE_VCC
G3	NC	SE_ISO_CLK	SE_SPI_IN(MOSI)

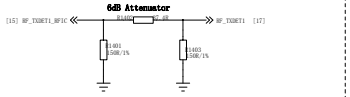
MT6177

DRDI

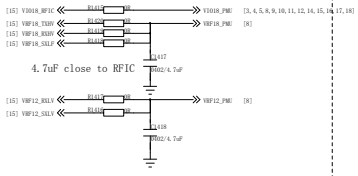




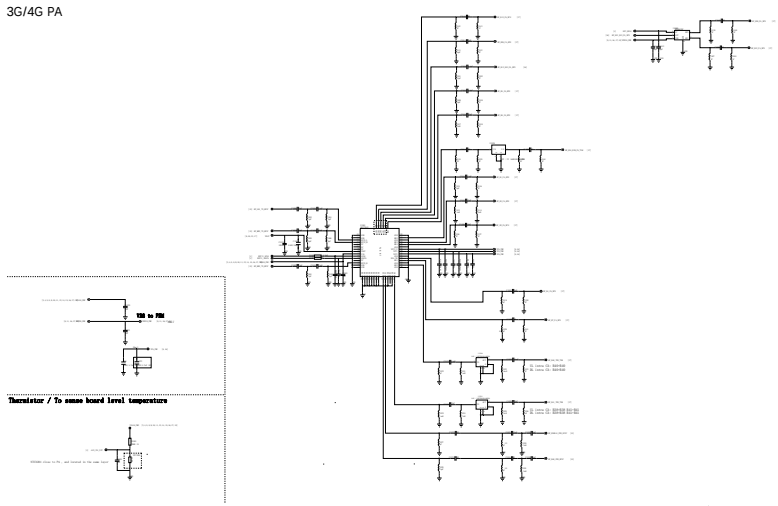
Attenuator for Detector



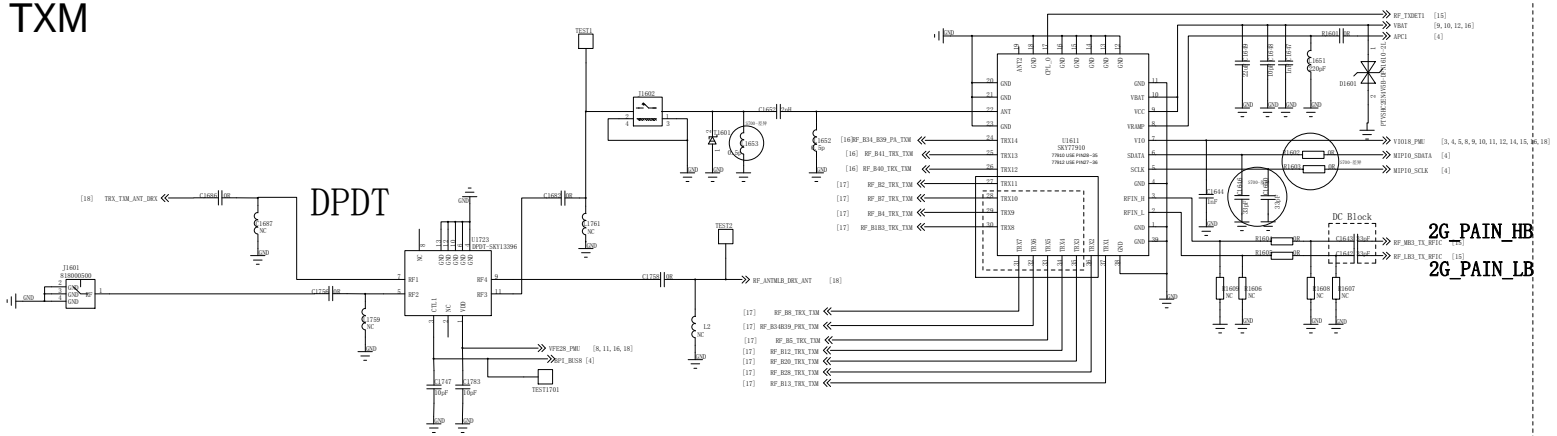
Power For MT6177



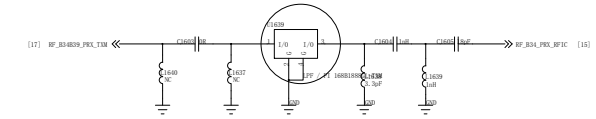
3G/4G PA



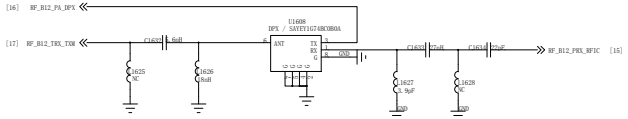
TXM



DCS1800/PCS1900/B34/B39 PRX

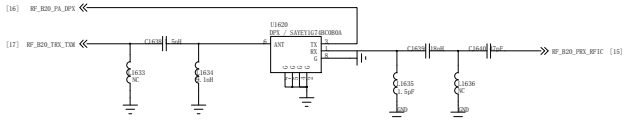


B12/17 TRX

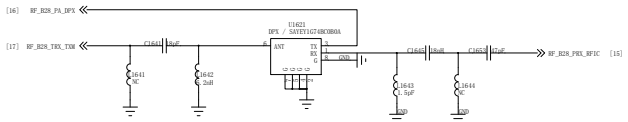


B20 TRX

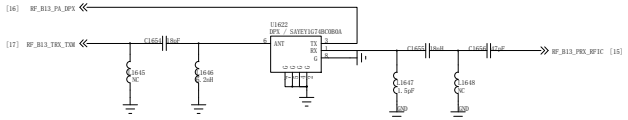
UL intra CA: B20+B20
DL intra CA: B20+B20



B28AB TRX

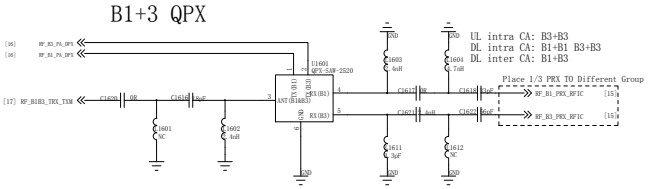


B13 TRX



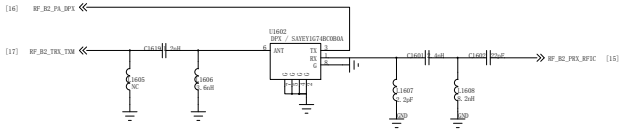
B1+3 QPX

UL intra CA: B3+B3
DL intra CA: B1+B1 B3+B3
DL inter CA: B1+B3



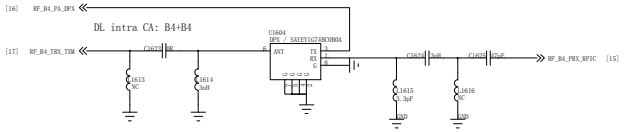
B2(BC1) TRX

B25 TX:1850----1915MHz and RX:1930----1995MHz
B2 TX:1850----1910MHz and RX:1930----1990MHz



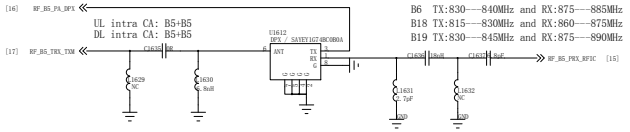
B4 TRX

B66 TX:1710----1780MHz and RX:2110----2200MHz
B4 TX:1710----1755MHz and RX:2110----2155MHz

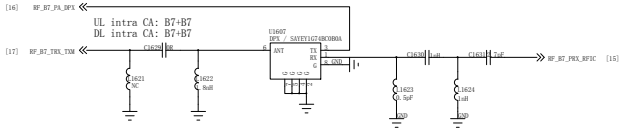


B5(B6/B19/BC0) TRX

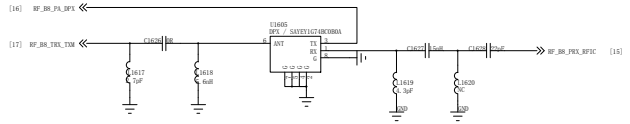
B26 TX:814----849MHz and RX:859----894MHz
B5 TX:824----849MHz and RX:869----894MHz
B6 TX:830----840MHz and RX:875----885MHz
B18 TX:815----830MHz and RX:860----875MHz
B19 TX:830----845MHz and RX:875----890MHz



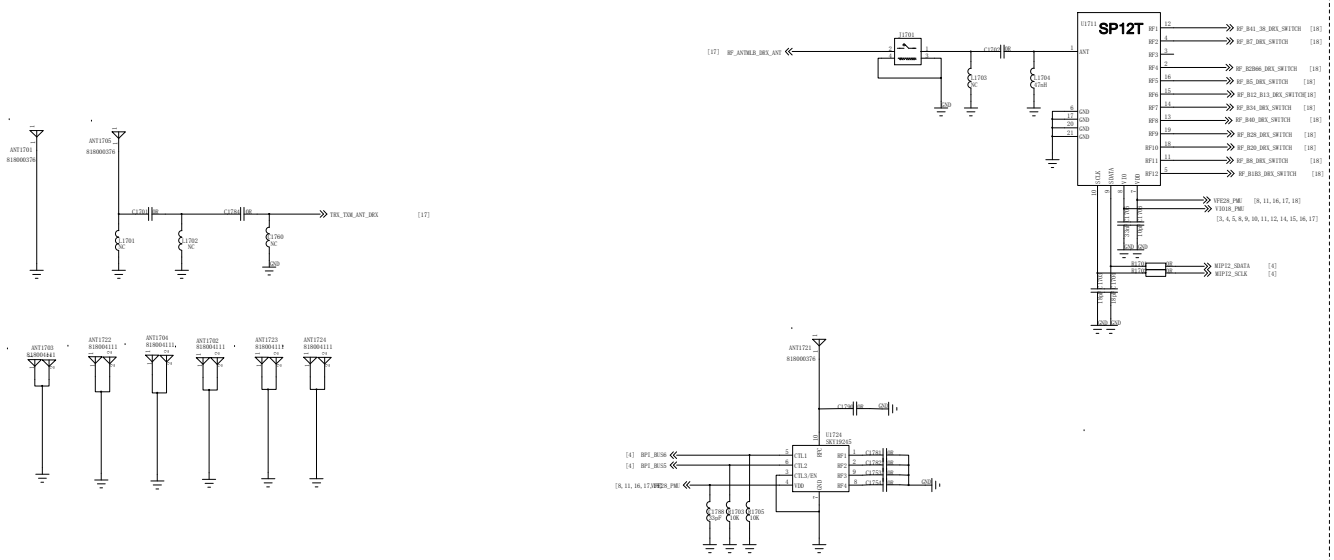
B7 TRX



B8 TRX

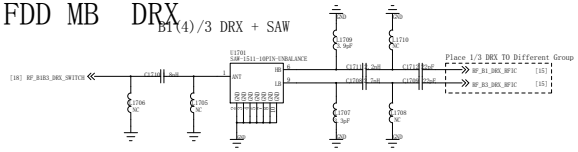


DRX ANT



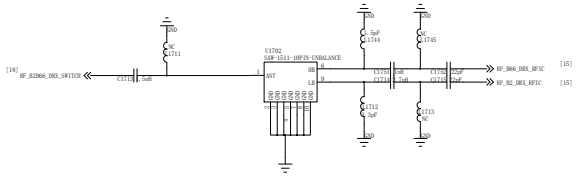
FDD MB DRX

B1(4)/3 DRX + SAW

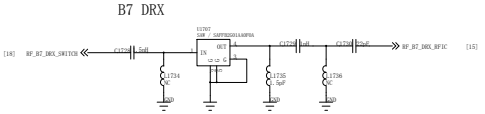


B2(B25)+B66 DRX

B25 TX:1850----1915MHz and RX:1930----1995MHz
B2 TX:1850----1910MHz and RX:1930----1990MHz

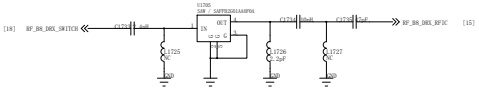


B7 DRX

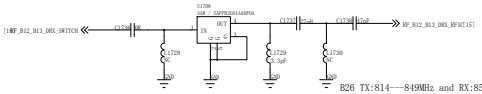


FDD LB DRX

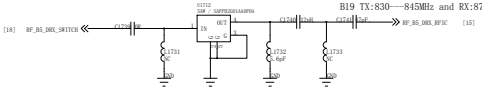
B8 DRX



B12/13/17 DRX

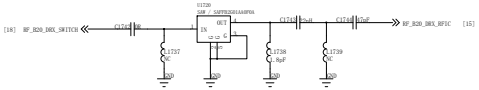


B5(B6/B19/BC0) DRX

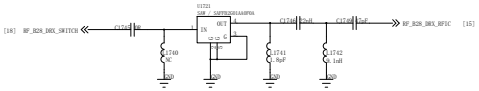


B26 TX:814----849MHz and RX:859----894MHz
B5 TX:824----849MHz and RX:869----894MHz
B6 TX:830----840MHz and RX:875----885MHz
B18 TX:815----830MHz and RX:860----875MHz
B19 TX:830----845MHz and RX:875----890MHz

B20 DRX

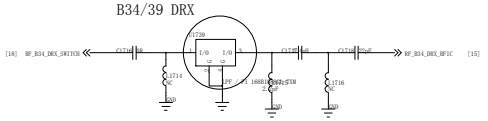


B28 DRX

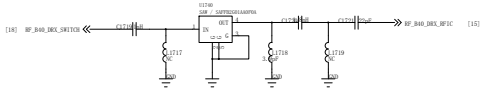


TDD MB DRX

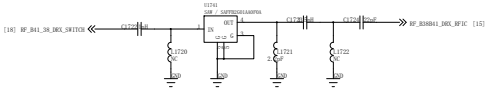
B34/39 DRX



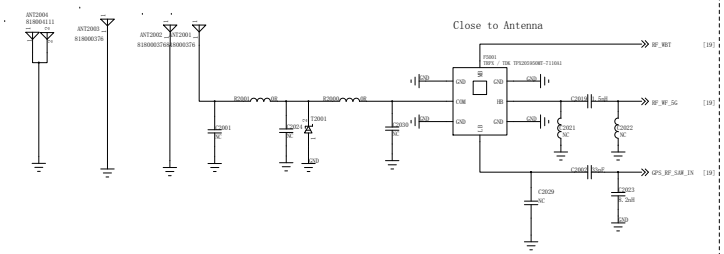
B40 DRX

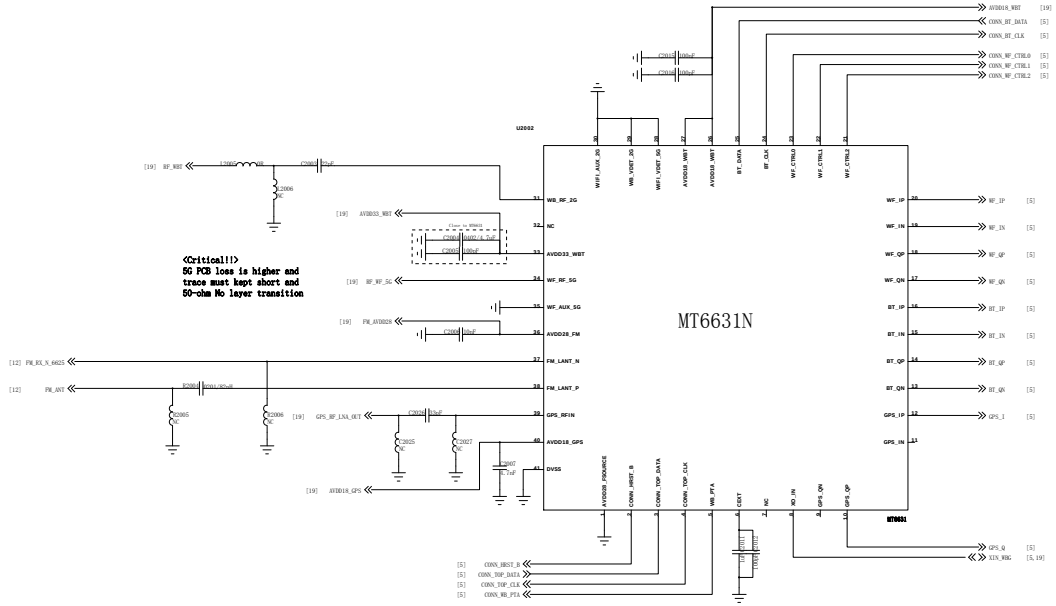


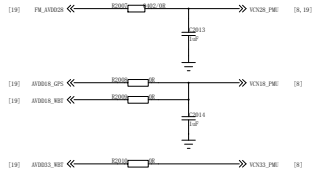
B38/41 DRX

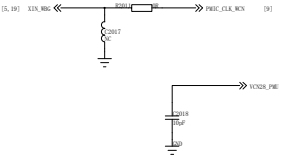


WCN-MT6331

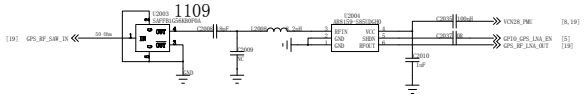


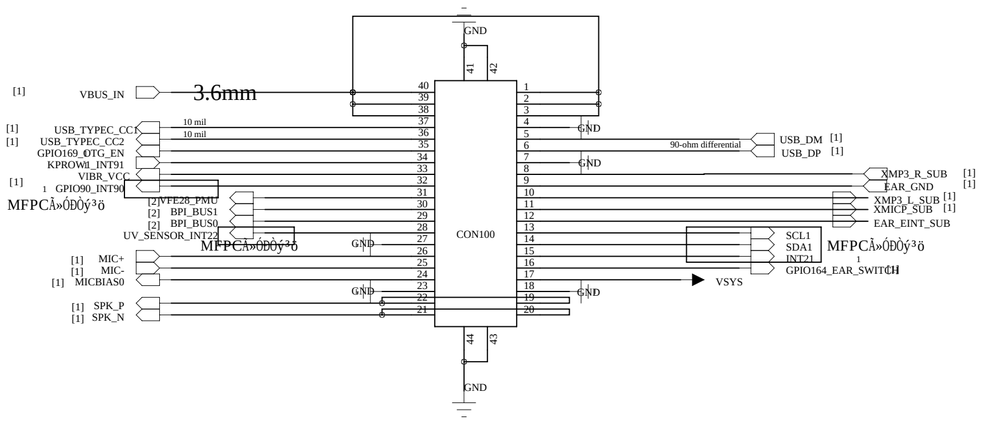




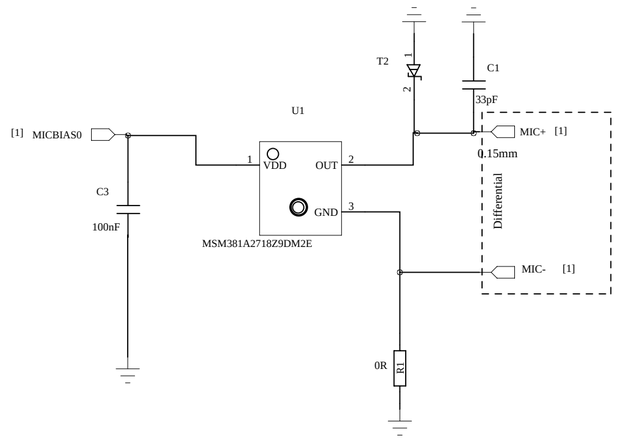


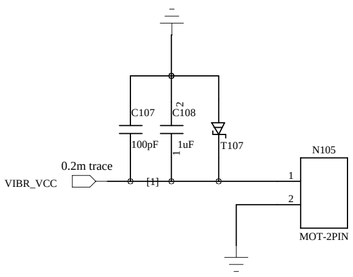
Close to ANT





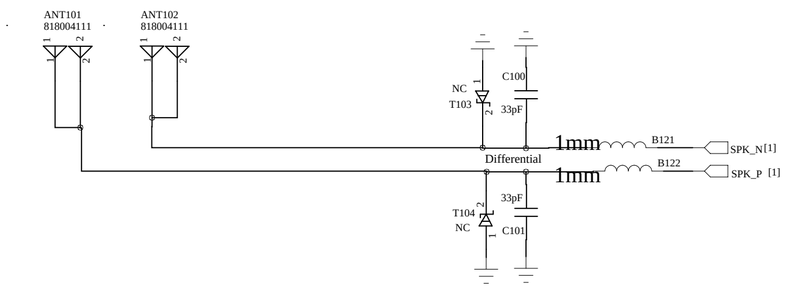
MEMS MIC±³½øÒô



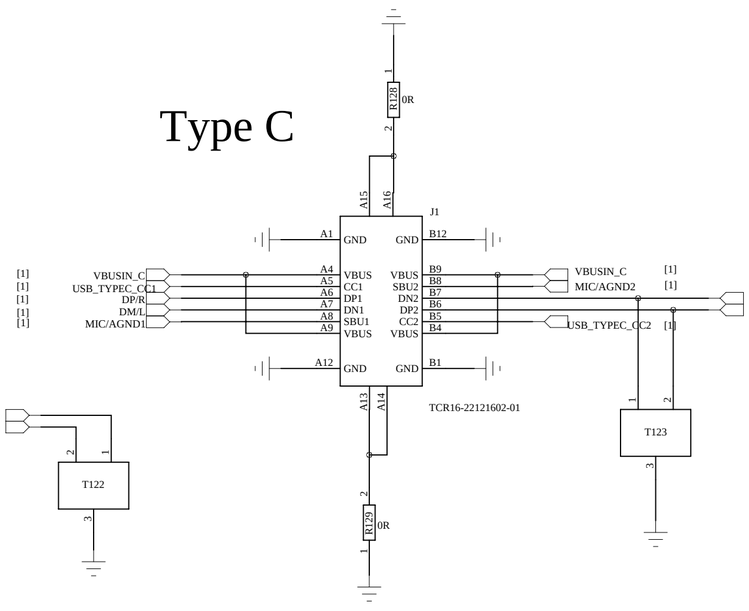


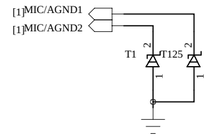
MOTOR

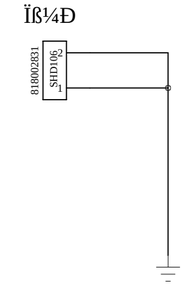
Speaker

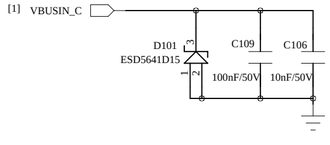


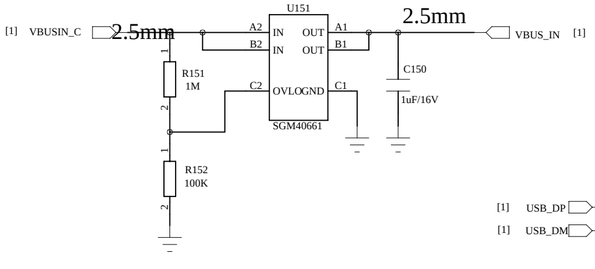
Type C

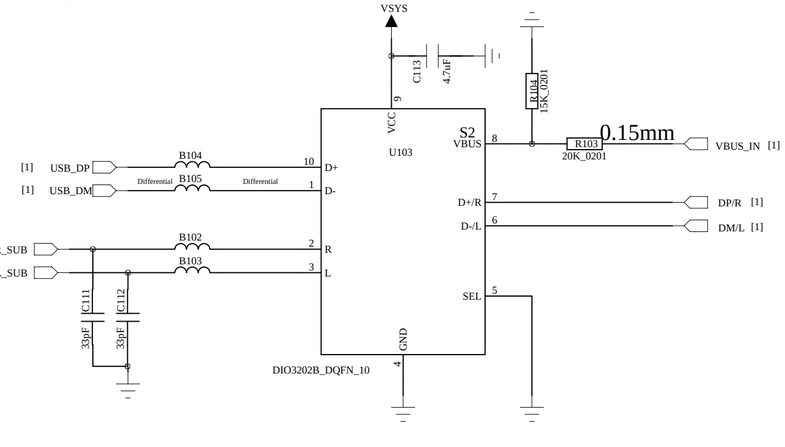




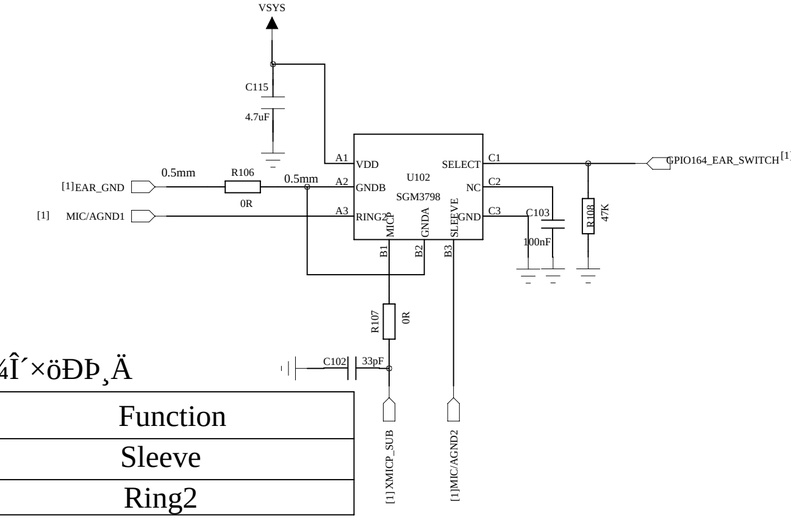






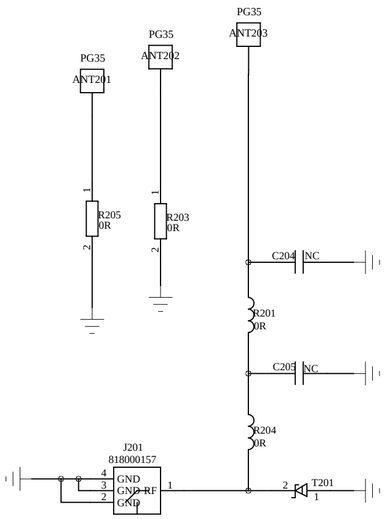


BCT4321NETB-TR



¶Ô±ÈA1Ô-ÀíÍ¼Î´×öÐÞ¸Ä

Select	Function
0	Sleeve
1	Ring2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ANT201
PG35
ANT202
PG35
ANT203
R205
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R203
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R201
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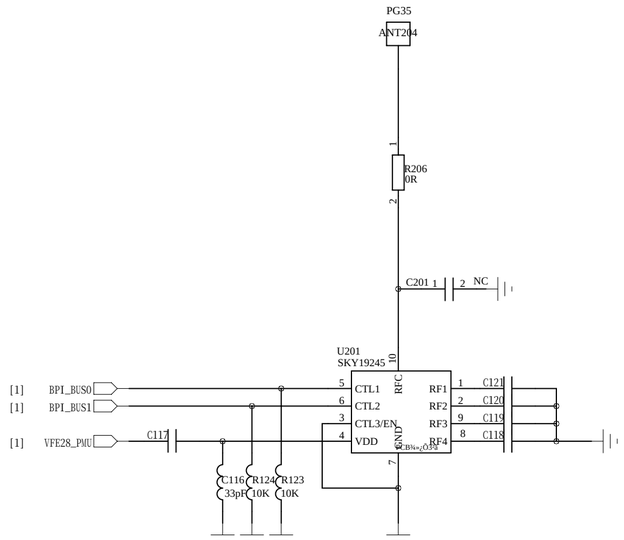
0R
J201
818000157
GND
GND_RF
GND
T201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0R
C201 NC
U201
SKY19245
BPI_BUS0
BPI_BUS1
VFE28_PMU
CTL1
CTL2
CTL3/EN
VDD
RFC
GND
RF1
RF2
RF3
RF4
C121
C120
C119
C118
C117
C116
33pF
R124
10K
R123
10K