SNM758 Hardware Design Guide

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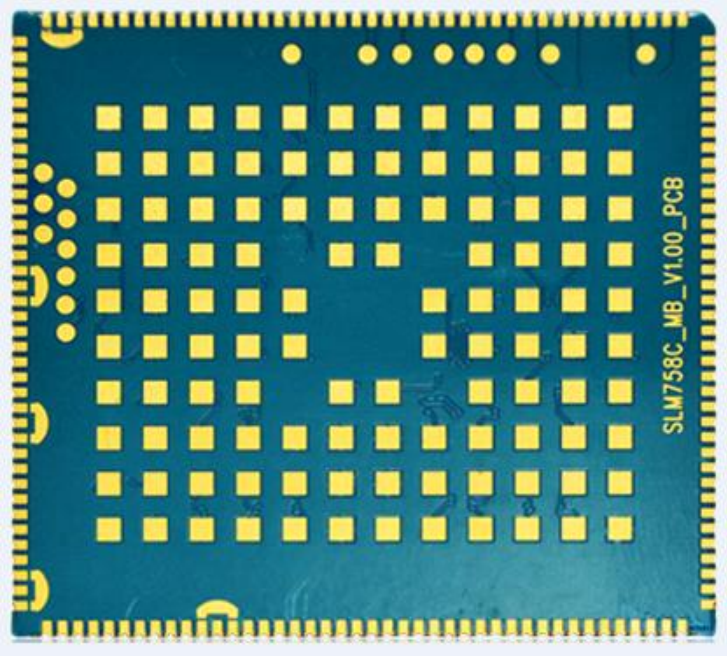
Safety Warning

Pay attention to the following security precautions in the process of using or repairing any terminal or mobile phone. Terminal devices should be informed of the following security information. Otherwise, MeiG will not bear any consequences that the user does not follow these warning operations.

Logo	Requirement
	When you are at a hospital or medical facility, observe the restrictions on using your phone. If necessary, please turn off the terminal or mobile phone, otherwise the medical device may malfunction due to radio frequency interference.
	Turn off the wireless terminal or mobile phone before boarding. To prevent interference with the communication system, wireless communication equipment is prohibited on the aircraft. Ignoring the above will violate local laws and may result in a flight accident.
	Do not use mobile terminals or mobile phones in front of flammable gases. Turn off the mobile terminal when you are near an explosion, chemical factory, fuel depot, or gas station. It is dangerous to operate a mobile terminal next to any potentially explosive electrical equipment.
	The mobile terminal receives or transmits radio frequency energy when it is turned on. It can interfere with TV, radio, computer or other electrical equipment.
	Road safety first! Do not use a handheld terminal or mobile phone while driving, please use a hands-free device. Stop before using your handheld terminal or mobile phone.
	GSM mobile terminals operate under RF signals and cellular networks, but are not guaranteed to be connected in all situations. For example, there is no credit or invalid SIM card. When in this situation and need emergency services, remember to use an emergency call. In order to be able to call and receive calls, the mobile terminal must be powered on and in a service area where the mobile signal is strong enough. Emergency calls are not allowed when certain network services or telephony features are in use, such as feature locks, keyboard locks. These functions should be removed before using an emergency call. Some networks require effective SIM card support.

SNM758 Hardware Design Guide_V1.14



Foreword

Thank you for using the SNM758 module from MeiG Smart. This product can provide data communication services. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

The company does not assume responsibility for property damage or personal injury caused by improper operation of the user. Users are requested to develop the corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety issues that mobile products should focus on.

Before the announcement, the company has the right to modify the contents of this manual according to the needs of technological development.

Contents

Version History

Version	Date	Change Description	Author
1.00	2017-06-12	First edition	Zheng Lei
1.01	2017-08-15	Correction	Guo Qianghua
1.02	2017-11-01	Modify information	Zheng Lei
1.03	2017-11-01	Modify information	Zheng Lei
1.04	2018-1-5	Modify information	Zheng Lei
1.05	2018-6-14	Modify frequency band information	Zheng Lei
1.06	2018-8-3	Add I2S and CBL information	Zheng Lei
1.07	2018-9-6	Update image information	Zheng Lei
1.08	2019-2-26	Delete Programmable Range of Table 4.2	Zheng Lei
1.09	2019-12-2	Modify current parameter	MEIG HW
1.10	2020-1-2	Modify Figure 3.2	MEIG HW
1.11	2020-3-25	Modify Figure 4.6.1	MEIG HW
1.12	2022-8-10	Modify information	MEIG HW
1.13	2023-1-10	Modify Figure 2	MEIG HW

1. Introduction

This document describes the hardware application interfaces of the module, including the connection of the circuit and the RF interface for customer's applications. It can help users quickly understand the interface definition, electrical performance, mechanical details and other relevant information of SNM758 modules. Associated with other application documents, users can quickly use modules to design mobile communication applications.

2. Module Overview

SNM758 series SoC modules, designed based on the MSM8953/SDM450 chipset, its CPU is made of 14nm FinFET, built in 64bit ARM, 8 cores Cortex A-53, main frequency 1.8/2.0/2.2GHz processor(main frequency of SDM450 is 1.8Ghz), supporting LPDDR3 SDRAM memory. This module is suitable for broadband intelligent wireless communication of TD-LTE/ FDD-LTE /WCDMA /EVDO/TD-SCDMA /CDMA/GSM network standards.

The working frequency bands supported by SNM758 module are:

SNM758C

- TDD-LTE: B38/39/40/41
- FDD-LTE: B1/3/5/8
- TD-SCDMA: B34/39
- WCDMA: B1/B5/B8
- EVDO: BC0
- CDMA: BC0
- GSM: B3/5/8

SNM758S

- TDD-LTE: B34/B38/B39/B40/B41
- FDD-LTE: B1/B3/B5/B7/B8/B20
- TD-SCDMA: B34/39
- WCDMA: B1/B5/B8
- EVDO:BC0
- CDMA :BC0
- GSM: B3/B5/B8

SNM758WE/E

- TDD-LTE: B38/40/41
- FDD-LTE: B1/3/5/7/8/20
- WCDMA: B1/B5/B8
- GSM: B5/3/8

SNM758 module provides voice, SMS, address book, WiFi, BT functions while providing high-speed broadband data access; it supports dual 1300W 3D camera or depth of field camera, and can be widely used in VR Camera, intelligent robot, Video surveillance, security, automotive equipment, intelligent platform handheld terminals and other products.

The physical interface of the module is a 272-pin pad that provides the following hardware interfaces:

- Four 1.8V UART serial ports, supporting four or two wires.
- Main LCD（MIPI interface）+ Secondary LCD（MIPI interface）.
- LCD backlight interface.
- Three-way Camera interface（MIPI data）.
- Flashlight interface.

- A high-speed USB interface.
- Two Audio input interface.
- Four Audio output interface.
- Two-way UIM card interface.
- GPIO interface.
- Six groups of I2C interfaces.
- Two sets of SPI interfaces.
- One TF card interface.
- Support GNSS，WiFi2.4G/5G，Bluetooth 4.2 functions.

2.1. Summary of features

Table 1 SNM758 features

Product Characteristics	Description
Platform	Qualcomm MSM8953/SDM450
CPU	Octa-core A53 (64bit) 8*1.8GHz Octa-core A53 (64bit) 8*2.0GHz Octa-core A53 (64bit) 8*2.2GHz
GPU	Adreno506;650MHz(MSM8953)/600MHz(SDM450)
System memory	16GB eMMC + 2GB LPDDR3 933Mhz compatible to 64GB+4GB
OS	Android 7.1/Android8.1/Android 9/Android10
Size	45.5x41.0x3.0mm，160pin LCC+112pin LGA
Frequency Bands SNM758	**SNM758C** TDD-LTE: B38/39/40/41 FDD-LTE: B1/3/5/8 TD-SCDMA: B34/39 WCDMA: B1/5/8 EVDO: BC0 CDMA: BC0 GSM: B5/3/8 **SNM758S**(Finished product code:758S364Q & 758S167A-B7) TDD-LTE: B34/B38/B39/B40/B41 FDD-LTE: B1/B3/B5/B7/B8/B20 TD-SCDMA: B34/39 WCDMA: B1/B5/B8 EVDO:BC0 CDMA :BC0 GSM: B3/B5/B8 **SNM758WE/E** TDD-LTE: B38/40/41

		FDD-LTE: B1/3/5/7/8/20 WCDMA: B1/B5/B8 GSM: B5/3/8
Wi-Fi		WCN3660B:IEEE 802.11b/g/n 2.4G&5G WCN3680B:IEEE 802.11b/g/n/ac 2.4G&5G
Bluetooth		BT 4.2
Data Access	TD-LTE	Cat4 TD-LTE 117/30Mbps
	FDD-LTE	Cat4 FDD-LTE 150/50Mbps
	DC-HSPA+	42/11.2Mbps
	TD-HSPA	2.8/2.3Mbps
	EVDO Rev.A	3.1/1.8Mbps
	EDGE	Class12, 236.8kbps/236.8kbps
	GPRS	Class12, 85.6kbps/85.6kbps
SIM		DSDS(Dual Sim-card Dual Standby) 3.0/1.8V Support SIM hot plug Android 9/Android 10： L/W/G/T+G L/W/G/T+W L/W/G/T+1X L/EVDO/CDMA1X+G Android 7/Android 8 G+1X Don’t support dual CDMA card
Display （Home screen/sub-screen）		Matrix: MSM8953: FULL HD: 1920*1200 60fps; SDM450: FHD+:2090p 30 fps external wireless display
		LCD Size: User defined
		Interface: 1st LCM：MIPI DSI 4-lane; 2nd LCM：MIPI DSI 4-lane
Camera (Front and Rear)		Interface: Support three sets of CSI, each group is 4-Lane
		Camera Pixel:Rear 13-24Mp/Front up to 13Mp, Dual ISP can support dual 13MP Camera at the same time
	Video decode	MSM8953: 4K 30fps, 1080p 60fps, H.264/H.265/ VP8 SDM450：

		1080p60,H.264/H.265/VP8
	Video encode	MSM8953: 4K 30fps,1080p 60 fps: H.264/ H.26/ VP8/VP9 1080P 60fps De +1080p 30fps En SDM450: 1080p60,H.264/H.265/VP8/VP9
Input Device	Key（Power on/off, Home, Volume+, Volume-）	
	Capacitive TP	
Reset	Support HW reset	
Application interface	Interface name	Main function description
	VBAT	3pin，Power input，3.5V～4.2V，Nominal value3.8V
	SDIO *1	TF Card，Support 256GB max
	USB2.0(3.0)	Support OTG USB_BOOT（Force USB boot for emergency downloads）
	BLSP ports	8 ports(BLSP1-8)，multiplexed serial interface functions
	UART*4	BLSP2,BLSP4-6 support UART，up to 4M bps
	I2C*6	BLSP2-6&BLSP8 support I2C, These BLSPs use bits for I2C
	SPI(master only)	SPI is only support via BLSP
	ADC*3	Support
	Charge	Support5V/2A
	Vibrator	Support
	GPIO	18 GPIOs，Excluded BLSP multiplexing GPIO and GPIO involved in LCM、 TP and CAMERA
	VCOIN	Real time clock backup battery
	RF Interface	Multi-mode LTE main antenna Multi-mode LTE diversity antenna 2.4G WiFi/BT antenna 5G WIFI antenna
	Audio	One main MIC One noise reduction MIC One Hands free speaker（Built in 0.8W Class D amplifier） One earpiece

One stereo headphone(With headphone MIC)
One audio output
Two I2S signal

3. Module Package

3.1.Pin Distribution Diagram

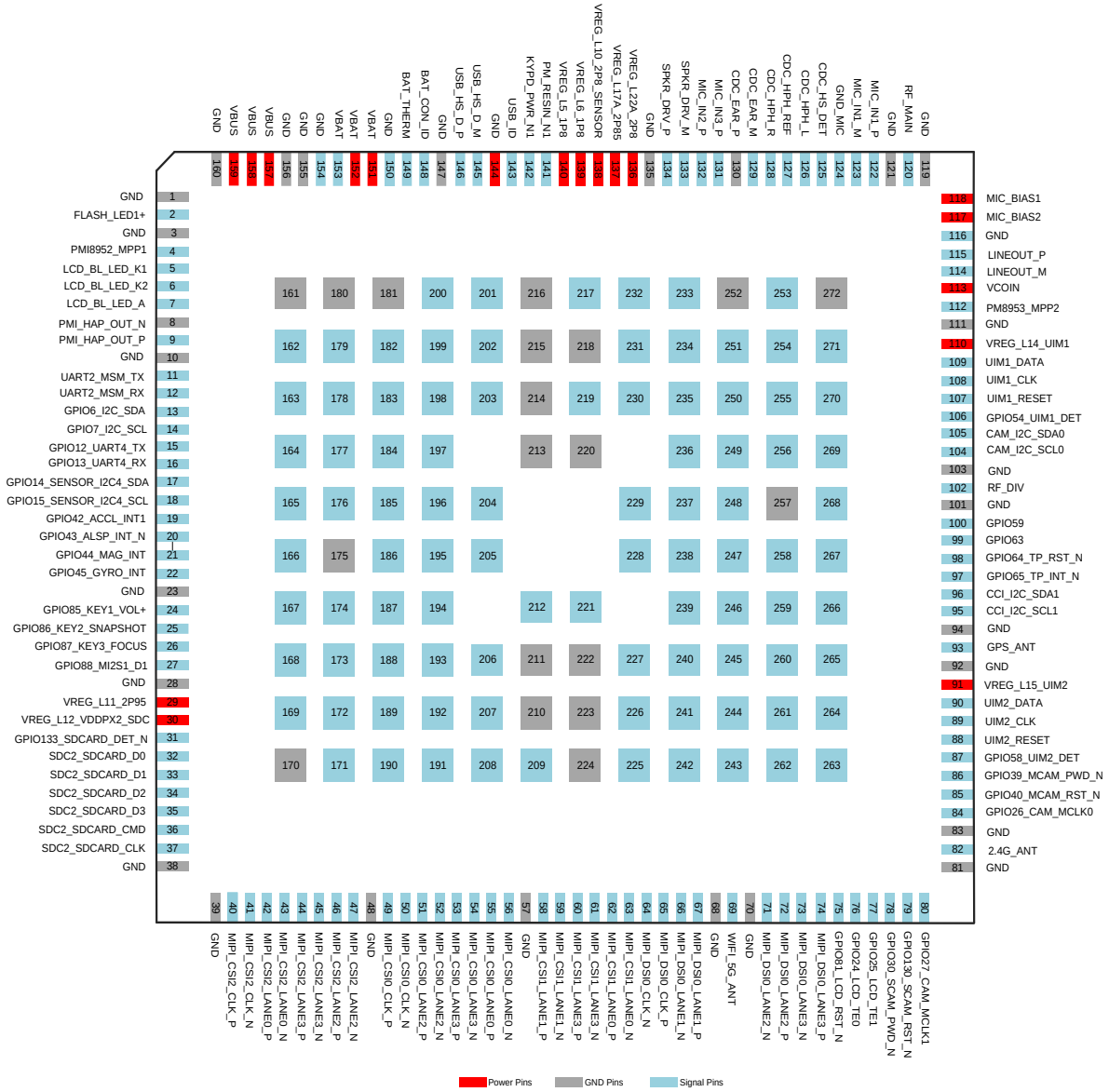


Figure 1 module pin diagram (top view)

3.2.Pin Definitions

Table 2 Pin Characteristics

#	Name	GPIO Interruppt	I/O	Function Description	Remark
1	GND		GND	GND	
2	FLASH_LED1+		AO	FLASH LED anode(1A)	758C supports 1A, 758W/S supports 1.5A. This pin is not available for PMI module
3	GND		GND	GND	
4	PMI8952_MPP1		AO-Z,AI,DO	Configurable MPP,PWM,ADC	Remove the PMI module, this pin is not available
5	LCD_BL_LED_K1		AI	LCD Backlight cathode1(20 mA)	30mA MAX, remove Remove PMI and 758S/758W module, this pin is not available, need to add backlight IC
6	LCD_BL_LED_K2		AI	LCD Backlight cathode2(20 mA)	30mA MAX, remove PMI and 758S/758W module, this pin is not available, need to add backlight IC
7	LCD_BL_LED_A		PO	LCD Backlight anode	28V MAX, remove PMI and 758S/758W module, this pin is not available, need to add backlight IC
8	PMI_HAP_OUT_N		AI	Haptics driver enter negative	Input 28V MAX, remove PMI and 758S/758W module, this pin is not available, need to add backlight IC
9	PMI_HAP_OUT_P		AO	Haptics driver output positive	758W/S only supports ERM, 758C supports ERM, LRA, remove PMI module, this pin is not available
10	GND		GND	GND	
11	UART2_MSM_TX	GPIO_4	B-PD:nppukp	Configurable I/O,UART2 TX（debug serial port）	
12	UART2_MSM_RX	GPIO_5*	B-PD:nppukp	Configurable I/O,UART2 RX（debug serial port）	
13	GPIO6_I2C2_SDA	GPIO_6	B-PD:nppukp	Configurable I/O, I2C SDA	
14	GPIO7_I2C2_SCL	GPIO_7	B-PD:nppukp	Configurable I/O, I2C SCL	
15	GPIO12_UART4_T	GPIO_12*	B-PD:npp	Configurable I/O,UART4	

	X		ukp	TX	
16	GPIO13_UART4_RX	GPIO_13*	B-PD:nppukp	Configurable I/O,UART4 RX	
17	GPIO14_SENSOR_I2C4_SDA	GPIO_14	B-PD:nppukp	Configurable I/O,SENSOR I2C SDA	This GPIO can only be used as SENSOR I2C and cannot be occupied
18	GPIO15_SENSOR_I2C4_SCL	GPIO_15	B-PD:nppukp	Configurable I/O, SENSOR I2C SCL	This GPIO can only be used as SENSOR I2C and cannot be occupied
19	GPIO42_ACCL_INT1	GPIO_42*	B-PD:nppukp	Configurable I/O,ACC INT	
20	GPIO43_ALSP_INT_N	GPIO_43*	B-PD:nppukp	Configurable I/O,ALSP INT	
21	GPIO44_MAG_INT	GPIO_44*	B-PD:nppukp	Configurable I/O,MAG INT	
22	GPIO45_GYRO_INT	GPIO_45*	B-PD:nppukp	Configurable I/O,GYRO INT	
23	GND		GND	GND	
24	GPIO85_KEY1_VOL+	GPIO_85*	B-PD:nppukp	Configurable I/O,KEY VOL+	
25	GPIO86_KEY2_SNAPSHOT	GPIO_86*	B-PD:nppukp	Configurable I/O, KEY 2	
26	GPIO87_KEY3_FOCUS	GPIO_87*	B-PD:nppukp	Configurable I/O, HOME KEY	
27	GPIO88_MI2S1_D1	GPIO_88	B-PD:nppukp	Configurable I/O or I2S_D1	
28	GND		GND	GND	
29	VREG_L11_2P95		PO	PMIC output 2.95V for SD-card power	
30	VREG_L12_VDDPX2_SDC		PO	PMIC output 2.95V for SD signal	
31	GPIO133_SDCAR	GPIO_133*	B-PD:npp	Configurable I/O,SD card	

	D_DET_N	ukp	detection
32	SDC2_SDCARD_D0	BH-NP:pdpukp	Secure digital controller data bit 0
33	SDC2_SDCARD_D1	BH-NP:pdpukp	Secure digital controller data bit 1
34	SDC2_SDCARD_D2	BH-NP:pdpukp	Secure digital controller data bit 2
35	SDC2_SDCARD_D3	BH-NP:pdpukp	Secure digital controller data bit 3
36	SDC2_SDCARD_CMD	BH-NP:pdpukp	Secure digital controller command
37	SDC2_SDCARD_CLK	BH-NP:pdpukp	Secure digital controller clock
38	GND	GND	GND
39	GND	GND	GND
40	MIPI_CSI2_CLK_P	AI	MIPI camera serial interface 2 clock+
41	MIPI_CSI2_CLK_N	AI	MIPI camera serial interface 2 clock-
42	MIPI_CSI2_LANE0_P	AI	MIPI camera serial interface 2 lane0+
43	MIPI_CSI2_LANE0_N	AI	MIPI camera serial interface 2 lane0-
44	MIPI_CSI2_LANE3_P	AI	MIPI camera serial interface 2 lane3+
45	MIPI_CSI2_LANE3_N	AI	MIPI camera serial interface 2 lane3-

46	MIPI_CSI2_LANE2_P	AI	MIPI camera serial interface 2 lane2+
47	MIPI_CSI2_LANE2_N	AI	MIPI camera serial interface 2 lane2-
48	GND	GND	GND
49	MIPI_CSI0_CLK_P	AI	MIPI camera serial interface 0 clock+
50	MIPI_CSI0_CLK_N	AI	MIPI camera serial interface 0 clock-
51	MIPI_CSI0_LANE2_P	AI	MIPI camera serial interface 0 lane2+
52	MIPI_CSI0_LANE2_N	AI	MIPI camera serial interface 0 lane2-
53	MIPI_CSI0_LANE3_P	AI	MIPI camera serial interface 0 lane3+
54	MIPI_CSI0_LANE3_N	AI	MIPI camera serial interface 0 lane3-
55	MIPI_CSI0_LANE0_P	AI	MIPI camera serial interface 0 lane0+
56	MIPI_CSI0_LANE0_N	AI	MIPI camera serial interface 0 lane0-
57	GND	GND	GND
58	MIPI_CSI1_LANE1_P	AI	MIPI camera serial interface 1 lane1+

59	MIPI_CSI1_LANE1_N	AI	MIPI camera serial interface 1 lane1-
60	MIPI_CSI1_LANE3_P	AI	MIPI camera serial interface 1 lane3+
61	MIPI_CSI1_LANE3_N	AI	MIPI camera serial interface 1 lane3-
62	MIPI_CSI1_LANE0_P	AI	MIPI camera serial interface 1 lane0+
63	MIPI_CSI1_LANE0_N	AI	MIPI camera serial interface 1 lane0-
64	MIPI_DSI0_CLK_N	AO	MIPI display serial interface 0 clock-
65	MIPI_DSI0_CLK_P	AO	MIPI display serial interface 0 clock+
66	MIPI_DSI0_LANE1_N	AO	MIPI display serial interface 0 lane1-
67	MIPI_DSI0_LANE1_P	AO	MIPI display serial interface 0 lane1+
68	GND	GND	GND
69	5G_ANT	AI	RF signal for 5G WIFI
70	GND	GND	GND
71	MIPI_DSI0_LANE2_N	AO	MIPI display serial interface 0 lane2-
72	MIPI_DSI0_LANE2	AO	MIPI display serial

	_P			interface 0 lane2+	
73	MIPI_DSI 0_LANE3 _N		AO	MIPI display serial interface 0 lane3-	
74	MIPI_DSI 0_LANE3 _P		AO	MIPI display serial interface 0 lane3+	
75	GPIO61_ LCD_RS T_N	GPIO_61*	B-PD:npp ukp	Configurable I/O, primary LCD RESET	
76	GPIO24_ LCD_TE0	GPIO_24	B-PD:npp ukp	Configurable I/O, primary LCD TE	
77	GPIO25_ LCD_TE1	GPIO_25*	B-PD:npp ukp	Configurable I/O, secondary LCD TE	
78	GPIO130 _SCAM_ PWD_N	GPIO_130*	B-PD:npp ukp	Configurable I/O, CSI2 PWDN	No pull-up resistors can be added to this pin This GPIO can only be used for proactive power-off control and cannot be occupied
79	GPIO129 _SCAM_ RST_N	GPIO_129*	B-PD:npp ukp	Configurable I/O, CSI2 RESET	
80	GPIO27_ CAM_MC LK1		B-PD:npp ukp	Configurable I/O, CSI2 MCLK	This GPIO can only be used for proactive clock control and cannot be occupied
81	GND		GND	GND	
82	2.4G_AN T		AI	RF signal for 2.4G WIFI&BT	
83	GND		GND	GND	
84	GPIO26_ CAM_MC LK0	GPIO_26	B-PD:npp ukp	Configurable I/O, CSI0 MCLK	This GPIO can only be used for the clock control of the rear camera and cannot be occupied
85	GPIO40_ MCAM_R ST_N	GPIO_40	B-PD:npp ukp	Configurable I/O, CSI0 RESET	
86	GPIO39_ MCAM_P WD_N	GPIO_39	B-PD:npp ukp	Configurable I/O, CSI0 PWDN	This GPIO can only be used as the power-off control of the rear camera and cannot be occupied
87	GPIO58_ UIM2_DE	GPIO_58*	B-PD:npp	UIM2 removal detection	

	T		ukp		
88	UIM2_RESET		B-PD:nppukp	UIM2 reset	
89	UIM2_CLK		B-PD:nppukp	UIM2 clock	
90	UIM2_DATA		B-PD:nppukp	UIM2 data	
91	VREG_L15_UIM2		PO	PMIC output for UIM2	
92	GND		GND	GND	
93	ANT		AI	RF signal for ANT	
94	GND		GND	GND	
95	CAM_I2C_SCL1	GPIO_32	B-PD:nppukp	Configurable I/O, CSI1 I2C1 SCL	This GPIO can only be used as CAMERA I2C and cannot be occupied
96	CAM_I2C_SDA1	GPIO_31*	B-PD:nppukp	Configurable I/O, CSI1 I2C1 SDA	This GPIO can only be used as CAMERA I2C and cannot be occupied
97	GPIO65_TP_INT_N	GPIO_65*	B-PD:nppukp	Configurable I/O,TP INT	
98	GPIO64_TP_RST_N	GPIO_64	B-PD:nppukp	Configurable I/O,TP RESET	
99	GPIO63	GPIO_63*	B-PD:nppukp	Configurable I/O,	
100	GPIO59	GPIO_59*	B-PD:nppukp	Configurable I/O,	
101	GND		GND	GND	
102	RF_DIV		AI	RF signal for diversity ANT	
103	GND		GND	GND	
104	CAM_I2C_SCL0		B-PD:nppukp	CSI2 I2C SCL	
105	CAM_I2C_SDA0		B-PD:nppukp	Configurable I/O, CSI2 I2C SDA	
106	GPIO54_	GPIO_54*	B-	UIM1 removal	

	UIM1_DET	PD:nppukp	detection
107	UIM1_RESET	B-PD:nppukp	UIM1 reset
108	UIM1_CLK	B-PD:nppukp	UIM1 clock
109	UIM1_DATA	B-PD:nppukp	UIM1 data
110	VREG_L14_UIM1	PO	PMIC output for UIM1
111	GND	GND	GND
112	PM8953_MPP2	AO-Z,DI,DO	Configurable MPP,PWM,ADC
113	VCOIN	AI,AO	RTC battery
114	LINEOUT_M	AO	Audio lineout minus for audio PA
115	LINEOUT_P	AO	Audio lineout plus for audio PA
116	GND	GND	GND
117	MIC_BIAS2	AO	Microphone bias for earphone mic
118	MIC_BIAS1	AO	Microphone bias
119	GND	GND	GND
120	RF_MAIN	AI	RF signal for main ANT
121	GND	GND	GND
122	MIC_IN1_P	AI	Microphone 1input plus
123	MIC_IN1_M	AI	Microphone input minus
124	GND_MIC	GND	Microphone bias filter ground
125	CDC_HS_DET	AI	MBHC mechanical insertion/removal-detection

126	CDC_HPH_L	AO	Headphone output, left channel
127	CDC_HPH_REF	AI	Headphone ground reference
128	CDC_HPH_R	AO	Headphone output, right channel
129	CDC_EAR_M	AO	Earpiece output, minus
130	CDC_EAR_P	AO	Earpiece output, plus
131	MIC_IN3_P	AI	Auxiliary MIC positive
132	MIC_IN2_P	AI	Headphone MIC positive
133	SPKR_DRV_M	AO	PA(0.85W) output, minus
134	SPKR_DRV_P	AO	PA(0.85W) output, plus
135	GND	GND	GND
136	VREG_L22_2P8	PO	CAM AVDD 2.8V Supply voltage
137	VREG_L17_2P85	PO	LCD,CAM,TP 2.8V Supply voltage
138	VREG_L10_2P8_SENSOR	PO	Sensor 2.8V Supply voltage
139	VREG_L6_1P8	PO	LCD,CAM,TP, sensor 1.8V Supply voltage
140	VREG_L5_1P8	PO	digital I/Os 1.8V Supply voltage
141	PM_RESIN_N1	DI	RESET
142	KYPD_PWR_N1	DI	KEY POWER ON/OFF
143	USB_ID	AI	USB ID
144	GND	GND	GND
145	USB_HS_D_M	AI,AO	USB data minus

146	USB_HS_D_P	AI,AO	USB data plus	
147	GND	GND	GND	
148	BAT_CON_ID	AI	Battery ID input to ADC	Remove the PMI module, this pin is not available
149	BAT_THERM	AI	Battery temperature input to ADC	Remove the PMI module, this pin is not available
150	GND	GND	GND	
151	VBAT	PI,PO	Battery,3.5V-4.2V,default 3.8V	
152	VBAT	PI,PO	Battery,3.5V-4.2V,default 3.8V	
153	VBAT	PI,PO	Battery,3.5V-4.2V,default 3.8V	758S this pin is VBAT_SNS_P (to PMI's 758S, please NC for this pin)
154	GND	GND	GND	758S this pin is VBAT_PACK_SNS_M (to PMI's 758S, please NC for this pin)
155	GND	GND	GND	
156	GND	GND	GND	
157	VBUS	PI,PO	5V charging input power/OTG output power	
158	VBUS	PI,PO	5V charging input power/OTG output power	
159	VBUS	PI,PO	5V charging input power/OTG output power	
160	GND	GND	GND	
161	GND	GND	GND	
162	Reserved (HAPTICS_CDC_LOUT3)		Reserved	
163	Reserved (CODEC_DIV_CLK)		Reserved	
164	GPIO98_I2C8_SDA	GPIO_98	B-PD:npp	Configurable I/O, I2C SDA

			ukp		
165	GPIO99_I2C8_SCL	GPIO_99	B-PD:nppukp	Configurable I/O, I2C SCL	
166	GPIO33	GPIO_33	B-PD:nppukp	Configurable I/O	
167	GPIO35	GPIO_35*	B-PD:nppukp	Configurable I/O	No pull-up resistors can be added to this pin
168	GPIO36	GPIO_36*	B-PD:nppukp	Configurable I/O	
169	GPIO91_MI2S_1_SCK	GPIO_91*	B-PD:nppukp	Configurable I/O, I2S1_SCK	
170	GND		GND	GND	
171	MIPI_CSI1_LANE2_P		AI	CSI1 MIPI lane2+	
172	MIPI_CSI1_LANE2_N		AI	CSI1 MIPI lane2-	
173	USB3_SS_RX_M		AI	USB3 super-speed receive – minus	
174	USB3_SS_RX_P		AI	USB3 super-speed receive – plus	
175	GND		GND	GND	
176	GPIO20_UART6_TX	GPIO_20	B-PD:nppukp	Configurable I/O,UART6 TX	
177	GPIO21_UART6_RX	GPIO_21*	B-PD:nppukp	Configurable I/O,UART6 RX	
178	Reserved			Reserved	
179	Reserved			Reserved	
180	GND		GND	GND	
181	GND		GND	GND	
182	CHG_LED		AO	Current sink for charging indication	Remove the PMI module, this pin is not available
183	Reserved			Reserved	

184	GPIO22_I2C6_SDA	GPIO_22	B-PD:nppukp	Configurable I/O, I2C SDA	
185	GPIO23_I2C6_SCL	GPIO_23	B-PD:nppukp	Configurable I/O, I2C SCL	
186	USB3_SS_TX_P		AO	USB super-speed transmit – plus	
187	USB3_SS_TX_M		AO	USB super-speed transmit – minus	
188	GPIO139_USB_SS_SEL	GPIO_139	B-PD:nppukp	Configurable I/O, USB Type C switch control	此引脚不能加上拉电阻
189	MIPI_DSI0_LANE0_N		AO	MIPI DSI0 interface lane0-	
190	MIPI_DSI0_LANE0_P		AO	MIPI DSI0 interface lane0+	
191	MIPI_CSI2_LANE1_P		AI	MIPI CSI2 interface lane1+	
192	MIPI_CSI2_LANE1_N		AI	MIPI CSI2 interface 2 lane1-	
193	MIPI_CSI0_LANE1_P		AI	MIPI CSI0 interface lane1+	
194	MIPI_CSI0_LANE1_N		AI	MIPI CSI0 interface lane1-	
195	GPIO94	GPIO_94	B-PD:nppukp	Configurable I/O	
196	GPIO95	GPIO_95	B-PD:nppukp	Configurable I/O	
197	GPIO96	GPIO_96	B-PD:nppukp	Configurable I/O	No pull-up resistors can be added to this pin
198	GPIO97	GPIO_97*	B-PD:npp	Configurable I/O	

			ukp		
199	VREG_L2_1P1		PO	CSI0 DVDD 1.1V Supply voltage	
200	VREG_L23_1P175		PO	CSI2 DVDD 1.175V Supply voltage	
201	USB_CC1		AI;AO	USB type C connector configuration channel1	
202	USB_CC2		AI;AO	USB type C connector configuration channel2	
203	CBL_PWR_N1		DI	Cable power-on; initiates power on when grounded	
204	GPIO89	GPIO_89	B-PD:nppukp	Configurable I/O	DMIC0_CLK
205	GPIO90	GPIO_90*	B-PD:nppukp	Configurable I/O	DMIC0_DATA
206	FORCE_USB_BOOT		DI	Force download port	
207	MIPI_CSI1_CLK_N		AI	MIPI CSI1 clock-	
208	MIPI_CSI1_CLK_P		AI	MIPI CSI1 clock+	
209	PM8953_MPP4		AO-Z,DI,DO	Configurable MPP,PWM,ADC	
210	GND		GND	GND	
211	GND		GND	GND	
212	GPIO66	GPIO_66	B-PD:nppukp	Configurable I/O	
213	GND		GND	GND	
214	GND		GND	GND	
215	GND		GND	GND	

216	GND		GND	GND	
217	VREG_L13_3P075		PO	audio codec 3.075V Supply voltage	
218	GND		GND	GND	
219	VREG_S4_2P05		PO	audio codec 2.05V Supply voltage	
220	GND		GND	GND	
221	GPIO46_PRESSURE_INT	GPIO_46*	B-PD:nppukp	Configurable I/O, PRESSURE INT	
222	GND		GND	GND	
223	GND		GND	GND	
224	GND		GND	GND	
225	MIPI_DSI1_LANE0_P		AO	MIPI DSI1 lane0+	
226	MIPI_DSI1_LANE0_N		AO	MIPI DSI1 lane0-	
227	Reserved（WCD_RF_PA_ON）			Reserved	This pin is left open
228	GPIO50	GPIO_50	B-PD:nppukp	Configurable I/O	
229	Reserved（WCD_MSM_MCLK）			Reserved	This pin is left open
230	Reserved（WCD_RST_N）			Reserved	This pin is left open
231	GPIO9	GPIO_9*	B-PD:nppukp	Configurable I/O,	
232	GPIO8	GPIO_8	B-PD:nppukp	Configurable I/O,	
233	GPIO11_TP_I2C3_	GPIO_11	B-PD:npp	Configurable I/O, CTP I2C	

	SCL		ukp	SCL	
234	GPIO10_TP_I2C3_SDA	GPIO_10	B-PD:nppukp	Configurable I/O, CTP I2C SDA	
235	GPIO47	GPIO_47	B-PD:nppukp	Configurable I/O,	
236	Reserved（SLIMBUS_DATA1）			Reserved	This pin is left open
237	Reserved（SLIMBUS_DATA0）			Reserved	This pin is left open
238	Reserved（SLIMBUS_CLK）			Reserved	This pin is left open
239	MIPI_DSI1_LANE1_P		AO	MIPI DSI1 lane1+	
240	MIPI_DSI1_LANE1_N		AO	MIPI DSI1 lane1-	
241	MIPI_DSI1_CLK_P		AO	MIPI DSI1 clock+	
242	MIPI_DSI1_CLK_N		AO	MIPI DSI1 clock-	
243	MIPI_DSI1_LANE2_P		AO	MIPI DSI1 lane2+	
244	MIPI_DSI1_LANE2_N		AO	MIPI DSI1 lane2-	
245	MIPI_DSI1_LANE3_P		AO	MIPI DSI1 lane3+	
246	MIPI_DSI1_LANE3_N		AO	MIPI DSI1 lane3-	
247	Reserved（WCD_INTR2）			Reserved	This pin is left open
248	Reserved（WCD_INTR1）			Reserved	This pin is left open

249	GPIO128	GPIO_128	B-PD:nppukp	Configurable I/O,	
250	Reserved			Reserved	
251	GPIO38	GPIO_38*	B-PD:nppukp	Configurable I/O,	
252	GND		GND	GND	
253	GPIO19_NFC_I2C5_SCL	GPIO_19	B-PD:nppukp	Configurable I/O,NFC I2C SCL	
254	GPIO18_NFC_I2C5_SDA	GPIO_18	B-PD:nppukp	Configurable I/O, NFC I2C SDA	
255	GPIO17_UART5_RX	GPIO_17*	B-PD:nppukp	Configurable I/O,UART5 RX	
256	GPIO16_UART5_TX	GPIO_16	B-PD:nppukp	Configurable I/O,UART5 TX	
257	GND		GND	GND	
258	GPIO3_SPI1_CLK	GPIO_3	B-PD:nppukp	Configurable I/O, SPI1 CLK	
259	GPIO2_SPI1_CS	GPIO_2	B-PD:nppukp	Configurable I/O, SPI1 CS	
260	GPIO1_SPI_MISO	GPIO_1*	B-PD:nppukp	Configurable I/O, SPI MISO	
261	GPIO0_SPI_MOSI	GPIO_0	B-PD:nppukp	Configurable I/O, SPI MOSI	
262	GPIO132_DCAM_PWD_N	GPIO_132*	B-PD:nppukp	Configurable I/O, CSI1 pwdn	No pull-up resistors can be added to this pin This GPIO can only be used as the power-off control of the secondary camera and cannot be occupied
263	GPIO131_DCAM_RST_N	GPIO_131*	B-PD:nppukp	Configurable I/O, CSI1 reset	
264	GPIO28_CAM_MCLK2	GPIO_28*	B-PD:nppukp	Configurable I/O, CSI1 MCLK	This GPIO can only be used as the clock control of the sub-camera and cannot be occupied
265	GPIO93_MI2S_1_	GPIO_93*	B-PD:npp	Configurable I/O, I2S1_D0	

	D0		ukp		
266	GPIO138_FP_SPI_MISO	GPIO_138	B-PD:nppukp	Configurable I/O, fingerprint SPI MISO，I2S2_D1	MI2S_2_D1
267	GPIO137_FP_SPI_MOSI	GPIO_137*	B-PD:nppukp	Configurable I/O, fingerprint SPI MOSI，MI2S_2_D0	MI2S_2_D0
268	GPIO136_FP_SPI_CS	GPIO_136	B-PD:nppukp	Configurable I/O, fingerprint SPI CS，I2S2_WS	MI2S_2_WS
269	GPIO135_FP_SPI_CLK	GPIO_135	B-PD:nppukp	Configurable I/O, fingerprint SPI CLK，I2S2_SCK	MI2S_2_SCK
270	GPIO48_FP_INT_N	GPIO_48*	B-PD:nppukp	Configurable I/O, fingerprint INT	
271	GPIO92_MI2S_1_WS	GPIO_92	B-PD:nppukp	Configurable I/O, MI2S1_WS	
272	GND		GND	GND	

*：Wake-up system interrupt pin

B：Bidirectional digital with CMOS input

H：High-voltage tolerant

NP：pdpukp=default no-pull with programmable options following the colon (:)

PD：nppukp=default pull down with programmable options following the colon (:)

PU：nppdkp=default pull up with programmable options following the colon (:)

KP：nppdpu=default keeper with programmable options following the colon (:)

3.3. Mechanical Dimensions

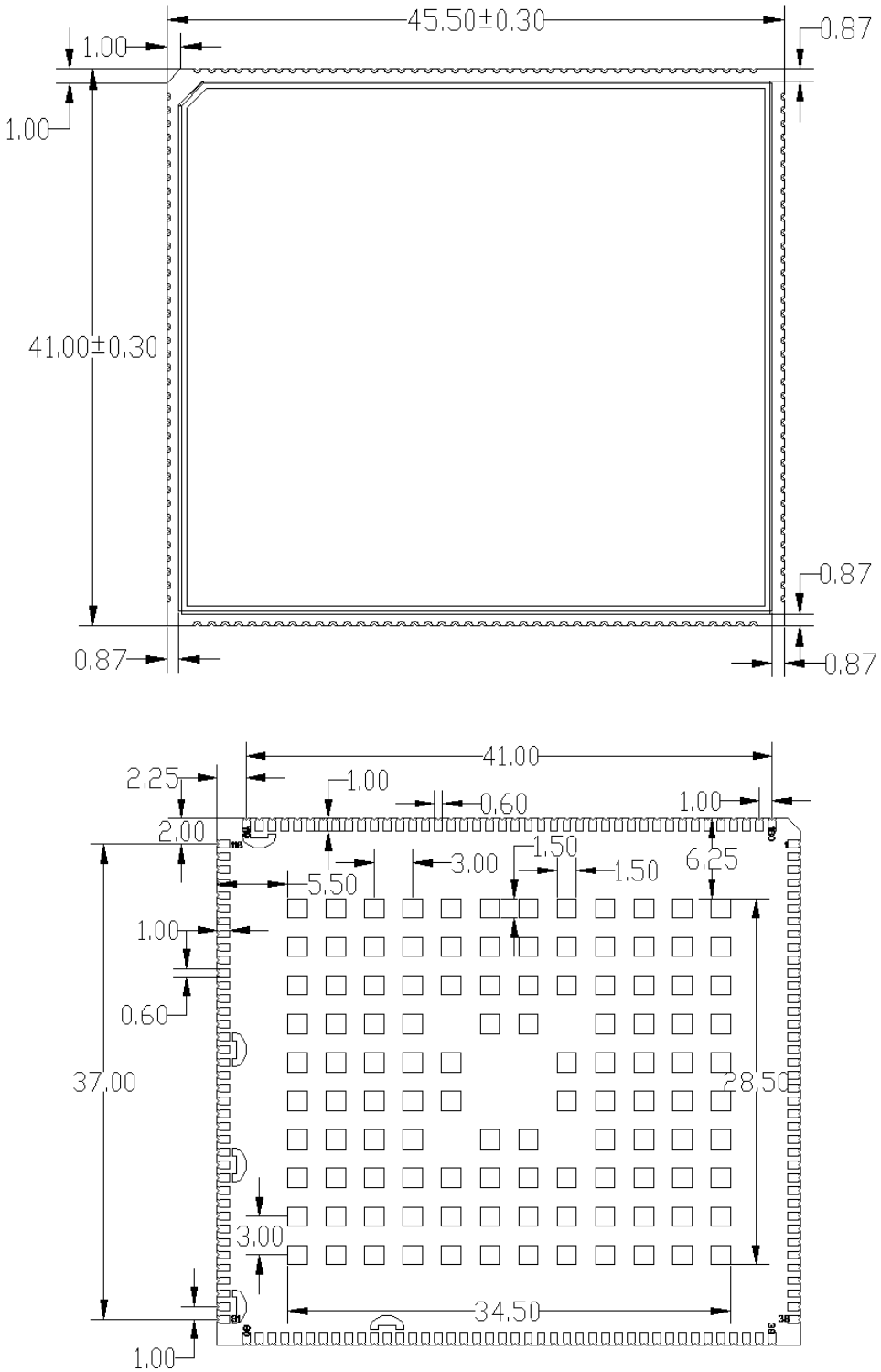


Figure 2 Module 3D size（unit：mm）

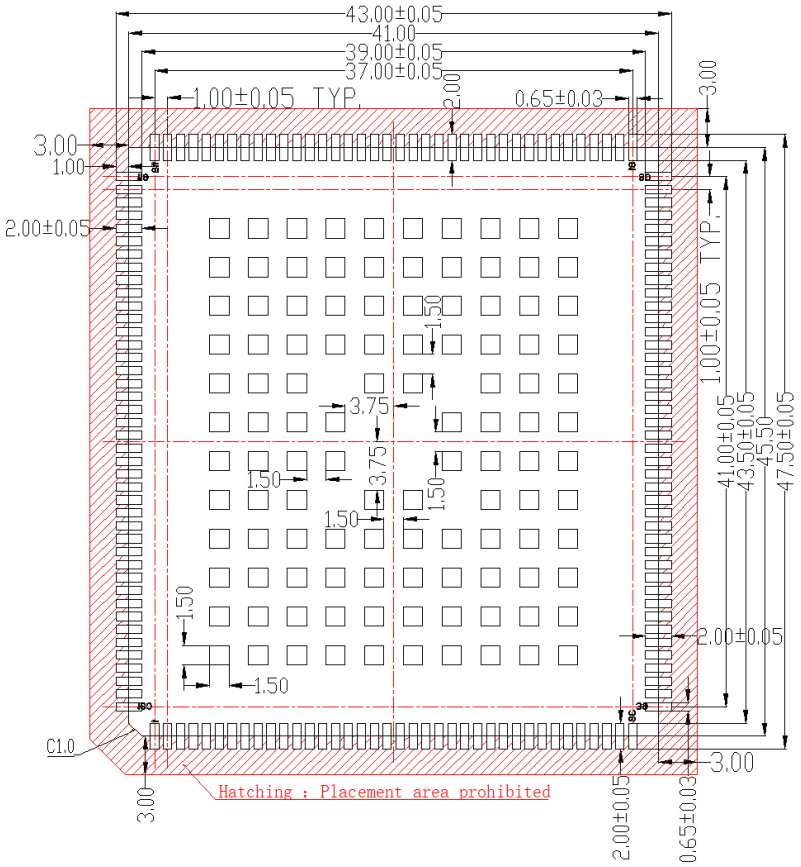


Figure 3 Recommended PCB package size (unit: mm)

4. Interface Application

4.1. Power Supply

Take a battery powered device, for example, the voltage input range of the module VBAT is 3.5V to 4.2V, and the recommended voltage is 3.8V. In the GSM band,When this module transmits at the maximum charge, the peak current can reach 3A causing the maximum voltage to drop to VBAT.

It is recommended to use a large capacitor regulator close to VBAT. It is recommended to use two 47uF ceramic capacitors. Parallel 33PF and 10PF capacitors can effectively remove high frequency interference. To prevent damage to the chip due to ESD and surge, it is recommended to use a suitable TVS tube and a 5.6V/500mW Zener diode at the VBAT pin of the module. For PCB layout, the capacitors and diodes should be as close as possible to the VBAT pin of the module. The user can directly power the module with a 3.8V lithium-ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

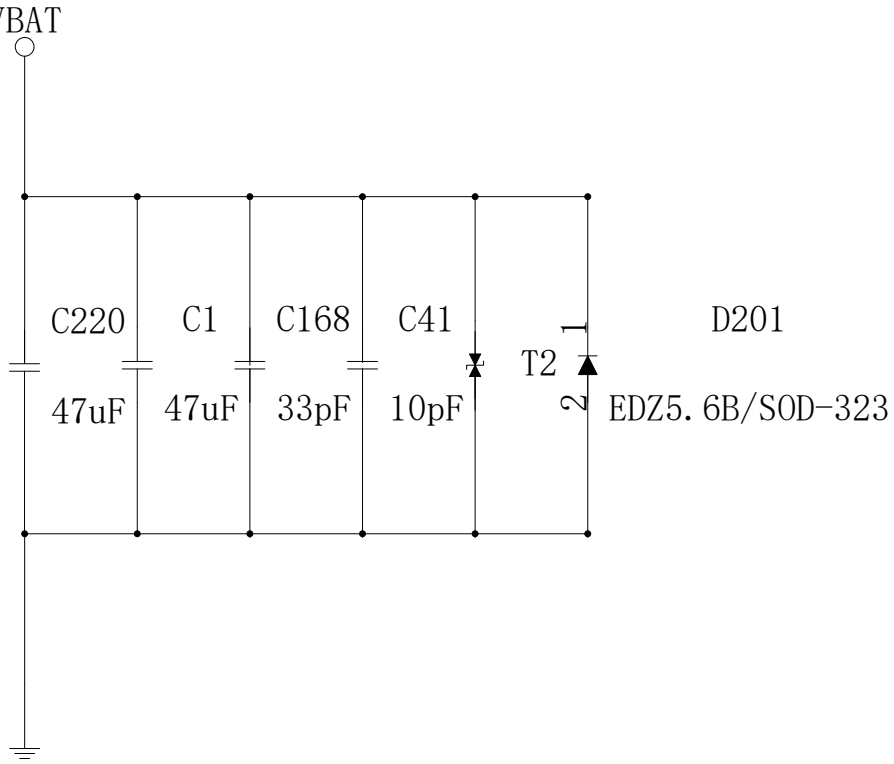


Figure 4 VBAT input reference circuit

If it is a device powered by DC power supply, the DC input voltage range is 5V~12V. The recommended circuit that can be powered by DC-DC is shown below:

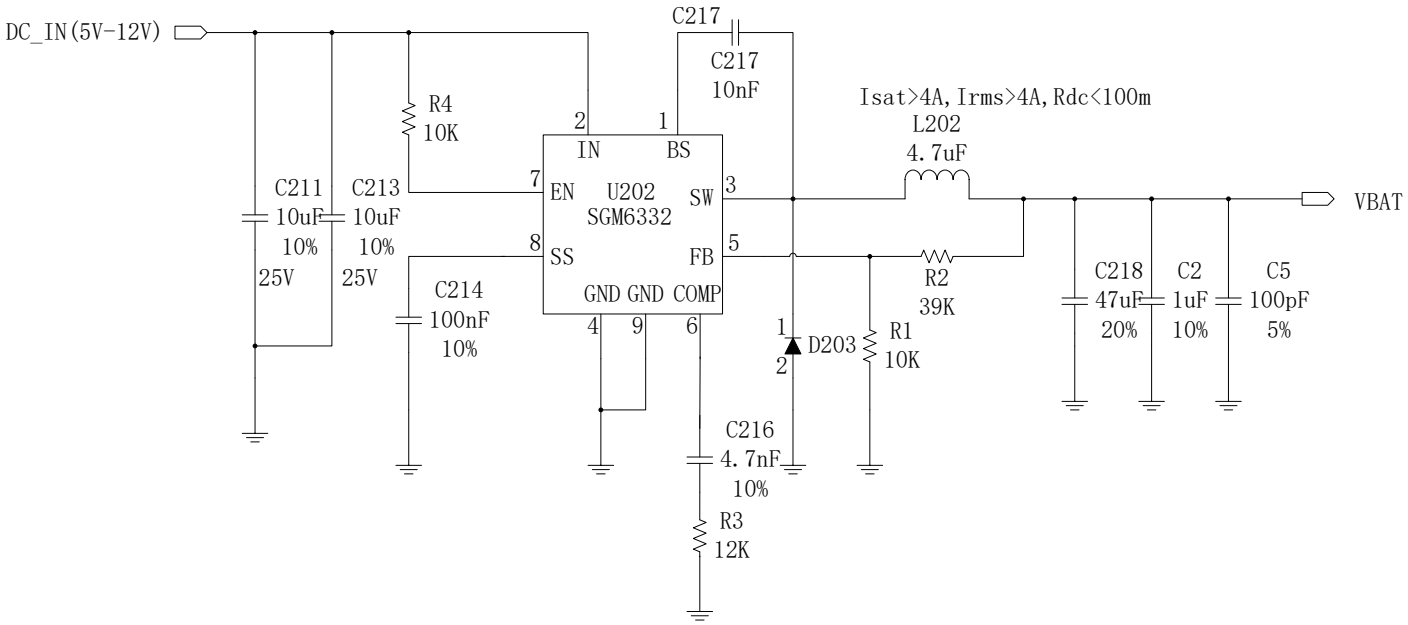


Figure 5 DC-DC power supply circuit

Note:

If the user does not use battery power, please note that a 10K resistor needed to be connected to the 149 pin (BAT_THERM) of the module and pulled down to GND to prevent the software from judging the abnormal battery temperature after the module is turned on, resulting in shutdown. The connection diagram is as follows:

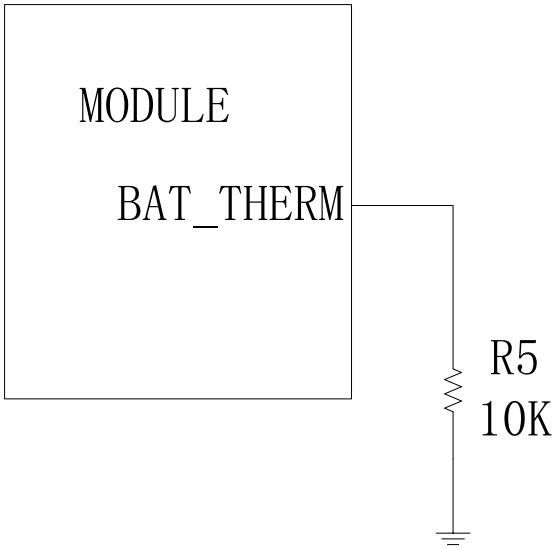


Figure 6 Connection diagram when not powered by battery

4.1.1. Power Pin

The VBAT pin (151, 152, 153) is used for power input. In the user's design, pay special attention to the design of the power supply section to ensure that the VBAT does not fall below 3.5V even when the module consumes 3A. If the voltage drops below 3.5V, the module may shut down. The PCB layout

from the VBAT pin to the power supply should be wide enough to reduce the voltage drop in the transmit burst mode.

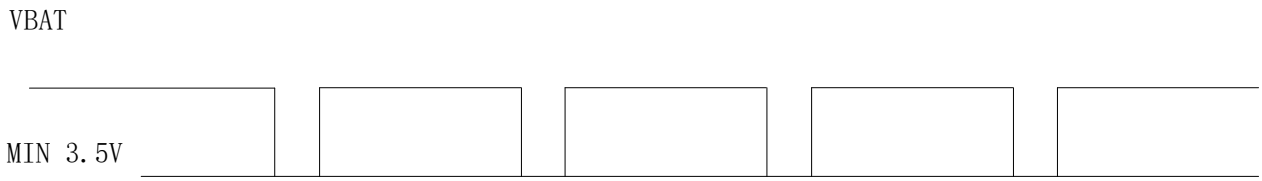


Figure 7 VBAT lowest voltage drop

4.1.2. Power PCB layout

Power traces must consider not only VBAT, but also the return GND of the power supply. The trace of the VBAT positive must be short and thick, the trace must first pass through the large capacitor, Zener diode and then the power PIN of the module. There are multiple PAD exposed copper at the bottom of the module. Make sure that the GND path of these exposed copper areas to the power supply is the shortest and smoothest. This ensures that the current path of the entire power supply is the shortest and the interference is minimal.

4.2. Power on and off

Do not turn on the module when the module's temperature and voltage limits are exceeded. In extreme cases, such operations can cause permanent damage to the module.

4.2.1. Turn on

The user can power on the module by pulling the KYPD_PWR_N1 pin (142) low. The pull-down time is at least 3 seconds. This pin has been pulled up to 1.8V in the module. The recommended circuit is as follows; or the CBL_PWR_N pin (203) is pulled low. CBL_PWR_N can be powered on by 10K pull-down resistor to GND. It does not need to release this signal after booting.

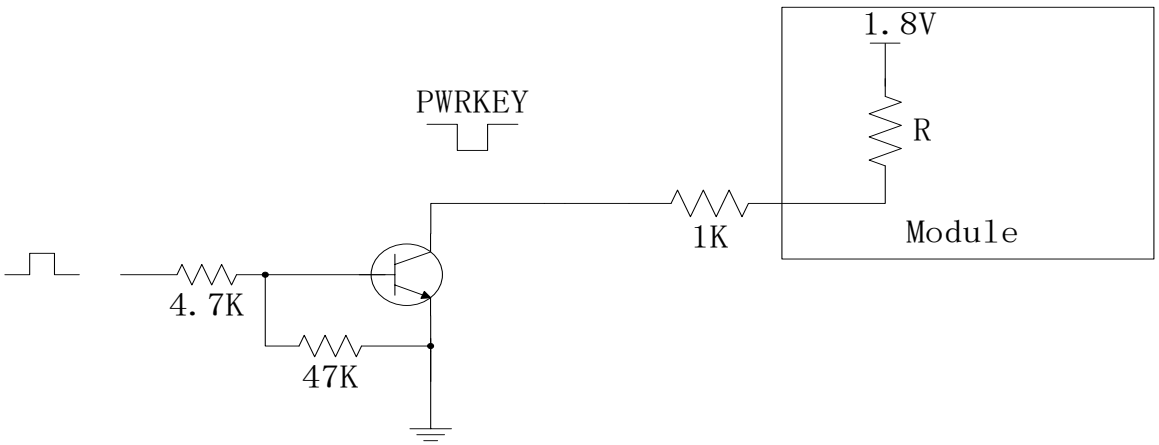


Figure 8 Using PWRKEY to turn on the module

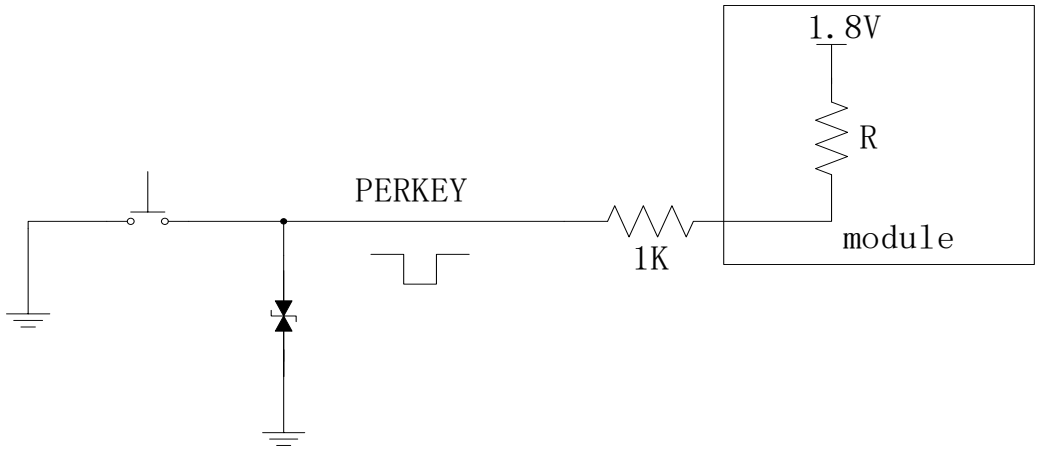


Figure 1 Booting with the button circuit

The following figure is the boot timing:

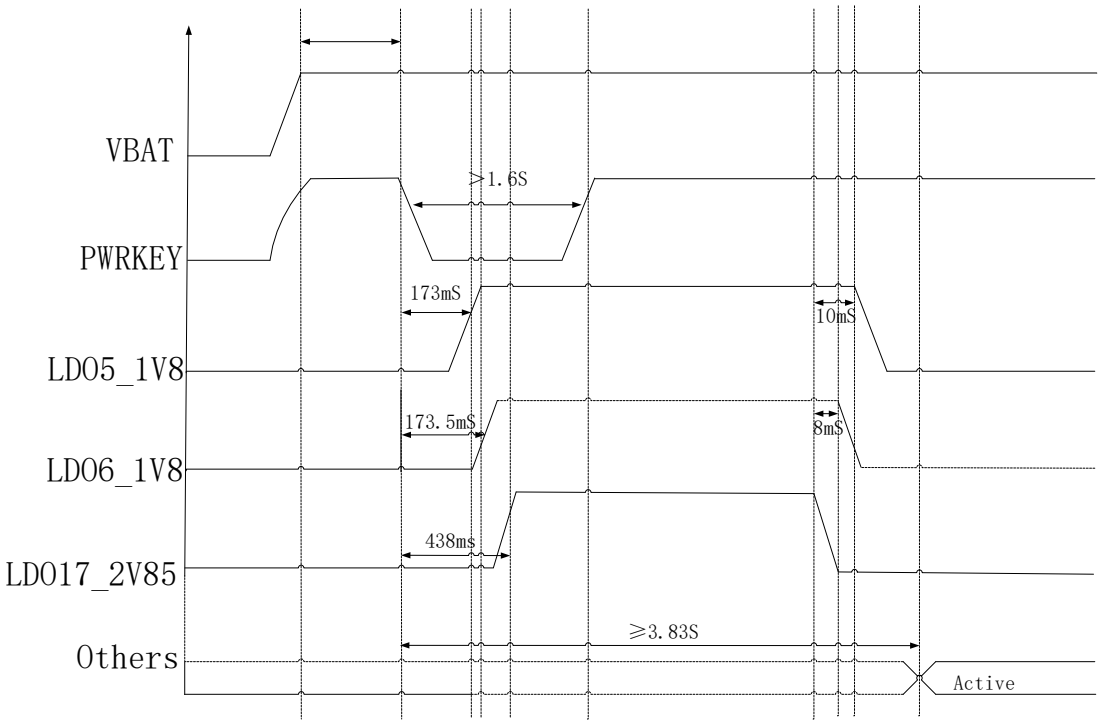


Figure 10 Using PWRKEY boot timing diagram

4.2.2. Turn off

Users can use the PWRKEY pin to turn off the module.

4.2.2.1.Turn off the module by PWRKEY

The user can turn off the PWRKEY signal by pulling it down for at least 3 seconds. The shutdown circuit can refer to the design of the boot circuit. After the module detects the shutdown action, a prompt window pops up on the screen to confirm whether to perform the shutdown action.

The user can achieve a forced reset by pulling PWRKEY down for a long time, pulling down for at least 15 seconds.

4.2.3. Module Reset

The SNM758 module supports a reset function that allows the user to quickly restart the module by pulling the RESET pin of the module low. The recommended circuit is as follows:

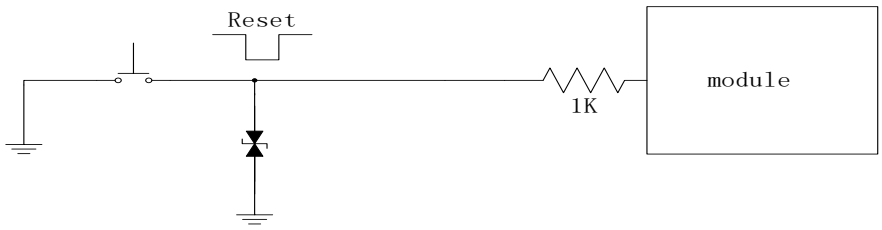


Figure 11 Reset using the key circuit

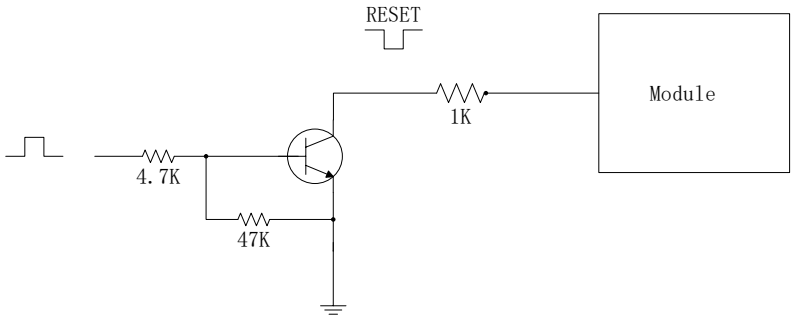


Figure 12 Reset Module Using External Signal

When the pin is high, the voltage is typically 1.8V. Therefore, for users with a level of 3V or 3.3V, it is not possible to directly use the GPIO of the MCU to drive the pin. An isolation circuit is required. The hardware parameters of the RESET can refer to the following table:

Table 3 RESET Hardware Parameters

		Pin	Description	Maximum	Unit
RESET	Input high level	1	-	-	V
	Input low level	-	-	0.65	V
	Pull down effective time	12		-	s

4.3. VCOIN Power

When VBAT is disconnected, user needs to save the real-time clock. The VCOIN pin cannot be left floating. It should be connected to a large capacitor or battery. When external capacitor is connected, the recommended value is 100uF, and the real-time clock can be kept for 1 minute. The reference

design circuit is used when the RTC power supply uses an external large capacitor or battery to power the RTC inside the module:

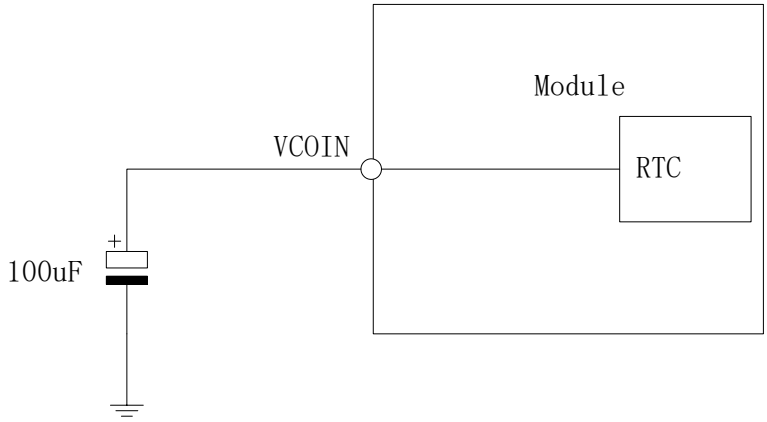


Figure 13 External Capacitor Powering the RTC

Rechargeable battery powered:

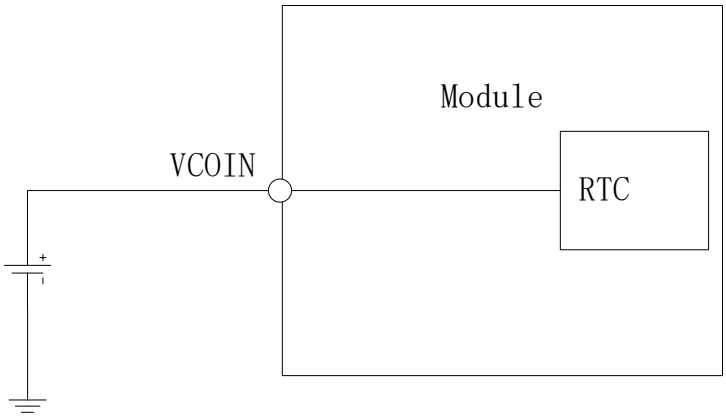


Figure 14 Rechargeable Battery Powers RTC

The input voltage range of this VCOIN power supply is 2.5-3.1V, and the typical value is 3.0V, and consumes approximately 3uA when VBAT is disconnected.

4.4. Power Output

The SNM758 has multiple power outputs. For LCD, Camera, touch panel, etc. In application, it is recommended to add parallel 33PF and 10PF capacitors to each power supply to effectively remove high frequency interference.

Table 4 Power Description

Signal	Default Voltage(V)	Drive Current(mA)
VREG_L2_1P1	1.1	1000
VREG_L5_1P8	1.80	300

VREG_L6_1P8	1.80	100
VREG_L11_SDC	2.95	600
VREG_L12_SDC	1.8	100
VREG_L14_UIM1	1.8/3.3	50
VREG_L15_UIM2	1.8/3.3	50
VREG_L10_2P8_SENSOR	2.8	100
VREG_L17_2P85	2.85	400
VREG_L22_2P8_AVDD	2.8	150
VREG_L23_1P175	1.175	150

4.5. Serial Port

The SNM758 provides four serial ports for communication. And corresponding to three groups of I2C interfaces can be multiplexed into hardware flow control, note that the I2C interface can not be added to the UART_RTS/CTS when the pull resistor can be added.

Table 5 UART Pin Description

Name	Pin	Direction	Function
UART2_MSM_TX	11	DI	UART2 Data Transmission
UART2_MSM_RX	12	DO	UART2 Data Reception
GPIO6_I2C2_SDA	13	DI	UART2 Clear To Send（CTS）
GPIO7_I2C2_SCL	14	DO	UART2 Request To Send（RTS）
GPIO12_UART4_TX	15	DI	UART4 Data Transmission
GPIO13_UART4_RX	16	DO	UART4 Data Reception
GPIO14_SENSOR_I2C4_SDA	17	DI	UART4 Clear To Send（CTS）
GPIO15_SENSOR_I2C4_SCL	18	DO	UART4 Request To Send（RTS）
GPIO16_UART5_TX	256	DI	UART5 Data Transmission

GPIO17_UART5_RX	255	DO	UART5 Data Reception
GPIO18_NFC_I2C5_SDA	254	DI	UART5 Clear To Send（CTS）
GPIO19_NFC_I2C5_SCL	253	DO	UART5 Request To Send（RTS）
GPIO20_UART6_TX	176	DO	UART6 Data Transmission
GPIO21_UART6_RX	177	DI	UART6 Data Reception
GPIO22_I2C6_SDA	184	DI	UART6 Clear To Send（CTS）
GPIO23_I2C6_SCL	185	DO	UART6 Request To Send（RTS）

Please refer to the following connection method:

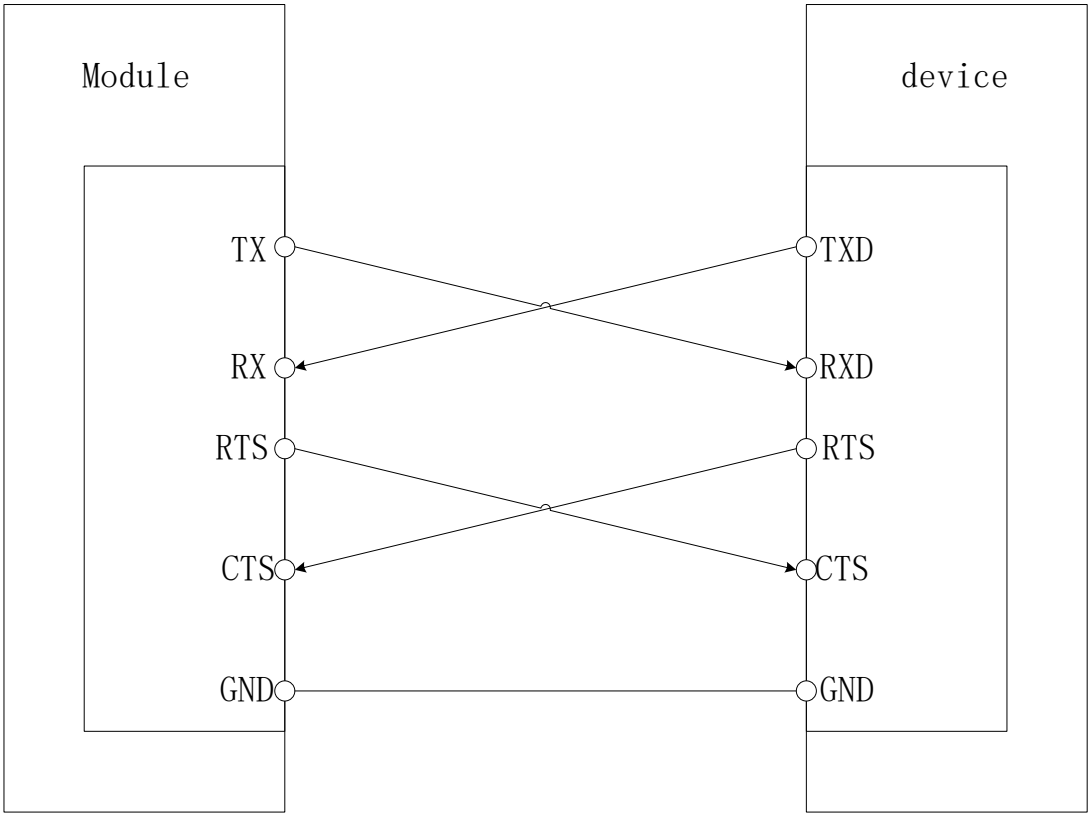


Figure 15 Serial Port Connection Diagram

When the serial level used by the user does not match the module, in addition to adding the level shifting IC, the following figure can also be used to achieve level matching. Only the matching circuits on TX and RX are listed here. Other low speed signals can refer to this two circuits.

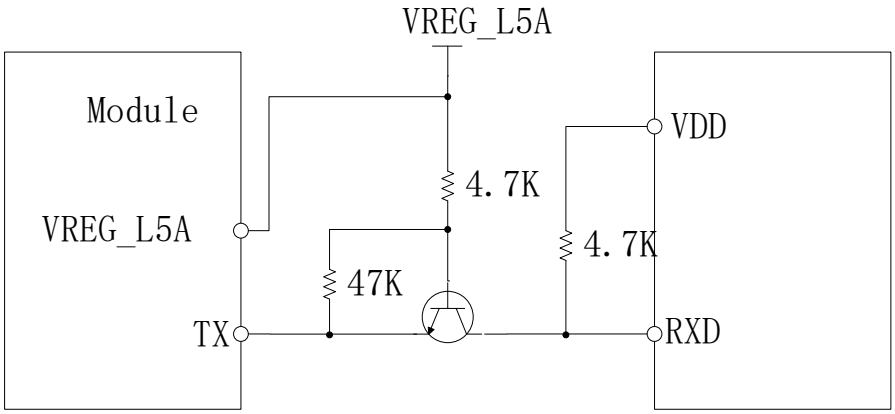


Figure 16 TX Connection Diagram

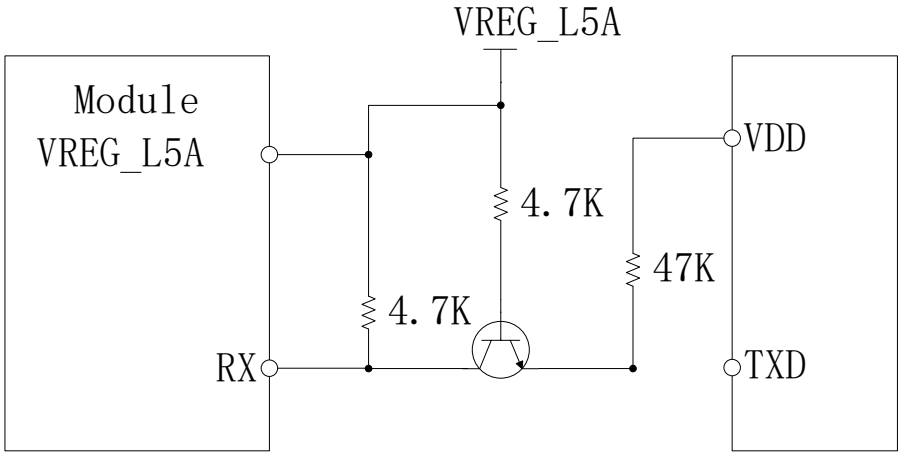


Figure 17 RX Connection Diagram

Note： When using Levels Isolation in Figures 17 and 18, it is necessary to use VREG_L5_1P8 as the pull-up power supply. VREG_L6_1P8 will enter the low power mode during sleep. It is not recommend-ed.

Table 6 Serial Port Hardware Parameters

Description	Minimum	Maximum	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Input low level	-	0.45	V
Input high level	1.35	-	V

Note：

1. The serial port of the module is a CMOS interface, and the RS232 signal cannot be directly connected. If necessary, please use the RS232 conversion chip.
2. If the 1.8V output of the module cannot meet the high level range of the user terminal, please add a level shifting circuit.

4.6. MIPI Interface

The SNM758 supports the Mobile Industry Processor Interface (MIPI) interface for Camera and LCD. The module supports FULL HD (1920*1200) display. The MIPI interface Main Camera supports up to 13MP, and the Front Camera supports 8MP.

4.6.1. LCD Interface

The SNM758 module supports the MIPI interface of two LCD displays, supports dual-screen display, and has a compatible screen identification signal. The resolution of the screen can be up to 1920*1200. The signal interface is shown in the following table. In the Layout, the MIPI signal line should strictly control the differential 85+/-15 ohm impedance and the equal length between the signal line group and the group.

The module's MIPI interface is a 1.2V power domain. When the user needs a compatible screen design, the module's LCD_ID pin or ADC pin can be used. At the same time, the module can provide 2.8V power to the LCD. The LCD interface is as follows:

Table 7 Primary and secondary screen interface definition

Home Screen Interface		
MIPI_DSI0_CLK_N	64	MIPI_LCD clock line
MIPI_DSI0_CLK_P	65	
MIPI_DSI0_LANE0_N	189	MIPI_LCD data line
MIPI_DSI0_LANE0_P	190	
MIPI_DSI0_LANE1_N	66	
MIPI_DSI0_LANE1_P	67	
MIPI_DSI0_LANE3_N	73	
MIPI_DSI0_LANE3_P	74	
MIPI_DSI0_LANE2_N	71	
MIPI_DSI0_LANE2_P	72	

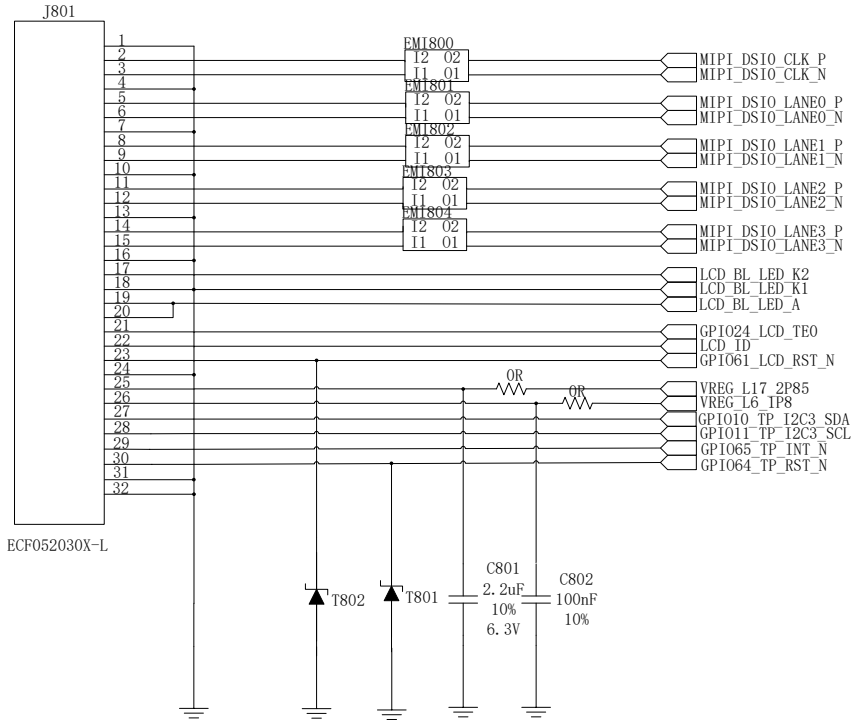
GPIO61_LCD_RST_N	75	LCD reset pin
GPIO24_LCD_TE0	76	LCD frame sync signal
LCD_BL_LED_K1	5	LCD series backlight negative pole 1（Only SNM758C has backlight, other models must be NC）
LCD_BL_LED_K2	6	LCD series backlight negative pole 2（Only SNM758C has backlight, other models must be NC）
LCD_BL_LED_A	7	LCD series backlight negative pole（Only SNM758C has backlight, other models must be NC）
VREG_L6_1P8	139	1.8V power supply
VREG_L17_2P85	137	2.8V power supply

Secondary Screen Interface		
MIPI_DSI1_CLK_N	242	MIPI_LCD2 clock line
MIPI_DSI1_CLK_P	241	
MIPI_DSI1_LANE0_N	226	MIPI_LCD2 data line
MIPI_DSI1_LANE0_P	225	
MIPI_DSI1_LANE1_N	240	
MIPI_DSI1_LANE1_P	239	
MIPI_DSI1_LANE2_N	244	

MIPI_DSI1_LANE2_P	243	
MIPI_DSI1_LANE3_N	246	
MIPI_DSI1_LANE3_P	245	
GPIO63_LCD2_RST_N	99	LCD2 reset pin
GPIO25_LCD_TE1	77	LCD2 frame sync signal
PM8953_MPP2	112	LCD2 frame sync signal
VREG_L6_1P8	139	1.8V power supply
VREG_L17_2P85	137	2.8V power supply

LCD_ID of the module, this pin is internally GPIO. When used as LCD_ID, please confirm the internal circuit of LCD. If the internal divider of the LCD uses resistor divider, please pay attention to the voltage to meet the high or low range of GPIO.

MIPI is a high-speed signal line. To avoid EMI interference, it is recommended to place a common-mode inductor near the LCD side.



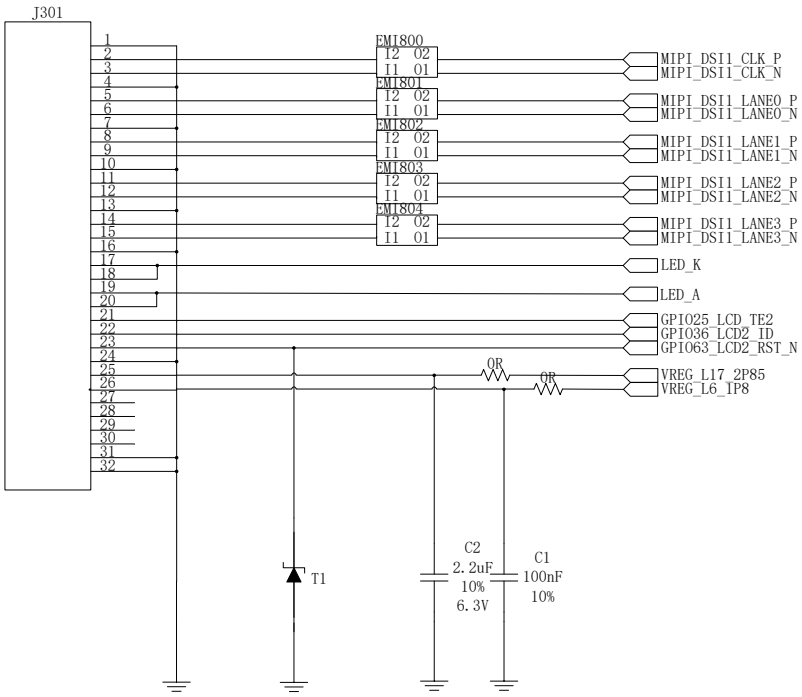


Figure 18 Main LCD and sub LCD interface circuit

Both the primary and secondary LCDs require a backlight circuit. The backlight driving circuit of the ma-in LCD is driven inside the SNM758C module. It can directly use LCD_BL_LED_A, LCD_BL_LED_K1, LCD_BL_LED_K2 to support up to 2 strings of 8 LEDs in total. The SNM758W & SNM758S backlight driving circuit of the main LCD and secondary LCD can refer to Figure 20. Adjusting the brightness of the backlight can be realized by PM8953_MPP2 of the module. The modulation method is PWM mode.

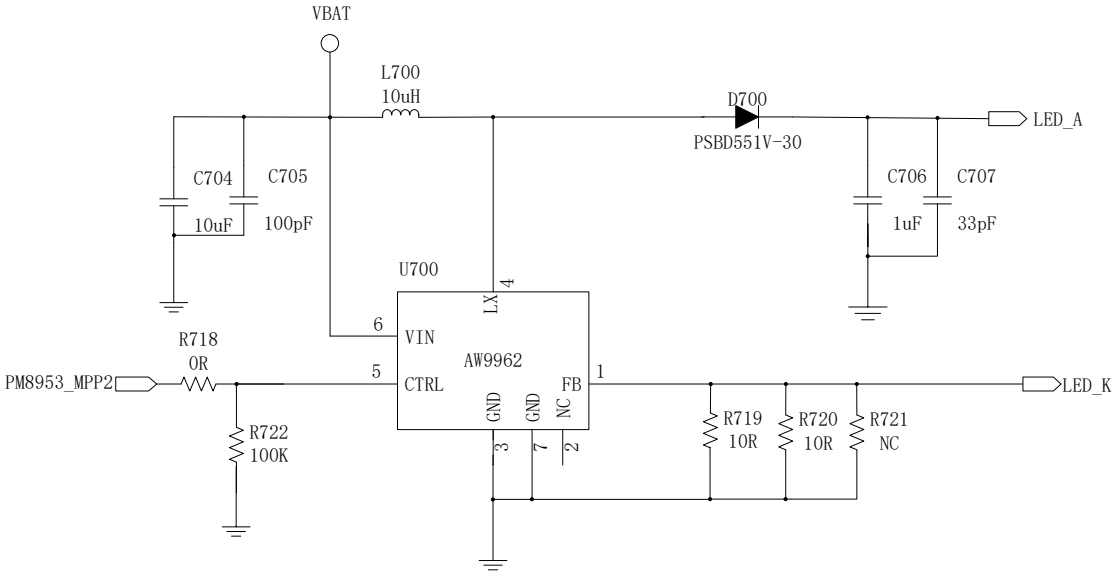


Figure 19 Backlight drive schematic

Note: The backlight circuit should select the chip according to the backlight circuit of the LCD. Users should carefully read the LCD document and select the correct driver chip. The reference circuit provided in this document is a series-type PWM dimming backlight driver circuit; if it is a series-type one-line dimming backlight driver circuit, it needs to be controlled by GPIO.

4.6.2. MIPI Camera Interface

The SNM758 module supports the MIPI interface Camera and provides a dedicated camera power supply. The main camera is a CSI0 interface that supports four sets of data lines and can support up to 13M pixels. The front camera is a CSI2 interface that supports four sets of data lines and can support 8M pixels. There is also a set of CSI1 interface, which can do dual 13M dual camera design with the main camera, or as a dual camera design for the depth of field camera; it can also be used as the MIPI interface scan head design. The module provides the power required by the Camera, including AVDD-2.8V, IOVDD-1.8V\AFVDD-2.8V (powered by the focus motor) and D-VDD1.2V (CAM core voltage).

Table 8 MIPI Camera Interface Definition

Main Camera Interface			
Name	**Pin**	**Input/output**	**Description**
MIPI_CSI0_CLK_N	50	AI	CSI0 camera MIPI clock signal
MIPI_CSI0_CLK_P	49	AI	
MIPI_CSI0_LANE0_N	56	AI	CSI0 camera MIPI data signal
MIPI_CSI0_LANE0_P	55	AI	
MIPI_CSI0_LANE1_N	194	AI	
MIPI_CSI0_LANE1_P	193	AI	
MIPI_CSI0_LANE2_N	52	AI	
MIPI_CSI0_LANE2_P	51	AI	
MIPI_CSI0_LANE3_N	54	AI	
MIPI_CSI0_LANE3_P	53	AI	
GPIO26_MCAM_MCLK	84	DO	CSI0 camera clock signal
GPIO40_MCAM_RST_N	85	DO	CSI0 camera reset signal
GPIO39_MCAM_PWD_N	86	DO	CSI0 camera sleep signal
CAM_I2C_SDA0	105	DO	I2C data
CAM_I2C_SCL0	104	DO	I2C clock
VREG_L6_1P8	139	PO	1.8V IOVDD
VREG_L17_2P85	137	PO	2.8V AFVDD（Focus motor power supply）

VREG_L22_2P8	136	PO	2.8V AVDD
VREG_L2_1P1	199	PO	1.1V DVDD

Front Camera Interface			
Name	**Pin**	**Input/output**	**Description**
MIPI_CSI2_CLK_P	40	AI	CSI2 camera MIPI clock signal
MIPI_CSI2_CLK_N	41	AI	
MIPI_CSI2_LANE0_P	42	AI	CSI2 camera MIPI data signal
MIPI_CSI2_LANE0_N	43	AI	
MIPI_CSI2_LANE1_P	191	AI	
MIPI_CSI2_LANE1_N	192	AI	
MIPI_CSI2_LANE2_P	46	AI	
MIPI_CSI2_LANE2_N	47	AI	
MIPI_CSI2_LANE3_P	44	AI	
MIPI_CSI2_LANE3_N	45	AI	
GPIO27_SCAM_MCLK	80	DO	CSI2 camera clock signal
GPIO129_SCAM_RST_N	79	DO	CSI2 camera reset signal
GPIO130_SCAM_PWDN	78	DO	CSI2 camera sleep signal
CAM_I2C_SDA1	96	DO	I2C data
CAM_I2C_SCL1	95	DO	I2C clock
VREG_L6_1P8	139	PO	1.8V IOVDD
VREG_L17_2P85	137	PO	2.8V AFVDD（Focus motor power supply）
VREG_L22_2P8	136	PO	2.8V AVDD
VREG_L23_1P175	200	PO	1.175V DVDD

Depth Camera Interface			
Name	**Pin**	**Input/output**	**Description**
MIPI_CSI1_CLK_N	207	AI	CSI1 MIPI clock signal
MIPI_CSI1_CLK_P	208	AI	
MIPI_CSI1_LANE0_N	63	AI	CSI1 MIPI data signal
MIPI_CSI1_LANE0_P	62	AI	
MIPI_CSI1_LANE1_N	59	AI	
MIPI_CSI1_LANE1_P	58	AI	
MIPI_CSI1_LANE2_N	172	I/O	
MIPI_CSI1_LANE2_P	171	I/O	
MIPI_CSI1_LANE3_N	61	AI	
MIPI_CSI1_LANE3_P	60	AI	
GPIO28_CAM_MCLK2	264	DO	CSI1 clock signal
GPIO131_DCAM_RST_N	263	DO	CSI1 reset signal
GPIO132_DCAM_PWD_N	262	DO	CSI1 sleep signal
CAM_I2C_SDA1	96	DO	I2C date
CAM_I2C_SCL1	95	DO	I2C clock
VREG_L6_1P8	139	PO	1.8V IOVDD
VREG_L17_2P85	137	PO	2.8V AFVDD（Focus motor power supply）
VREG_L22_2P8	136	PO	2.8V AVDD
VREG_L2_1P1	199	PO	1.1V DVDD

If the user designs to use the CAMERA module with autofocus function, please note that the I2C of the module cannot be directly connected to the AF device. The I2C of the AF device should be connected to the driver chip of CAMERA, and the correct connection is as follows:

The MIPI interface has a high rate. The user should control the impedance by 85±15 ohms during the routing. Please pay attention to the length of the trace. It is not recommended to add a small capacitor on the MIPI signal line. This may affect the rising edge of the MIPI data. This in turn causes the MIPI data to be invalid.

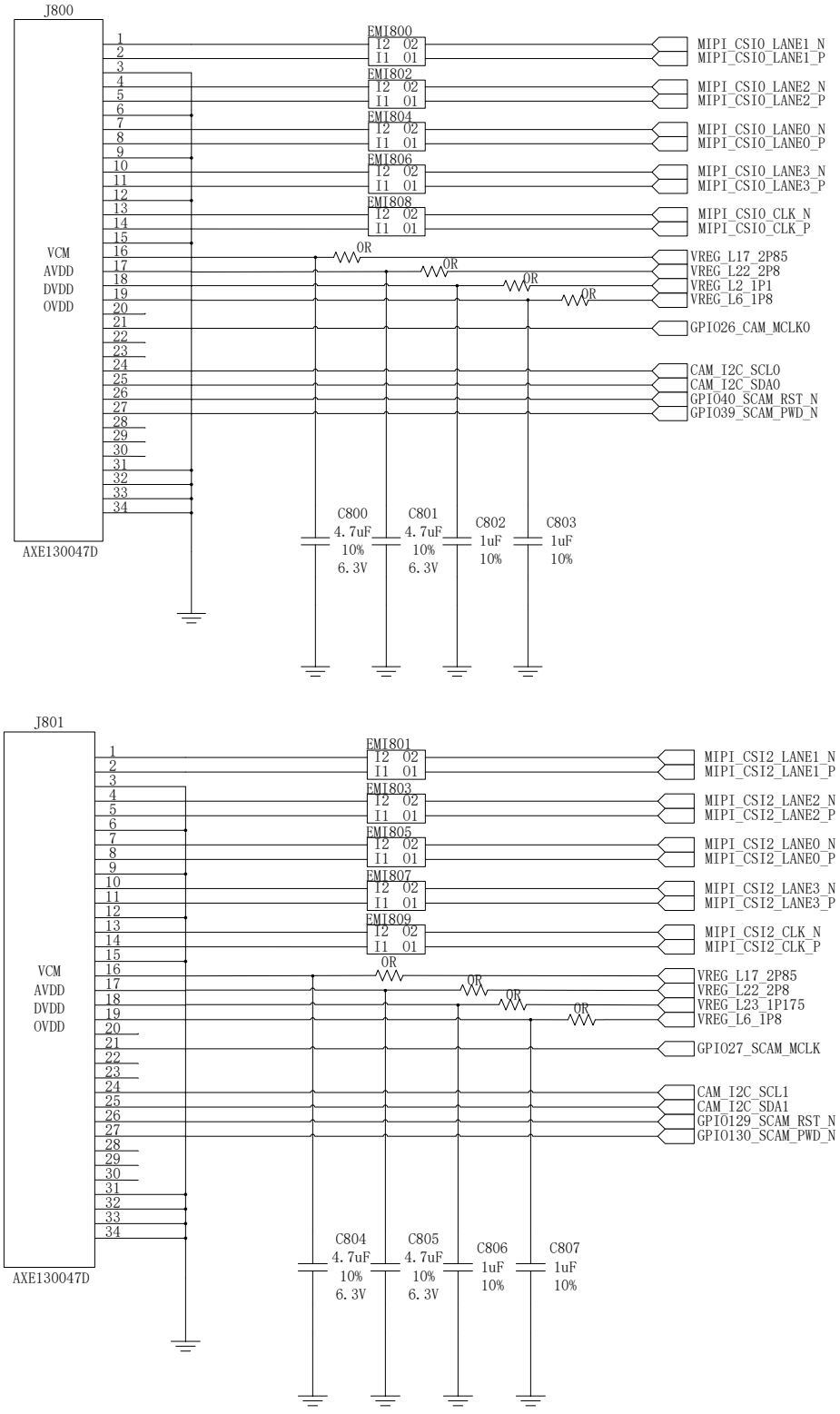


Figure 20 MIPI Camera Reference Circuit

4.6.3. MIPI PCB layout

MIPI is a high-speed signal line. In the Layout stage, please follow the impedance and length requirements strictly, and control the length of the differential pair within the group and the group length. The total length should be as short as possible. Users must pay attention to protection during the layout stage, so that they can be away from the signal lines that are easily interfered. The GND processing must be performed on the upper and lower sides, and the traces are differential pairs. 85+/-15ohm

differential impedance matching is performed. Ensure impedance consistency and do not bridge different GND planes as much as possible.

The MIPI interface selects a small-capacity TVS when selecting an ESD device. It is recommended that the parasitic capacitance be less than 1pF.

The MIPI routing requirements are as follows:

The total length of the cable does not exceed 150mm.

It is required to control 100 ohm differential impedance with an error of ±10%.

The error of the differential line length within the group is controlled within 0.7mm.

The length error between groups is controlled within 1.4mm.

4.7. Capacitive Touch Interface

The module provides a set of I2C interfaces that can be used to connect capacitive touches while providing the required power and interrupt pins. The default interface pins for capacitive touch software are defined as follows:

Table 9 Capacitive Touch Interface Definitions

Name	Pin	Input/Output	Description
GPIO10_TP_I2C3_SDA	234	DO	The capacitive touch I2C interface needs to be pulled up toVREG_L5_1P8
GPIO11_TP_I2C3_SCL	233	DO	
GPIO65_TP_INT_N	97	DI	Interrupt
GPIO64_TP_RST_N	98	DO	Reset
VREG_L5_1P8	140	PO	1.8V Power supply
VREG_L10_2P8_SENSOR	138	PO	2.8V Power supply

Note: The interface definition of the capacitive touch can be adjusted by software, and the user can change the GPIO and I2C according to the design needs.

4.8. Audio Interface

The GSM antenna is the main source of coupling interference for TDD, so users should pay attention to keeping the audio trace away from the GSM antenna and VBAT during PCB layout and routing. The filter capacitor of the audio is preferably placed close to the module end and placed next to

the interface end. The audio output should be routed according to the differential signal rules.The conducted interference is mainly caused by the voltage drop of VBAT. If the Audio PA is directly powered by VBAT, it is easier to hear the “zizi” sound at the SPK output. Therefore, it is better to connect in parallel with the input of the Audio PA in the schematic design, some large capacitance capacitors and series magnetic beads.The conducted interference is also strongly related to TDD and GND. If GND is not handled well, many high-frequency interference signals will interfere with MIC and Speaker through devices such as bypass capacitors, so users should ensure good performance of GND during PCB design.

The module provides three analog audio inputs, MIC_IN1_P/M for the main microphone, MIC_IN2_P for the microphone, and MIC_IN3_P for the noise reduction microphone. The module also provides three analog audio outputs (HPH_L/R, REC_P/N, SPK_P/N). The audio pin is defined as follows:

Table 10 Audio Pin Definitions

Name	Pin	Input/Output	Description
MIC_IN1_M	123	AI	Main MIC negative, grounded at MIC
MIC_IN1_P	122	AI	Main MIC positive
MIC_IN2_P	132	AI	Headphone MIC positive
GND_MIC	124	GND	Headphone MIC, noise reduction MIC negative
MIC_IN3_P	131	AI	Noise reduction MIC positive
MIC_BIAS1	118	AO	BIAS voltage of the main MIC for silicon wheat
MIC_BIAS2	117	AO	BIAS voltage of the headphone MIC for silicon wheat design
CDC_HPH_R	128	AO	Headphone right channel
CDC_HPH_L	126	AO	Headphone left channel
CDC_HS_DET	125	AI	Headphone plug detection
CDC_HPH_REF	127	AI	Headphone reference ground
CDC_EAR_M	129	AO	Earpiece output negative
CDC_EAR_P	130	AO	Earpiece output positive
SPKR_DRV_M	133	AO	Amplifier (0.85W) output negative
SPKR_DRV_P	134	AO	Amplifier (0.85W) output positive

Users are advised to use the following circuit according to the actual application to get better sound

effects.

4.8.1. Earpiece Interface Circuit

The Earpiece interface circuit places the following devices near the REC end, and B302 and B303 can be changed to magnetic beads according to actual effects.

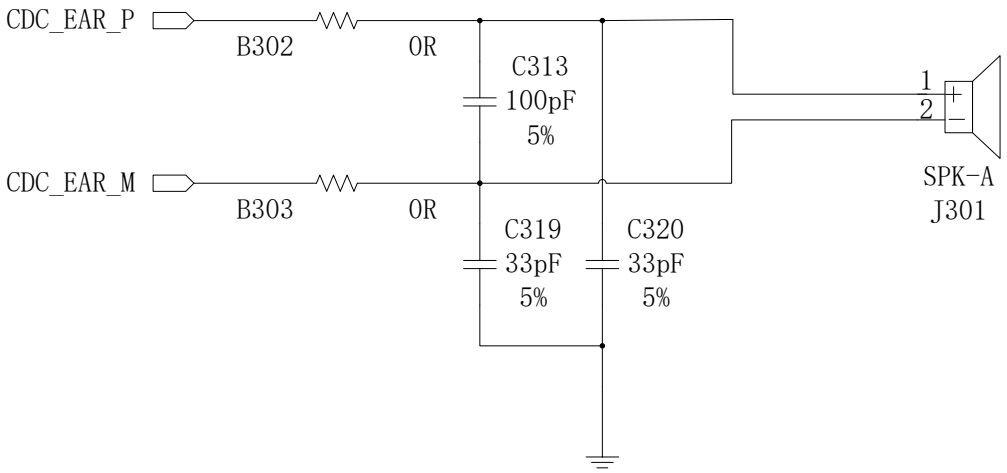


Figure 21 Earpiece Interface Circuit

4.8.2. Microphone Receiving Circuit

On the right is the MEMS microphone interface circuit, which has more BIAS power than the electret MIC. The negative signal of the main MIC must be designed from 0R to ground resistance near the MIC. As shown in Figure R301.

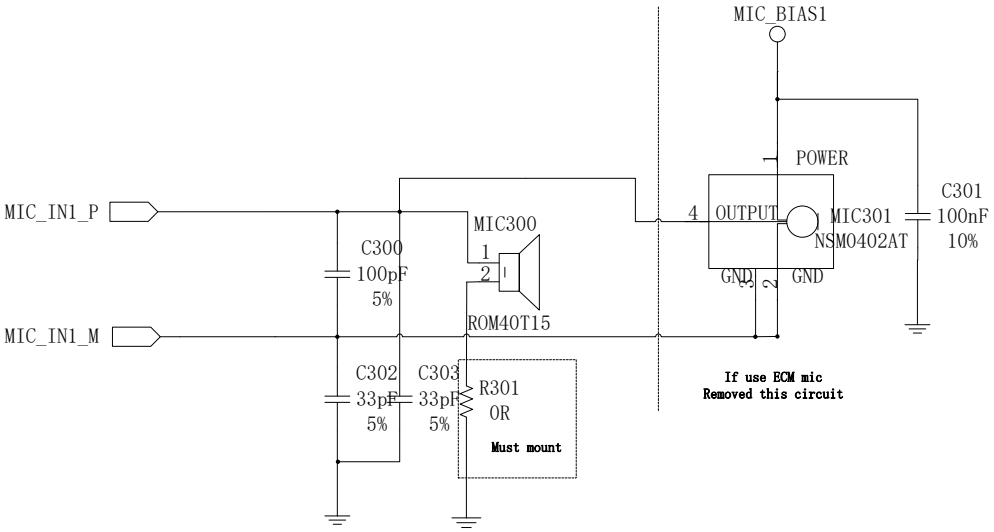


Figure 22 Microphone Differential Interface Circuit

4.8.3. Headphone Interface Circuit

The module integrates a stereo headphone jack. Users are advised to reserve ESD devices during the design phase to prevent ESD damage. The HS_DET pin of the module can be set as an interrupt. In software, this pin is the earphone interrupt by default. The user can use this pin to detect the plugging and unplugging of the earphone.

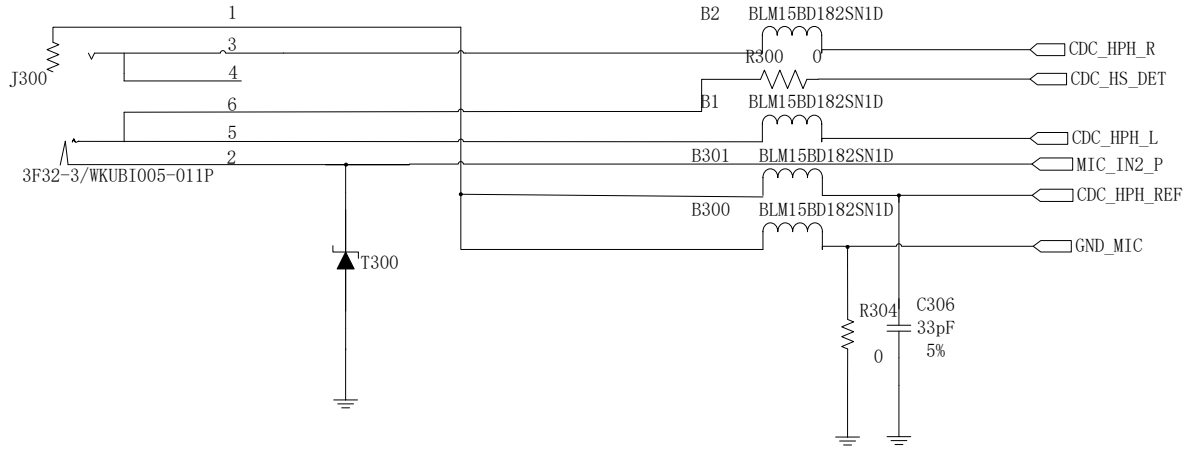


Figure 23 Headphone Interface Circuit

Note:

1. The earphone holder in Figure 24 is normally closed. If the user is using the normally open mode earphone holder, please modify the detection circuit according to the actual pin and modify the software accordingly.
2. We recommend that the headphone detection pin HS_DET and HPH_L form a detection circuit (the connection method in the above figure), because HPH_L has a pull-down resistor inside the chip, which can ensure that HS_DET is low when connected with HPH_L, if the user will HS_DET and HPH_R To connect, please reserve a 1K pull-down resistor on HPH_R.
3. The standard of the headphone interface is the European standard OMPT. If you need to design the American standard CTIA interface, you need to swap the GND and MIC signals for the network. If you want to be compatible with both headset standards, you need an external dedicated chip, such as the TI-TS3A226AE.

4.8.4. Speaker Interface Circuit

The module integrates a Class-D audio amplifier with an output power of 0.85W and an output signal of SPKR_OUT_P / SPKR_OUT_M.

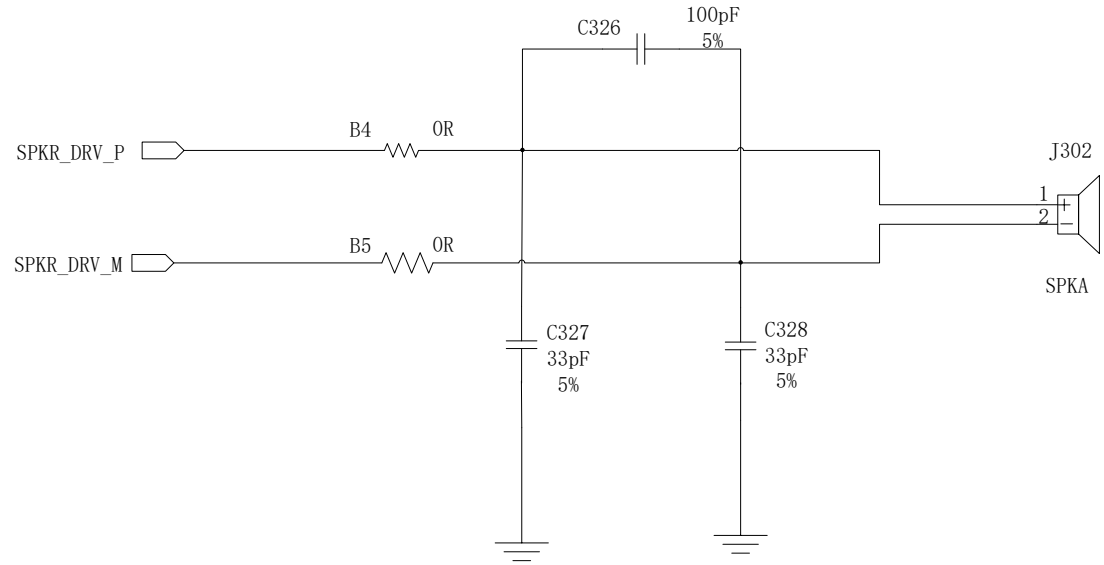


Figure 24 Recommended circuit with internal audio amplifier

It is also possible to add an audio amplifier externally, using CDC_HPH_R as a single-ended input signal, and the reference circuit is shown below.

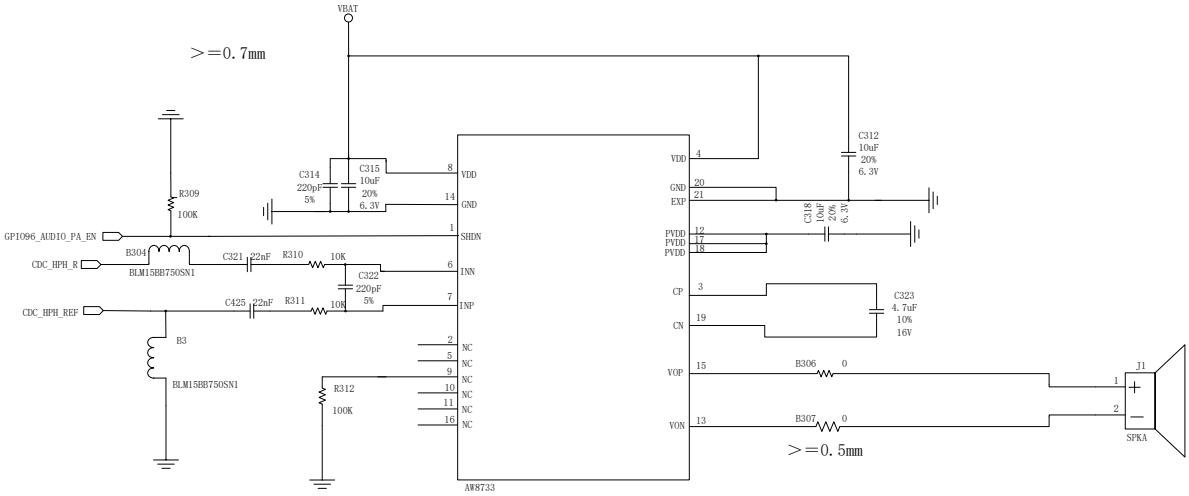


Figure 25 Recommended circuit with external audio amplifier

4.8.5. LINE OUT Interface Circuit

The output of the LINEOUT interface adopts differential output, which requires an external audio power amplifier driver.

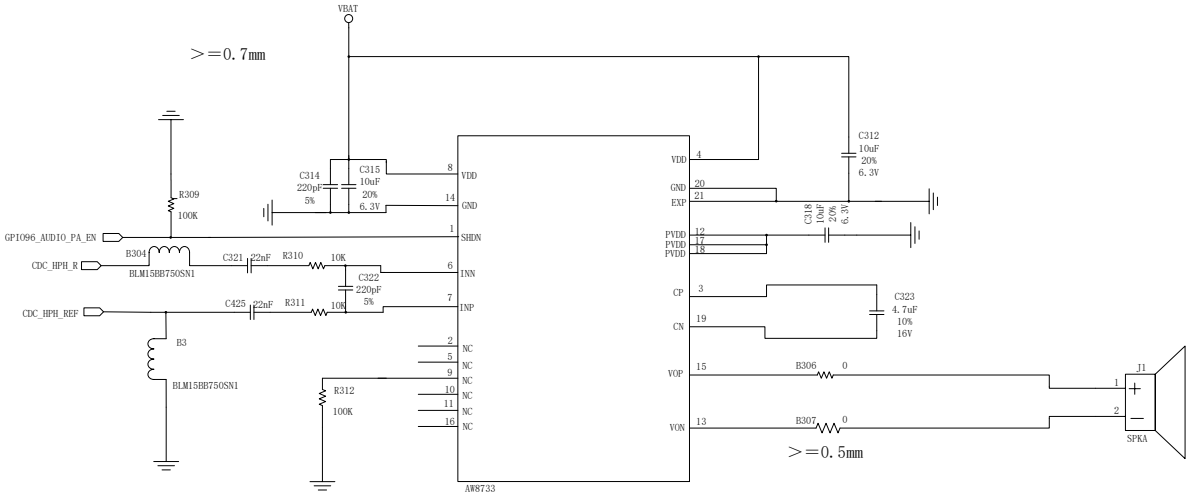


Figure 26 LINEOUT circuit with external audio amplifier

4.8.6. AUDIO PCB Layout

Analog signals are susceptible to interference from high-speed digital signals. So please stay away from high-speed digital signal lines. The module supports the GSM standard, and the GSM signal can interfere with the audio through coupling and conduction. Users can add 33pF and 10pF capacitors to the audio path to filter out coupling interference. The 33pF capacitor mainly filters out the interference in the GSM850/EGSM900 frequency band, and the 10pF capacitor mainly filters out the interference in the DCS1800 frequency band. The coupling interference of TDD has a lot to do with the user's PCB design. In some cases, the TDD in the GSM850/EGSM900 frequency band is more serious, and in some cases the TDD interference in the DCS1800 frequency band is serious. Therefore, users can select the required filter capacitors according to the actual test results, and sometimes even do not

need to paste filter capacitors. The GSM antenna is the main source of coupling interference for TDD, so users should pay attention to keeping the audio traces away from the GSM antenna and VBAT during PCB layout and routing. It is best to place a set of audio filter capacitors close to the module end, and another set close to the interface end. The audio output should be routed according to the differential signal rules. The conducted interference is mainly caused by the voltage drop of VBAT. If the Audio PA is directly powered by VBAT, it is easier to hear the "squeak" sound at the output end of the SPK. Therefore, it is best to connect the input end of the Audio PA in parallel in the schematic design. Some bulk capacitors and ferrite beads in series. TDD and GND are also closely related. If the GND is not handled properly, many high-frequency interference signals will interfere with the MIC and Speaker through bypass capacitors and other devices. Therefore, the user should ensure the good performance of the GND during the PCB design stage.

4.9. I2S Interface

There are two sets of GPIO-compatible I2S interfaces inside the module. The pins used by this function are as follows:

Table 2 I2S pin definition

Name	Pin	Input/Output	Description
GPIO88_MI2S1_D1	27	DI	I2S1 input DATA
GPIO93_MI2S_1_D0	265	DO	I2S1 output DATA
GPIO92_MI2S_1_WS	271	DO	I2S1_ WS
GPIO91_MI2S_1_SCK	169	DO	I2S1_ SLK
GPIO138_FP_SPI_MISO	266	DI	I2S2 input DATA
GPIO137_FP_SPI_MOSI	267	DO	I2S2 output DATA
GPIO136_FP_SPI_CS	268	DO	I2S2_WS
GPIO135_FP_SPI_CLK	269	DO	I2S2_SCK

4.9.1. AUDIO PCB layout

Analog signals are susceptible to interference from high speed digital signals. So stay away from high-speed digital signal lines. The module supports the GSM system, and the GSM signal can interfere with the audio by coupling and conduction. Users can add 33pF and 10pF capacitors to the audio path to filter out coupling interference. The 33pF capacitor mainly filters out the interference of the GSM850/EGSM900 band, and the 10pF capacitor mainly filters out the interference of the DCS1800 band. The coupling interference of TDD has a great relationship with the PCB design of the user. In some cases, the TDD of the GSM850/EGSM900 frequency band is more serious, and in some cases, the TDD interference of the DCS1800 frequency band is more serious. Therefore, the user can select

the required filter capacitor according to the actual test result, and sometimes even do not need to paste the filter capacitor.

4.10. USB Interface

The SNM758 supports a USB 2.0 /3.0High/Super speed interface. It must control the 90 ohm differential impedance during Layout and control the external trace length.

The module supports high-speed USB interface at a rate of 480Mbps. The user recommends adding a common-mode inductor during the schematic design phase to effectively suppress EMI interference. If you need to increase the static protection, please select a TVS tube with a parasitic capacitance of less than 1pF. Please refer to the following notes when planning Layout:

- The common mode inductor should be close to the side of the USB connector.
- Require control of 90 ohm differential impedance with an error of ±10%.
- The differential line length error is controlled within 6mm.
- If the USB has a charging function, please note that the VBUS cable is as wide as possible.
- If there is a test point, try to avoid the split line and put the test point on the path of the trace.

Table 12 Internal USB cable length of the module

Pin	Signal	Length (mm)	Length Error（P-N）
14	USB_DP	46.3	0.2mm
13	USB_DM	46.4	

The module supports OTG function at the same time and can output 5V/1A current.

The voltage input range during charging is as follows:

Table 13 Voltage input range during charging

Name	Description	Minimum	Typical	Maximum	Unit
VBUS	Input range	3.7	-	5.8	V

The USB plug-in detection of the module is realized by the VBUS and DP/DM data lines. When the USB cable is inserted, the VBUS voltage is detected first, and then the DM/DP pull-up state is detected to determine whether the USB data line or the charger is inserted or not. Therefore, if you need to use the USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is a high-speed mode. It is recommended to connect a common-mode inductor to the side of the USB connector to effectively suppress EMI interference. At the same time, the USB interface is an external interface. The DM/DP must add a TVS tube to prevent static damage caused by plugging and unplugging the data cable. When selecting the TVS, the user should pay attention to the load capacitance of less than 1pf. VBUS also needs to increase the TVS tube. If there is anti-surge demand,

it is also necessary to increase the anti-surge tube. The connection diagram is as follows:

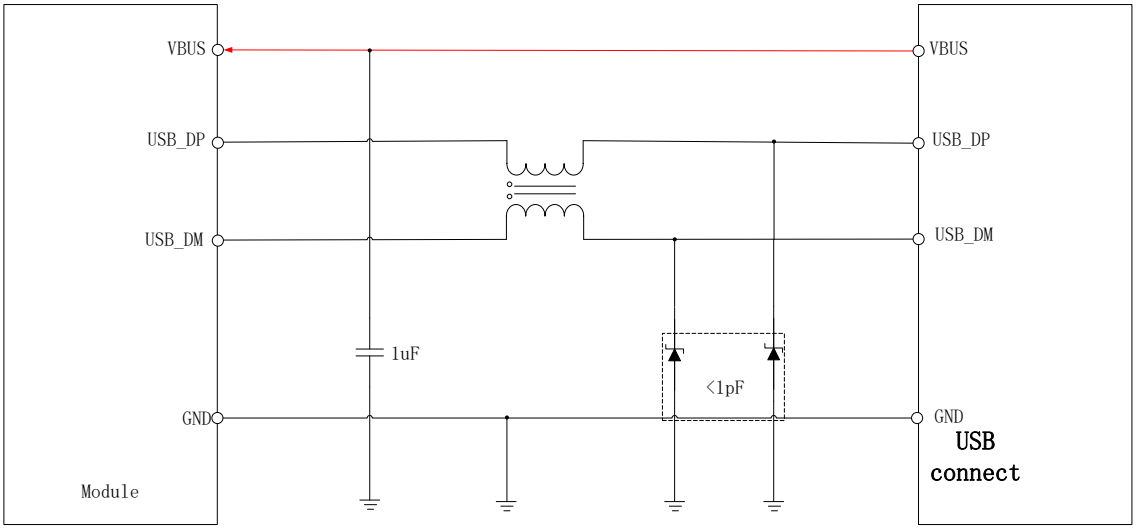


Figure 27 USB Connection Diagram

4.10.1. USB OTG

The SNM758 module can provide USB OTG function. The pins used in this function are as follows:

Table 3 USB OTG Pin Description

Pin Name	Pin	Description
VBUS	157、158、159	5V charging input / OTG output power.
USB_HS_D_M	145	USB Date-
USB_HS_D_P	146	USB Date+
USB_ID	143	USB ID

The recommended circuit diagram of USB OTG is as follows:

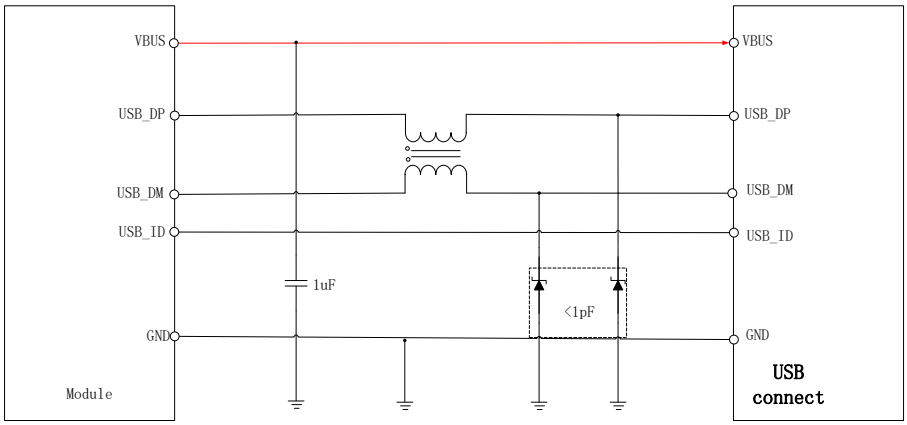


Figure 28 USB-OTG Connection Diagram

4.11. Charging Interface

The SNM758 module integrates a 2A charging solution. The charging related content of this manual is only described by the internal charging scheme. The MSM8953 platform uses the Qualcomm PMI8952 internal integrated charging chip by default. The chip is in switching mode and has high efficiency. It integrates a 15-bit battery voltage detection ADC and a 15-bit current detection ADC. The charging current can be up to 2A.

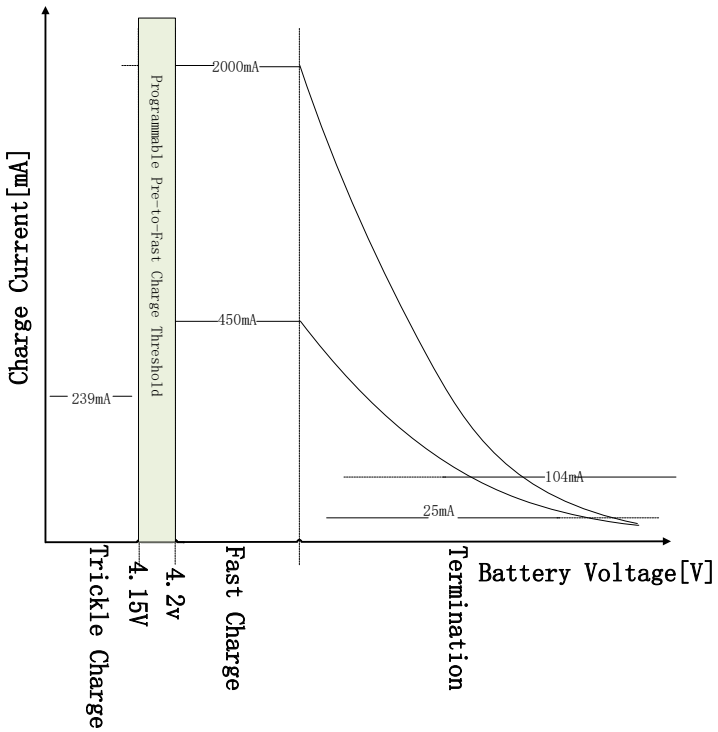


Figure 29 Charging diagram

4.11.1. Charging Detection

when the charger is plugged in, internal VBUS of the module will generate a hardware interrupt. The software determines whether the charger is inserted or the USB data cable is inserted by judging the status of USB_DP/USB_DM.

4.11.2. Charge Control

The SNM758 module can charge the over-discharged battery. The charging process includes trickle charge, pre-charge, constant current, and constant-voltage charge. When the VBAT voltage is lower than 2.8V, the module is pre-charged; when VBAT is between 3.5V and 4.2V, it is charged by the constant current plus constant voltage method optimized for the lithium battery. At present, the software's charge cut-off voltage is 4.2V, and the back-off voltage is 4.05V.

4.11.3. BAT_CON_TEM

The SNM758 module has battery temperature detection and can be implemented by BAT_THERM (149PIN). This requires the internal integration of a 10KΩ thermistor (negative temperature coefficient) inside the battery to connect the thermistor to the BAT_THERM pin. During the charging process, the software reads the voltage of the BAT_THERM pin to determine if the battery

temperature is too high. If the temperature is too high or too low, the battery will stop charging immediately to prevent battery damage. The battery charging connection diagram is shown below:

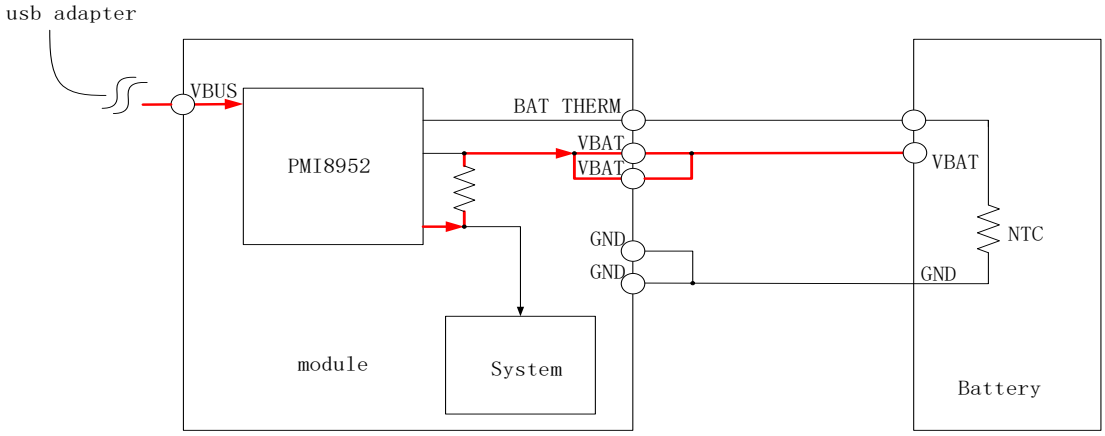


Figure 30 Charging circuit connection diagram

Please refer to the specific reference design for the charging circuit design. The 758S charging circuit is different.

4.12. UIM Card Interface

4.12.1. UIM Interface Circuit

The SNM758 can support two SIM cards at the same time to achieve dual card dual standby. Support SIM card hot swap, can automatically recognize 1.8V and 3.0V cards. The figure below is the SIM recommended interface circuit. In order to protect the SIM card, it is recommended to use TVS devices for electrostatic protection. The device of the peripheral circuit of the SIM card should be close to the SIM card holder.

The reference circuit is as follows:

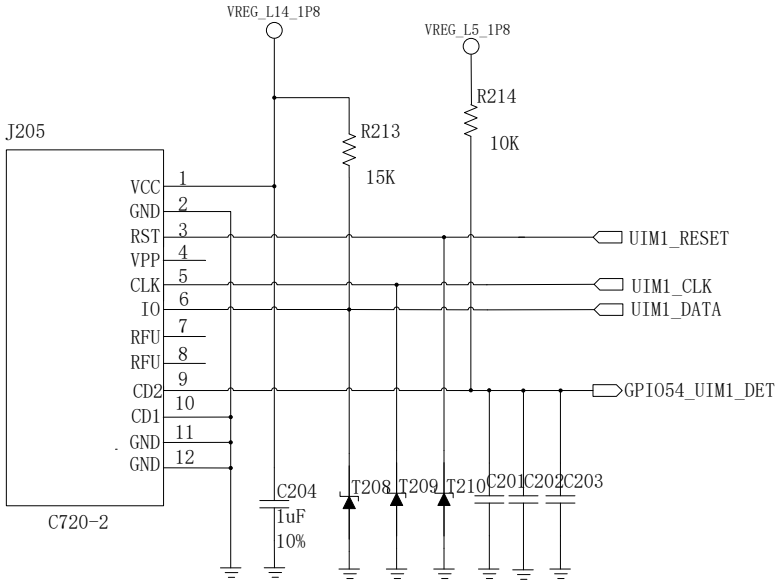


Figure 31 UIM card interface circuit

4.12.2. UIM PCB layout

The SIM card has a large area and does not have an anti-EMI interference device. It is relatively susceptible to interference. Therefore, in the layout, first ensure that the SIM card is away from the antenna and the antenna extension cable inside the product. Place it as close as possible to the module. The SIM_CLK signal is protected, and the SIM_DATA, SIM_RST, and SIM_VDD signals of the SIM card are away from the power source and away from the high-speed signal line. If the processing is not easy, it may cause problems such as not knowing the card or dropping the card. Therefore, please follow the following principles when designing:

- Keep the SIM card holder away from the GSM antenna during the PCB layout phase;
- SIM card routing should be as far away as possible from RF line, VBAT and high-speed signal lines, and the SIM card should not be too long;
- The GND of the SIM card holder should be in good communication with the GND of the module to make the GND equipotential between the two.
- To prevent SIM_CLK from interfering with other signals, it is recommended to protect SIM_CLK.
- It is recommended to place a 100nF capacitor on the SIM_VDD signal line which is near the SIM card holder;
- Place TVS near to the SIM card holder. The parasitic capacitance of the TVS should not exceed 50pF, and the 51Ω resistor in series with the module can enhance ESD protection.
- The SIM card signal line increases the capacitance of 22pF to ground to prevent radio frequency interference.
- The return path of VBAT has a large current, so the SIM card trace should avoid the return path of VBAT as much as possible.

4.13. SD Card Interface

SNM758 supports SD card interface and supports up to 256GB.

The reference circuit is as follows:

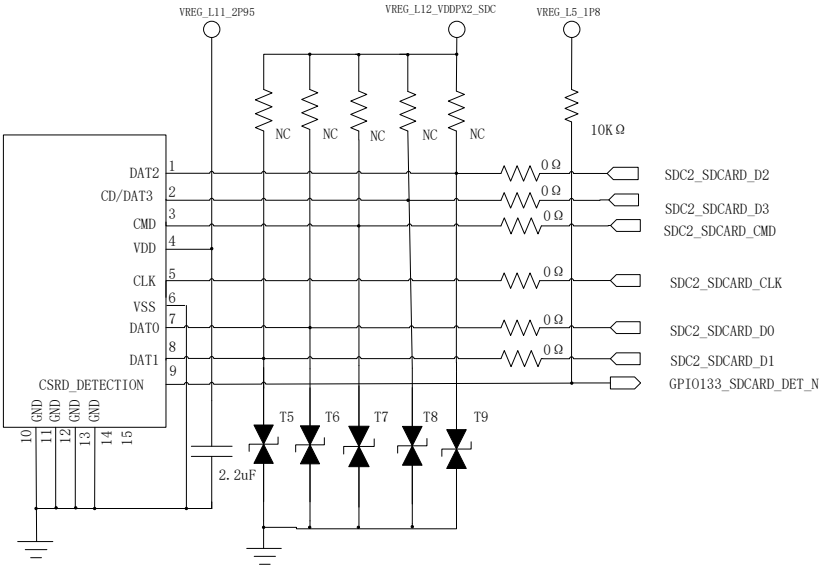


Figure 32 SD Card Interface Circuit

4.14. I2C Bus Interface

The SNM758 module supports four hardware I2C bus interfaces and one camera-specific CCI interface. The pin definitions and default functions are as follows:

Name	Pin	Default Function
CAM_I2C_SDA0	105	Camera dedicated
CAM_I2C_SCL0	104	
GPIO14_SENSOR_I2C4_SDA	17	General purpose I2C, default for sensor
GPIO15_SENSOR_I2C4_SCL	18	
GPIO6_I2C2_SDA	13	General purpose I2C
GPIO7_I2C2_SCL	14	
CAM_I2C_SDA1	96	Camera dedicated
CAM_I2C_SCL1	95	
GPIO10_TP_I2C3_SDA	234	General purpose I2C, default for TP
GPIO11_TP_I2C3_SCL	233	
GPIO18_NFC_I2C5_SDA	254	Universal I2C, default for NFC
GPIO19_NFC_I2C5_SCL	253	

Table 4 I2C Interface Pin Description

Note: It is recommended to use the 2.2KΩ pull-up resistor to 1.8V when using as an I2C bus interface, refer to Table 15 - I2C Interface.

4.15. Analog to Digital Converter (ADC)

The SNM758 module provides three MPP function signals from the power management chip: PMI8953_MPP1 (4PIN) and PM8953_MPP2 (112PIN), PM8953_MPP4 (209PIN) MPP can be configured as an ADC or PWM signal. Note: PM8953_MPP2 and PM8953_MPP4 cannot be configured as PWM functions at the same time.

The ADC signal is 16 bit resolution, and its performance parameters are as follows:

Table 16 ADC Performance Parameters

Description	Minimum	Typical	Maximum	Unit
Input Voltage Range	-	1.8	-	V
ADC Resolution	-	-	15	bits
Analog Input Bandwidth	-	100	-	kHz
Sampling Frequency	-	2.4	-	MHz
INL	-8	-	8	LSB
DNL	-4	-	4	LSB
Offset error	-1	-	1	%
Gain error	-1	-	1	%

4.16. PWM

The PWM pin can be used as a backlight adjustment for the LCD to adjust the backlight brightness by tuning the duty cycle.

4.17. Motor

The SNM758 supports motor functions and can be implemented by the user via PMI_HAP_OUT_N -(8PIN) and PMI_HAP_OUT_P (9PIN). The reference schematic diagram is as follows. Note that the uF-level capacitor cannot be placed on the signal line.

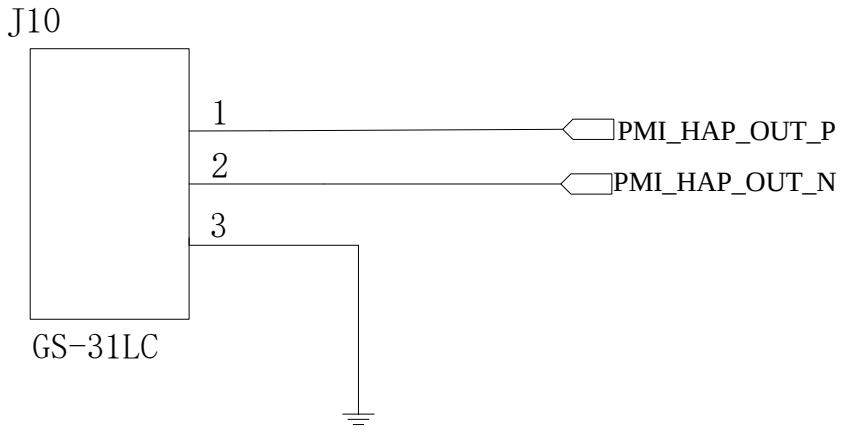


Figure 33 Motor interface circuit

For motor interface circuit design, please refer to the specific reference design. The motor interface circuit of different modules is different.

4.18. Antenna Interface

The module provides four antenna interfaces: MAIN antenna, DRX antenna, and WiFi/BT antenna.

4.18.1. Main Antenna

The module provides the MAIN antenna interface pin Pin1 RF_MAIN. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

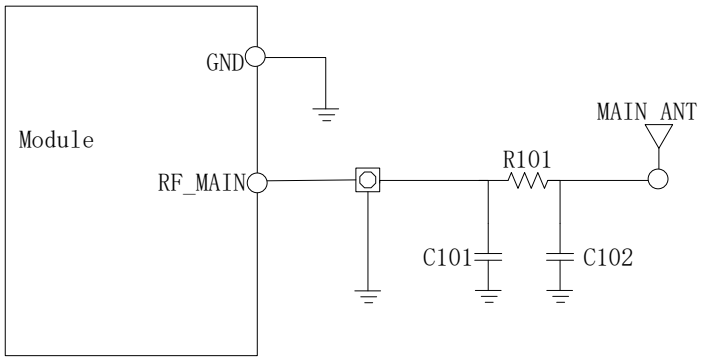


Figure 34 MAIN Antenna Interface Connection Circuit

In the figure, R101, C101, and C102 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R101 defaults to 0R, C101 and C102 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

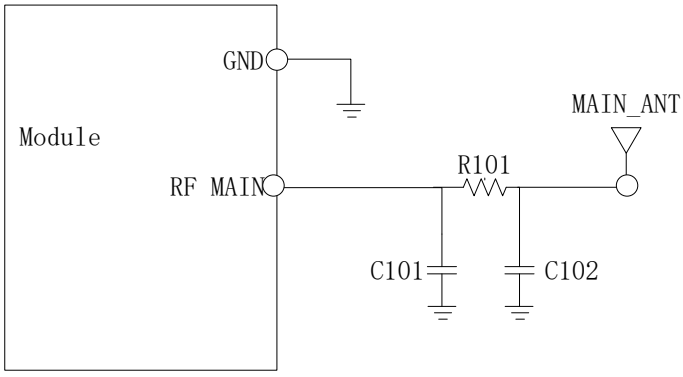


Figure 35 MAIN Antenna Interface Simplified Connection Circuit

In the above figure, R101 defaults to 0R, and C101 and C102 do not paste by default.

4.18.2. DRX Antenna

The module provides the DRX antenna interface pin RF_DIV, and the antenna on the user's motherboard should be connected to the module's antenna pins using a 50-ohm characteristic micros-

trip or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

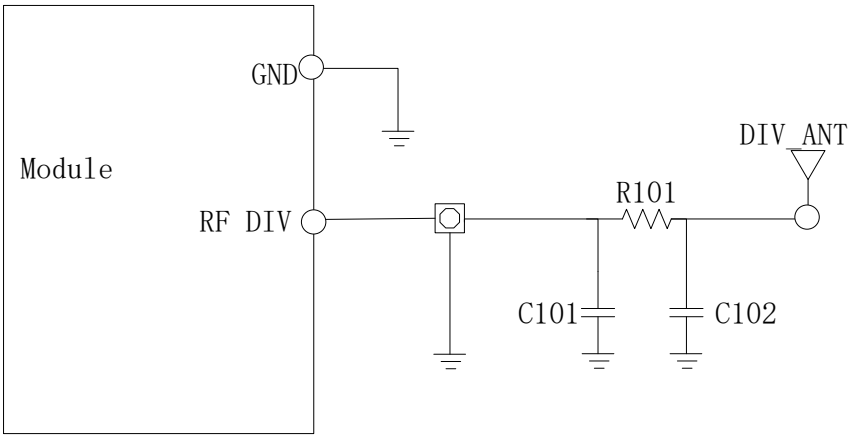


Figure 36 DRX Antenna Interface Connection Circuit

In the figure, R102, C103, and C104 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R102 defaults to 0R, C103 and C104 are not posted by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

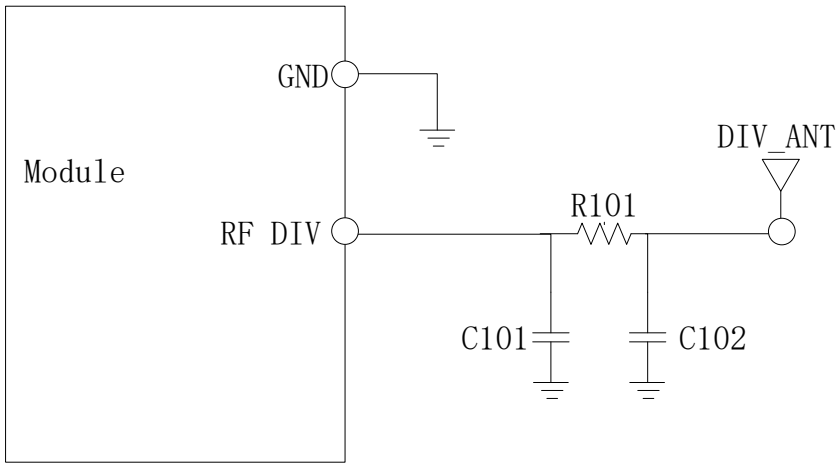


Figure 37 DRX Antenna Interface Simplified Connection Circuit

In the above figure, R102 defaults to 0R, C103 and C104 are not attached by default.

4.18.3. WiFi/BT Antenna

The module provides the WiFi/BT antenna pin RF_WIFI/BT. The antenna on the user's motherboard should be connected to the antenna pin of the module using a 50 ohm microstrip line or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna

matching network should be added. The recommended circuit diagram is as follows:

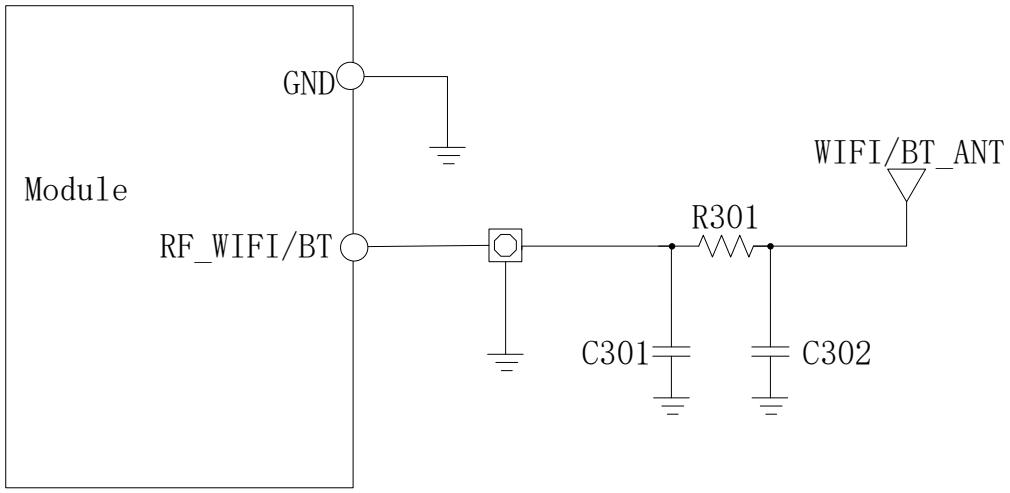


Figure 39 WiFI_BT antenna interface connection circuit

In the figure, R301, C301, and C302 are antenna matching components, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R301 defaults to 0R, C301 and C302 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

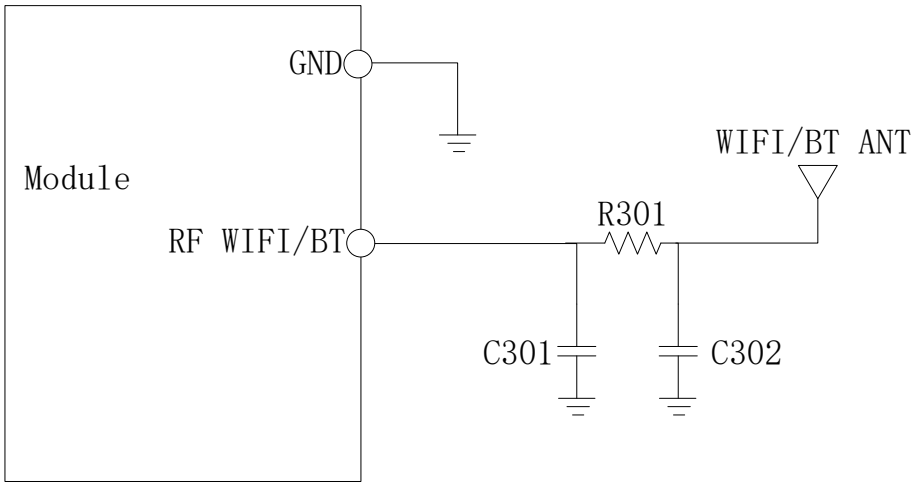


Figure 40 WIFI_BT antenna interface simplified connection circuit

In the above figure, R301 defaults to 0R, and C301 and C302 not mounted by default.

4.18.4. Antenna PCB layout

In order to ensure that the user's products have good wireless performance, the antenna selected by the user should meet the requirement that the input impedance is 50 ohms in the working frequency band and the VSWR is less than 2.

Pay attention to component placement and RF routing:

The RF test head is used to test the conducted RF performance and should be placed as close as

possible to the antenna pins of the module.

The antenna matching circuit needs to be placed close to the antenna end;

The connection between the antenna pin of the module and the antenna matching circuit must be controlled by 50 ohm impedance;

The device and wiring between the antenna pin and the antenna connector of the module must be away from high-speed signal lines and strong interference sources to avoid crossing or parallel with any signal lines in adjacent layers.

The length of the RF cable between the antenna pin of the module and the antenna connector should be as short as possible. The situation of crossing the entire PCB should be absolutely avoided.

If the antenna is connected by a coaxial RF line, care should be taken to avoid the coaxial RF line spanning the SIM card, power supply circuit, and high-speed digital circuits to minimize the effects of each other.

5. Electrical, Reliability

5.1. Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits can cause permanent damage to the module.

Table 5 Absolute Maximum

Parameter	Minimum	Typical	Maximum	Unit
VBAT	-	-	6	V
VBUS	-	-	10.5	V
Peak current	-	-	3	A

5.2. Working Temperature

The table below shows the operating temperature range of the module:

Table 6 Module Operating Temperature

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-25	-	75	℃
Storage temperature	-40	-	90	℃

5.3. Working Voltage

Table 7 Module Operating Voltage

Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.5		4.2	V
VBUS	4	5	5.8	V
Hardware shutdown voltage	3.2		-	V

5.4 Digital Interface Features

Table 8 Digital Interface Features (1.8V)

Parameter	Description	Minimum	Typical	Maximum	Unit
VIH	Input high level voltage	1.17	-	-	V
VIL	Input low level voltage	-	-	0.63	V
VOH	Output high level voltage	1.35	-	-	V
VOL	Output low level voltage	-	-	0.45	V

5.5. SIM_VDD Characteristics

Table 9 SIM_VDD Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
V_O	Output voltage	-	3	-	V
		-	1.8	-	
I_O	Output current	-	-	55	mA

5.6. PWRKEY Feature

Table 10 PWRKEY Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
PWRKEY	High level	1.4	-	-	V
	Low level	-	-	0.6	V
	Effective time	3000			ms

5.7. VCOIN Feature

Table 11 VCOIN Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
VCOIN-IN	VCOIN input voltage	2	3	3.25	V
VCOIN-OUT	VCOIN Output voltage	-	3	-	V

5.8. Current Consumption (VBAT = 3.8V)

Table 12 Current consumption

Parameter	Description	Condition	Minimum	Typical	Maximum	Unit
VBAT	voltage	Voltage must be between the maximum and minimum values	3.5	3.8	4.2	V
Ivbat	Average current	Shutdown mode	-	-	65	uA
		GSM Standby power consumption	-	-	4.0	mA
		WCDMA Standby power consumption	-	-	2.99	mA
		TD-S Standby power consumption	-	-	3.27	mA
		CDMA Standby power consumption	-	-	3.25	mA
		FDD Standby power consumption			3.47	mA
		TDD Standby power consumption			3.24	mA

6.Production

6.1. Top and Bottom Views of the Module

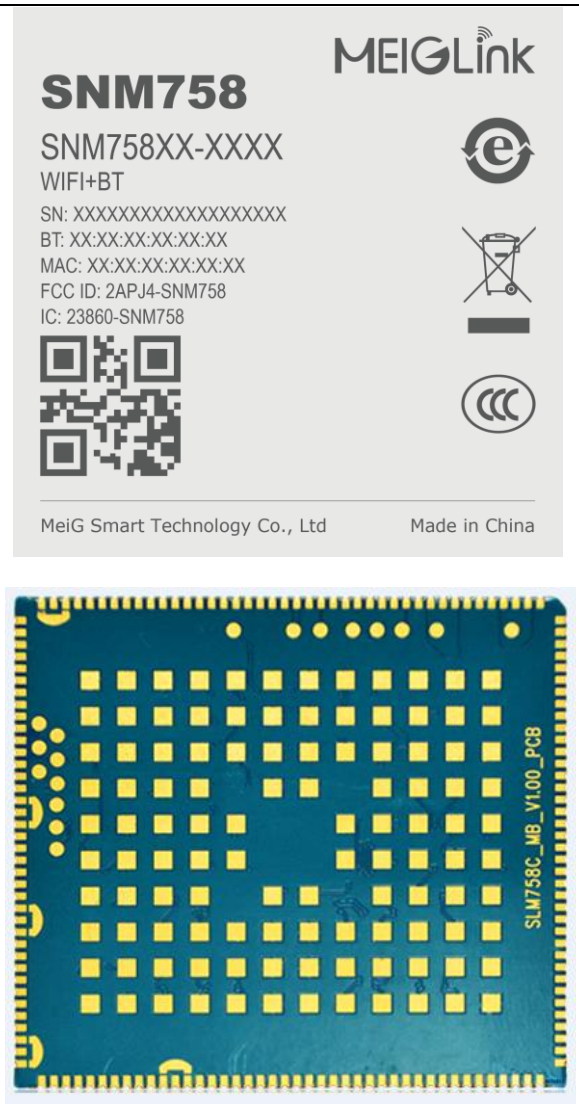


Figure 41 Module top and bottom views

6.2. Recommended Soldering Furnace Temperature Curve

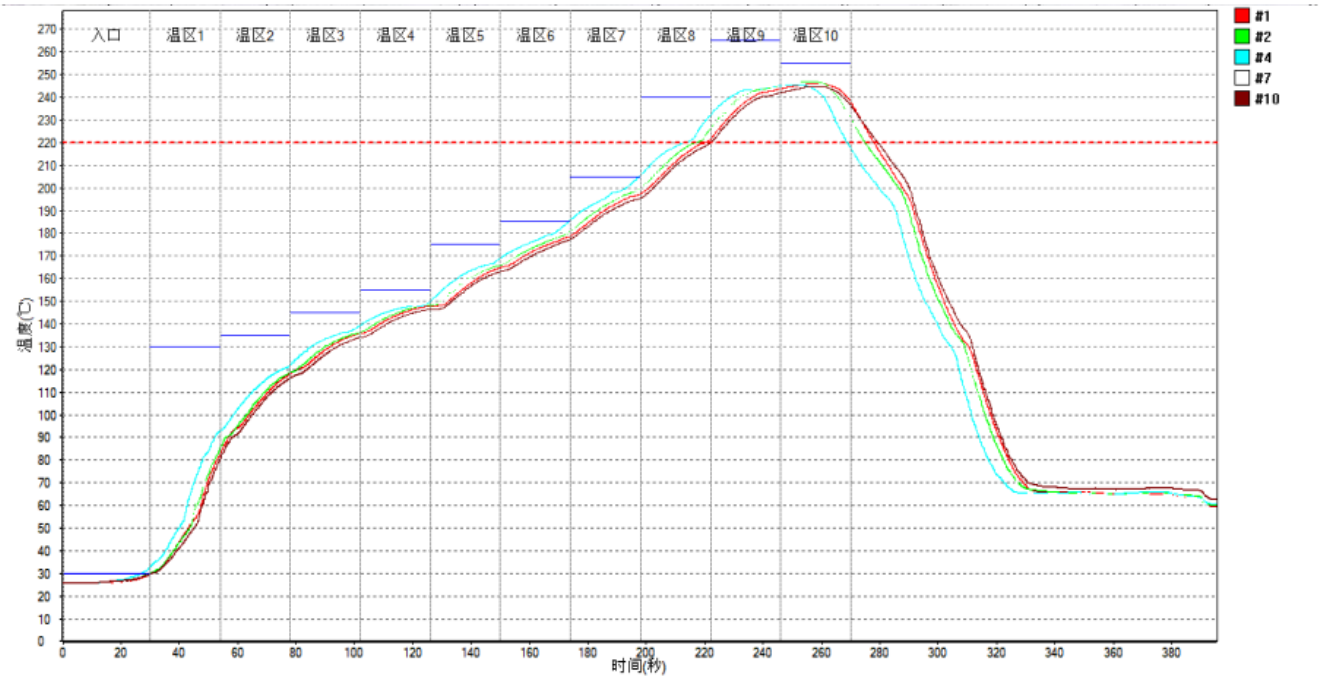


Figure 42 Module recommended soldering furnace temperature curve

6.3. Humidity Sensitivity (MSL)

The SNM758 module meets moisture sensitivity level 3. The dry package is subjected to the J-STD-020C specification in accordance with the IPC/JEDEC standard under ambient conditions of temperature <30 degrees and relative humidity <60%. Under ambient conditions of temperature <40 degrees and relative humidity <90%, the shelf life is at least 6 months without unpacking. After unpacking, Table 22 lists the shelf life of the modules for different moisture sensitivity levels.

Table 13 Humidity sensitivity level distinction

Grade	Factory environment≦+30℃/60%RH
1	Indefinite quality in the environment≦+30℃/85% RH Under conditions
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Use it after forced baking. After baking, the module must be patched within the time limit specified on the label.

After unpacking, the SMT patch should be taken within 168 hours under ambient conditions of <30 degrees and relative humidity <60%. If the above conditions are not met, baking is required. Note: Oxidation risk: Baking SMD packages can cause metal oxidation and, if excessive, can cause solder ability problems during board assembly. The temperature and time of the SMD package are baked, thus limiting solder ability considerations. The accumulation of baking time should be no more than 96 hours at temperatures above 90°C and as high as 125°C

6.4. Baking Requirements

Due to the humidity sensitivity of the module, the SNM758 should be thoroughly baked prior to reflow soldering, otherwise the module may cause permanent damage during reflow soldering. The SNM758 should be baked for 192 hours in a cryogenic vessel at 40°C +5°C/-0°C and a relative humidity of less than 5%, or in a high temperature vessel at 80°C±5°C.Bake for 72 hours. Users should note that the tray is not resistant to high temperatures. The user should take the module out of the tray for baking, otherwise the tray may be damaged by high temperature.

Table 14 Baking requirements:

Baking Temperature	Humidity	Baking Time
40°C±5°C	<5%	192 hours
120°C±5°C	<5%	4 hours

7.Appendix

7.1. Related Documents

Table 34 Related documents

#	File Name	Comment
[1]	GSM 07.07：	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10：	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05：	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)
[4]	GSM 11.14：	Digital cellular telecommunications system (Phase 2+);Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11：	Digital cellular telecommunications system (Phase 2+);Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38：	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2)；Mobile Station (MS) conformance specification；Part 1：Conformance specification
[8]	AN_Serial Port	AN_Serial Port

7.2. Terms and Explanations

Table 35 Terms and explanations

Term	Explanation
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)

DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction

SIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
Phone book abbreviation	Explanations
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

8.FCC/IC warning

8.1. FCC warning

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify

compliance as a composite system. When testing the host device for compliance with Part

15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to MEIge that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

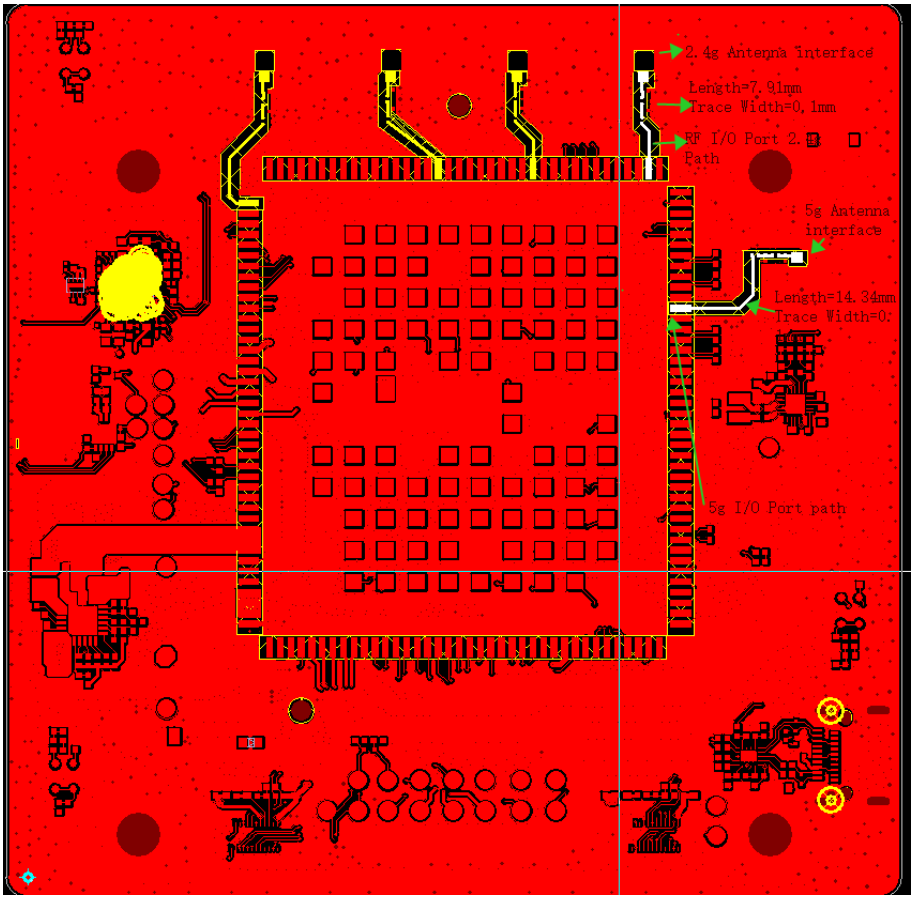
End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: 2APJ4-SNM758”

“Contains IC: 23860-SNM758 “

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Trace



Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	2.4GHz band	5.2GHz band	5.3GHz band	5.5GHz band	5.8GHz band

	Peak Gain (dBi)	Peak Gain (dBi)	Peak Gain (dBi)	Peak Gain (dBi)	Peak Gain (dBi)
Glue Stick	0	1	1	1	1

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15.247 and 15.407 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1. The antenna must be installed such that 20 cm is maintained between the antenna and users.
2.The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

8.2. IC warning

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the

following two conditions:

(1) This device may not cause interference; and

(2) This device must accept any interference, including interference that may cause undesired

operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

RSS-247 Section 6.4 (5) (6) (for local area network devices, 5GHz)

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;

The maximum antenna gain permitted for devices in the bands 5250–5350 MHz and 5470–5725 MHz shall comply with the e.i.r.p. limit; and

The maximum antenna gain permitted for devices in the band 5725–5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;

Le gain d'antenne maximal autorisé pour les dispositifs dans les bandes 5250-5350 MHz et 5470-5725 MHz doit être conforme à la norme e.r.p. limite; et

Le gain d'antenne maximal autorisé pour les appareils de la bande 5725-5825 MHz doit être conforme à la norme e.i.r.p. les limites spécifiées pour un fonctionnement point à point et non point à point, selon le cas.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1.The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2. The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC:23860-SNM758”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 23860-SNM758 ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this

module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

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