SLM500 Hardware Design Guide

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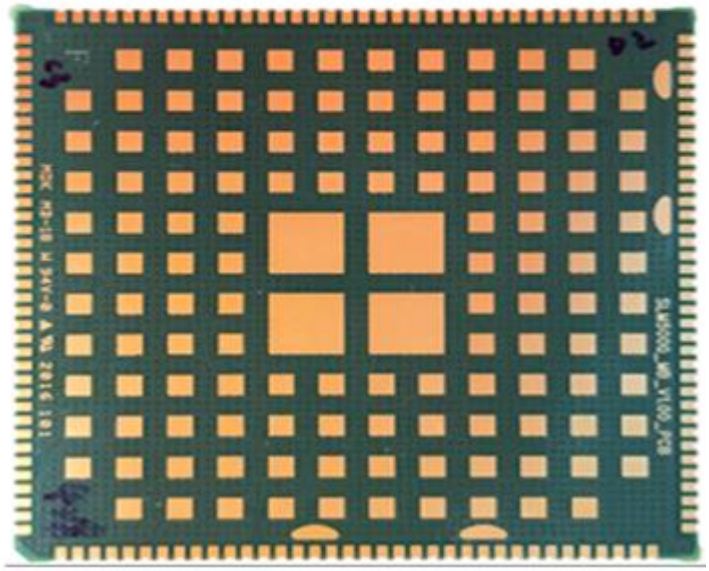

Foreword

Thank you for using the SLM500 module from Meg Smart. This product can provide data communication services. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

The company does not assume responsibility for property damage or personal injury caused by improper operation of the user. Users are requested to develop the corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety issues that mobile products should focus on.

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Contents

Version History

Date	Version	Change description	Author
2020-07-02	1.00	First edition	MeiG Hardware

1.Introduction

This document describes the hardware application interface of the module, including the connection of the circuit and the RF interface. It can help users quickly understand the interface definition, electrical performance, and structural dimensions of the module. Combining this document with other application documents, users can quickly use modules to design mobile communication applications.

2.Module overview

SLM500 module uses the Qualcomm solution based on arm cotex-A53 four core processor, with the highest main frequency of 4 * 1.3GHz, and the memory supports single channel 32-bit LPDDR3/672MHz.This module is suitable for broadband intelligent wireless communication modules of TD-LTE/FDD-LTE/WCDMA/EVDO/TD-SCDMA/CDMA/GSM network standards.

The physical interface of the module is a 272-pin pad that provides the following hardware interfaces:

- Three 1.8V UART serial ports, supporting four or two wires.
- Main LCD（MIPI interface）.
- Two groups of Camera interface（MIPI data）.
- USB2.0 interface.
- Three groups of Audio input interface.
- Three groups of Audio output interface.
- Dual-Sim card interface.
- GPIO interface.
- Five groups of I2C interfaces.
- One sets of SPI interfaces.
- TF card interface.
- Support GNSS，WiFi，Bluetooth 4.2

2.1 Summary of features

Table 2.1： SLM500 features

Product characteristics		Description	
CPU		Quad-core A53 (64bit) 1.3GHz	
GPU		Adreno 308 @485MHz	
System memory		8GB eMMC + 1GB LPDDR3 compatible with 16GB+2GB	
OS		Android 10	
Size		40.5x40.5x2.8mm，LCC 146pin+LGA 128pin	
RF band--SLM500A		FDD-LTE: B2/4/5/7/12/13/17/25/26/66 WCDMA: B2/4/5 GSM: B2/5	
Wi-Fi		IEEE 802.11b/g/n 2.4G 802.11a/n 5G	
Bluetooth		BT 4.2	
FM		No support	
GNSS		GPS/ Beidou/ Glonass	
Data Access	TD-LTE	Cat4 TD-LTE 117/30Mbps	
	FDD-LTE	Cat4 FDD-LTE 150/50Mbps	
	DC-HSPA+	42/11.2Mbps	
	TD-HSPA	2.8/2.3Mbps	
	EVDO Rev.A	3.1/1.8Mbps	
	EDGE	Class12, 236.8kbps/236.8kbps	
	GPRS	Class12, 85.6kbps/85.6kbps	
SIM		DSDS(Dual Sim & Dual Stanby) 3.0/1.8V Support SIM hot plug L/W/G+G with CSFB to W/G L/TDS/G+G with CSFB to TDS/G L/EVDO/CDMA1X+ G L/W/TDS/G+CDMA1X Don’t support dual CDMA SIM card	
Display		Matrix: HD+： 1440*720 60fps	
		LCD Size: User defined	
		Interface: One MIPI DSI 4-lane;	
Camera (Front and Rear)		Interface: main: MIPI CSI 4-lanes; front: MIPI CSI 4-lanes	
		Camera Pixel: Max. Rear 5Mp/Front up to 13Mp	
		Video decode	1080p 30 fps: H.264/VP8/HEVC (H.265) 720p 30fps in SW
		Video encode	1080p 30 fps: H.264

Input Device	Key（Power on/off, Reset , Home, Volume+, Volume-）	
	Capacitive TP	
Reset	Support HW reset	
Application interface	Interface name	Main function description
	VBAT	4pin，Power input，3.4V～4.2V，Nominal value3.8V
	SDIO *1	TF Card，Support 32GB max
	USB	Support OTG USB_BOOT（Force USB boot for emergency downloads）
	BLSP ports	6 ports(BLSP2-7), 4-bits each, multiplexed serial interface functions
	UART*3	Max up to 4 Mbps
	I2C*5	Support
	SPI (master only)	Support
	ADC*1	Support
	PWM*1	Support
	Charge	Max up to 1.44A
	Vibrator	Support
	GPIO	40 GPIOs，Excluded BLSP multiplexing GPIO.
	VCOIN	Real time clock backup battery
	RF Interface	Multimode LTE main antenna Multimode LTE diversity antenna The GPS antenna 2.4G +5G WiFi/BT antenna
	Audio	One main MIC One noise reduction MIC One Handsfree speaker. One earpiece One stereo headphone.
Accessories versions	SLM500QW_MB_V1.01_PCB	
Software versions	SLM500Q_EQ000_2774.2AAF2F74.BCA2CDE_200628_100_V01_T09	

2.2 Block diagram

The following figure lists the main functional parts of the module:

- baseband chip
- power management chip
- Transceiver chip
- WCN3660-WIFI/BT Two in one chip
- Antenna interface
- LCD/CAM-MIPI interface
- EMCP memory chip
- AUDIO interface
- UART、SD card interface，SIM card interface，I2Cinterface,etc.

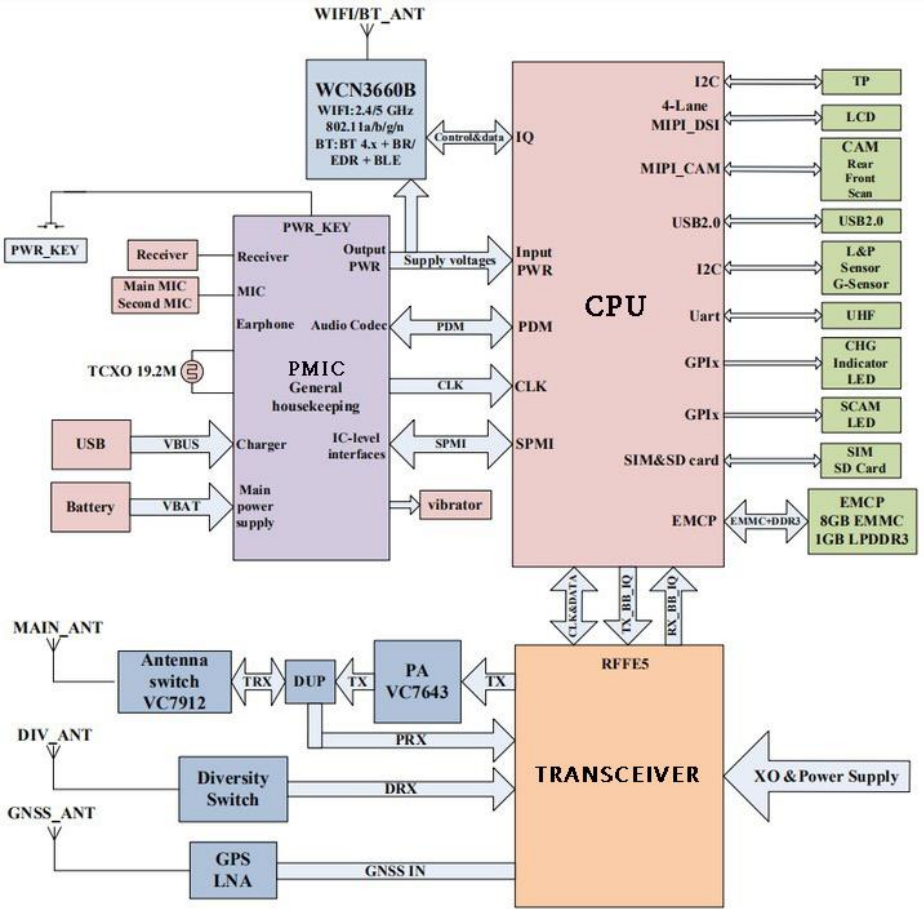


Figure 2.1: module function block diagram

3. Module Package

3.1.Pin distribution diagram

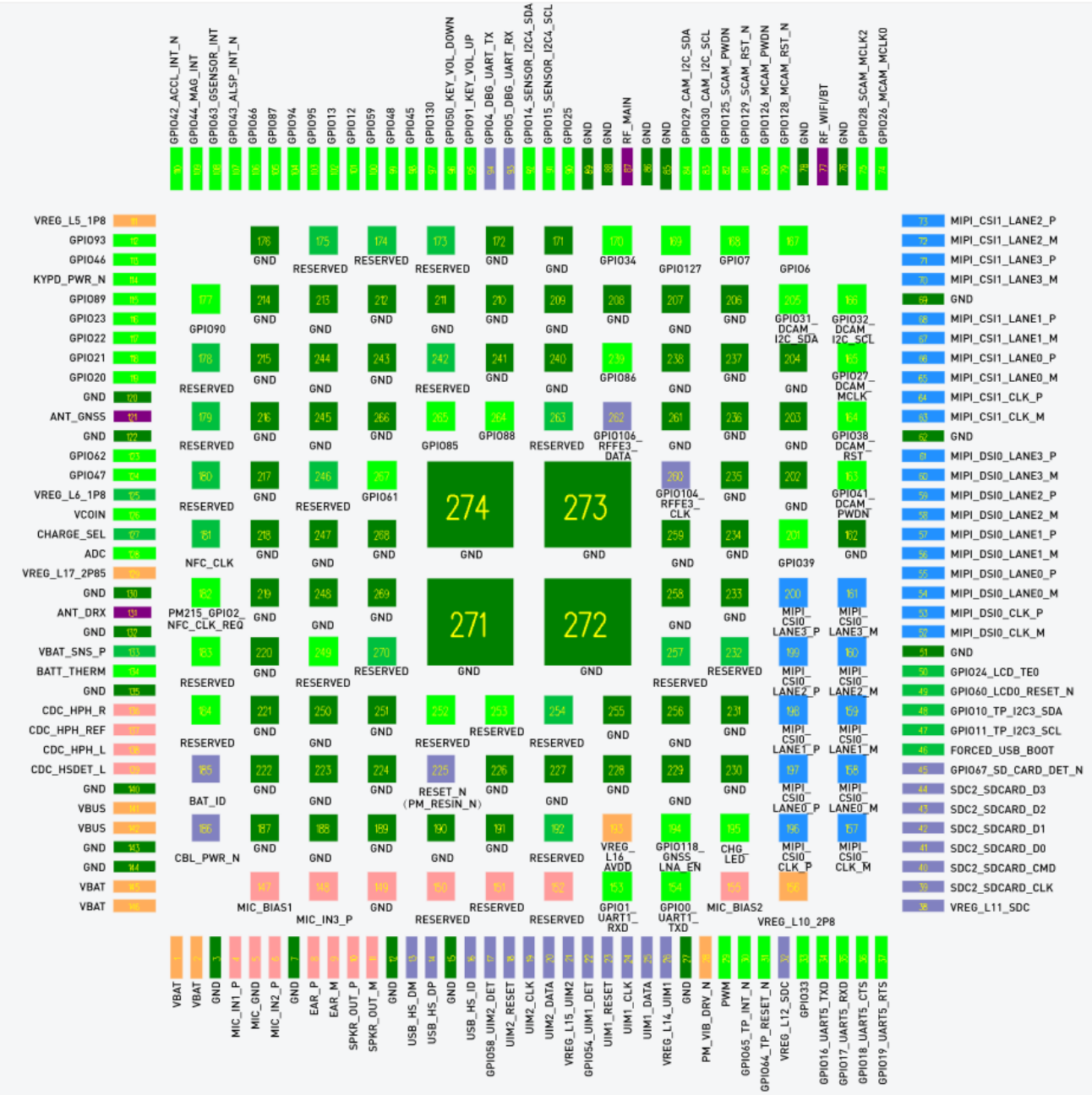


Figure 3.1： module pin diagram (top view)

3.2. Pin definitions

table 3.1：Pin description

Pin number	Pin number	I/O	Description	Comment
The power supply				
VBAT	1、2、145、146	I	The module provides Four VBAT power pin pins. The SLM500 operates from a single supply with a voltage range from 3.4V to 4.2V for VBAT.	Externally, large capacitors and Zener diodes must be added for surge protection.
VBUS	141、142	I/O	5V charging input power.	
VCOIN	126	I/O	When the VBAT of the system power is absent, the external backup battery provides power to the system real-time clock. When VBAT is present, the backup battery is charged.	VCOIN pins connect 3V button batteries or large capacitors.
VREG_L5_1P8	111	O	1.8V power output, Power supply always available for IO port pull-up and level conversion, not for peripheral power supply	50mA
VREG_L6_1P8	125	O	1.8 V power output, standby will be closed, used for Camera, LCD and other small current power supply.	100mA
VREG_L10_2P8	156	O	2.8V power output, used for Sensor, TP power supply.	150mA
VREG_L17_2P85	129	O	2.85 V power output, for LCD, Camera 2.8V.	300mA
VREG_L11_SDC	38	O	TF card power supply pin	500mA
VREG_L12_ SDC	32	O	TF card signal pull-up power supply pin	50mA
VREG_L14_UIM1	26	O	UIM power supply pins	50mA
VREG_L15_UIM2	21	O	UIM power supply pins	50mA
VREG_L16_AVDD	193	O	Camera AVDD	50mA
GND	3、7、12、15、27、51、62、69、76、78、85、86、88、89、120、122、130、132、135、140、143、144、149、162 、171、172、176 、187~191、202~204 206~224、226~231 233~238、240、241、243、244、245、247、248、		GND	

	250、251、255、256、258、259、261、266、268、269、271~274			
display interface (MIPI)				
MIPI_DSI0_CLK_M	52	I/O	MIPI_LCD clock	
MIPI_DSI0_CLK_P	53	I/O		
MIPI_DSI0_LANE0_M	54	I/O	MIPI_LCD data	
MIPI_DSI0_LANE0_P	55	I/O		
MIPI_DSI0_LANE1_M	56	I/O		
MIPI_DSI0_LANE1_P	57	I/O		
MIPI_DSI0_LANE2_M	58	I/O		
MIPI_DSI0_LANE2_P	59	I/O		
MIPI_DSI0_LANE3_M	60	I/O		
MIPI_DSI0_LANE3_P	61	I/O		
GPIO61_LCD_RST_N	49	O	LCD reset	
GPIO24_LCD_TE0	50	I/O	LCD frame sync signal	
UART(1.8V)				
GPIO0_UART1_TXD	154	I	UART1 data transmit	
GPIO1_UART1_RXD	153	O	UART1 data receive	
GPIO4_DBG_UART_TX	94	I	UART2 data receive	
GPIO5_DBG_UART_RX	93	O	UART2 data transmit	
GPIO16_UART5_TXD	34	I	UART5 data receive	
GPIO17_UART5_RXD	35	O	UART5 data transmit	
GPIO18_UART5_CTS	36	I	UART5 Clear To Send（CTS）	
GPIO19_UART5_RTS	37	O	UART5 Request To Send（RTS）	
UIM card Interface				
GPIO54_UIM1_DET	22	I	UIM1 insert detect	
UIM1_RESET	23	O	UIM1 reset	
UIM1_CLK	24	O	UIM1 clock	
UIM1_DATA	25	I/O	UIM1 data	
GPIO58_UIM2_DET	17	I	UIM2 insert detect	
UIM2_RESET	18	O	UIM2 reset	
UIM2_CLK	19	O	UIM2 clock	
UIM2_DATA	20	I/O	UIM2 data	
Front Camera				

MIPI_CSI0_CLK_M	157	I/O	Front Camera MIPI clock	
MIPI_CSI0_CLK_P	196	I/O		
MIPI_CSI0_LANE0_M	158	I/O	Front Camera MIPI data	
MIPI_CSI0_LANE0_P	197	I/O		
MIPI_CSI0_LANE1_M	159	I/O		
MIPI_CSI0_LANE1_P	198	I/O		
MIPI_CSI0_LANE2_M	160	I/O		
MIPI_CSI0_LANE2_P	199	I/O		
MIPI_CSI0_LANE3_M	161	I/O		
MIPI_CSI0_LANE3_P	200	I/O		
GPIO28_SCAM_MCLK2	75	I/O	Front Camera main clock	
GPIO129_SCAM_RST_N	81	I/O	Front Camera reset	
GPIO125_SCAM_PWDN	82	I/O	Front Camera dormancy	
Rear Camera				
MIPI_CSI1_CLK_M	63	I/O	Rear Camera MIPI clock	
MIPI_CSI1_CLK_P	64	I/O		
MIPI_CSI1_LANE0_M	65	I/O	Rear Camera MIPI data	
MIPI_CSI1_LANE0_P	66	I/O		
MIPI_CSI1_LANE1_M	67	I/O		
MIPI_CSI1_LANE1_P	68	I/O		
MIPI_CSI1_LANE2_M	72	I/O		
MIPI_CSI1_LANE2_P	73	I/O		
MIPI_CSI1_LANE3_M	70	I/O		
MIPI_CSI1_LANE3_P	71	I/O		
GPIO26_MCAM_MCLK0	74	I/O	Rear Camera main clock	
GPIO128_MCAM_RST_N	79	I/O	Rear Camera reset	
GPIO126_MCAM_PWDN	80	I/O	Rear Camera dormancy	
Audio Interface				
MIC_GND	5		The main MIC negative	
MIC_IN1_P	4	I	The main MIC positive	
MIC_IN2_P	6	I	Headphone MIC positive	
MIC_IN3_P	148	I	Secondary MIC positive	
MIC_BIAS1	147	O	The BIAS voltage of main MIC is used in the design of silicon wheat	
MIC_BIAS2	155	O	The BIAS voltage of the earphone MIC is used in the design of silicon wheat	

CDC_HPH_R	136	O	Right channel of earphone	
CDC_HPH_L	138	O	Left channel of earphone	
CDC_HSDET_L	139	I	Headphone plug and unplug detection	
CDC_HPH_REF	137	I	Earphone reference GND	
EAR_P	8	O	Earpiece output negative	
EAR_M	9	O	Earpiece output positive	
SPKR_OUT_P	10	O	Power amplifier output negative	Class D
SPKR_OUT_M	11	O	Power amplifier output positive	Class D
SD card Interface				
GPIO67_SD_CARD_DET_N	45	I/O	SD card insertion detection	
SDC2_SDCARD_CMD	40	I/O	SD CMD	
SDC2_SDCARD_CLK	39	I/O	SD clock	
SDC2_SDCARD_D0	41	I/O	SD data	
SDC2_SDCARD_D1	42	I/O		
SDC2_SDCARD_D2	43	I/O		
SDC2_SDCARD_D3	44	I/O		
I2C				
GPIO29_CAM_I2C_SDA0	84	I/O	Special I2C signal can only be used for CAM	Pullup to VREG_L6_1P8
GPIO30_CAM_I2C_SCL0	83	I/O		
GPIO31_DCAM_I2C_SDA1	205	I/O	Default for DCAM	
GPIO32_DCAM_I2C_SCL1	166	I/O		
GPIO14_SENSOR_I2C4_SDA	92	I/O	Special I2C signal can only be used for SENSOR	
GPIO15_SENSOR_I2C4_SCL	91	I/O		
GPIO10_TP_I2C3_SDA	48	I/O	Universal I2C signal, which is used by default for TP	Pullup to VREG_L5_1P8
GPIO11_TP_I2C3_SCL	47	I/O		
GPIO6	167	I/O	Universal I2C signal,。	
GPIO7	168	I/O		
TP				
GPIO10_TP_I2C3_SDA	48	I/O	Universal I2C signal, which is used by default for TP	Pullup to VREG_L5_1P8
GPIO11_TP_I2C3_SCL	47	I/O		
GPIO65_TP_INT_N	30	I	TP interrupt	
GPIO64_TP_RESET_N	31	O	TP reset	
USB				
USB_HS_DM	13	I/O	USB DM	
USB_HS_DP	14	I/O	USB DP	
USB_HS_ID	16	I	USB ID	

Antenna interface				
RF_MAIN	87	I/O	The main antenna	
RF_WIFI/BT	77	I/O	WIFI/BT antenna	
RF_DIV	131	I	Diversity antenna	
RF_GPS	121	I	GPS antenna	
GPIOand default function				
GPIO20	119	I/O	Generic GPIO, SPI MOSI	
GPIO21	118	I/O	Generic GPIO, SPI MISO	
GPIO22	117	I/O	Generic GPIO, SPI CS	
GPIO23	116	I/O	Generic GPIO, SPI CLK	
GPIO89	115	I/O	Generic GPIO, without default configuration	
GPIO44_MAG_INT	109	I/O	The default configuration is the compass interrupt signal.	
GPIO42_ACCL_INT_N	110	I/O	The default configuration is G-sensor interrupt	
GPIO43_ALSP_INT_N	107	I/O	The default configuration is Ps-sensor interrupt signal	
GPIO63_GYRO_INT	108	I/O	The default configuration is the gyroscope interrupt signal.	
GPIO34	170	I/O	Generic GPIO, without default configuration	
GPIO85	265	I/O	Generic GPIO, MI2S1 SCK	
GPIO86	239	I/O	Generic GPIO, MI2S1 D1	
GPIO87	105	I/O	Generic GPIO, MI2S1 WS	
GPIO88	264	I/O	Generic GPIO, MI2S1 D0	
GPIO32_DCAM_I2C_SCL1	166	I/O	default configuration Depth camera I2C	
GPIO31_DCAM_I2C_SDA1	205	I/O	default configuration Depth camera I2C	
GPIO27_DCAM_MCLK	165	I/O	default configuration Depth camera MCLK	
GPIO38_DCAM_RST	164	I/O	default configuration Depth camera reset	
GPIO41_DCAM_PWDN	163	I/O	default configuration Depth camera power down	
GPIO12	101	I/O	General purpose GPIO, no default configuration	
GPIO48	99	I/O	Generic GPIO, without default configuration	
GPIO59	100	I/O	Generic GPIO, without default configuration	
GPIO13	102	I/O	Generic GPIO, without default configuration	
GPIO61	267	I/O	Generic GPIO, without default configuration	

GPIO45	98	I/O	Generic GPIO, without default configuration	
GPIO25	90	I/O	Generic GPIO, without default configuration	
GPIO33	33	I/O	Generic GPIO, without default configuration	
GPIO39	201	I/O	Generic GPIO, without default configuration	
GPIO46	113	I/O	Generic GPIO, without default configuration	
GPIO47	124	I/O	Generic GPIO, without default configuration	
GPIO62	123	I/O	Generic GPIO, without default configuration	
GPIO66	106	I/O	Generic GPIO, without default configuration	
GPIO90	177	I/O	Generic GPIO, without default configuration	
GPIO93	112	I/O	Generic GPIO, without default configuration	
GPIO94	104	I/O	Generic GPIO, without default configuration	
GPIO95	103	I/O	Generic GPIO, without default configuration	
GPIO127	169	I/O	Generic GPIO, without default configuration	
GPIO25	90	I/O	Generic GPIO, without default configuration	
GPIO130	97	I/O	Generic GPIO, without default configuration	
GPIO104_RFFE3_CLK	260	I/O	GRFC only used for RF Tuner, control, not for general GPIO	
GPIO106_RFFE3_DATA	262	I/O		
GNSS_LNA_EN	194	I/O	External GPS LNA enable	
Other functional pin				
FORCED_USB_BOOT	46	I	Pull up to 1.8 V into the emergency download mode	
CHARGE_SEL	127	I	SMB1360 (external charge IC) is used, the pin shall be grounded; when PM215is used, the pin shall be suspended.	
CHG_LED	195	O	The charging indicator light negative	
GPIO91_KEY_VOL_UP_N	95	I/O	Control volume increase	
GPIO50_KEY_VOL_DOWN	96	I/O	Control volume decrease	
KYPD_PWR_N	114	I	Pull down to power on / off	
RESET_N	225	I	Pull down to reset	
BATT_THERM	134	I	Battery temperature detection, Battery terminal NTC resistance default 47K).	

VBAT_SNS_P	133	I	Battery voltage monitoring	
PM_VIB_DRV_N	28	O	Motor negative control	
ADC	128	I	Analog voltage input can be used as ADC input	
PWM	29	O	Analog voltage input can be used as PWM input	optional
NFC_CLK	181	O	NFC Clock	
NFC_CLK_REQ	182	I	Default PM215 GPIO2	
CBL_PWR_N	186	I	Grounding support power on automatic startup	
BAT_ID	185	I	Battery type detection	
RESERVED	150、151、152、173、174、175、178、179、180、183、184、192、232、242、246、249、252、253、254、257、263、270			

Table 3.2: Pin Characteristics

PIN#	SLM500 Pin name	GPIO Interrupt	Pad characteristics	Functional description
1	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
2	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
3	GND		GND	GND
4	MIC_IN1_P		AI	Microphone 1 input plus
5	MIC_GND		GND	Microphone bias filter ground
6	MIC_IN2_P		AI	Microphone 2 input plus
7	GND		GND	GND
8	EAR_P		AO	Earpiece output, plus
9	EAR_M		AO	Earpiece output, minus
10	SPKR_OUT_P		AO	Class-D speaker driver output, plus
11	SPKR_OUT_M		AO	Class-D speaker driver output, minus
12	GND		GND	GND
13	USB_HS_DM		AI,AO	USB data minus
14	USB_HS_DP		AI,AO	USB data plus
15	GND		GND	GND

16	USB_HS_ID		AI	USB ID
17	GPIO58_UIM2_DET	GPIO58*	B-PD:nppukp	Configurable I/O,UIM2 removal detection
18	UIM2_RESET	GPIO57	B-PD:nppukp	Configurable I/O,UIM2 reset
19	UIM2_CLK	GPIO56	B-PD:nppukp	Configurable I/O,UIM2 clock
20	UIM2_DATA	GPIO55	B-PD:nppukp	Configurable I/O,UIM2 data
21	VREG_L15_UIM2		PO	PMIC output for UIM2
22	GPIO54_UIM1_DET	GPIO54*	B-PD:nppukp	Configurable I/O,UIM1 removal detection
23	UIM1_RESET	GPIO53	B-PD:nppukp	Configurable I/O,UIM1 reset
24	UIM1_CLK	GPIO52	B-PD:nppukp	Configurable I/O,UIM1 clock
25	UIM1_DATA	GPIO51	B-PD:nppukp	Configurable I/O,UIM1 data
26	VREG_L14_UIM1		PO	PMIC output for UIM1
27	GND		GND	GND
28	PM_VIB_DRV_N		PI	Haptics driver output negative
29	PWM		AO-Z,DI,DO	Configurable MPP,PWM,ADC
30	GPIO65_TP_INT_N	GPIO65*	B-PD:nppukp	Configurable I/O,TP INT
31	GPIO64_TP_RESET_N	GPIO64	B-PD:nppukp	Configurable I/O,TP RESET
32	VREG_L12_SDC		PO	PMIC output 2.95V for SDC2 signal
33	GPIO33	GPIO33	B-PD:nppukp	Configurable I/O
34	GPIO16_UART5_TXD	GPIO16	B-PD:nppukp	Configurable I/O,UART5 TX
35	GPIO17_UART5_RXD	GPIO17*	B-PD:nppukp	Configurable I/O,UART5 RX
36	GPIO18_UART5_CTS	GPIO18	B-PD:nppukp	Configurable I/O,UART5 CTS
37	GPIO19_UART5_RTS	GPIO19	B-PD:nppukp	Configurable I/O,UART5 RTS
38	VREG_L11_SDC		PO	PMIC output 2.95V for SD-card power
39	SDC2_SDCARD_CLK		BH-NP:pdpukp	Secure digital controller 2 clock
40	SDC2_SDCARD_CMD		BH-NP:pdpukp	Secure digital controller 2 command
41	SDC2_SDCARD_D0		BH-NP:pdpukp	Secure digital controller 2 data bit 0
42	SDC2_SDCARD_D1		BH-NP:pdpukp	Secure digital controller 2 data bit 1
43	SDC2_SDCARD_D2		BH-NP:pdpukp	Secure digital controller 2 data bit 2
44	SDC2_SDCARD_D3		BH-NP:pdpukp	Secure digital controller 2 data bit 3
45	GPIO67_SD_CARD_DET_N	GPIO67*	B-PD:nppukp	Configurable I/O,SD card detection
46	FORCED_USB_BOOT	GPIO37*	DI	pullup with VREG_L5 to forced USB boot
47	GPIO11_TP_I2C3_SCL	GPIO11	B-PD:nppukp	Configurable I/O,TP I2C SCL
48	GPIO10_TP_I2C3_SDA	GPIO10	B-PD:nppukp	Configurable I/O,TP I2C SDA
49	GPIO60_LCD_RESET_N	GPIO60	B-PD:nppukp	Configurable I/O, LCD RESET
50	GPIO24_LCD_TE0	GPIO24	B-PD:nppukp	Configurable I/O, LCD TE
51	GND		GND	GND

52	MIPI_DSI0_CLK_M		AO	MIPI display serial interface 0 clock-
53	MIPI_DSI0_CLK_P		AO	MIPI display serial interface 0 clock+
54	MIPI_DSI0_LANE0_M		AI	MIPI display serial interface 0 lane0-
55	MIPI_DSI0_LANE0_P		AI	MIPI display serial interface 0 lane0+
56	MIPI_DSI0_LANE1_M		AI	MIPI display serial interface 0 lane1-
57	MIPI_DSI0_LANE1_P		AI	MIPI display serial interface 0 lane1+
58	MIPI_DSI0_LANE2_M		AI	MIPI display serial interface 0 lane2-
59	MIPI_DSI0_LANE2_P		AI	MIPI display serial interface 0 lane2+
60	MIPI_DSI0_LANE3_M		AI	MIPI display serial interface 0 lane3-
61	MIPI_DSI0_LANE3_P		AI	MIPI display serial interface 0 lane3+
62	GND		GND	GND
63	MIPI_CSI1_CLK_M		AI	MIPI camera serial interface 0 clock-
64	MIPI_CSI1_CLK_P		AI	MIPI camera serial interface 0 clock+
65	MIPI_CSI1_LANE0_M		AI	MIPI camera serial interface 0 lane0-
66	MIPI_CS1_LANE0_P		AI	MIPI camera serial interface 0 lane0+
67	MIPI_CSI1_LANE1_M		AI	MIPI camera serial interface 0 lane1-
68	GND		GND	GND
69	MIPI_CSI1_LANE3_M		AI	MIPI camera serial interface 1 lane3-
70	MIPI_CSI1_LANE3_P		AI	MIPI camera serial interface 1 lane3+
71	MIPI_CSI1_LANE2_M		AI	MIPI camera serial interface 1 lane2-
72	MIPI_CSI1_LANE2_P		AI	MIPI camera serial interface 1 lane2+
73	GPIO26_MCAM_MCLK0	GPIO26	B-PD:nppukp	Configurable I/O,main CAM MCLK
74	GPIO28_SCAM_MCLK2	GPIO28*	B-PD:nppukp	Configurable I/O,front CAM MCLK
75	GND		GND	GND
76	RF_WIFI/BT		AI	RF signal for WIFI/BT
77	GND		GND	GND
78	GPIO128_MCAM_RST_N	GPIO128*	B-PD:nppukp	Configurable I/O,main CAM RESET
79	GPIO126_MCAM_PWDN	GPIO126*	B-PD:nppukp	Configurable I/O,main CAM PWDN
80	GPIO129_SCAM_RST_N	GPIO129	B-PD:nppukp	Configurable I/O,front CAM RESET
81	GPIO125_SCAM_PWDN	GPIO125	B-PD:nppukp	Configurable I/O,front CAM PWDN
82	GPIO30_CAM_I2C_SCL0	GPIO30	B-PD:nppukp	Configurable I/O,Dedicated camera I2C0 SCL
83	GPIO29_CAM_I2C_SDA0	GPIO29	B-PD:nppukp	Configurable I/O,Dedicated camera I2C0 SDA
84	GND		GND	GND
85	GND		GND	GND
86	RF_MAIN		AI	RF signal for main ANT
87	GND		GND	GND

88	GND		GND	GND
89	GND		GND	GND
90	GPIO25	GPIO25*	B-PD:nppukp	Configurable I/O
91	GPIO15_SENSOR_I2C4_SCL	GPIO15	B-PD:nppukp	Configurable I/O,SENSOR I2C SCL
92	GPIO14_SENSOR_I2C4_SDA	GPIO14	B-PD:nppukp	Configurable I/O,SENSOR I2C SDA
93	GPIO5_DBG_UART_RX	GPIO5*	B-PD:nppukp	Configurable I/O,UART2 RX
94	GPIO4_DBG_UART_TX	GPIO4	B-PD:nppukp	Configurable I/O,UART2 TX
95	GPIO91_KEY_VOL_UP_N	GPIO91*	B-PD:nppukp	Configurable I/O,KEY VOL+
96	GPIO50_KEY_VOL_DOWN_N	GPIO127*	B-PD:nppukp	Configurable I/O,KEY VOL-
97	GPIO130	GPIO130*	B-PD:nppukp	Configurable I/O
98	GPIO45	GPIO45*	B-PD:nppukp	Configurable I/O
99	GPIO48	GPIO48*	B-PD:nppukp	Configurable I/O
100	GPIO59	GPIO59*	B-PD:nppukp	Configurable I/O
101	GPIO12	GPIO12*	B-PD:nppukp	Configurable I/O
102	GPIO13	GPIO13*	B-PD:nppukp	Configurable I/O
103	GPIO95	GPIO95	B-PD:nppukp	Configurable I/O
104	GPIO94	GPIO94	B-PD:nppukp	Configurable I/O
105	GPIO87	GPIO87	B-PD:nppukp	Configurable I/O, MI2S1 WS
106	GPIO66	GPIO66	B-PD:nppukp	Configurable I/O
107	GPIO43_ALSP_INT_N	GPIO43*	B-PD:nppukp	Configurable I/O,ALSP INT
108	GPIO63_GYRO_INT	GPIO63*	B-PD:nppukp	Configurable I/O, GYRO INT
109	GPIO44_MAG_INT	GPIO44*	B-PD:nppukp	Configurable I/O, MAG INT
110	GPIO42_ACCL_INT_N	GPIO42*	B-PD:nppukp	Configurable I/O, ACCL INT
111	VREG_L5_1P8		PO	PMIC output 1.8V for digital I/Os
112	GPIO93	GPIO93*	B-PD:nppukp	Configurable I/O
113	GPIO46	GPIO46*	B-PD:nppukp	Configurable I/O
114	KYPD_PWR_N		DI	KEY POWER ON/OFF
115	GPIO89	GPIO89	B-PD:nppukp	Configurable I/O
116	GPIO23	GPIO23	B-PD:nppukp	Configurable I/O, SPI CLK
117	GPIO22	GPIO22	B-PD:nppukp	Configurable I/O, SPI CS
118	GPIO21	GPIO21*	B-PD:nppukp	Configurable I/O, SPI MISO
119	GPIO20	GPIO20	B-PD:nppukp	Configurable I/O, SPI MOSI
120	GND		GND	GND
121	RF_GPS		AI	RF signal for GPS ANT
122	GND		GND	GND
123	GPIO62	GPIO62*	B-PD:nppukp	Configurable I/O

124	GPIO47	GPIO47	B-PD:nppukp	Configurable I/O
125	VREG_L6_1P8		PO	PMIC output 1.8V for LCD,CAM,TP,sensor
126	VCOIN		AI,AO	Coin-cell battery or backup battery
127	CHARGE_SEL		AI	Charger select
128	ADC		AO-Z,AI,DO	Configurable MPP,PWM,ADC
129	VREG_L17_2P85		PO	PMIC output 2.8V for LCD,CAM
130	GND		GND	GND
131	RF_DIV		AI	RF signal for diversity ANT
132	GND		GND	GND
133	VBAT_SNS_P		AI	battery voltage input to ADC
134	BATT_THERM		AI	Battery temperature input to ADC
135	GND		GND	GND
136	CDC_HPH_R		AO	Headphone output, right channel
137	CDC_HPH_REF		AI	Headphone ground reference
138	CDC_HPH_L		AO	Headphone output, left channel
139	CDC_HSDET_L		AI	MBHC mechanical insertion/removal-detection
140	GND		GND	GND
141	VBUS		PI,PO	USB Voltage
142	VBUS		PI,PO	USB Voltage
143	GND		GND	GND
144	GND		GND	GND
145	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
146	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
147	MIC_BIAS1		AO	Microphone bias #1
148	MIC_IN3_P		AI	Microphone 3 input plus
149	GND		GND	GND
150	RESERVED			Reserved
151	RESERVED			Reserved
152	RESERVED			Reserved
153	GPIO1_UART1_RXD	GPIO1*	B-PD:nppukp	Configurable I/O,UART1 RX
154	GPIO0_UART1_TXD	GPIO0	B-PD:nppukp	Configurable I/O,UART1 TX
155	MIC_BIAS2		AO	Microphone bias #2
156	VREG_L10_2P8		PO	PMIC output 2.8V for TP, Sensor
157	MIPI_CSI0_CLK_M		AI	MIPI camera serial interface 0 clock-
158	MIPI_CSI0_LANE0_M		AI	MIPI camera serial interface 0 lane0-
159	MIPI_CSI0_LANE1_M		AI	MIPI camera serial interface 0 lane1-

160	MIPI_CSI0_LANE2_M		AI	MIPI camera serial interface 0 lane2-
161	MIPI_CSI0_LANE3_M		AI	MIPI camera serial interface 0 lane3-
162	GND		GND	GND
163	GPIO41_DCAM_PWDN	GPIO41*	B-PD:nppukp	Configurable I/O, depth CAM PWDN
164	GPIO38_DCAM_RST	GPIO38*	B-PD:nppukp	Configurable I/O, depth CAM RESET
165	GPIO27_DCAM_MCLK	GPIO27	B-PD:nppukp	Configurable I/O, depth CAM MCLK
166	GPIO32_DCAM_I2C_SCL1	GPIO32	B-PD:nppukp	Configurable I/O, Dedicated camera I2C1 SCL
167	GPIO6	GPIO6	B-PD:nppukp	Configurable I/O, I2C2 SDA
168	GPIO7	GPIO7	B-PD:nppukp	Configurable I/O, I2C2 SCL
169	GPIO127	GPIO127*	B-PD:nppukp	Configurable I/O
170	GPIO34	GPIO34*	B-PD:nppukp	Configurable I/O
171	GND		GND	GND
172	GND		GND	GND
173	RESERVED			Reserved
174	RESERVED			Reserved
175	RESERVED			Reserved
176	GND		GND	GND
177	GPIO90	GPIO90*	B-PD:nppukp	Configurable I/O
178	RESERVED			Reserved
179	RESERVED			Reserved
180	RESERVED			Reserved
181	NFC_CLK		DO	NFC CLK
182	NFC_CLK_REQ		DO-Z,DI	Configurable I/O, NFC CLK REQ
183	RESERVED			Reserved
184	RESERVED			Reserved
185	BAT_ID		DI	Battery ID
186	CBL_PWR_N		DI	Cable power-on
187	GND		GND	GND
188	GND		GND	GND
189	GND		GND	GND
190	GND		GND	GND
191	GND		GND	GND
192	RESERVED			Reserved
193	VREG_L16_AVDD		PO	PMIC output 2.8V for CAM AVDD
194	GNSS_LNA_EN	GPIO118	B-PD:nppukp	Configurable I/O, GNSS_LNA_EN
195	CHG_LED		AO	Current sink for charging indication

196	MIPI_CSI0_CLK_P		AI	MIPI camera serial interface 0 clock+
197	MIPI_CSI0_LANE0_P		AI	MIPI camera serial interface 0 lane0+
198	MIPI_CSI0_LANE1_P		AI	MIPI camera serial interface 0 lane1+
199	MIPI_CSI0_LANE2_P		AI	MIPI camera serial interface 0 lane2+
200	MIPI_CSI0_LANE3_P		AI	MIPI camera serial interface 0 lane3+
201	GPIO39	GPIO39	B-PD:nppukp	Configurable I/O
202	GND		GND	GND
203	GND		GND	GND
204	GND		GND	GND
205	GPIO31_DCAM_I2C_SDA1	GPIO31*	B-PD:nppukp	Configurable I/O, Dedicated camera I2C1 SDA
206	GND		GND	GND
207	GND		GND	GND
208	GND		GND	GND
209	GND		GND	GND
210	GND		GND	GND
211	GND		GND	GND
212	GND		GND	GND
213	GND		GND	GND
214	GND		GND	GND
215	GND		GND	GND
216	GND		GND	GND
217	GND		GND	GND
218	GND		GND	GND
219	GND		GND	GND
220	GND		GND	GND
221	GND		GND	GND
222	GND		GND	GND
223	GND		GND	GND
224	GND		GND	GND
225	RESET_N		DI	KEY RESET
226	GND		GND	GND
227	GND		GND	GND
228	GND		GND	GND
229	GND		GND	GND
230	GND		GND	GND
231	GND		GND	GND

232	RESERVED			Reserved
233	GND		GND	GND
234	GND		GND	GND
235	GND		GND	GND
236	GND		GND	GND
237	GND		GND	GND
238	GND		GND	GND
239	GPIO86	GPIO86*	B-PD:nppukp	Configurable I/O,MI2S1 D1
240	GND		GND	GND
241	GND		GND	GND
242	RESERVED			Reserved
243	GND		GND	GND
244	GND		GND	GND
245	GND		GND	GND
246	RESERVED			Reserved
247	GND		GND	GND
248	GND		GND	GND
249	RESERVED			Reserved
250	GND		GND	GND
251	GND		GND	GND
252	RESERVED			Reserved
253	RESERVED			Reserved
254	RESERVED			Reserved
255	GND		GND	GND
256	GND		GND	GND
257	RESERVED			Reserved
258	GND		GND	GND
259	GND		GND	GND
260	GPIO104_RFFE3_CLK	GPIO104	B-PD:nppukp	Configurable I/O,RFFE3 CLK
261	GND		GND	GND
262	GPIO106_RFFE3_DATA	GPIO106	B-PD:nppukp	Configurable I/O,RFFE3 DATA
263	RESERVED			Reserved
264	GPIO88	GPIO88	B-PD:nppukp	Configurable I/O, MI2S1 D0
265	GPIO85	GPIO85	B-PD:nppukp	Configurable I/O, MI2S1 SCK
266	GND		GND	GND
267	GPIO61	GPIO61*	B-PD:nppukp	Configurable I/O

268	GND		GND	GND
269	GND		GND	GND
270	RESERVED			Reserved
271	GND		GND	GND
272	GND		GND	GND
273	GND		GND	GND
274	GND		GND	GND

*：Wake-up system interrupt pin

B：Bidirectionaldigital with CMOS input

H：High-voltage tolerant

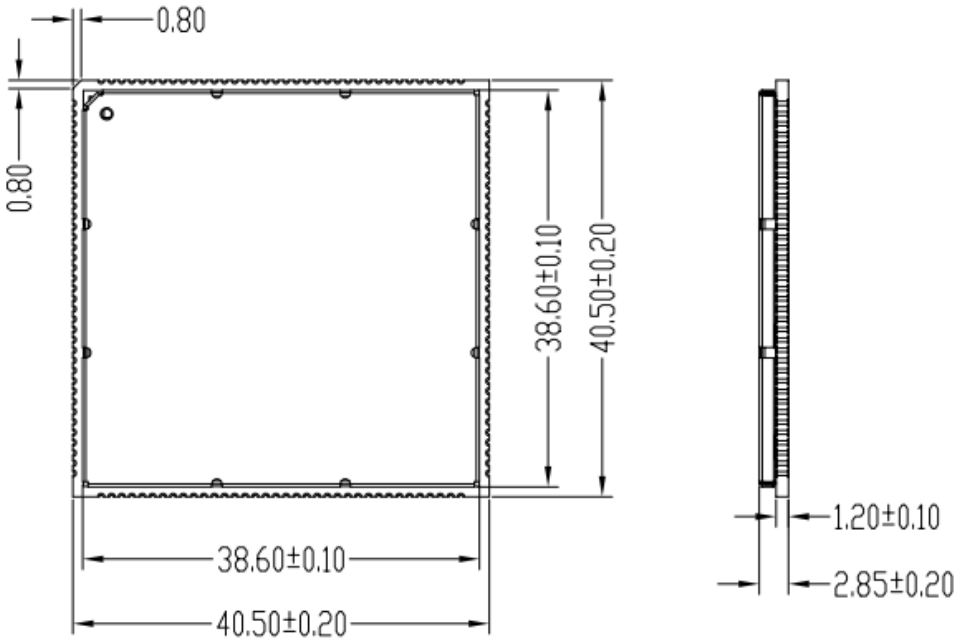
NP：pdpukp=defaultno-pull with programmable options following the colon (:)

PD：nppukp=defaultpulldown with programmable options following the colon (:)

PU：nppdkp=defaultpullup with programmable options following the colon (:)

KP：nppdpu=defaultkeeper with programmable options following the colon (:)

3.3. Mechanical Dimensions



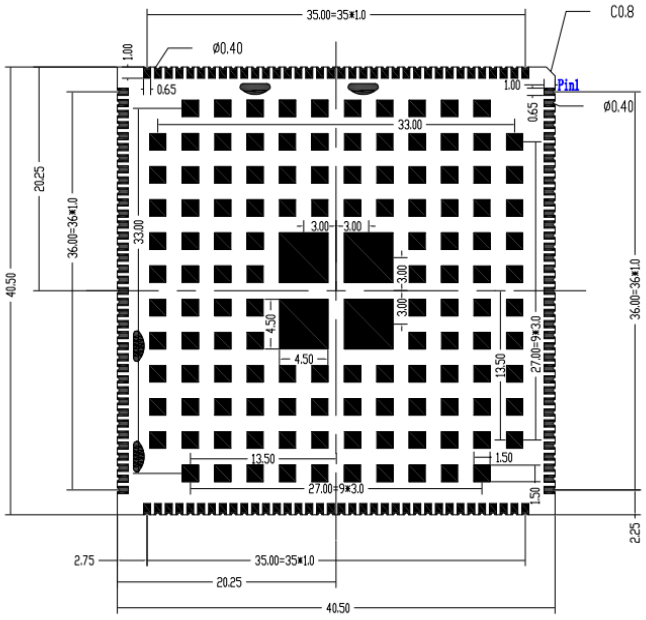


Figure 3.2：Module 3D size（unit： mm）

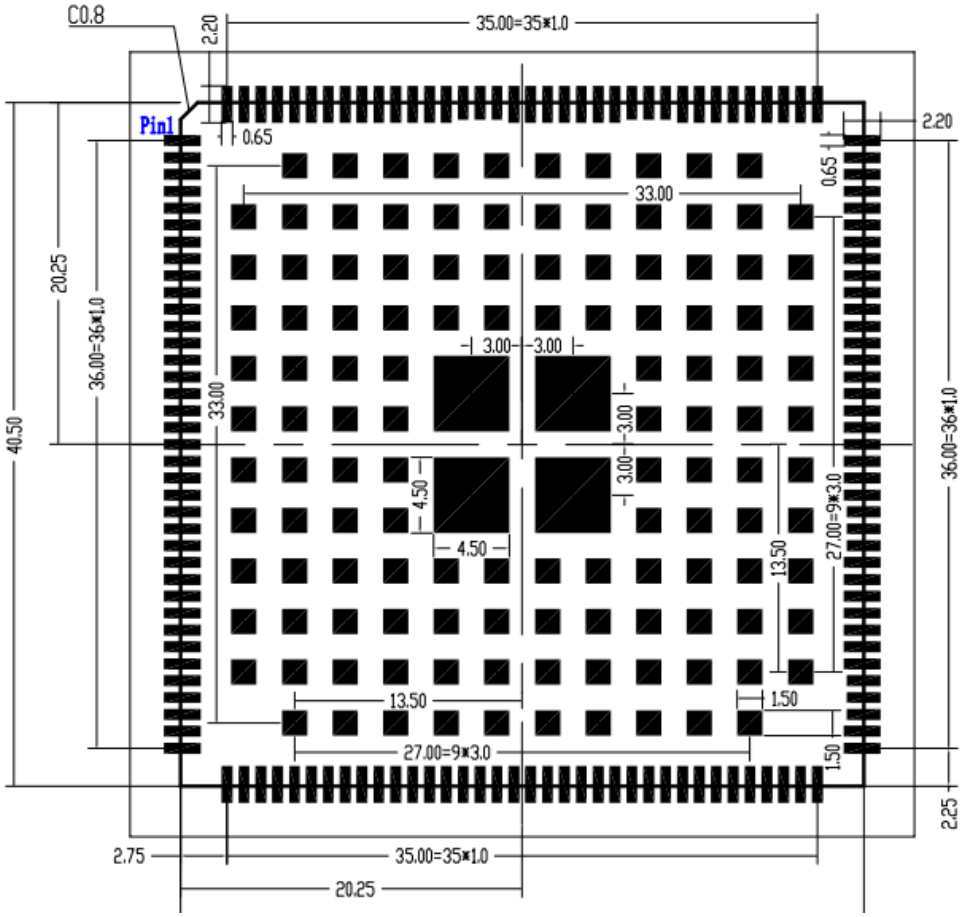


Figure 3.3：Recommended PCB package size（unit： mm）

3. Interface application

4.1. Power Supply

In the case of a battery device, the voltage input range of the module VBAT is 3.4V to 4.2V, and the recommended voltage is 3.8V. In the GSM band, when the module is transmitting at maximum power, the peak current can reach up to 3A, resulting in a large voltage drop on VBAT.

It is recommended to use a large capacitor regulator close to VBAT. It is recommended to use two 47uF ceramic capacitors. Parallel 33PF and 10PF capacitors can effectively remove high frequency interference. To prevent damage to the chip due to ESD and surge, it is recommended to use a suitable TVS tube and a 5.1V/500mW Zener diode at the VBAT pin of the module. For PCB layout, the capacitors and diodes should be as close as possible to the VBAT pin of the module. The user can directly power the module with a 3.7V lithium-ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

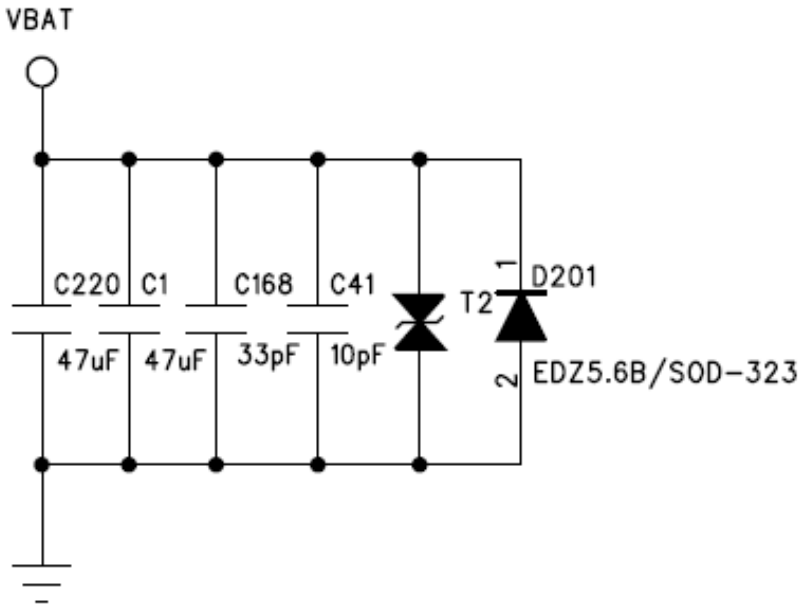


Figure 4.1： VBAT input reference circuit

If it is a DC power supply device, the DC input voltage is 5V-12V. The recommended circuit that can be powered by DC-DC is shown below:

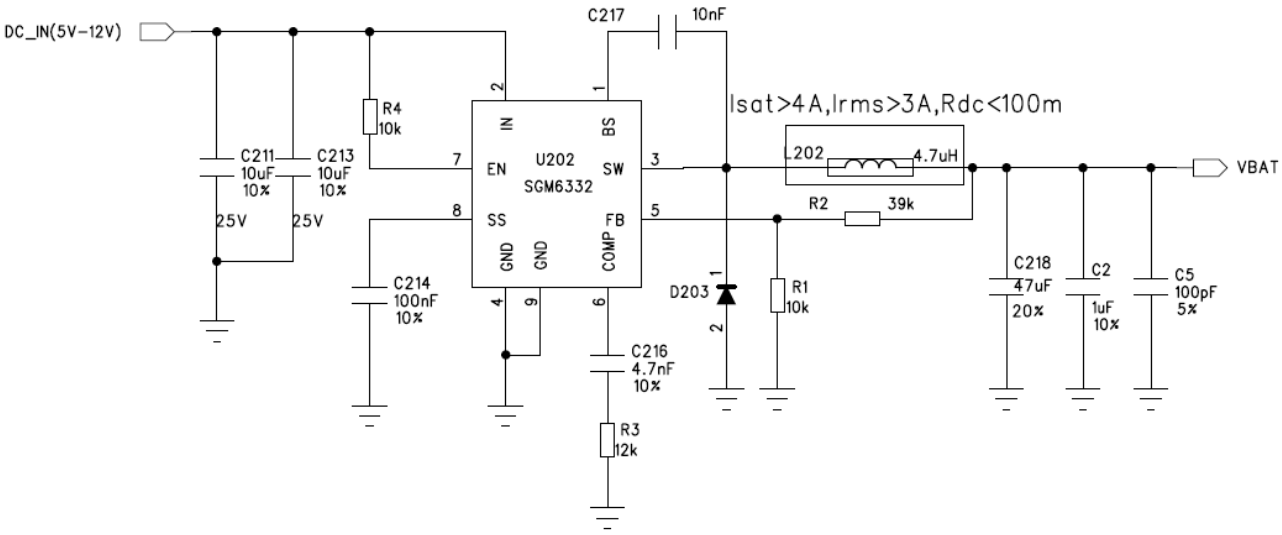


Figure 4.2：DC-DC power supply circuit

Note：If the user does not use battery power, please note that a 47K resistor is connected to the 134 pin (BAT_THERM) of the module and pulled down to GND to prevent the software from judging the abnormal battery temperature after the module is turned on, resulting in shutdown. The connection diagram is as follows:

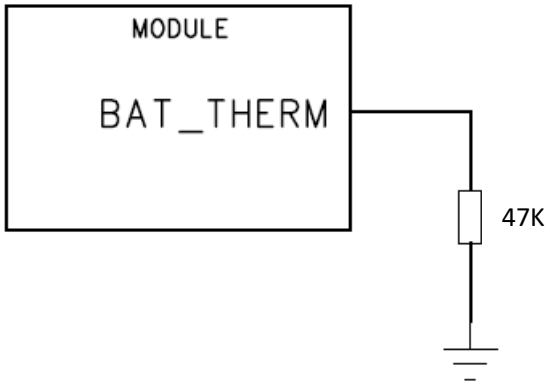


Figure 4.3：Connection diagram when not powered by battery

4.1.1. Power Pin

The VBAT pin (1、2、145、146) is used for power input. In the user's design, pay special attention to the design of the power supply section to ensure that the VBAT does not fall below 3.4V even when the module consumes 2A. If the voltage drops below 3.4V, the module may shut down. The PCB layout from the VBAT pin to the power supply should be wide enough to reduce the voltage drop in the transmit burst mode.

Figure4.4：VBAT lowest voltage drop

4.2. Power on and off

Do not turn on the module when the module's temperature and voltage limits are exceeded. In extreme cases, such operations can cause permanent damage to the module.

4.2.1. Module Boot

The user can power on the module by pulling the KYPD_PWR_N pin (114) low. The pull-down time is at least 5 seconds. This pin has been pulled up to 1.8V in the module. The recommended circuit is as follows; or the CBL_PWR_N pin (186) is pulled low. CBL_PWR_N can be powered on by 10K pull-down resistor to GND. It does not need to release this signal after booting.

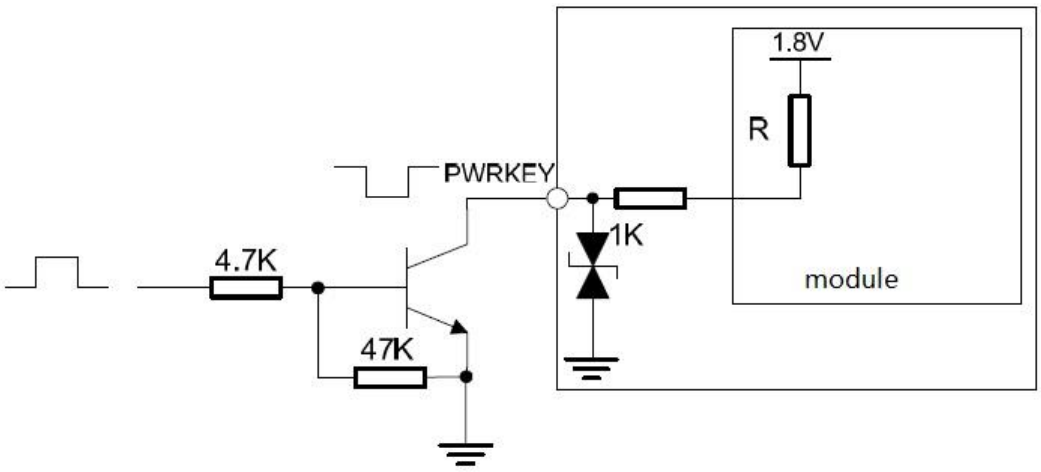


Figure 4.5：Using an external signal to drive the module to boot

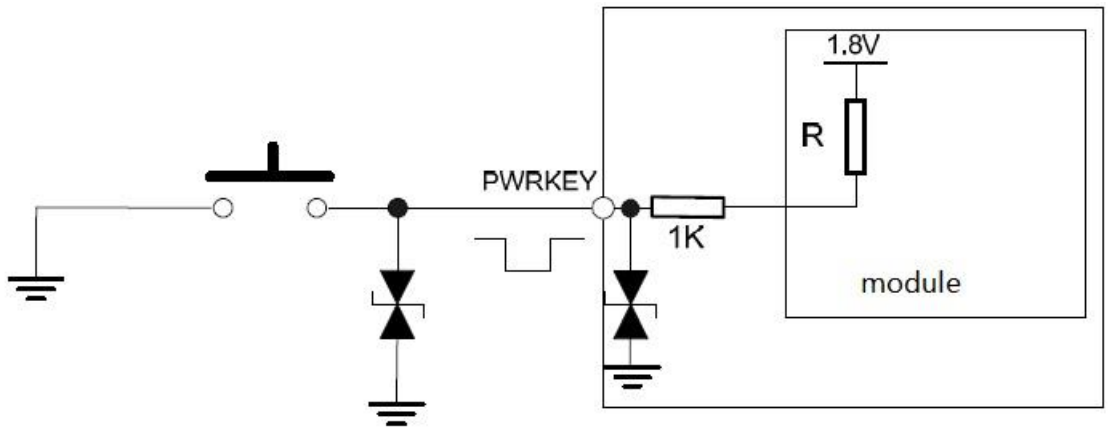


Figure 4.6：Booting with the button circuit

The following figure is the boot timing description:

Order	SMPS/LDO
1	VREG_S4A
2	VREG_S3A
3	VREG_L2A
4	VREG_S1A
5	VREG_S2A
6	VDD_PX_BIAS
7	VREG_L5A
8	eLDO3
9	eLDO1
10	VREG_L7A
11	VREG_L6A
12	VREG_L13A
13	VREG_L8A
14	VREG_L12A
15	VREG_L11A

Figure 4.7：Using PWRKEY boot timing diagram

4.2.2. Module Shutdown

Users can use the PWRKEY pin to shutdown.

4.2.2.1 PWRKEY Shutdown

The user can turn off the PWRKEY signal by pulling it down for at least 3 seconds. The shutdown circuit can refer to the design of the boot circuit. After the module detects the shutdown action, a prompt window pops up on the screen to confirm whether to perform the shutdown action.

The user can achieve a forced shutdown by pulling PWRKEY down for a long time, pulling down for at least 15 seconds.

4.2.3.Module Reset

The SLM500 module supports a reset function that allows the user to quickly restart the module by pulling the RESET_N pin（225） of the module low. The recommended circuit is as follows:

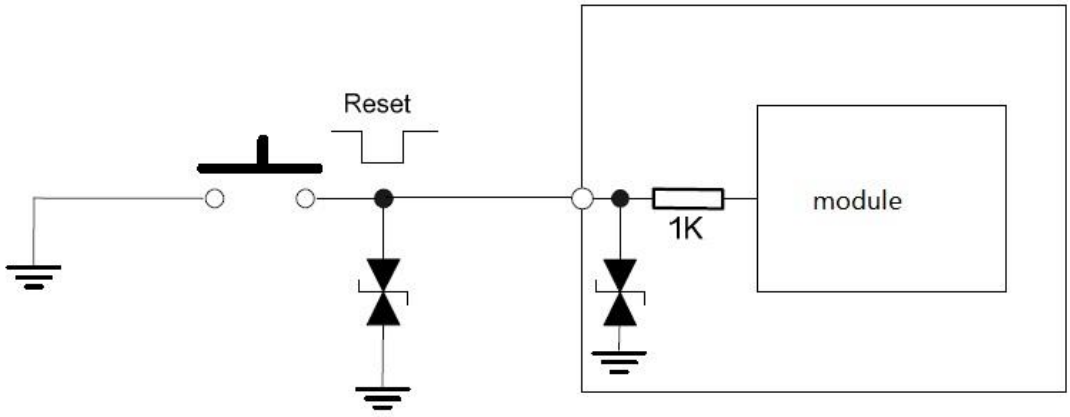


Figure 4.8：Reset using the key circuit

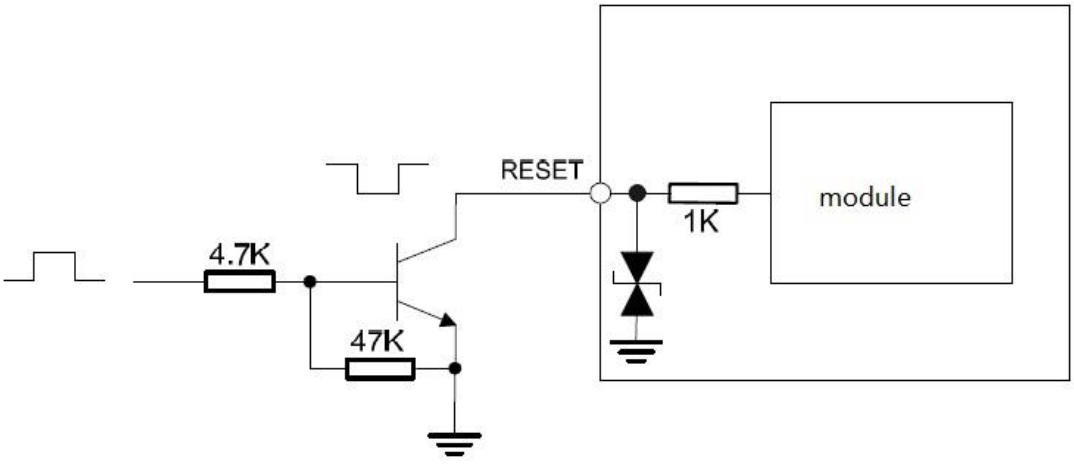


Figure 4.9： Reset Module Using External Signal

When the pin is high, the voltage is typically 1.8V. Therefore, for users with a level of 3V or 3.3V, it is not possible to directly use the GPIO of the MCU to drive the pin. An isolation circuit is required. The hardware parameters of the RESET(225) can refer to the following table:

Table 4.1：RESET Hardware Parameters

Pin	Description	Minimum	Typical	Maximum	Unit
RESET_N	Input high level	1	-	-	V
	Input low level	-	-	0.65	V
	Pull down effective time	500		-	ms

4.3. VCOIN Power

When VBAT is disconnected, the user needs to save the real-time clock. The VCOIN pin cannot be left floating. It should be connected to a large capacitor or battery. When external capacitor is connected, the recommended value is 100uF, and the real-time clock can be kept for 1 minute. The reference design circuit is used when the RTC power supply uses an external large capacitor or battery to power the RTC inside the module:

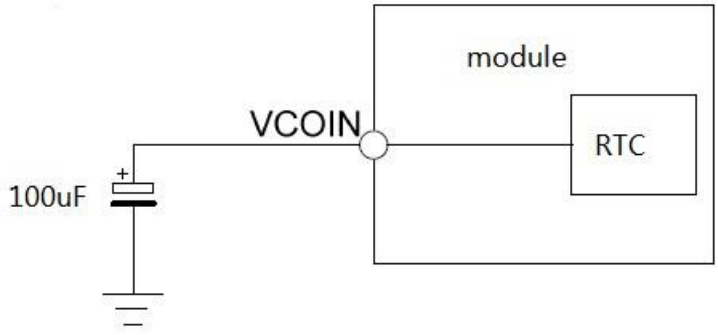


Figure 4.10：External Capacitor Powering the RTC

Non-rechargeable battery powered:

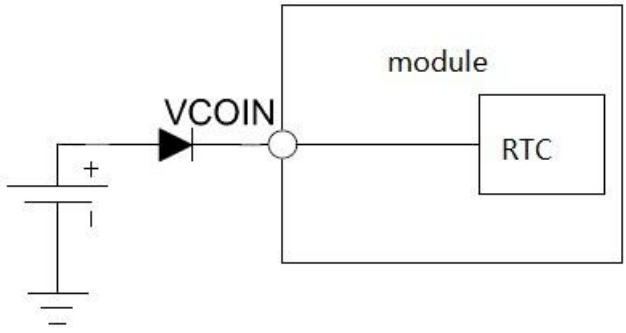


Figure 4.11：Non-rechargeable battery to power the RTC

Rechargeable battery powered:

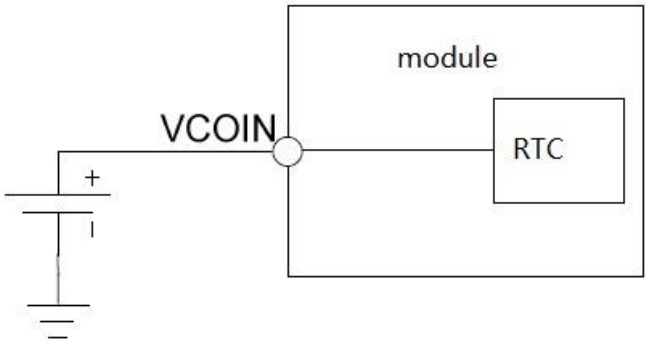


Figure 4.12： Rechargeable Battery Powers RTC

Notes：This VCOIN power supply is 2.0-3.25V, typical typically 3.0V

4.4. Power Output

The SLM500 has multiple power outputs. For LCD, Camera, touch panel, etc. In application, it is recommended to add parallel 33PF and 10PF capacitors to each power supply to effectively remove high frequency interference.

Table 4.2：Power Description

Signal	Default Voltage(V)	Drive Current(mA)
VREG_L5_1P8	1.8	100
VREG_L6_1P8	1.8	100
VREG_L10_2P8	2.8	150
VREG_L11_SDC	2.95	600
VREG_L12_SDC	2.95	50
VREG_L14_UIM1	1.8/2.95	55
VREG_L15_UIM2	1.8/2.95	55
VREG_L16_AVDD	2.8	55
VREG_L17_2P85	2.85	300

4.5. Serial Port

The SLM500 provides three serial ports for communication. And corresponding to one groups of I2C interfaces can be multiplexed into hardware flow control, note that the I2C interface can not be added to the UART_RTS/CTS when the pull resistor can be added.

Table 4.3：UART Pin Description

Name	Pin	Direction	Function
GPIO0_UART1_TXD	154	I	UART1 Data Transmission

GPIO1_UART1_RXD	153	O	UART1 Data Reception
GPIO4_DBG_UART_TX	94	I	UART2 Data Transmission
GPIO5_DBG_UART_RX	93	O	UART2 Data Reception
GPIO16_UART5_TXD	34	I	UART5 Data Transmission
GPIO17_UART5_RXD	35	O	UART5 Data Reception
GPIO18_UART5_CTS	36	I	UART5 Clear To Send（CTS）
GPIO19_UART5_RTS	37	O	UART5 Request To Send（RTS）

Please refer to the following connection method:

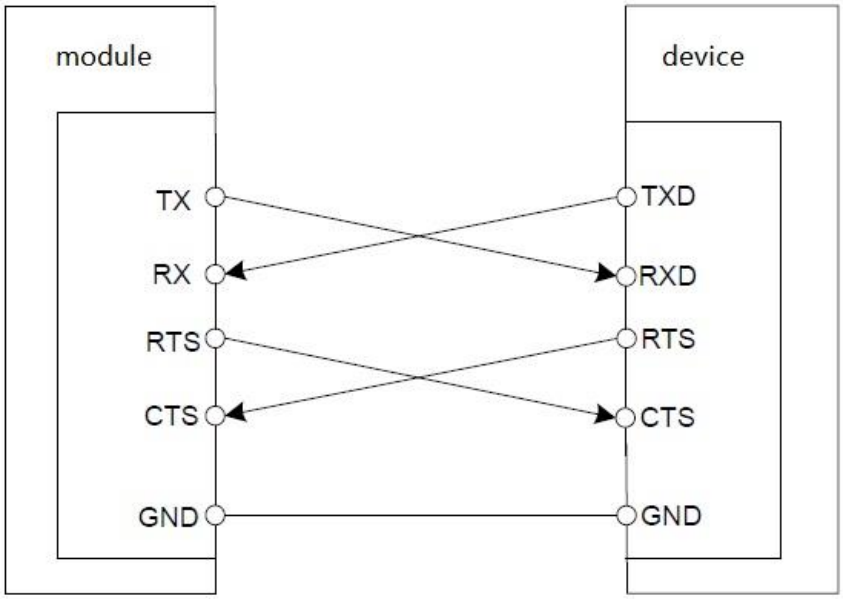


Figure 4.13：Serial Port Connection Diagram

When the serial level used by the user does not match the module, in addition to adding the level shifting IC, the following figure can also be used to achieve level matching. Only the matching circuits on TX and RX are listed here. Other low speed signals can refer to this two circuits.

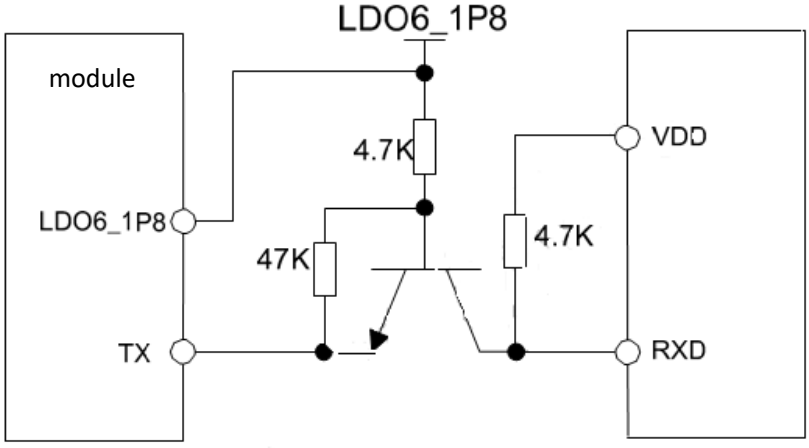


Figure 4.14：TX Connection Diagram

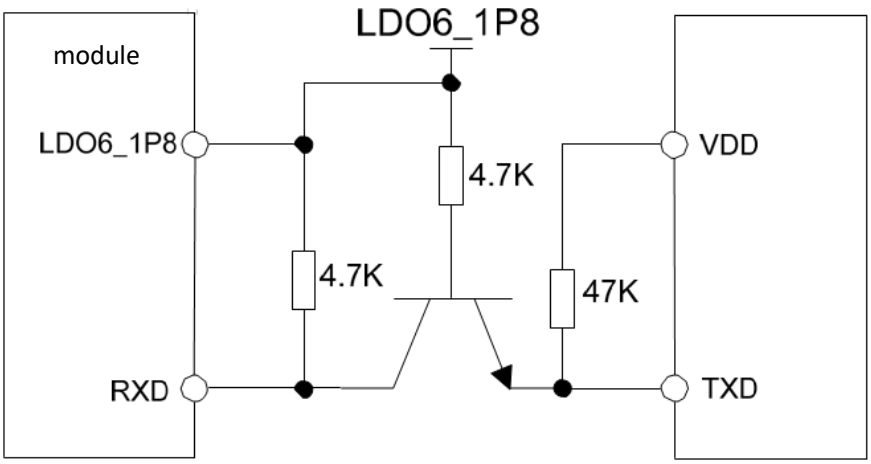


Figure 4.15：RX Connection Diagram

Note：When using Levels Isolation in Figures 14 and 15, Attention should be paid to LDO6_1P8 output timing, the serial port can communicate normally after the normal output.

Table 4.4：Serial Port Hardware Parameters

Description	Minimum	Maximum	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Input low level	-	0.45	V
Input high level	1.35	-	V

Note：1. The serial port of the module is a CMOS interface, and the RS232 signal cannot be directly connected. If necessary, please use the RS232 conversion chip.

2. If the 1.8V output of the module cannot meet the high level range of the user terminal, please add a level shifting circuit.

4.6. MIPI Interface

The SLM500 supports the Moble Industry Processor Interface (MIPI) interface for Camera and LCD. The module supports HD+(1440*720)display. The MIPI interface Main Camera supports up to 13MP, and the Front Camera supports 5MP.

MIPI is a high-speed signal line. In the Layout stage, please follow the impedance and length requirements strictly, and control the length of the differential pair within the group and the group length. The total length should be as short as possible.

4.6.1. LCD Interface

The SLM500 module supports the MIPI interface of one LCD displays, supports dual-screen display, and has a compatible screen identification signal. The resolution of the screen can be up to 1440*720. The signal interface is shown in the following table. In the Layout, the MIPI signal line should strictly control the differential 100 ohm impedance and the equal length between the signal line group and the group.

The module's MIPI interface is a 1.2V power domain. When the user needs a compatible screen design, the module's LCD_ID pin or ADC pin can be used. At the same time, the module can provide 2.8V power to the LCD. The LCD interface is as follows:

Table 4.5：Primary screen interface definition

Main screen interface			
MIPI_DSI0_CLK_M	52	O	MIPI_LCD clock line
MIPI_DSI0_CLK_P	53	O	
MIPI_DSI0_LANE0_M	54	I/O	MIPI_LCD data line
MIPI_DSI0_LANE0_P	55	I/O	
MIPI_DSI0_LANE1_M	56	I/O	
MIPI_DSI0_LANE1_P	57	I/O	
MIPI_DSI0_LANE3_M	60	I/O	
MIPI_DSI0_LANE3_P	61	I/O	
MIPI_DSI0_LANE2_M	58	I/O	
MIPI_DSI0_LANE2_P	59	I/O	
GPIO60_LCD_RESET_N	49	O	LCD reset pin
GPIO24_LCD_TE0	50	I/O	LCD frame sync signal
VREG_L6_1P8	125	O	1.8V power supply
VREG_L17_2P85	129	O	2.8V power supply

LCD_ID of the module, this pin is internally GPIO. When used as LCD_ID, please confirm the internal circuit of LCD. If the internal divider of the LCD uses resistor divider, please pay attention to the voltage to meet the high or low range of GPIO.

MIPI is a high-speed signal line. To avoid EMI interference, it is recommended to place a common-mode inductor near the LCD side.

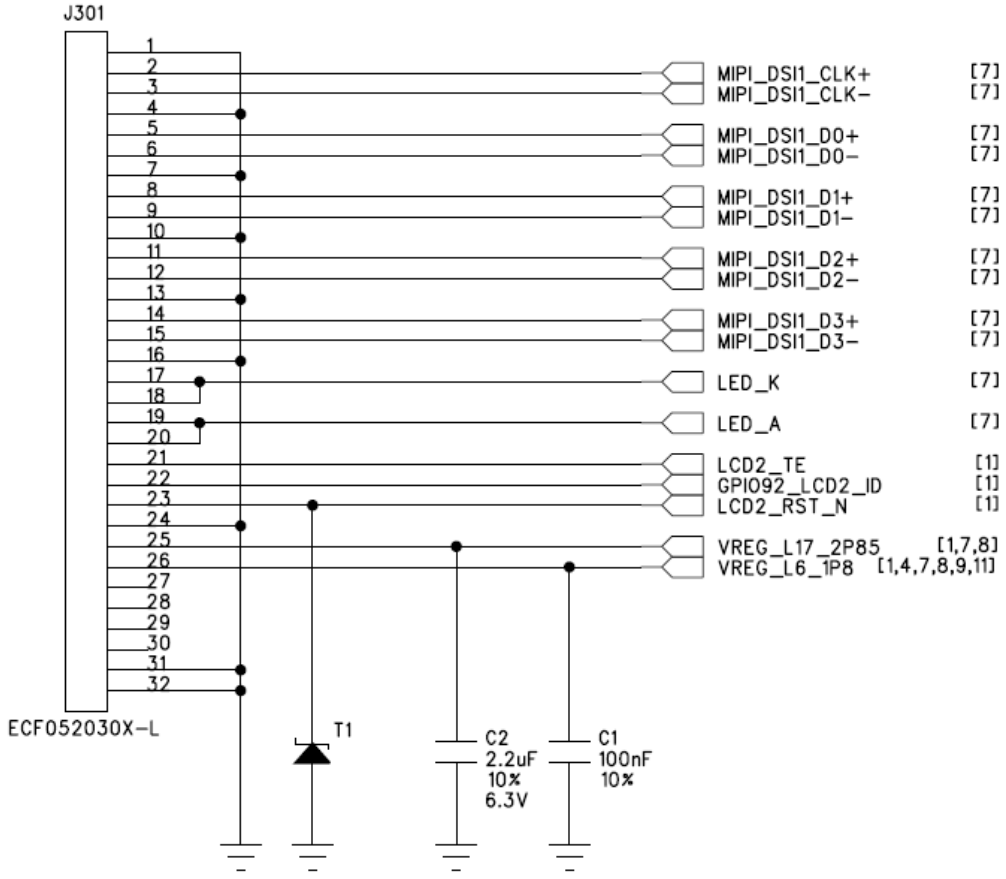


Figure 4.16： LCD interface circuit

PMIC does not support backlight drive. LCD backlight driver circuit needs to be added by customers. Please refer to the following figure for specific circuit

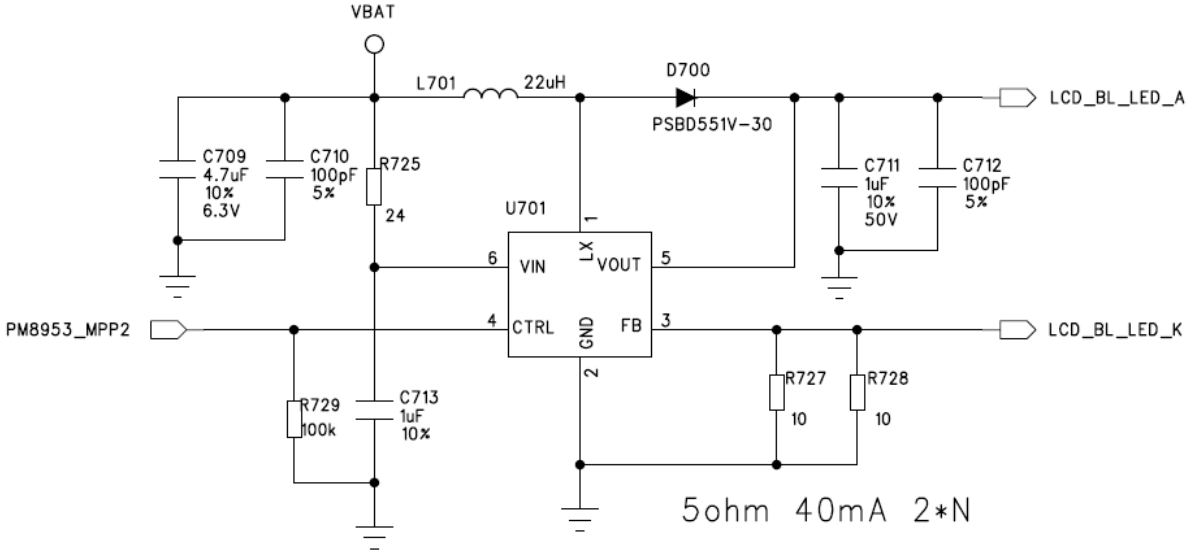


Figure 4.17： Backlight drive schematic

4.6.2.MIPI Camera Interface

The SLM500 module supports the MIPI interface Camera and provides a dedicated camera power supply. The main camera is a CSI1 interface that supports four sets of data lines and can support up to 13M pixels. The front camera is a CSI0 interface that supports four sets of data lines and can support 5M pixels. The module provides the power required by the Camera, including AVDD-2.8V, IOVDD-1.8V\AFVDD-2.8V (powered by the focus motor) and D-VDD1.2V (CAM core voltage). D-VDD1.2V(CAM Core Votage) Please add external circuit by yourself。

Table 4.6：MIPI Camera Interface Definition

Main camera interface			
Name	Name	Name	Name
GPIO26_MCAM_MCLK0	74	O	Main camera clock signal
GPIO128_MCAM_RST_N	79	O	Main camera reset signal
GPIO126_MCAM_PWDN	80	O	Main camera sleep signal
MIPI_CSI1_CLK_M	63	I	Main camera MIPI clock signal
MIPI_CSI1_CLK_P	64	I	
MIPI_CSI1_LANE0_M	65	I/O	Main camera MIPI data signal
MIPI_CSI1_LANE0_P	66	I/O	
MIPI_CSI1_LANE1_M	67	I/O	
MIPI_CSI1_LANE1_P	68	I/O	
MIPI_CSI1_LANE2_M	72	I/O	
MIPI_CSI1_LANE2_P	73	I/O	
MIPI_CSI1_LANE3_M	70	I/O	
MIPI_CSI1_LANE3_P	71	I/O	
GPIO29_CAM_I2C_SDA0	84	I/O	I2C data
GPIO30_CAM_I2C_SCL0	83	I/O	I2C clock
VREG_L6_1P8	125	O	1.8V IOVDD
VREG_L16_AVDD	193	O	2.8V AVDD
VREG_L17_2P85	129	O	2.8V AFVDD

Front camera interface			
Name	Name	Name	Name
GPIO28_SCAM_MCLK2	75	O	Front camera clock signal
GPIO129_SCAM_RST_N	81	O	Front camera reset signal
GPIO125_SCAM_PWDN	82	O	Front camera sleep signal
MIPI_CSI0_CLK_M	157	I	Front camera MIPI clock signal

MIPI_CSI0_CLK_P	196	I	
MIPI_CSI0_LANE0_M	158	I/O	Front camera MIPI data signal
MIPI_CSI0_LANE0_P	197	I/O	
MIPI_CSI0_LANE1_M	159	I/O	
MIPI_CSI0_LANE1_P	198	I/O	
MIPI_CSI0_LANE2_M	160	I/O	
MIPI_CSI0_LANE2_P	199	I/O	
MIPI_CSI0_LANE3_M	161	I/O	
MIPI_CSI0_LANE3_P	200	I/O	
GPIO29_CAM_I2C_SDA0	84	I/O	I2C data
GPIO30_CAM_I2C_SCL0	83	I/O	I2C clock
VREG_L6_1P8	125	O	1.8V IOVDD
VREG_L16_AVDD	193	O	2.8VAVDD
VREG_L17_2P85	129	O	2.8V AFVDD

If the user designs to use the CAMERA module with autofocus function, please note that the I2C of the module cannot be directly connected to the AF device. The I2C of the AF device should be connected to the driver chip of CAMERA, and the correct connection is as follows:

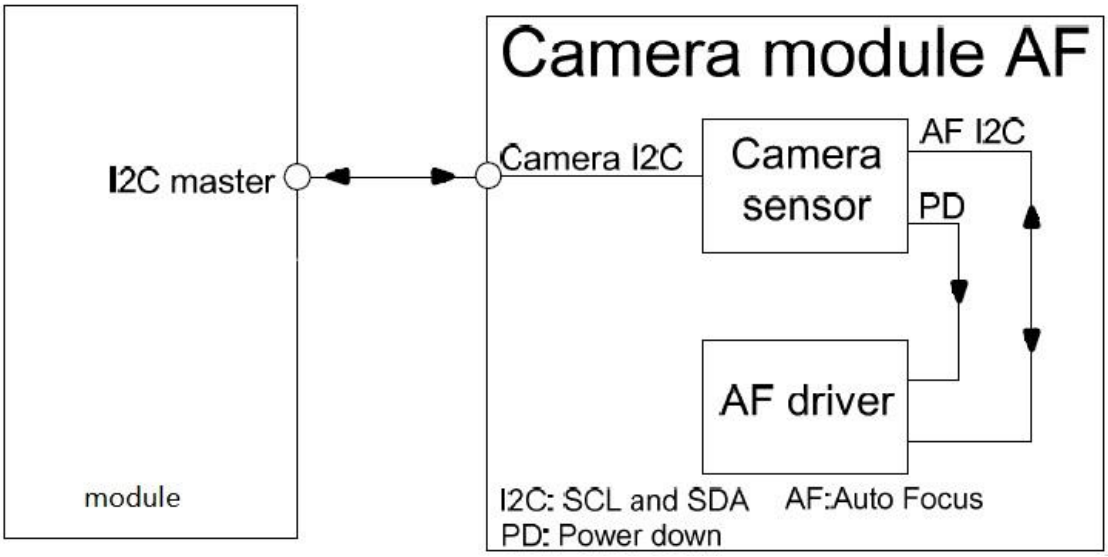


Figure 4.18： Correct CAMERA connection diagram

The MIPI interface has a high rate. The user should control the impedance by 100 ohms during the routing. Please pay attention to the length of the trace. It is not recommended to add a small capacitor on the MIPI signal line. This may affect the rising edge of the MIPI data. This in turn causes the MIPI data to be invalid.

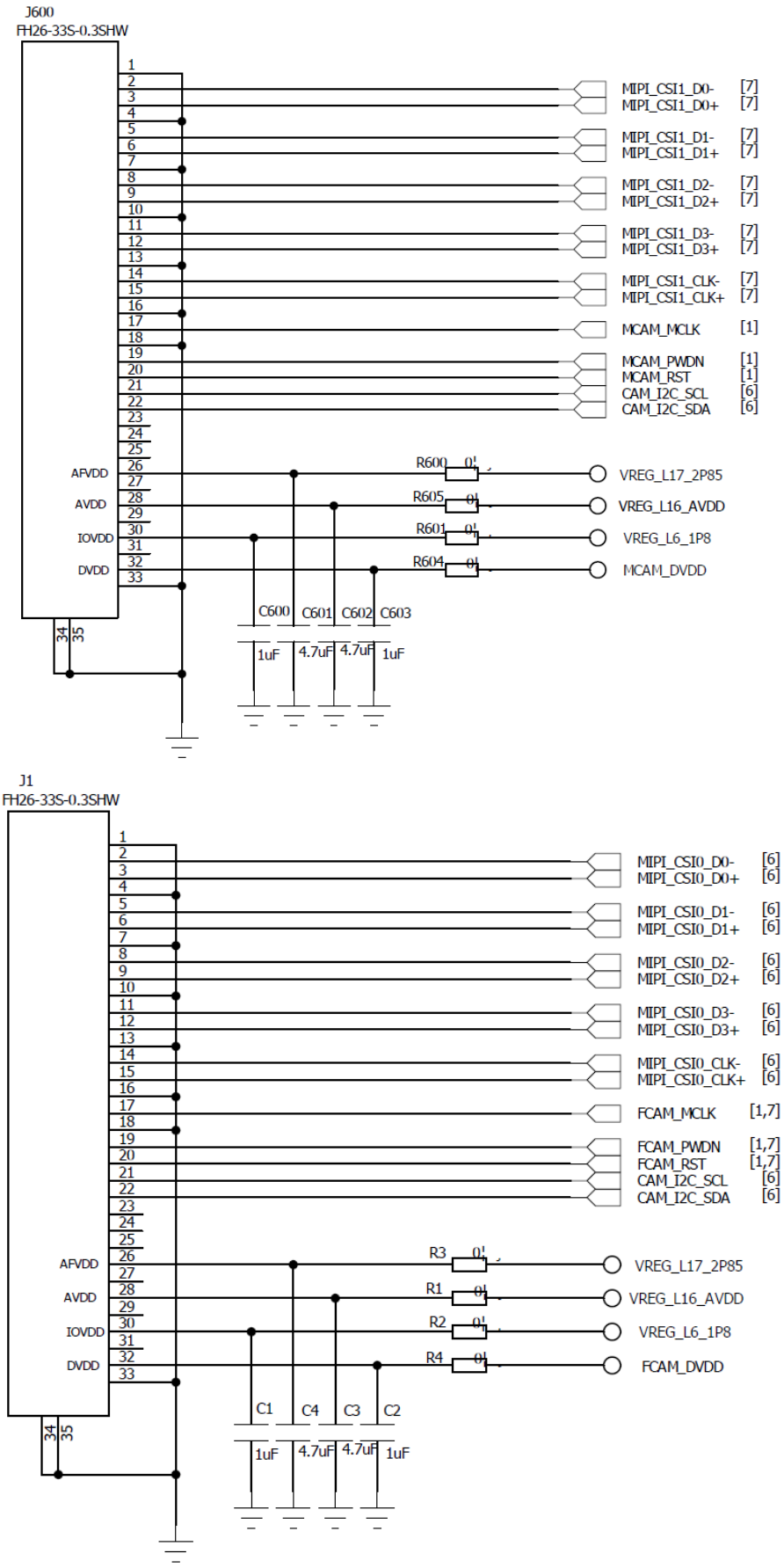


Figure 4.19： MIPI Camera Reference Circuit

Important note: When designing the camera function, you need to pay attention to the position of the connector. There will be a small person in the specification of the camera to indicate the imaging direction. You need to ensure that the villain is standing on the long side of the LCD, otherwise the camera will be flipped. The software cannot be adjusted at 90°. As shown in the two figures below.

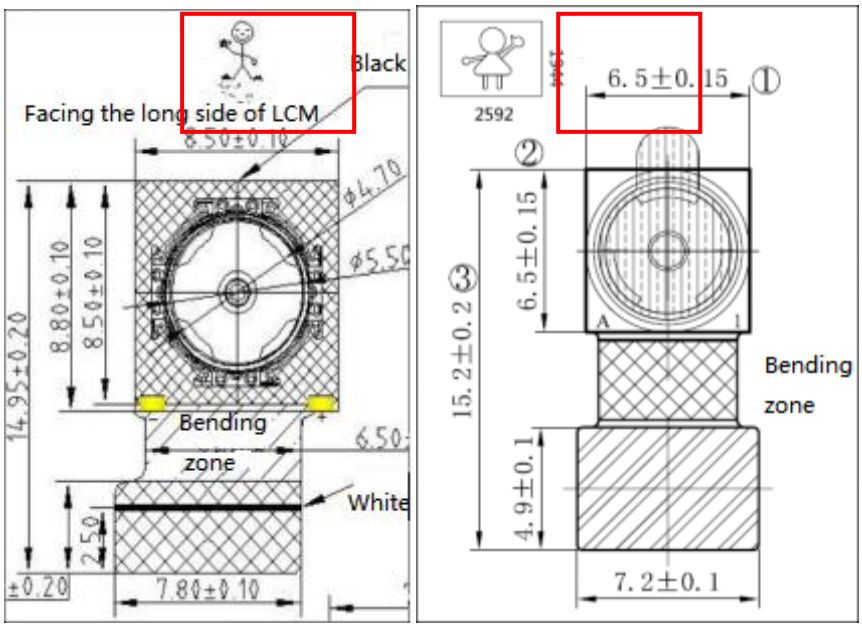


Figure 4.20: Camera imaging diagram

4.7.CapacitiveTouch Interface

The module provides a set of I2C interfaces that can be used to connect capacitive touches while providing the required power and interrupt pins. The default interface pins for capacitive touch software are defined as follows:

Table 4.7: Capacitive Touch Interface Definitions

Name	Pin	Input/Output	Description
GPIO10_TP_I2C3_SDA	48	I/O	The capacitive touch I2C interface needs to be pulled up toVREG_L5_1P8
GPIO11_TP_I2C3_SCL	47	I/O	
GPIO65_TP_INT_N	30	I	TP Interrupt
GPIO64_TP_RESET_N	31	O	TP Reset
VREG_L6_1P8	125	O	1.8V Power supply to TP I/O
VREG_L10_2P8	156	O	2.8V Power supply to TP VDD

Note: The interface definition of the capacitive touch can be adjusted by software, and the user can change the GPIO and I2C according to the design needs.

4.8.Audio Interface

The module provides three analog audio inputs, MIC_IN1_P for the main microphone, MIC_IN2_P for the microphone, and MIC_IN3_P for the noise reduction microphone. The module also provides three analog audio outputs (HPH_L/R, REC_P/N, SPK_P/N). The audio pin is defined as follows:

Table 4.8：Audio Pin Definitions

Name	Pin	Input/Ou	Description
MIC_IN1_P	4	I	Main MIC positive
MIC_IN2_P	6	I	Headphone MIC positive
MIC_GND	5	I	Headphone MIC, Headphone MIC，noise reduction MIC negative
MIC_IN3_P	148	I	Noise reduction MIC positive
MIC_BIAS1	147	O	BIAS voltage of the main MIC for
MIC_BIAS2	155	O	BIAS voltage of the headphone MIC
CDC_HPH_R	136	O	Headphone right channel
CDC_HPH_L	138	O	Headphone left channel
CDC_HSDET_L	139	I	Headphone plug detection
CDC_HPH_REF	137	I	Headphone reference ground
EAR_M	9	O	Earpiece output negative
EAR_P	8	O	Earpiece output positive
SPKR_OUT_M	11	O	Amplifier (0.7W) output negative
SPKR_OUT_P	10	O	Amplifier (0.7W) output positive

Users are advised to use the following circuit according to the actual application to get better sound effects.

4.8.1Receiver Interface Circuit

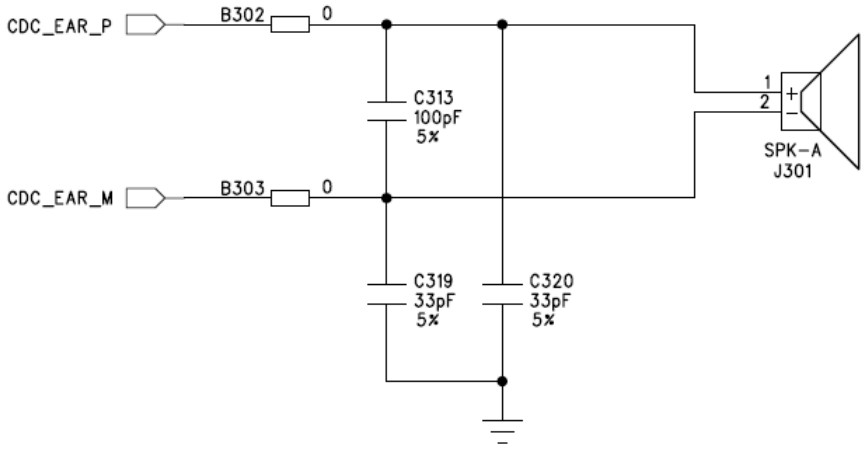


Figure 4.21： Receiver Interface Circuit

4.8.2 Microphone receiving Circuit

The figure below shows the interface circuit of MEMS microphone.

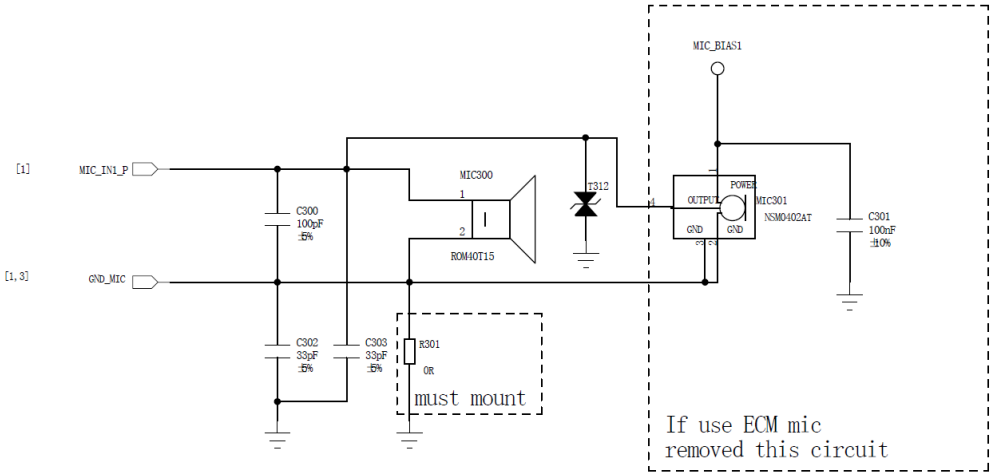


Figure 4.22： Microphone Differential Interface Circuit

4.8.3.Headphone Interface Circuit

The module integrates a stereo headphone jack. Users are advised to reserve ESD devices during the design phase to prevent ESD damage. The HS_DET pin of the module can be set as an interrupt. In software, this pin is the earphone interrupt by default. The user can use this pin to detect the plugging and unplugging of the earphone.

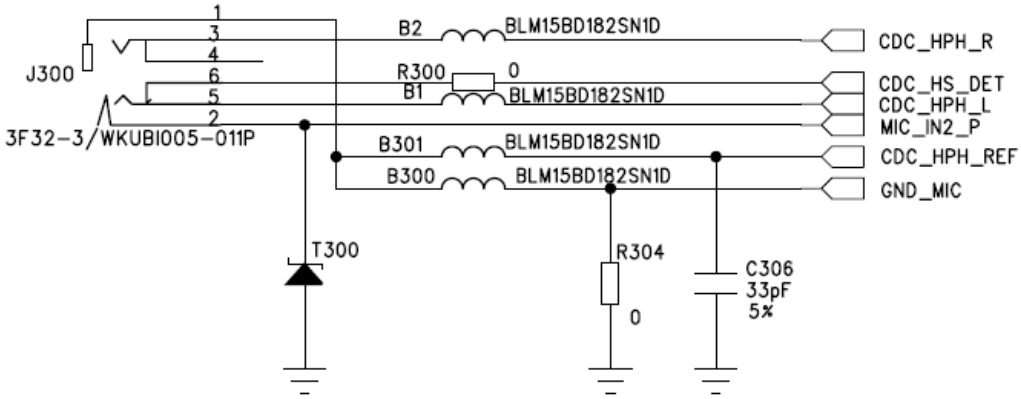


Figure 4.23：Headphone Interface Circuit

Note:

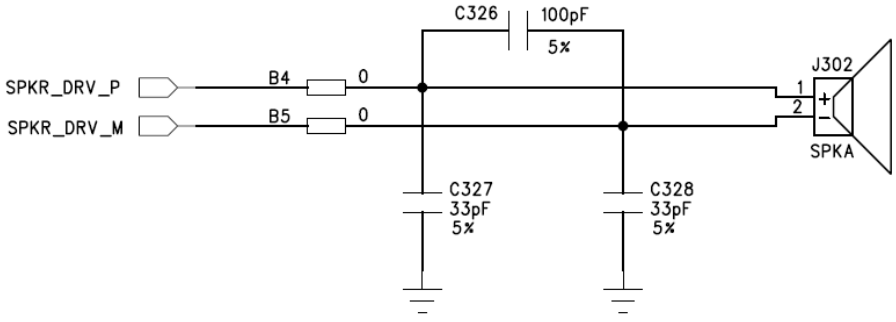
1. The earphone holder in Figure 4.24 is normally closed. If the user is using the normally open mode earphone holder, please modify the detection circuit according to the actual pin and modify the software accordingly.

2. We recommend that the headphone detection pin HS_DET and HPH_L form a detection circuit (the connection method in the above figure), because HPH_L has a pull-down resistor

inside the chip, which can ensure that HS_DET is low when connected with HPH_L, if the user will HS_DET and HPH_R To connect, please reserve a 1K pull-down resistor on HPH_R.
3 The standard of the headphone interface is the European standard OMPT. If you need to design the American standard CTIA interface, you need to swap the GND and MIC signals for the network. If you want to be compatible with both headset standards, you need an external dedicated chip, such as the TI-TS3A226AE.

4.8.4.Speaker Interface Circuit

The module integrates a Class-D audio amplifier with an output power of 800mW and an output signal of SPKR_OUT_P / SPKR_OUT_M.



4.24：Recommended circuit with Internal audio amplifier

4.8.5.I2S Interface

There are one sets of GPIO-compatible I2S interfaces inside the module. The pins used by this function are as follows:

Name	Pin	Intput/Output	Description
GPIO88	264	O	I2S1 Data out
GPIO87	105	O	I2S1 WS
GPIO86	239	I	I2S1 Data in
GPIO85	265	O	I2S1 SLK

4.9. USB Interface

The SLM500 supports a USB 2.0 High speed interface. It must control the 90 ohm differential impedance during Layout and control the external trace length.

The module supports OTG function.

The voltage input range during charging is as follows:

Table 4.9: Voltage input range during charging

Name	Description	Minimum	Typical	Maximum	Unit
VBUS	Input range	4	-	6.3	V

The USB plug-in detection of the module is realized by the VBUS and DP/DM data lines. When the USB cable is inserted, the VBUS voltage is detected first, and then the DM/DP pull-up state is detected to determine whether the USB data line or the charger is inserted. Therefore, if you need to use the USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is a high-speed mode. It is recommended to connect a common-mode inductor to the side of the USB connector to effectively suppress EMI interference. At the same time, the USB interface is an external interface. The DM/DP must add a TVS tube to prevent static damage caused by plugging and unplugging the data cable. When selecting the TVS, the user should pay attention to the load capacitance of less than 1pf. VBUS also needs to increase the TVS tube. If there is anti-surge demand, it is also necessary to increase the anti-surge tube. The connection diagram is as follows:

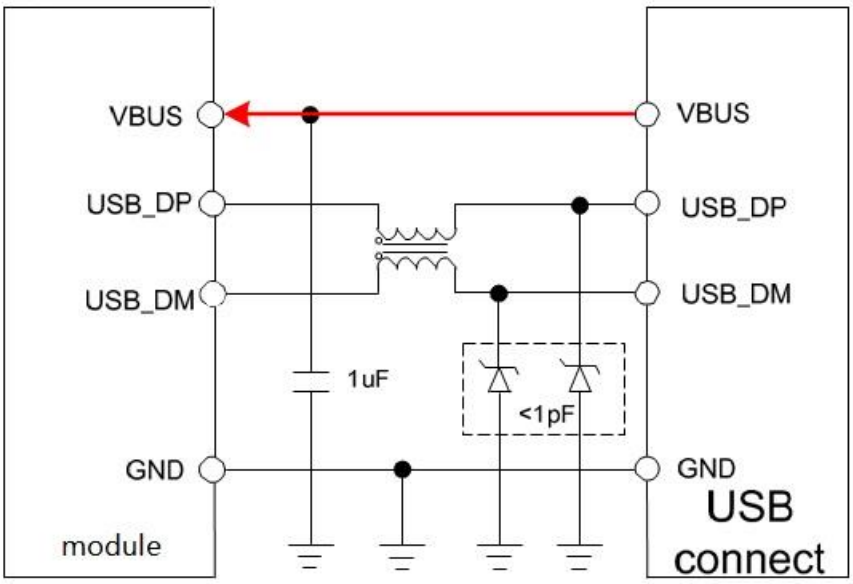


Figure 4.26: USB Connection Diagram

4.9.1. USB OTG

The SLM500 module can provide USB OTG function. The pins used in this function are as follows:

Table 4.10: USB OTG Pin Description

Pin name	Pin	Description
VBUS	141、142	5V charging input / OTG output power.
USB_HS_DM	13	USB Date-
USB_HS_DP	14	USB Date+
USB_HS_ID	16	USB ID

The recommended circuit diagram of USB OTG is as follows:

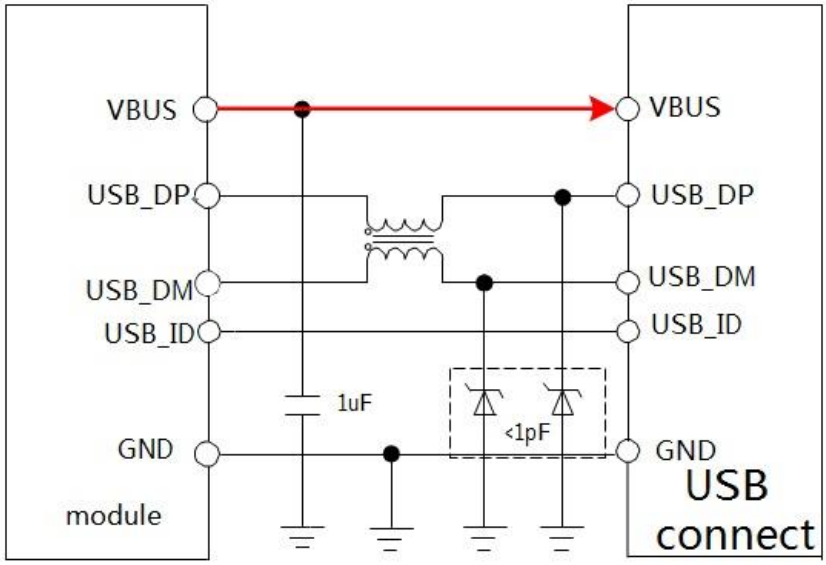


Figure 4.27: USB-OTG Connection Diagram

4.10. Charging Interface

The SLM500 module integrates a 1.44A charging solution. The charging related content of this manual is only described by the internal charging scheme. The QCM2150 platform uses the Qualcomm PM215 internal integrated charging chip by default. The chip is in liner mode.

Trickle charging: it is divided into two parts: trickle charging-A: the charging current is 90mA when the battery voltage is lower than 2.8V; trickle charging-B: the charging current is 450mA when the battery voltage is between 2.8V and 3.2V;

Constant current charging: when the battery voltage is between 3.2V ~ 4.2V, the charging current is 1.44A , when charging with USB is 450mA;

Constant voltage charging: when the battery voltage reaches 4.2V, the charging current gradually decreases, and the charging current reduces to about 100mA to stop charging.

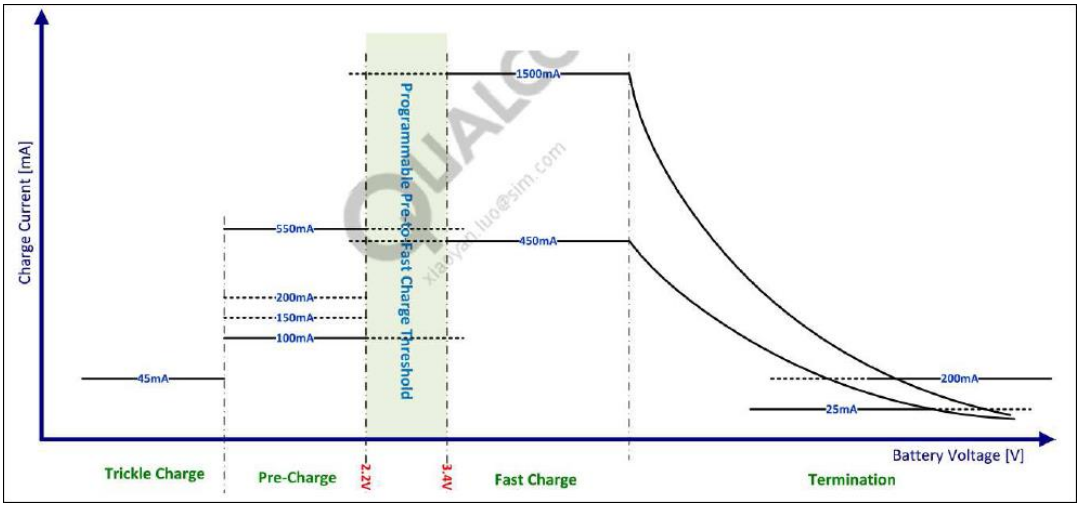


Figure 4.28: Charging diagram

4.10.1. Charging Detection

When the VBUS pin voltage is higher than 4.0V, a hardware interrupt will be generated inside the module. The software determines whether the charger is inserted or the USB data cable is inserted by judging the status of USB_DP/USB_DM.

4.10.2. Charge Control

The SLM500 module can charge the over-discharged battery. The charging process includes trickle charge, pre-charge, constant current, and constant-voltage charge. When the VBAT voltage is lower than 3.4V, the module is pre-charged; when VBAT is between 3.4V and 4.2V, it is charged by the constant current plus constant voltage method optimized for the lithium battery. At present, the software's charge cut-off voltage is 4.2V, and the back-off voltage is 4.05V.

4.10.3. BAT_CON_TEM

The SLM500 module has battery temperature detection and can be implemented by BAT_THERM (134 PIN). This requires the internal integration of a 47KΩ thermistor (negative temperature coefficient) inside the battery to connect the thermistor to the BAT_THERM pin. During the charging process, the software reads the voltage of the BAT_THERM pin to determine if the battery temperature is too high. If the temperature is too high or too low, the battery will stop charging immediately to prevent battery damage. The battery charging connection diagram is shown below:

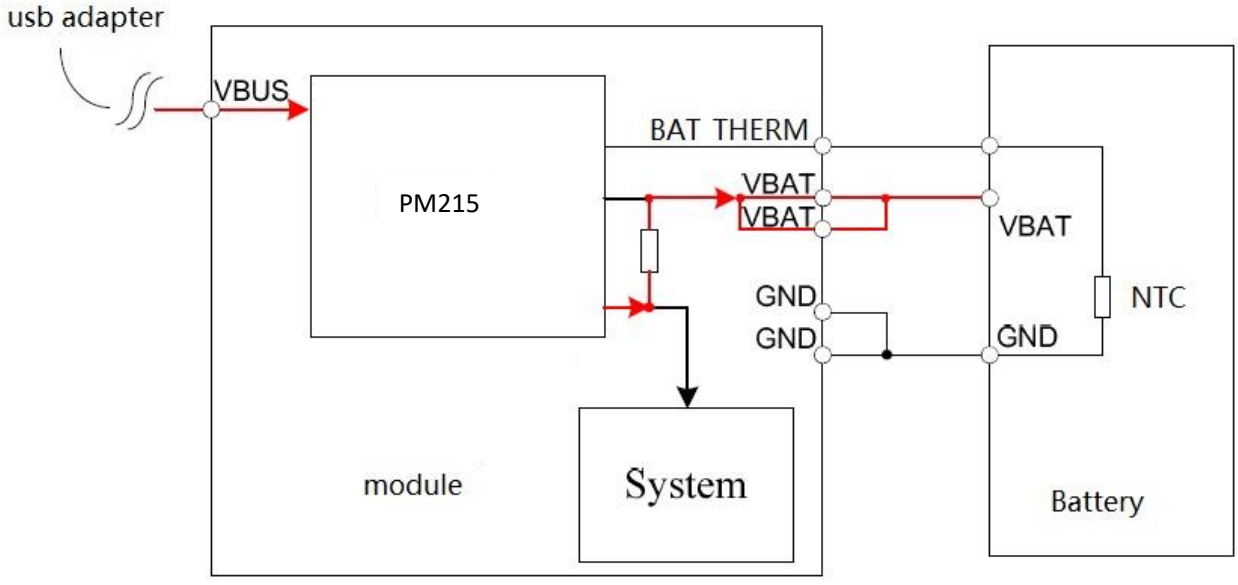


Figure 4.29: Charging circuit connection diagram

4.11 UIM Card Interface

The SLM500 can support two SIM cards at the same time to achieve dual card dual standby. Support SIM card hot swap, can automatically recognize 1.8V and 3.0V cards. The figure

below is the SIM recommended interface circuit. In order to protect the SIM card, it is recommended to use TVS devices for electrostatic protection. The device of the peripheral circuit of the SIM card should be close to the SIM card holder.
The reference circuit is as follows:

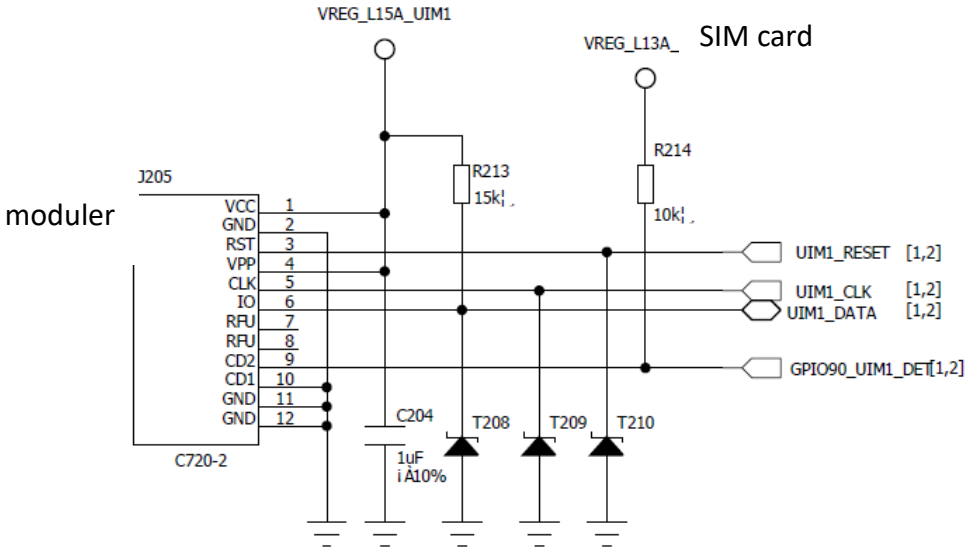


Figure 4.30: UIM card interface circuit

4.12. SD Card Interface

SLM500 supports SD card interface.
The reference circuit is as follows:

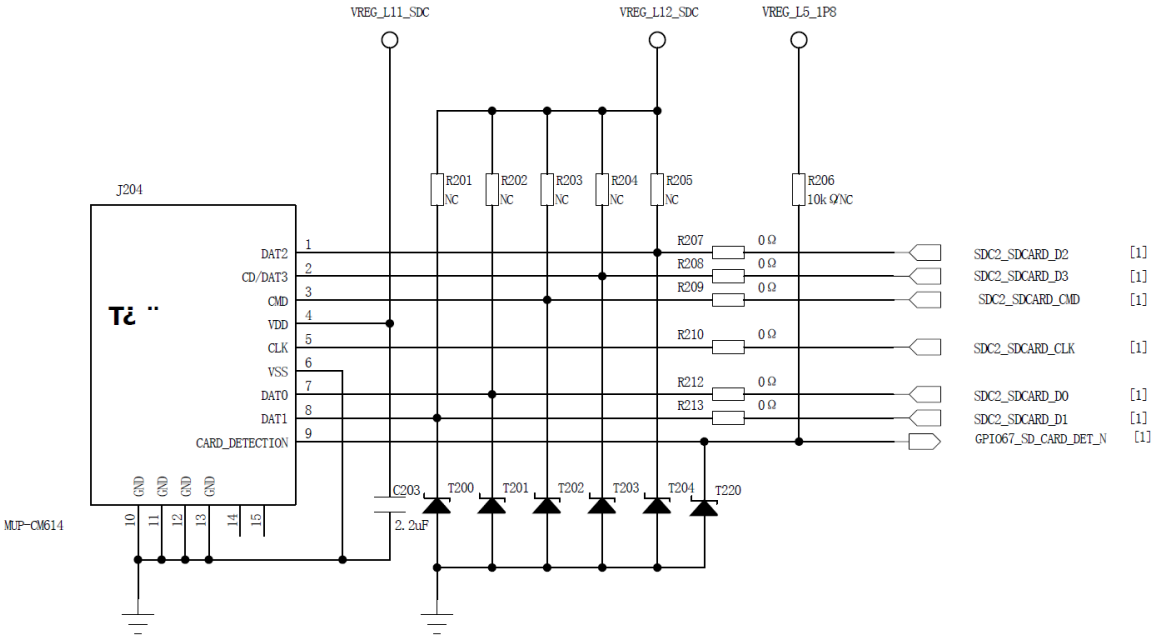


Figure 4.31: SD Card Interface Circuit

4.13 I2C Bus Interface

The SLM500 module supports five hardware I2C bus interfaces include two camera-specific CCI interface. The pin definitions and default functions are as follows:

Table 4.11: I2C Interface Pin Description

Name	Pin	Default function
GPIO14_SENSOR_I2C4_SDA	92	Dedicated I2C for sensors only|(G-sensor, compass, gyroscope, etc.)
GPIO15_SENSOR_I2C4_SCL	91	
GPIO29_CAM_I2C_SDA0	84	Main Camera dedicated
GPIO30_CAM_I2C_SCL0	83	
GPIO32_DCAM_I2C_SCL1	166	Depth Camera 专用
GPIO31_DCAM_I2C_SDA1	205	
GPIO10_TP_I2C3_SDA	48	General purpose I2C, default for TP
GPIO11_TP_I2C3_SCL	47	
GPIO6	167	Universal I2C

Note: To use the 2.2KΩ pull-up resistor to 1.8V .

Gpio14 / 15 can only be used to connect sensor devices in Qualcomm QVL, not other devices.

4.14 Analog to Digital Converter (ADC)

The SLM500 module provides two MPP function signals from the power management chip: PWM（29PIN） and ADC（128PIN）, MPP can be configured as an ADC or PWM signal.

The ADC signal is 16 bit resolution, and its performance parameters are as follows:

Table 4.12: ADC Performance Parameters

Description	Minimum	Typical	Maximum	Unit
Input Voltage Range	-	1.8	-	V
ADC Resolution	-	-	15	bits
Analog Input Bandwidth	-	100	-	kHz
Sampling Frequency	-	2.4	-	MHz
INL	-	-	±8	LSB
DNL	-	-	±4	LSB
Offset error	-	-	±1	%
Gain error	-	-	±1	%

4.15. PWM

The PWM pin can be used as a backlight adjustment for the LCD to adjust the backlight brightness by adjusting the duty cycle.

4.16. Motor

The SLM500 supports motor functions and can be implemented by the user via PM_VIB_DRV_N (28PIN) . The reference schematic diagram is as follows. Note that the uF-level capacitor cannot be placed on the signal line.

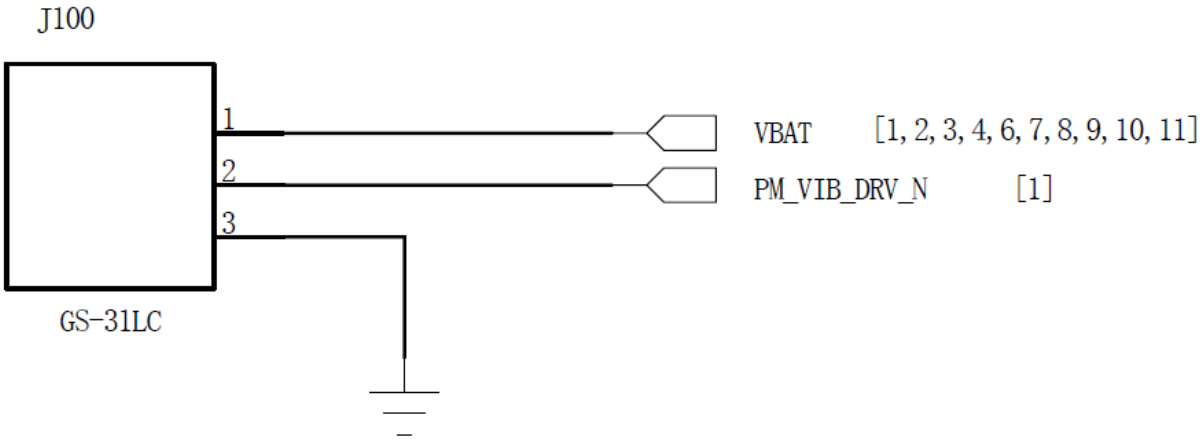


Figure 4.32: Motor interface circuit

4.17 Antenna Interface

The module provides four antenna interfaces: MAIN antenna, DRX antenna, GPS antenna and WiFi/BT antenna. In order to ensure that the user's products have good wireless performance, the antenna selected by the user should meet the requirement that the input impedance is 50 ohms in the working frequency band and the VSWR is less than 2.

4.17.1 Main Antenna

The module provides the MAIN antenna interface pin Pin1 RF_MAIN. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

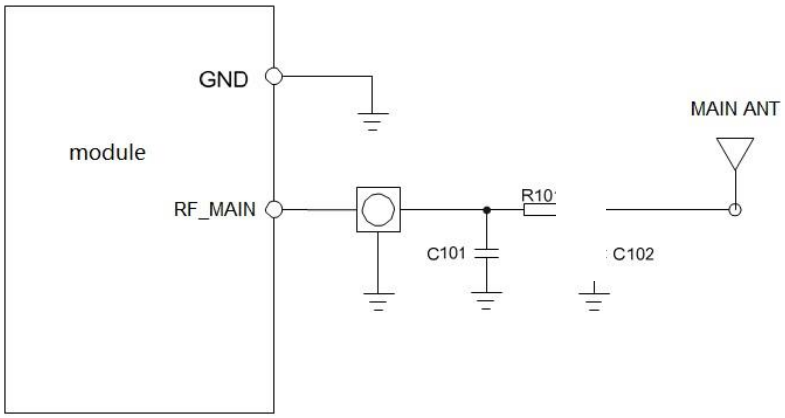


Figure 4.34: MAIN Antenna Interface Connection Circuit

In the figure, R101, C101, and C102 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R101 defaults to 0R, C101 and C102 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

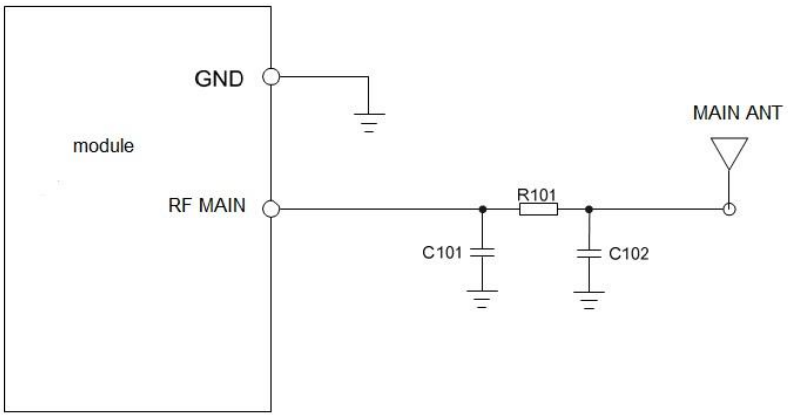


Figure 4.35: MAIN Antenna Interface Simplified Connection Circuit

In the above figure, R101 defaults to 0R, and C101 and C102 do not paste by default.

4.17.2 DRX Antenna

The module provides the DRX antenna interface pin RF_DIV, and the antenna on the user's motherboard should be connected to the module's antenna pins using a 50-ohm characteristic microstrip or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

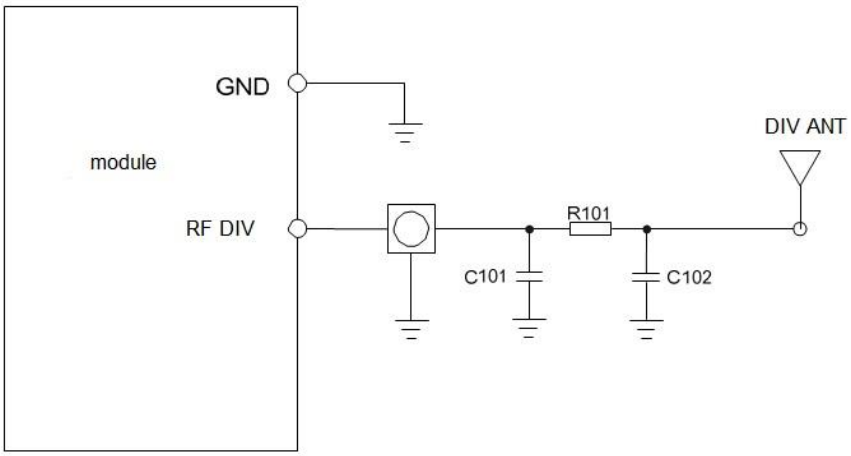


Figure 4.36: DRX Antenna Interface Connection Circuit

In the figure, R102, C103, and C104 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R102 defaults to 0R, C103 and C104 are not posted by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

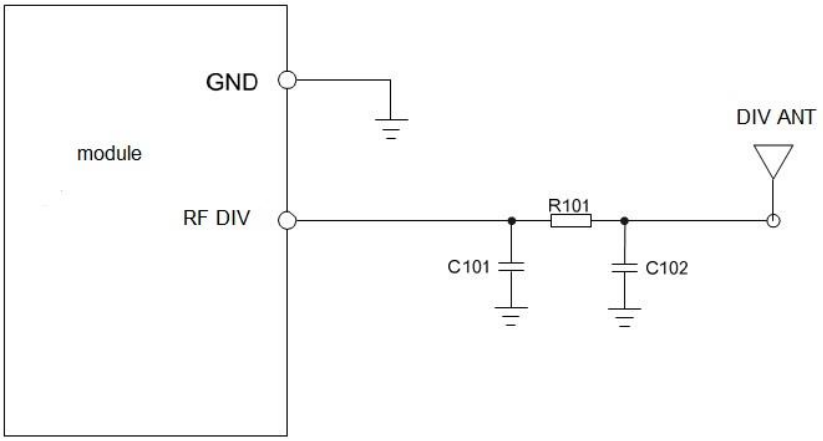


Figure 4.37: DRX Antenna Interface Simplified Connection Circuit

In the above figure, R102 defaults to 0R, C103 and C104 are not attached by default.

4.18.3 GPS Antenna

The module provides the GNSS antenna pin RF_GPS. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line.

The LNA is integrated inside the module.

To improve GNSS reception performance, customers can use external active antennas. The recommended circuit connections are as follows:

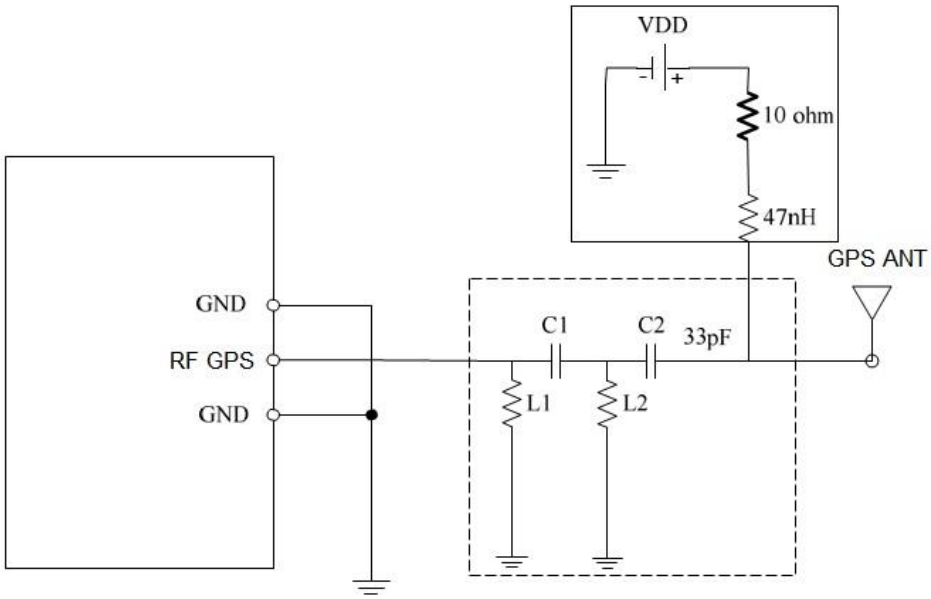


Figure 4.38: Connecting Active Antennas

4.18.4 WiFi/BT antenna

The module provides the WiFi/BT antenna pin RF_WIFI/BT. The antenna on the user's motherboard should be connected to the antenna pin of the module using a 50 ohm microstrip line or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

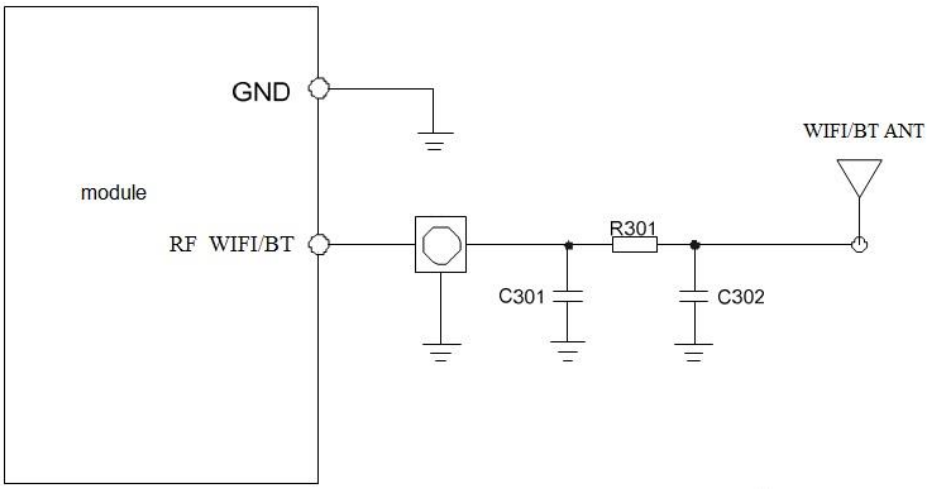


Figure 4.40: WiFI_BT antenna interface connection circuit

In the figure, R301, C301, and C302 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R301 defaults to 0R, C301 and C302 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

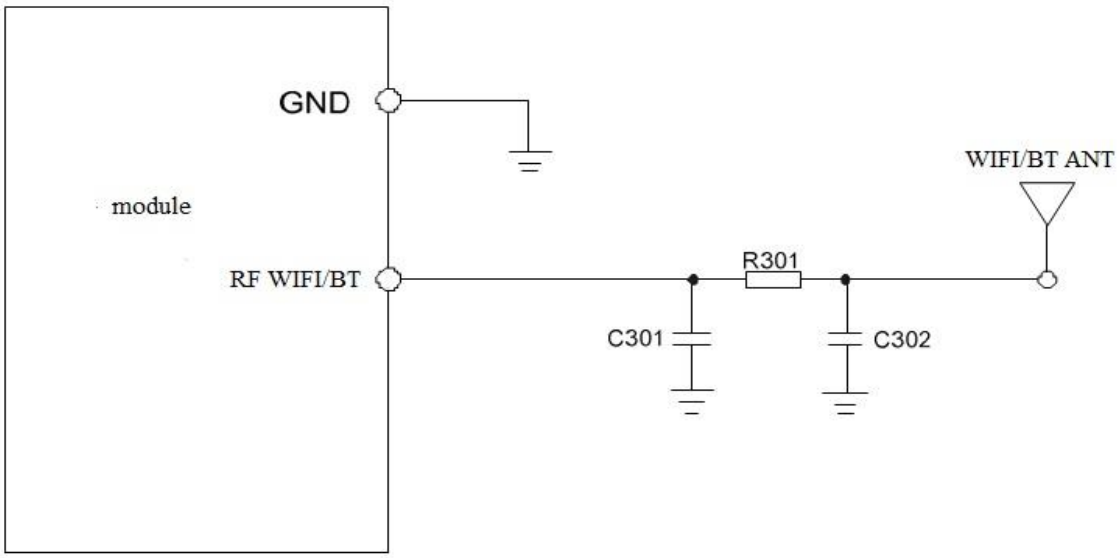


Figure 4.41: WIFI_BT antenna interface simplified connection circuit

In the above figure, R301 defaults to 0R, and C301 and C302 do not paste by default.

5.PCB Layout

The performance of a product depends largely on the PCB trace. As mentioned above, if the PCB layout is unreasonable, it may cause interference problems such as card loss. The way to solve these interferences is often to redesign the PCB. If you can plan a good PCB layout in the early stage, the PCB traces smoothly, saving a lot of time. Of course, it can also save a lot of costs. This chapter mainly introduces some things that users should pay attention to during the PCB layout stage, minimizing interference problems and shortening the user's development cycle.

The SLM500 module is an intelligent module with its own Android operating system. It includes sensitive data lines such as high-speed USB and MIPI. It also has strict requirements on the length and impedance of the signal line. If the high-speed signal processing is not good, it will cause serious EMI. The problem, more serious will also affect the USB identification, LCD display, so the PCB design requirements when using the SLM500 module is much higher than the previous 2G module, please read this chapter carefully, reduce the subsequent hardware debugging cycle.

When using the SLM500 module, the user is required to use at least 4 layers of via holes for the PCB to facilitate impedance control and signal line shielding.

5.1. Module PIN distribution

Before the PCB layout, first understand the pin distribution of the module, and rationally layout the related devices and interfaces according to the distribution defined by the pin. Please refer to Figure 2 to determine the distribution of the function feet of the module.

5.2. PCB Layout Principles

Several aspects of the main attention during the PCB layout phase:

5.2.1. Antenna

Antenna part design, SLM758 module has a total of 4 antenna interfaces, they are: ANT_MAIN, ANT_DRX, ANT_GNSS, ANT_WIFI. Pay attention to component placement and RF routing:

The RF test head is used to test the conducted RF performance and should be placed as close as possible to the antenna pins of the module.

The antenna matching circuit needs to be placed close to the antenna end;

The connection between the antenna pin of the module and the antenna matching circuit

must be controlled by 50 ohm impedance;

The device and wiring between the antenna pin and the antenna connector of the module must be away from high-speed signal lines and strong interference sources to avoid crossing or parallel with any signal lines in adjacent layers.

The length of the RF cable between the antenna pin of the module and the antenna connector should be as short as possible. The situation of crossing the entire PCB should be absolutely avoided.

If the antenna is connected by a coaxial RF line, care should be taken to avoid the coaxial RF line spanning the SIM card, power supply circuit, and high-speed digital circuits to minimize the effects of each other.

5.2.2 Power Supply

Power traces must consider not only VBAT, but also the return GND of the power supply. The trace of the VBAT positive must be short and thick, the trace must first pass through the large capacitor, Zener diode and then the power PIN of the module. There are multiple PAD exposed copper at the bottom of the module. Make sure that the GND path of these exposed copper areas to the power supply is the shortest and smoothest. This ensures that the current path of the entire power supply is the shortest and the interference is minimal.

5.2.3. SIM Card

The SIM card has a large area and does not have an anti-EMI interference device. It is relatively susceptible to interference. Therefore, in the layout, first ensure that the SIM card is away from the antenna and the antenna extension cable inside the product. Place it as close as possible to the module. When the PCB is routed, pay attention to it. The SIM_CLK signal is protected, and the SIM_DATA, SIM_RST, and SIM_VDD signals of the SIM card are away from the power source and away from the high-speed signal line. If the processing is not easy, it may cause problems such as not knowing the card or dropping the card. Therefore, please follow the following principles when designing:

Keep the SIM card holder away from the GSM antenna during the PCB layout phase;

SIM card routing should be as far away as possible from RF line, VBAT and high-speed signal lines, and the SIM card should not be too long;

The GND of the SIM card holder should be in good communication with the GND of the module to make the GND equipotential between the two.

To prevent SIM_CLK from interfering with other signals, it is recommended to protect SIM_CLK.

It is recommended to place a 100nF capacitor on the SIM_VDD signal line near the SIM card holder;

Place TVS near the SIM card holder. The parasitic capacitance of the TVS should not exceed 50pF, and the 51Ω resistor in series with the module can enhance ESD protection.

The SIM card signal line increases the capacitance of 22pF to ground to prevent radio

frequency interference.

The return path of VBAT has a large current, so the SIM card trace should avoid the return path of VBAT as much as possible.

5.2.4. MIPI

MIPI is a high-speed signal line. Users must pay attention to protection during the layout stage, so that they are away from the signal lines that are easily interfered. The GND processing must be performed on the upper and lower sides, and the traces are differential pairs. 100 ohm differential impedance matching is performed. Ensure impedance consistency and do not bridge different GND planes as much as possible.

The MIPI interface selects a small-capacity TVS when selecting an ESD device. It is recommended that the parasitic capacitance be less than 1pF.

The MIPI routing requirements are as follows:

The total length of the cable does not exceed 305mm

It is required to control 100 ohm differential impedance with an error of ±10%.

The error of the differential line length within the group is controlled within 1mm.

The length error between groups is controlled within 2 mm.

5.2.5. USB

The module supports high-speed USB interface at a rate of 480Mbps. The user recommends adding a common-mode inductor during the schematic design phase to effectively suppress EMI interference. If you need to increase the static protection, please select a TVS tube with a parasitic capacitance of less than 1pF. Please refer to the following notes when planning Layout:

The common mode inductor should be close to the side of the USB connector.

Requires control of 90 ohm differential impedance with an error of ±10%.

The differential line length error is controlled within 6mm.

If the USB has a charging function, please note that the VBUS cable is as wide as possible.

If there is a test point, try to avoid the split line and put the test point on the path of the trace.

Table 5.1: Internal USB cable length of the module

Pin	Signal	Length mm)	Length Error（P-N）
14	USB_HS_DP	33.0	0.3mm
13	USB_HS_DM	33.3	

5.2.6.Audio

The module supports 3 analog audio signals. Analog signals are susceptible to interference from high speed digital signals. So stay away from high-speed digital signal lines. The module supports the GSM system, and the GSM signal can interfere with the audio by coupling and conduction. Users can add 33pF and 10pF capacitors to the audio path to filter out coupling interference. The 33pF capacitor mainly filters out the interference of the GSM850/EGSM900

band, and the 10pF capacitor mainly filters out the interference of the DCS1800 band. The coupling interference of TDD has a great relationship with the PCB design of the user. In some cases, the TDD of the GSM850/EGSM900 frequency band is more serious, and in some cases, the TDD interference of the DCS1800 frequency band is more serious. Therefore, the user can select the required filter capacitor according to the actual test result, and sometimes even do not need to paste the filter capacitor.

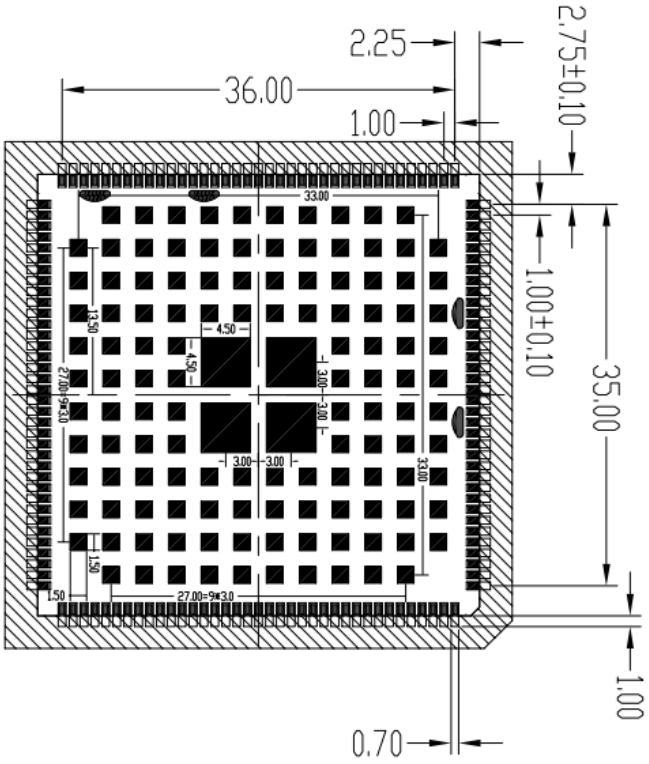
The GSM antenna is the main source of coupling interference for TDD, so users should pay attention to keeping the audio trace away from the GSM antenna and VBAT during PCB layout and routing. The filter capacitor of the audio is preferably placed close to the module end and placed next to the interface end. The audio output should be routed according to the differential signal rules.

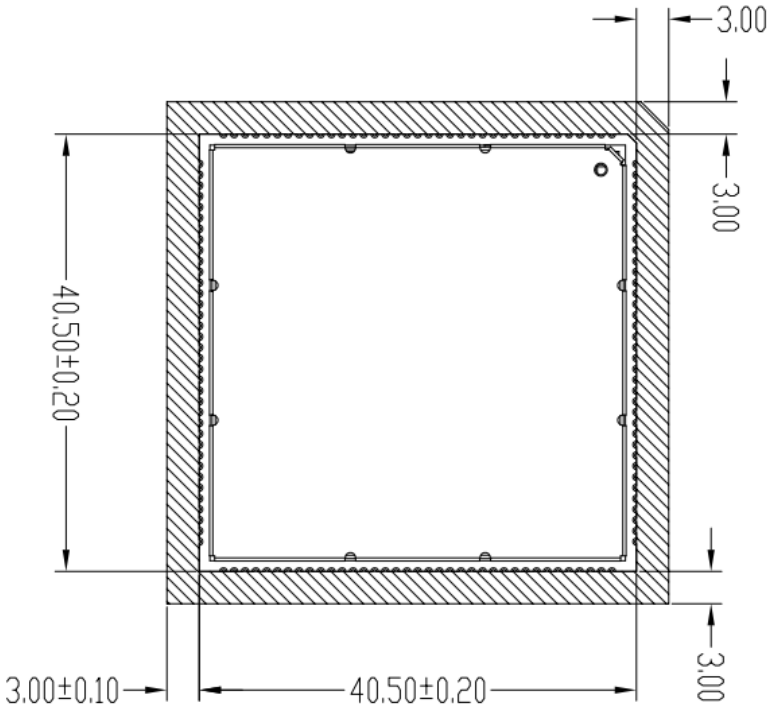
The conducted interference is mainly caused by the voltage drop of VBAT. If the Audio PA is directly powered by VBAT, it is easier to hear the “zizi” sound at the SPK output. Therefore, it is better to connect in parallel with the input of the Audio PA in the schematic design. Some large capacitance capacitors and series magnetic beads.

The conducted interference is also strongly related to TDD and GND. If GND is not handled well, many high-frequency interference signals will interfere with MIC and Speaker through devices such as bypass capacitors, so users should ensure good performance of GND during PCB design.

5.2.7. Other

Because the outer ring pad of the module is designed with stamp hole, it is necessary to expand the pad to enhance the tin climbing ability when making the SMD steel mesh. Therefore, a sufficient safety distance should be reserved between the module pad and other main board devices. The recommended safe distance is 3mm, as shown in the following figure:




3.00
3.00
40.50±0.20
3.00
3.00±0.10
40.50±0.20

6. Electrical, Reliability

6.1 Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits can cause permanent damage to the module.

Table 6.2: Absolute Maximum

Parameter	Minimum	Typical	Maximum	Unit
VBAT	-	-	6	V
VBUS	-	-	10.5	V
Peak current	-	-	3	A

6.2 Working Temperature

The table below shows the operating temperature range of the module:

Table 6.2: Module Operating Temperature

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-25	-	75	℃
Storage temperature	-40	-	90	℃

6.3 Working Voltage

Table 6.3: Module Operating Voltage

Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.4		4.2	V
VBUS	4	5	6	V
Hardware shutdown voltage	2.5	2.8	-	V

6.4 Digital Interface Features

Table 6.4: Digital Interface Features (1.8V)

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{IH}	Input high level voltage	1.17	-	-	V
V_{IL}	Input low level voltage	-	-	0.63	V
V_{OH}	Output high level voltage	1.35	-	-	V
V_{OL}	Output low level voltage	-	-	0.45	V

6.5 SIM_VDD Characteristics

Table 6.5: SIM_VDD Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
V_O	Output voltage	-	3	-	V
		-	1.8	-	
I_O	Output current	-	-	55	mA

6.6 PWRKEY Feature

Table 6.6: PWRKEY Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
PWRKEY	High level	1.4	-	-	V
	Low level	-	-	0.6	V
	Effective time	2000			ms

6.7 VCOIN Feature

Table 6.7: VCOIN Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
$VCOIN_{-IN}$	VCOIN input voltage	2	3	3.25	V
I_{RTC-IN}	VCOIN Current consumption	-		3	uA
$VCOIN_{-OUT}$	VCOIN Output voltage	-	3	-	V
$I_{RTC-OUT}$	VCOIN Output current	-		2	mA

6.8 Current Consumption (VBAT = 3.8V)

Table 6.8: Current consumption

Parameter	Description	Condition	Minimum	Typical	Maximum	Unit
VBAT	voltage	Voltage must be between the maximum and minimum values	3.4	3.8	4.2	V
Ivbat	Average	Shutdown mode	-	-	65	uA

	current	GSM Standby power consumption	-	-	4.0	mA
		WCDMA Standby power consumption	-	-	3.9	mA
		TD-S Standby power consumption	-	-	4.0	mA
		CDMA Standby power consumption	-	-	3.8	mA
		FDD Standby power consumption			4.45	mA
		TDD Standby power consumption			3.5	mA
	Call Current consumption	GSM900 CH62 32dBm	-	-	250	mA
		WCDMA2100 CH10700 22.5 dBm	-	-	550	mA
	Digital transmission	GPRS GSM900 CH62 PCL5 1DL 4UL	-	-	TBD	mA
		EGPRS GSM900 CH62 PCL8 1DL 4UL	-	-	TBD	mA
Imax	Peak current	Power control at maximum output power	-	-	3	A

6.9 Electrostatic Protection

The module is not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling, and operating modules.

6.10 Module Operating Frequency Band

The table below lists the operating frequency bands of the module and complies with the 3GPP TS 05.05 technical specification.

Table 6.9: Module Operating Band

Frequency band	Receive	Transmission	Physical channel
GSM850	869 ~ 894MHz	824 ~ 849MHz	128~251
EGSM900	925 ~ 960MHz	880 ~ 915MHz	0~124，975~1023
DCS1800	1805 ~ 1880MHz	1710 ~ 1785MHz	512~885
WCDMA B1	2110 ~ 2170 MHz	1920 ~ 1980 MHz	TX: 9612~9888
			RX: 10562~10838
WCDMA B5	869 ~ 894MHz	824 ~ 849MHz	TX: 4132~4233
			RX: 4357~4458
WCDMA B8	880 ~ 915MHz	925 ~ 960MHz	TX: 2712~2863
			RX: 2937~3088
CDMA BC0	869 ~ 894MHz	824 ~ 849MHz	1 ~ 799； 991 ~ 1023
TDSCDMA 1.9G	1880 ~ 1920 MHz	1880 ~ 1920MHz	9400 ~ 9600
TDSCDMA 2G	2010 ~ 2025 MHz	2010 ~ 2025MHz	10054 ~ 10121

LTE B1	2110 ~ 2170 MHz	1920 ~ 1980 MHz	TX: 18000 ~ 18599
			RX: 0~599
LTE B3	1805 ~ 1880 MHz	1710 ~ 1785 MHz	TX: 19200~19949
			RX: 1200~1949
LTE B5	869 ~ 894MHz	824 ~ 849MHz	TX: 20400 ~ 20649
			RX: 2400~2649
LTE B8	925 ~ 960MHz	880 ~ 915MHz	TX: 21450 ~ 21799
			RX: 3450~3799
LTE B34	2010 ~ 2025 MHz	2010 ~ 2025 MHz	36200 ~ 36349
LTE B38	2570 ~ 2620 MHz	2570 ~ 2620 MHz	37750 ~ 38249
LTE B39	1880 ~ 1920 MHz	1880 ~ 1920 MHz	38250 ~ 38649
LTE B40	2300 ~ 2400 MHz	2300 ~ 2400 MHz	38650 ~ 39649
LTE B41	2496 ~ 2690 MHz	2496 ~ 2690 MHz	39650 ~ 41589

Note: The SLM500Q's LTE TDD B41 band bandwidth is 100MHz (2555 ~ 2655 MHz), the channel is 40240 ~ 41240.

6.11 RF Characteristics

The following table lists the conducted RF output power of the module, in accordance with 3GPP TS 05.05 technical specification, 3GPP TS 134121-1 standard.

Table 6.10: Conducted Output Power

Frequency band	Standard output power (dBm)	Output power tolerance (dBm)
GSM850、EGSM900	33dBm	±2
DCS1800	30dBm	±2
WCDMA	24 dBm	+1/-3
CDMABC0	25 dBm	±2
TDSCDMA	24 dBm	+1/-3
LTE	23 dBm	±2.7

6.12 Module Conduction Receiving Sensitivity

The table below lists the conducted receive sensitivity of the module and is tested under static conditions.

Table 6.11: Conducted Receive Sensitivity

Frequency band	Receive sensitivity (typical)	Receive sensitivity (maximum)
GSM850、EGSM900	<-108dBm	3GPPrequirements
DCS1800	<-108dBm	3GPPrequirements
WCDMAB1	<-109 dBm	3GPPrequirements

WCDMAB5	<-109 dBm	3GPPrequirements
CDMABC0	<-110 dBm	3GPPrequirements
TDSCDMA1.9G	<-110 dBm	3GPPrequirements
TDSCDMA2G	<-110 dBm	3GPPrequirements
LTEFDD/TDD	See Table 6.12	3GPPrequirements

Table 6.12: LTE Reference Sensitivity 3GPP Dual Antenna Requirements (QPSK)

E-UTRA Frequency band number	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex mode
1	-	-	-100	-97	-95.2	-94	FDD
2	-102.7	-99.7	-98	-95	-93.2	-92	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	FDD
4	-104.7	-101.7	-100	-97	-95.2	-94	FDD
5	-103.2	-100.2	-98	-95			FDD
6	-	-	-100	-97			FDD
7	-	-	-98	-95	-93.2	-92	FDD
8	-102.2	-99.2	-97	-94			FDD
9	-	-	-99	-96	-94.2	-93	FDD
10	-	-	-100	-97	-95.2	-94	FDD
11	-	-	-100	-97			FDD
12	-101.7	-98.7	-97	-94			FDD
13			-97	-94			FDD
14		-	-97	-94			FDD
...							
17	-	-	-97	-94			FDD
18	-	-	-100[7]	-97[7]	-95.2[7]	-	FDD
19	-	-	-100	-97	-95.2	-	FDD
20			-97	-94	-91.2	-90	FDD
21			-100	-97	-95.2		FDD
22			-97	-94	-92.2	-91	FDD
23	-104.7	-101.7	-100	-97	-95.2	-94	FDD
24			-100	-97			FDD
25	-101.2	-98.2	-96.5	-93.5	-91.7	-90.5	FDD
26	-102.7	-99.7	-97.5[6]	-94.5[6]	-92.7[6]		FDD
27	-103.2	-100.2	-98	-95			FDD
28		-100.2	-98.5	-95.5	-93.7	-91	FDD
31	-99.0	-95.7	-93.5				FDD
...							
33	-	-	-100	-97	-95.2	-94	TDD
34	-	-	-100	-97	-95.2	-	TDD
35	-106.2	-102.2	-100	-97	-95.2	-94	TDD
36	-106.2	-102.2	-100	-97	-95.2	-94	TDD

37	-	-	-100	-97	-95.2	-94	TDD
38	-	-	-100	-97	-95.2	-94	TDD
39	-	-	-100	-97	-95.2	-94	TDD
40	-	-	-100	-97	-95.2	-94	TDD
41	-	-	-98	-95	-93.2	-92	TDD

6.13 WIFI Main RF Performance

The table below lists the main RF performance under WIFI conduction.

Table 6.13: Main RF performance parameters under WIFI conduction

Transmission performance (2.4G)				
	802.11B	802.11G	802.11N	
Transmit power (minimum rate)	18	18	18	dBm
Transmit power (maximum rate)	18	14.5	13	dBm
EVM (maximum rate)	20%	-27	-30	dB
Receiving performance (2.4G)				
Receiving sensitivity	802.11B	802.11G	802.11N	
Minimum rate	-92	-91	-90	dBm
Maximum rate	-89	-74.5	-72.5	dBm
Transmission performance(5G)				
	802.11a	802.11n		802.11a
Transmit power (minimum rate)	17	17	dBm	17
Transmit power (maximum rate)	17	15	dBm	17
EVM (maximum rate)	20%	-27	dB	20%
Receiving performance(5G)				
Receiving sensitivity	802.11a	802.11n		802.11a
Minimum rate	-91	-90	dBm	-91
Maximum rate	-74	-71	dBm	-74

6.14 BT Main RF Prformance

The table below lists the main RF performance under BT conduction.

Table 6.14: Main RF performance parameters under BT conduction

Transmission performance				
Transmit power	DH5	2DH5	3DH5	
	14	14	14	dBm
Receiving performance				
Receiving sensitivity	DH5	2DH5	3DH5	
	-94.5	-94.5	-86	dBm

6.15 GNSS Main RF Performance

The table below lists the main RF performance under GNSS conduction.

Table 6.15: Main RF performance parameters under GNSS conduction

GNSS working frequency band: 1575.42MHZ				
GNSS carrier-to-noise ratio CN0: 40dB/Hz				
GNSS sensitivity:	Capture (cold start)	Capture (hot start)	Track	
	-148	-156	-160	dBm
GNSS startup time	Hot start	Warm start	Cold start	
	5	10	38	S

7. Production

7.1. Top And Bottom Views Of The Module

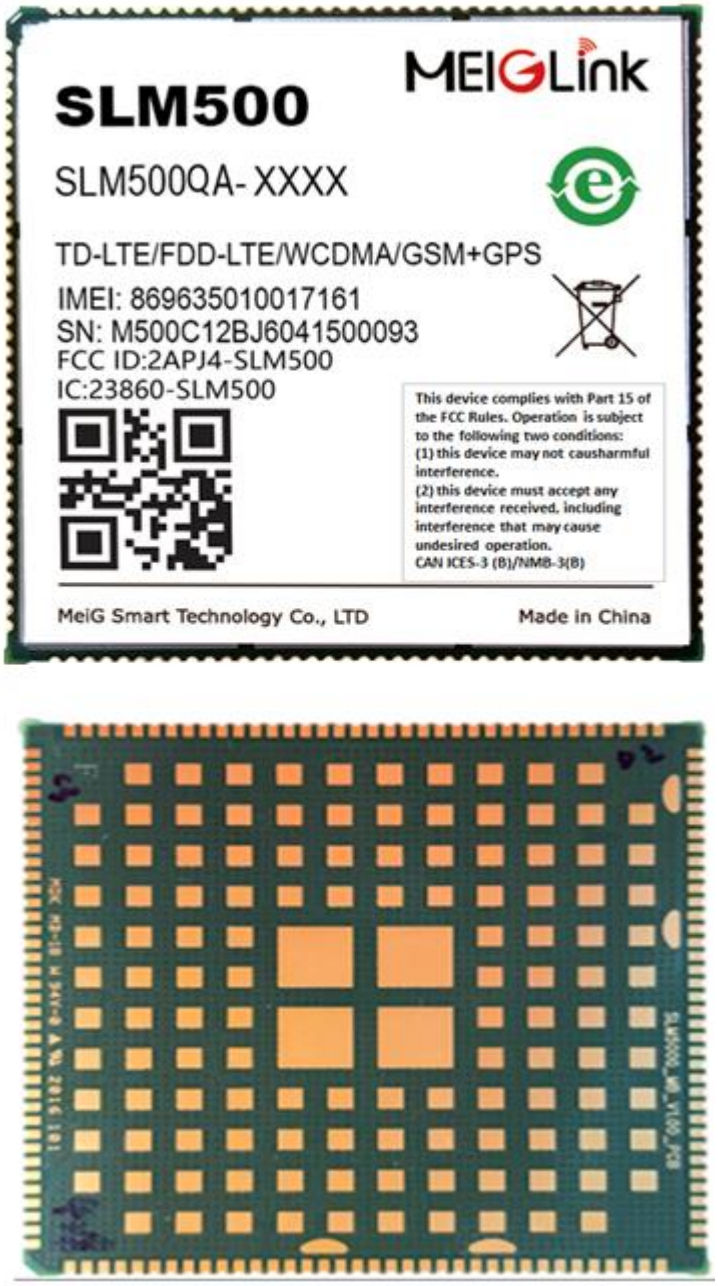


Figure 48: Module top and bottom views

7.2. Recommended Soldering Furnace Temperature Curve

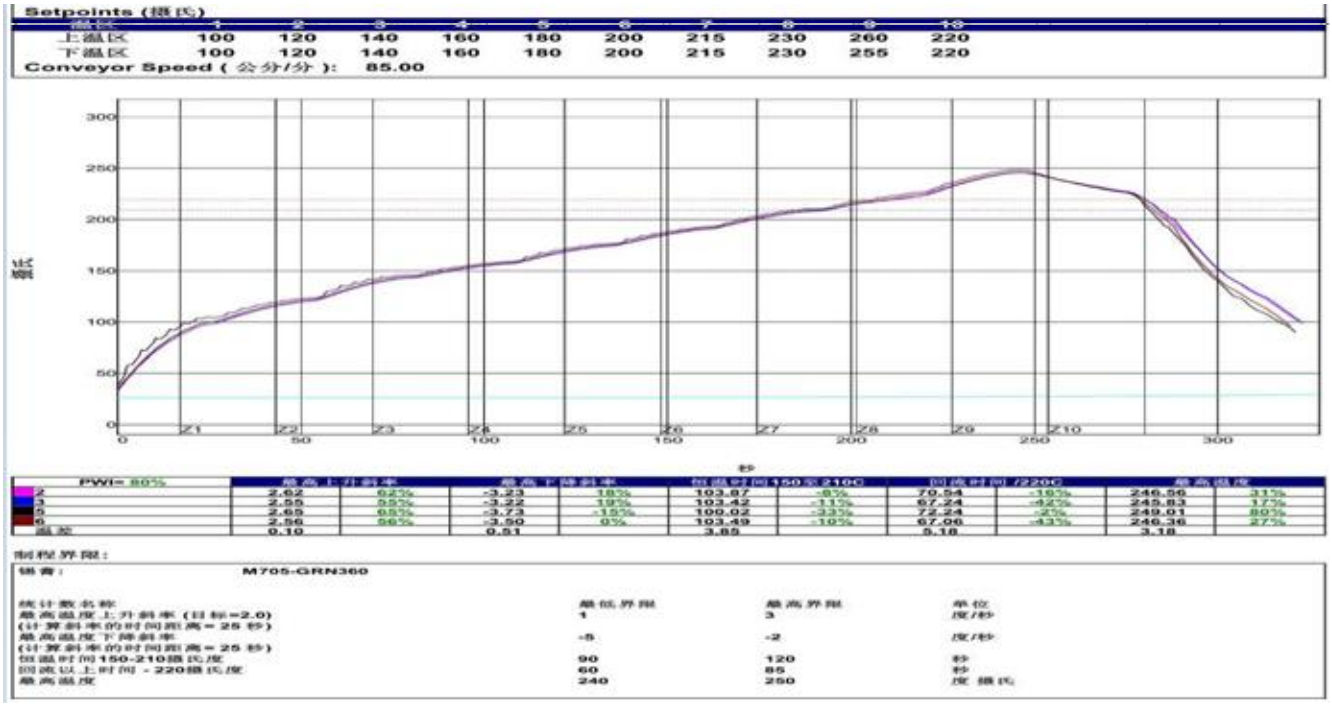


Figure 49: Module recommended soldering furnace temperature curve

7.3. Humidity Sensitivity (MSL)

The SLM500 module meets moisture sensitivity level 3. The dry package is subjected to the J-STD-020C specification in accordance with the IPC/JEDEC standard under ambient conditions of temperature <30 degrees and relative humidity <60%. Under ambient conditions of temperature <40 degrees and relative humidity <90%, the shelf life is at least 6 months without unpacking. After unpacking, Table 22 lists the shelf life of the modules for different moisture sensitivity levels.

Table 7.1: Humidity sensitivity level distinction

Grade	Factory environment≦+30℃/60%RH
1	Indefinite quality in the environment≦+30℃/85% RH Under conditions
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Use it after forced baking. After baking, the module must be patched within the

	time limit specified on the label.

After unpacking, the SMT patch should be taken within 168 hours under ambient conditions of <30 degrees and relative humidity <60%. If the above conditions are not met, baking is required. Note: Oxidation risk: Baking SMD packages can cause metal oxidation and, if excessive, can cause solderability problems during board assembly. The temperature and time of the SMD package are baked, thus limiting solderability considerations. The accumulation of baking time should be no more than 96 hours at temperatures above 90°C and as high as 125°C

7.4. Baking Requirements

Due to the humidity sensitivity of the module, the SLM500 should be thoroughly baked prior to reflow soldering, otherwise the module may cause permanent damage during reflow soldering. The SLM500 should be baked for 192 hours in a cryogenic vessel at 40°C +5°C/-0°C and a relative humidity of less than 5%, or in a high temperature vessel at 80°C±5°C.Bake for 72 hours. Users should note that the tray is not resistant to high temperatures. The user should take the module out of the tray for baking, otherwise the tray may be damaged by high temperature.

Table 7.2: Baking requirements:

Baking temperature	Humidity	Baking time
40℃±5℃	<5%	192 hours
120℃±5℃	<5%	4 hours

8. Support Peripheral Device List

Table 8.1: List of supported display models

Vendor	Drive IC	Specification
ILITEK	ILI9881P	1280x720

Table 8.2: Support for Camera Model List

Vendor	Drive IC	Specification
Sunny optical	S5K3M2XX	13M
Sunny optical	S5K4H7	8M
Sunny optical	S5K5E8	5M

Table 8.3: Support for touch screen model list

Vendor	Drive IC	Specification
GOODIX	GT5688	5"

Table 8.4: Support for G Sensor Model List

Vendor	Model	Specification
Bosch	BMI120	9-axis,16bit/16bit

Table 8.5: Support for Ecompass Model List

Vendor	Model	Specification
GMEMS	GMC303	3-Axis,14-bit

Table 8.6: Support PS/ALS Sensor Model List

Vendor	Model	Specification
LITEON	LTR-553ALS-01	ALS+PS

Table 8.7: Support for Gyro Sensor Model List

Vendor	Model	Specification
Bosch	BMI120	9-axis,16bit/16bit

9. Appendix

9.1. Related Documents

Table 9.1: Related documents

Serial number	File name	Comment
[1]	GSM 07.07：	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10：	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05：	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)
[4]	GSM 11.14：	Digital cellular telecommunications system (Phase 2+);Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11：	Digital cellular telecommunications system (Phase 2+);Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38：	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2)； Mobile Station (MS) conformance specification； Part 1： Conformance specification
[8]	AN_Serial Port	AN_Serial Port

9.2. Terms And Explanations

Table 9.2: Terms and explanations

Terms	Explanations
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate

IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
Phone book abbreviation	Explanations
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

OEM requirement and guidance for host manufactures
The module is limited to OEM installation ONLY
The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.

In case that FCC identification number and IC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: “Contains FCC ID: 2APJ4-SLM500” and “Contains IC: 23860-SLM500”

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. The devices must be installed and used in strict accordance with the manufacturer’s instructions as described in the user documentation that comes with the product. This device is intended only for OEM integrators under the followingconditions:1) The antenna must be installed such that 20 cm is maintained between the antenna and user.2) The transmitter module may not be co-located with any other transmitter or antenna.

Please take attention that changes or modification not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

This equipment complies with FCC/IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:
(1) this device may not cause interference, and
(2) this device must accept any interference, including interference that may cause undesired operation of the device.
Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radioexempts de licence. L'exploitation est autorisée aux deux conditions suivantes :
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

This equipment complies with FCC/IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

ce matériel est conforme aux limites de dose d'exposition aux rayonnements, FCC / CNR-102 énoncée dans un autre environnement.cette eqipment devrait être installé et exploité avec distance minimale de 20 entre le radiateur et votre corps.

The user manual for local area network devices shall contain instructions related to the restrictions mentioned in the above sections, namely that:
(i) the device for operation in the band 5150-5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
(ii) the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall comply with the e.i.r.p. limit; and
(iii) the maximum antenna gain permitted for devices in the band 5725-5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

(i)Les dispositifs fonctionnant dans la bande 5150-5250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux.

(ii) le gain d'antenne maximal autorisé pour les appareils dans les bandes 5250-5350 MHz et 5470-5725 MHz doivent respecter le pire limiter; et
(iii) le gain d'antenne maximal autorisé pour les appareils dans la bande 5725-5825 MHz doivent respecter le pire limites spécifiées pour le point-à-point et l'exploitation non point à point, le cas échéant.

Users should also be advised that high-power radars are allocated as primary users (i.e. priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

Les utilisateurs de radars de haute puissance sont désignés utilisateurs principaux (c.-à-d., qu'ils ont la priorité) pour les bandes 5250-5350 MHz et 5650-5850 MHz et que ces radars pourraient causer du brouillage et/ou des dommages aux dispositifs LAN-EL.

EU Conformity Statement

This product is marked with "CE" and comply therefore with the applicable harmonized European standards listed under the Radio Equipment Directive 2014/53/EU.

RF Exposure Information
This device has been tested and meets applicable limits for Radio Frequency (RF) exposure.

The device is restricted to indoor use only when operating in the 5150 to 5350 MHz frequency range.

	BE	EE	HR	IT	CY	LV	LT
	BG	IE	LU	HU	MT	NL	AT
	CZ	EL	PL	PT	RO	SI	SK
	DK	ES	FI	SE	DE	FR	LI
	NO	IS	CH	TR	UK(NI)		

(1) Operational use conditions
***if your module has professional users use condition limitations, please keep below sentence here

Module has professional users use condition limitations, Host product manufacturer please ensure giving such warning like “Product is limited to professional users use” in your product’s instruction.

(2) Antenna used

Antenna Type	Brand/ manufacturer	Model No.	Max. Antenna Gain
Dipole	Shanghai Jesoncom Communication Engineering Co., Ltd	5Q004D	1dBi
Xxx			
Xxx			

(3)Notice to Host Product Manufacturer
Any deviation(s) from the defined parameters of the antenna trace, as described by this instruction, host product manufacturer must notify us that you wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by us, or you (host manufacturer) can take responsibility through the change in FCC ID and IC ID (new application) procedure followed by a Class II permissive change application.

(4)Labelling Instruction for Host Product Integrator
Please notice that if the FCC and IC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains FCC ID: 2APJ4-SLM500" and "Contains IC: 23860-SLM500" any similar wording that expresses the same meaning may be used.

§ 15.19 and RSS-Gen Labelling requirements shall be complied on end user device.
Labelling rules for special device, please refer to *§2.925, § 15.19 (a)(5)* and relevant KDB publications. For E-label, please refer to *§2.935*.
(5)Installation Notice to Host Product Manufacturer
The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.
The module is limited to installation in mobile application, a separate approval is required for all other operating configurations, including portable configurations with respect to §*2.1093* and difference antenna configurations.
(6)Antenna Change Notice to Host manufacturer
If you desire to increase antenna gain and either change antenna type or use same antenna type certified, a Class II permissive change application is required to be filed by us, or you (host manufacturer) can take responsibility through the change in FCC ID and IC ID (new application) procedure followed by a Class II permissive change application.

(7)FCC other Parts, Part 15B Compliance Requirements for Host product manufacturer
This modular transmitter is only FCC authorized for the specific rule parts listed on our grant, host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.
Host manufacturer in any case shall ensure host product which is installed and operating with the module is in compliant with Part 15B requirements.
Please note that For a Class B or Class A digital device or peripheral, the instructions furnished the user manual of the end-user product shall include statement set out in *§15.105 Information to the user* or such similar statement and place it in a prominent location in the text of host product manual. Original texts as following:
For Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
—Reorient or relocate the receiving antenna.
—Increase the separation between the equipment and receiver.
—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
—Consult the dealer or an experienced radio/TV technician for help.

For Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

9.3. Multiplexing function

Table 9.3: Multiplexing Functions

GPIO	Module pin	Reuse function		
		SPI	UART	I2C
0	154		TX	
1	153		RX	
4	94	MOSI	TX	
5	93	MISO	RX	
6	167	CS_N	CTS	SDA
7	168	CLK	RTS	SCL
10	48	CS_N		SDA
11	47	CLK		SCL
12	101	MOSI		
13	102	MISO		
14	92	CS_N		SDA
15	91	CLK		SCL
16	34	MOSI	TX	
17	35	MISO	RX	
18	36	CS_N	CTS	SDA
19	37	CLK	RTS	SCL
20	119	MOSI	TX	
21	118	MISO	RX	
22	117	CS_N	CTS	SDA
23	116	CLK	RTS	SCL
85	265	MOSI		
86	239	MISO		
87	105	CS_N		
88	264	CLK		

Note: Blue is the default function

9.4. Safety Warning

Pay attention to the following safety precautions when using or repairing any terminal or mobile phone that contains modules. The user should be informed of the following safety information on the terminal device. Otherwise, Meig will not be responsible for any consequences caused by the user not following these warning actions.

Table 9.4: Security Warnings

Identification	Claim
	When you are at a hospital or medical facility, observe the restrictions on using your phone. If necessary, please turn off the terminal or mobile phone, otherwise the medical device may malfunction due to radio frequency interference.
	Turn off the wireless terminal or mobile phone before boarding. To prevent interference with the communication system, wireless communication equipment is prohibited on the aircraft. Ignoring the above will violate local laws and may result in a flight accident.
	Do not use mobile terminals or mobile phones in front of flammable gases. Turn off the mobile terminal when you are near an explosion, chemical factory, fuel depot, or gas station. It is dangerous to operate a mobile terminal next to any potentially explosive electrical equipment.
	The mobile terminal receives or transmits radio frequency energy when it is turned on. It can interfere with TV, radio, computer or other electrical equipment.
	Road safety first! Do not use a handheld terminal or mobile phone while driving, please use a hands-free device. Stop before using your handheld terminal or mobile phone.
	GSM mobile terminals operate under RF signals and cellular networks, but are not guaranteed to be connected in all situations. For example, there is no credit or invalid SIM card. When in this situation and need emergency services, remember to use an emergency call. In order to be able to call and receive calls, the mobile terminal must be powered on and in a service area where the mobile signal is strong enough. Emergency calls are not allowed when certain network services or telephony features are in use, such as feature locks, keyboard locks. These functions should be removed before using an emergency call. Some networks require effective SIM card support.

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