SLM336Q Hardware Design Manual

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Revision History

NO	Version number	Time	Author	Reasons for revision
1	V1.00	2023-10	Hardware Department	Initial establishment
2	V1.01	2024-6	Hardware Department	Modify the maximum value of VBAT limit to 5V; Modify PIN1 description comments；Modify Shutdown leakage current；

Content

1 Introduction

This document defines the SLM336Q module and the air interface and hardware interface between module and customer application.

This document can help customers quickly understand SLM336Q module interface specification electrical characteristics mechanical specifications and related product information. With the help of this document, combined with our application manual and user instructions, customers can quickly apply SLM336Q module to wireless applications.

SLM336Q is a wide band wireless terminal product applicable to FDD-LTE multiple frequency bands.

Supported access rates supported by SLM336Q

- FDD-LTE:10Mbps/5Mbps；

Except wireless data access, SLM336Q can be widely used in M2M field, such as OTT, CPE, router, data card, tablet computer, security and industrial PDA.

1.1 Safety Instruction

By following the following safety principles, you can ensure personal safety and help protect products and the working environment from potential damage:

	Driving safety first! When you drive, do not use the handheld mobile terminal device unless it has hands-free function. Please stop and call again!
	Please turn off the mobile terminal before boarding. The wireless function of the mobile terminal shall not be turned on the aircraft to prevent interference with the aircraft communication system. Ignoring this prompt may lead to flight safety and even violate the law.
	In hospitals or health care places, pay attention to whether there are restrictions on the use of mobile terminal equipment. RF interference will lead to abnormal operation of medical equipment, so it may be necessary to turn off the mobile terminal equipment.
	The mobile terminal device cannot be effectively connected under any circumstances. Where there is no phone charge or SIM is invalid in the mobile device. When you encounter the above situations in an emergency, please remember to make an emergency call and ensure that your device is turned on and in an area with sufficient signal strength.
	Your mobile terminal device receives and transmits radio frequency signals when it is turned on. Radio frequency interference may occur when near televisions, radios, computers or other electronic equipment.
	Keep your mobile device away from flammable gases. When you are close to gas stations, oil depots, chemical plants or explosive workplaces, please turn off the mobile terminal equipment. Operating electronic equipment in any place with potential explosion hazard has potential safety hazards.

1.2 Documentation Purposes

This article elaborates the basic functions, main features, hardware interface and its use method, structural characteristics, power consumption index and electrical characteristics of SLM336Q wireless module in detail, and guides users to apply SLM336Q module to various application terminals.

1.3 Content

This document is divided into the following parts:

- Chapter 1, mainly introduces security instructions, document purpose, revision history, etc.
- Chapter 2 describes the basic functions and main features of THE SLM336Q wireless module.
- Chapter 3 describes in detail the functional features and usage of each SLM336Q hardware interface
- Chapter 4, antenna interface related content and matters needing attention;
- Chapter 5, electrical characteristics of SLM336Q are described in detail;
- Chapter 6, the structural features and considerations of SLM336Q are described in detail；
- Chapter 7 describes in detail the storage and production considerations for SLM336Q；
- Chapter 8, Appendix A Reference documents and term abbreviations；

2 Product Overview

2.1 Basic Description

SLM336Q is a wireless communication module that supports FDD-LTE, and can provide voice (PCM) and analog voice SMS for customers.

Table 1 SLM336Q module support frequency band

Internet	SLM336Q
FDD-LTE	B2/B4/B5/B12/B13/B14/B66/B71

SLM336Q adopts an advanced highly integrated design scheme with RF and baseband onto PCB to realize radio transmission, receiving, baseband signal and audio signal processing. It is a single-sided layout, module size: 23.6*19.9* 2.45 mm, which can be widely used in M2M such as OTT,CPE, routers, data CARDS, data card, tablet, security and industrial-grade PDA, etc.

2.2 Main Performance

The following table shows the performance of the SLM336Q module.

Table 2 Lists the main features of the module

Parameters	Explain
Power supply	● VBAT Supply voltage range: 3.5V～4.2V ● Typical supply voltage: 3.8V
Transmitted power	● Class 3 (23dBm±2dB) for FDD-LTE bands
LTE character	● The maximum support CAT1 ● Support 1.4 ~ 20 MHZ radio frequency bandwidth ● FDD: The maximum UL rate is 5Mbps, and the maximum DL rate is 10Mbps
Network protocol characteristics	● TCPIP/UDP/HTTP(S)/MQTT/FTP/SSL/OneNet
Short message service（SMS）	● Text and PDU mode ● point-to-point MO and MT ● Short message storage ● Cell broadcast
USIM port	● Support USIM/SIM: 1.8V & 3V
PCM port（I2S）	● For audio use, external CODEC chip is needed
USB port	● Support USB2.0(Support slave mode), the maximum data transmission rate is 480 Mbps

	● To the AT command, data transmission, software debugging and software upgrades ● USB driver: Support Windows7, Windows 8/8.1, Windows10
Serial port	MAIN_UART/ UART2: ● To AT commands and data transmission ● Baud rate is default 115200bps ● MAIN_UART support RTS and CTS hardware fluid control, UART2 dose not support RTS and CTS hardware fluid control DBGU: ● For debugging, log output ● Baud rate is default115200bps
AT order	● Comply with 3GPP TS 27.007, 27.005, and has a new MeiG AT command
Network indicator	● NET_STATUS pin indicate the state of the network
Antenna port	● Main antenna interface（ANT_MAIN） ● GPS antenna interface ● 50 ω characteristic impedance
Physical property	● Size: 23.6×19.9×2.45mm
Temperature Range	● Normal operating temperature: -35℃～+75℃ ● Extended operating temperature: -40℃～+85℃ ● Storage temperature:-40℃ ~+90℃
Software upgrading	● USB port
RoHS	● All devices comply fully with EU RoHS standards
Port	● 126Pin ,LGA port
LCC functional interface	● power port ● USB2.0 High-Speed port ● UART port ● USIM/SIM port（support 3V、1.8V, USIM2 is compatible with UART2） ● PCM interface(I2S) ● Hardware reset interface ● Pilot light interface ● Flight mode control interface ● ADC port ● I2C port ● SPI port（SPI is compatible with DEBUG_UART） ● USB_BOOT port

2.3 Functional Block Diagram

The following is the block diagram of SLM336Q, illustrating its main functions.

- PMU
- BBU
- Internal memory
- The RF part
- Peripheral interface

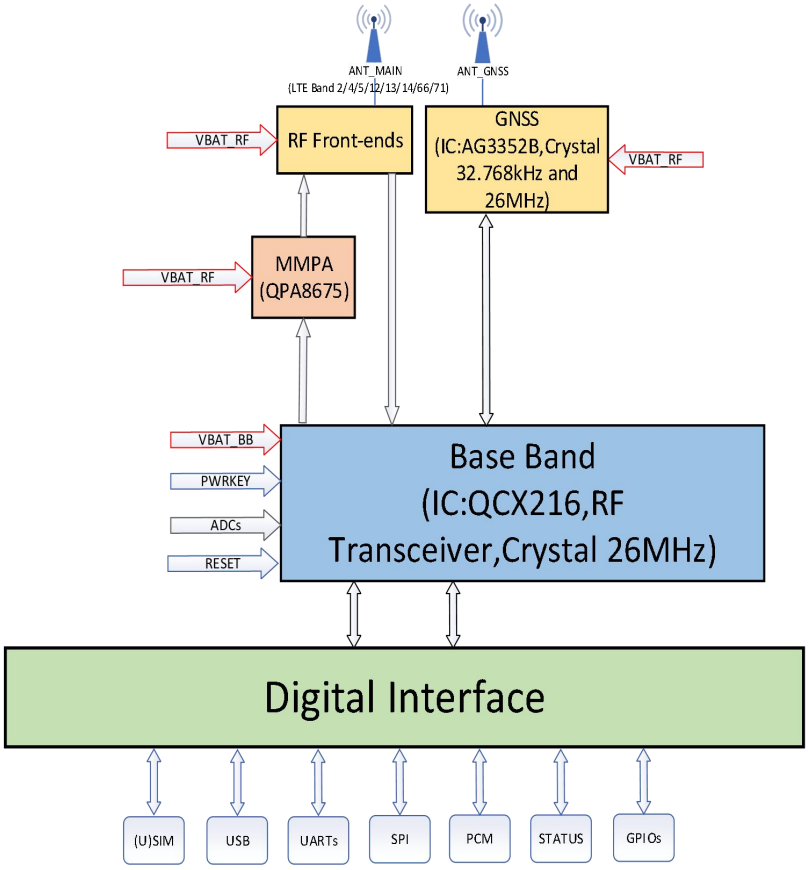


FIG. 1 Functional block diagram

2.4 Evaluation Board

For testing and use of SLM336Q, MeiG provides a set of evaluation board, including USB cables, antennas, and other peripherals.

Please refer to the “SLM336Q_USB_ZB User Manual” for the usage of the evaluation board.

3 Application Interface

3.1 Basic Description

SLM336Q adopts 126 pin LGA, providing the following functional interfaces:

- Power supply
- USB2.0 High-Speed interface（Only slave mode is supported）
- UART port
- USIM/SIM port（support 3V, 1.8V, support 3V、1.8V, USIM2 is compatible with UART2）
- PCM interface(I2S)
- Hardware reset interface
- Pilot light interface
- Flight mode control interface
- ADC port
- I2C port
- SPI port（SPI is compatible with DEBUG_UART）
- USB_BOOT port

3.2 LCC Card Pin Definition

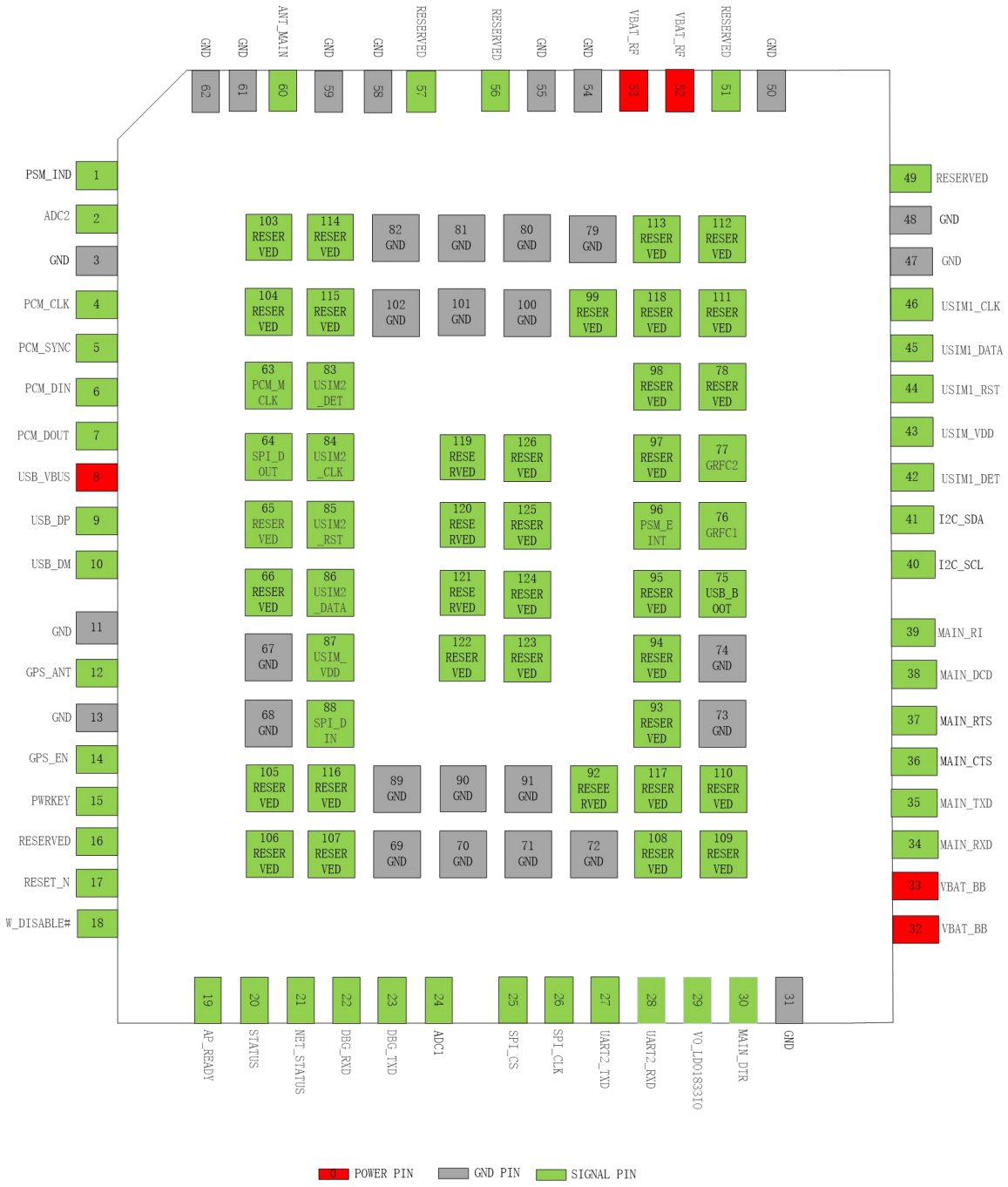


FIG. 2 Pin diagram of module sequence number

3.3 PIN Description

The following table shows the definition of each pin in the SLM336Q module.

Table 3 IO parameter definitions

Type	Description
IO	Input/Output
DI	Digital input signal.
DO	Digital output signal.
OD	Open drain output signal.
AI	Analog input
BOT	Bidirectional open drain output signal
PI	Power input
PO	Power output
G	GND

Table 4 Pin description

Pin Number	Pin Name	I/O	Electrical level	Description	Remark
1	PSM_IND	DO	VOLnom=0V VOHnom=1.8V	Enter PSM mode indication	Used as an indication to enter PSM mode by default;Can be used to pull this pin high from the outside to make the module exit PSM mode.
2	ADC2	AI		General ADC interface Voltage range: 0.1V~1.2V	

				Leave empty if not used	
3	GND	G		GND	
4	PCM_CLK	DI	VILnom=0V VIHnom=1.8V	PCM clock signal Leave empty if not used	
5	PCM_SYNC	DI	VILnom=0V VIHnom=1.8V	PCM frame signal synchronization Leave empty if not used	
6	PCM_DIN	DI	VILnom=0V VIHnom=1.8V	PCM data input signal Leave empty if not used	
7	PCM_DOUT	DO	VOLnom=0V VOHnom=1.8V	PCM data output signal Leave empty if not used	
8	USB_VBUS	AI	Vnorm=5.0V	USB Insertion signal Leave empty if not used	
9	USB_DP	AIO		USB Differential data（+） Leave empty if not used	
10	USB_DM	AIO		USB Differential data（-） Leave empty if not used	
11	GND	G		GND	
12	GPS_ANT	AIO		GPS antenna interface	

13	GND	G		GND	
14	GPS_EN	AIO		GPS Enable	
15	PWRKEY	DI	VILnom=0V VIHnom=VBAT	Power on/off Active at low level	
16	RESERVED			RESERVED	
17	RESET_N	DI	VILnom=0V VIHnom= VBAT	Module reset Active at low level	
18	W_DISABLE#	DI	VILnom=0V VIHnom=1.8V	Flight mode control Leave empty if not used	
19	AP_READY	DI	VILnom=0V VIHnom=1.8V	Application processor sleep state detection Leave empty if not used	
20	STATUS	DO	VOLnom=0V VOHnom=1.8V	Running status indication Leave empty if not used	
21	NET_STATUS	DO	VOLnom=0V VOHnom=1.8V	Network status indication Leave empty if not used	
22	DBG_RXD	DI	VILnom=0V VIHnom=1.8V	DBG UART RXD Leave empty if not used.	This pin is compatible with PIN88. If this pin is used, please leave PIN88 vacant
23	DBG_TXD	DO	VOLnom=0V VOHnom=1.8V	DBG UART TXD Leave empty if not used	This pin is compatible with PIN26. If this pin is used, please leave PIN26

					vacant
24	ADC1	AI		General ADC interface Voltage range: 0.1V~1.2V Leave empty if not used	
25	SPI_CS	DO	VOLnom=0V VOHnom=1.8V	SPI chip selection Leave empty if not used	
26	SPI_CLK	DO	VOLnom=0V VOHnom=1.8V	SPI CLK Leave empty if not used	This pin is compatible with PIN23. If this pin is used, please leave PIN23 vacant
27	UART2_TXD	DO	VOLnom=0V VOHnom=1.8V	UART2 TX Leave empty if not used	UART2 has been used by internal GPS. UART2 and GPS are compatible functions and cannot be used at the same time.
28	UART2_RXD	DI	VILnom=0V VIHnom=1.8V	UART2 RX Leave empty if not used	UART2 has been used by internal GPS. UART2 and GPS are compatible functions and cannot be used at the same time.This pin is compatible with PIN86. If this pin is used, please leave PIN86 vacant
29	VO_LDO1833IO	PO	1.8V	Digital level, 1.8V output, 200mA load capacity Leave empty if not used	

30	MAIN_DTR	DI	VILnom=0V VIHnom=1.8V	The main serial data terminal is ready Leave empty if not used	
31	GND	G		GND	
32	VBAT_BB	PI	Vmax=4.2 Vmin=3.5V Vnorm=3.8V	Module BB power	
33	VBAT_BB	PI	Vmax=4.2 Vmin=3.5V Vnorm=3.8V	Module BB power	
34	MAIN_RXD	DI	VILnom=0V VIHnom=1.8V	Main UART RX Leave empty if not used	
35	MAIN_TXD	DO	VOLnom=0V VOHnom=1.8V	Main UART TX Leave empty if not used	
36	MAIN_CTS	DO	VOLnom=0V VOHnom=1.8V	Main UART clear send Leave empty if not used	
37	MAIN_RTS	DI	VILnom=0V VIHnom=1.8V	Main UART Request to send data Leave empty if not used	
38	MAIN_DCD	DO	VOLnom=0V VOHnom=1.8V	Main UART output carrier detection Leave empty if not used	
39	MAIN_RI	DI	VILnom=0V VIHnom=1.8V	Main serial port output ringing prompt Leave empty if not used	
40	I2C_SCL	OD	VOLnom=0V VOHnom=1.8V	I2C serial clock Leave empty if not used	2.2K pull-up is used inside the module to 1.8V

41	I2C_SDA	OD	VOLnom=0V VOHnom=1.8V	I2C serial data Leave empty if not used	
42	USIM1_DET	DI	VILnom=0V VIHnom=1.8V	(U)SIM1 Hot swap detection signal the software turns off the detection function by default Leave empty if not used	
43	USIM_VDD	PO	1.8V/3.0V	(U)SIM1 Power	
44	USIM1_RST	DO	1.8V/3.0V	(U)SIM1 reset signal	
45	USIM1_DATA	DIO	1.8V/3.0V	(U)SIM1 data signal	
46	USIM1_CLK	DO	1.8V/3.0V	(U)SIM1 clock signa	
47	GND	G		GND	
48	GND	G		GND	
49	RESERVED			RESERVED	
50	GND	G		GND	

51	RESERVED			RESERVED	
52	VBAT_RF	PI	Vmax=4.2 Vmin=3.5V Vnorm=3.8V	Module RF power	
53	VBAT_RF	PI	Vmax=4.2 Vmin=3.5V Vnorm=3.8V	Module RF power	
54	GND	G		GND	
55	GND	G		GND	
56	RESERVED			RESERVED	
57	RESERVED			RESERVED	
58	GND	G		GND	
59	GND	G		GND	
60	ANT_MAIN	AIO		Main antenna interface	
61	GND	G		GND	
62	GND	G		GND	

63	PCM_MCLK	DI		PCM master clock Leave empty if not used	
64	SPI_DOUT	DO	VOLnom=0V VOHnom=1.8V	SPI Main mode output Leave empty if not used	
65	RESERVED			RESERVED	
66	RESERVED			RESERVED	
67~74	GND	G		GND	
75	USB_BOOT	DI	VILnom=0V VIHnom=1.8V	Emergency download mode control	Do not pull up before starting the module.
76	GRFC1	DO	VOLnom=0V VOHnom=1.8V	Universal radio frequency control 1 Leave empty if not used	
77	GRFC2	DO	VOLnom=0V VOHnom=1.8V	Universal radio frequency control 2 Leave empty if not used	
78	RESERVED			RESERVED	
79~82	GND	G		GND	
83	USIM2_DET*	DI	VILnom=0V VIHnom=1.8V	(U)SIM2Hot swap detection signal the software turns off the detection function by default Leave empty if	

				not used	
84	USIM2_CLK	DO	1.8V/3.0V	(U)SIM2 clock signal	
85	USIM2_RST	DO	1.8V/3.0V	(U)SIM2 reset signal	
86	USIM2_DATA	DIO	1.8V/3.0V	(U)SIM2 data signal	This pin is compatible with PIN28. If this pin is used, please leave PIN28 vacant
87	USIM_VDD	PO	1.8V/3.0V	(U)SIM2 Power	
88	SPI_DIN	DI	VILnom=0V VIHnom=1.8V	SPI Main mode input Leave empty if not used	This pin is compatible with PIN22. If this pin is used, please leave PIN22 vacant
89~91	GND	G		GND	
92~95	RESERVED			RESERVED	
96	PSM_EINT	DI	VILnom=0V VIHnom=1.8V	PSM Interrupt pin	Pull external high level to exit PSM
97~99	RESERVED			RESERVED	

100~102	GND	G		GND	
103~126	RESERVED			RESERVED	

Remark:

1. * means that the function is under development;

2. The above interface functions are not supported at the same time, some pins are multiplexed functions, please pay attention when selecting.

3. SLM336Q pin multiplexing is presented in the document “SLM336Q_GPIO Function Multiplexing”

3.4 Power

Table 5 Description of SLM336Q module power interface

Pin Name	I/O	Pin	Description
VBAT_BB	PI	32, 33	Module BB power supply, 3.5~4.2V, typical value 3.8
VBAT_RF	PI	52, 53	Module RF power supply, 3.5~4.2V, typical value 3.8
VO_LDO1833IO	PO	29	Voltage output, 1.8V, 200mAloading capacity
GND	G	3,11,13,31,47,48,50,54,55,58,59,61,62,67~74,79~82,89~91,100~102	GND

3.4.1 Power Supply

SLM336Q is supplied power through VBAT pin. The power design recommendation is shown in Figure 3

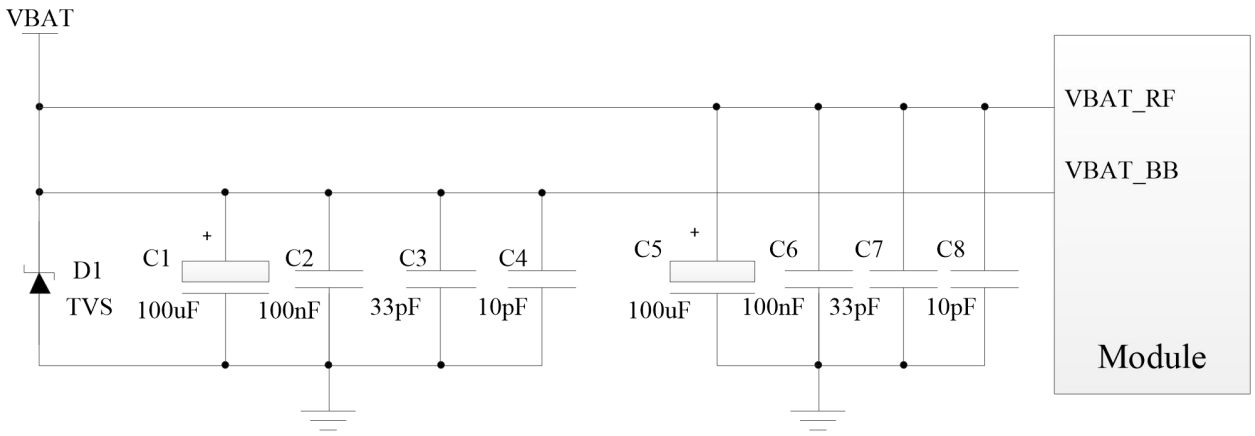


FIG. 3 Module power supply circuit

Remarks: The VBAT power supply needs star-shaped wiring to VBAT_BB and VBAT _RF, and the width of VBAT_RF wiring should be no less than 2.5mm. VBAT in subsequent documents includes VBAT_BB and VBAT_RF.

3.4.2 Reduce Voltage Drop

SLM336Q power supply range of 3.5 V ~ 4.2 V. During data transmission or calls, instantaneous high-power transmission will form a current peak value of up to 2A, which will cause large ripples in VBAT. The module will reboot or shut down. In order to ensure normal operation, the power supply must have sufficient power supply capacity, and the input voltage should not be lower than 3.5V.

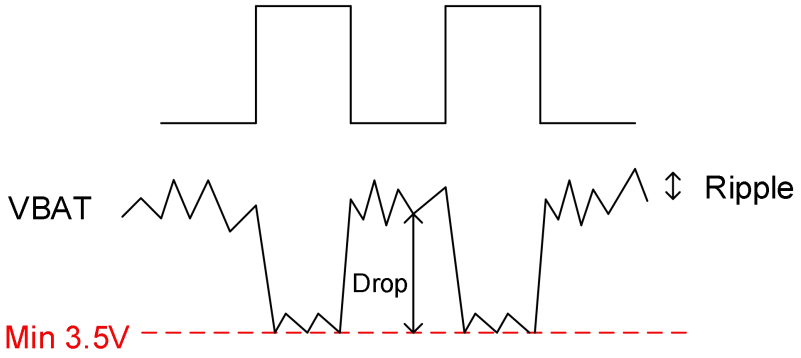


FIG. 4 Burst transmission power requirements

To reduce voltage drop, a 100uF filter capacitor with low ESR is required. MLCC has the best ESR. It is recommended to add 3 ceramic capacitors (100nF, 33pF, 10pF) to VBAT_BB and VBAT_RF pins, and the capacitors should be placed close to VBAT pins. At the same time, in order to ensure better power supply performance, a TVS tube is added near the input end of the module VBAT to improve the module's electrostatic bearing capacity. When the external power supply is connected to the module, VBAT_BB and VBAT_RF need to adopt star wiring. VBAT_BB wire width shall not be less than 2mm, and VBAT_RF wire width shall not be less than 2.5mm. In principle, the longer the line in VBAT, the wider the line.

3.4.3 Power Supply Reference Circuit

The design of the module power supply is very important, because the performance of the module depends largely on the power supply. The SLM336Q must select a power source that provides at least 2A current capability. If the voltage difference between the input voltage and the module supply voltage is not very large, it is recommended to choose LDO as the supply. If there is a large voltage difference between the input and output voltages, DCDC is recommended as the power supply for the module.

The figure below is the reference design of + 5V power supply circuit. The LDO of Micrel company is used in the design, and the model is MIC29302WU. The load current is 3A and the output voltage is 3.9V.

Note: that MIC29302WU has the requirement of minimum load current ≥ 10mA:

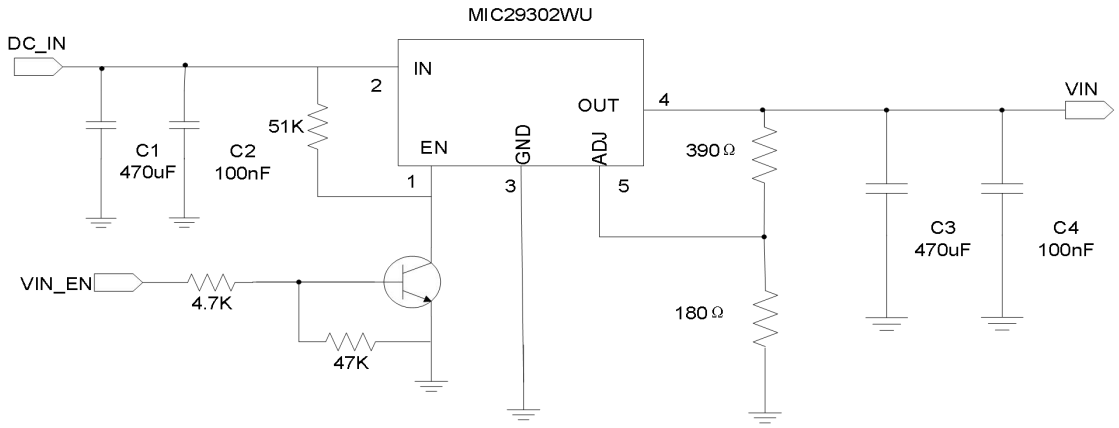


FIG. 5 Reference design for power supply input

3.4.4 VDD_EXT Voltage Output

When SLM336Q normally boot, the voltage of output Pin29 is 1.8v as well as current load is 200mA. This output voltage can be used as an external pull-up source, such as a level reference, and the Pin status can be detected whether the module power on or not.

Table 6 Description of SLM336Q module 1.8V voltage output interface

Pin Name	I/O	Pin	Description
VO_LDO1833IO(VDD_1V8)	PO	29	1.8V voltage output

3.5 Switch Machine

3.5.1 PWRKEY Pin boot

Table 7 Description of SLM336Q module 1.8V voltage output interface

Pin Name	I/O	Pin	Description
PWRKEY	DI	15	power on/off

When SLM336Q stays at shutdown mode, the module can be waked up through pulling down the PWRKEY for at least 2s. It is recommended to use an open set drive circuit to control PWRKEY pins. The reference circuit shows following:

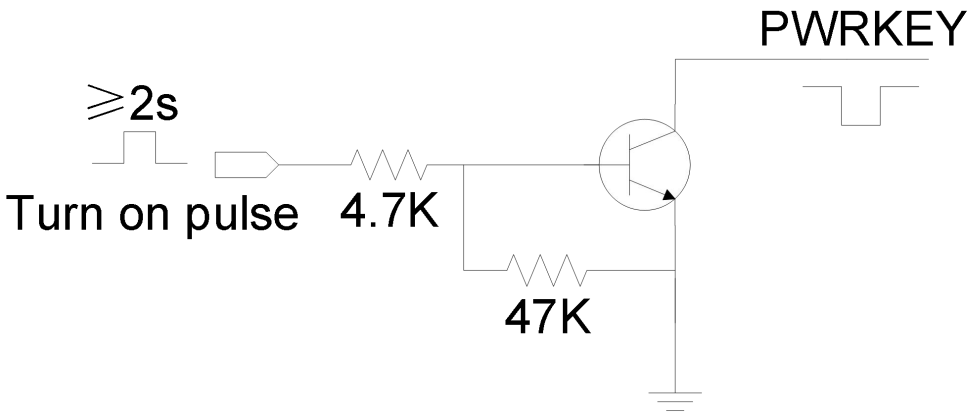


FIG. 6 Open set drive reference boot circuit

Another way to control the PWRKEY pin is through a switch button. A TVS is placed near the button for ESD protection. The reference circuit shows below:

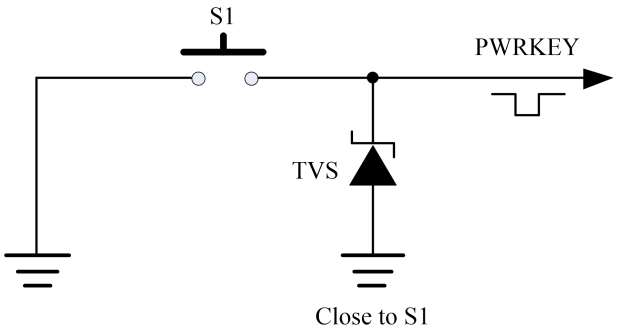


FIG. 7 Button startup reference circuit

The boot sequence is shown in the figure below:

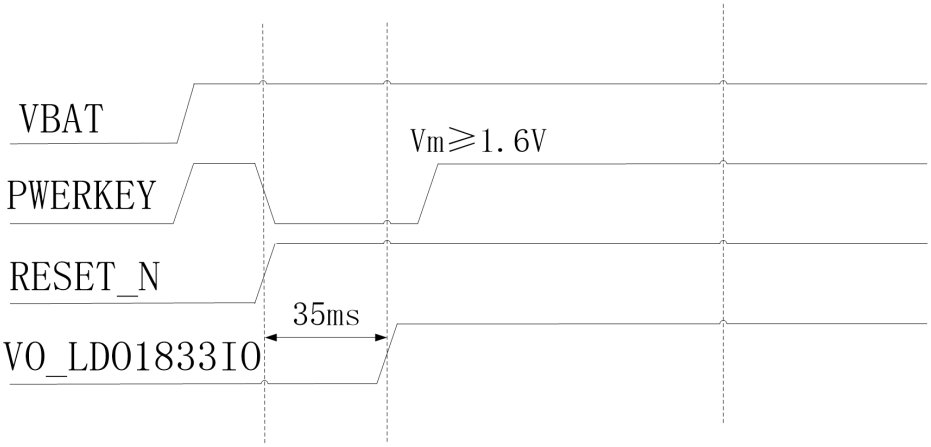


FIG.1 Power-on sequence diagram

Remarks:

Before pulling down PWRKEY pin, VBAT voltage should be stable indeed. It is recommended that the time interval between powering up VBAT and pulling down PWRKEY pins should be no less than 30ms.

If the module needs to be powered on and started automatically, PWRKEY pin can be directly pointed to the ground. The resistance value to earth should not exceed 1k at most. It is recommended to use 0R. This way the module is shut down, only direct power off.

3.5.2 Shutdown

Table 8 Description of two shutdown modes of the module:

Shutdown method	Shutdown step	Applicable scene
Low voltage shutdown	When VBAT voltage is too low or power is lost, the module will shut down	At this point, the module did not carry out the normal shutdown process, did not follow the process of logout from the base station
Hardware shutdown	Pull down PWRKEY(greater than 3. s) and release	Normal_shutdown

Remarks:

1. When the module is working normally, do not immediately cut off the power supply of the module to avoid damaging the Flash data inside the module. It is strongly recommended to close the module through the AT command before disconnecting the power.

2. When using the AT command to shut down, make sure that PWRKEY is in a high level state, otherwise, the module will start up again automatically after the shutdown is completed

3.6 Reset

There are two SLM336Q reset modes: hardware reset and AT command reset.

3.6.1 Hardware Reset

When the module is working, lower the RESET_N pin by at least 150ms to reset the module. RESET_N signal is sensitive to interference, so it suggests that the routing on the module interface board should be as short as possible and should be processed in package.

The reference circuit is similar to the PWRKEY control circuit, and the customer can control the RESET_N pin using an open set drive circuit or a button.

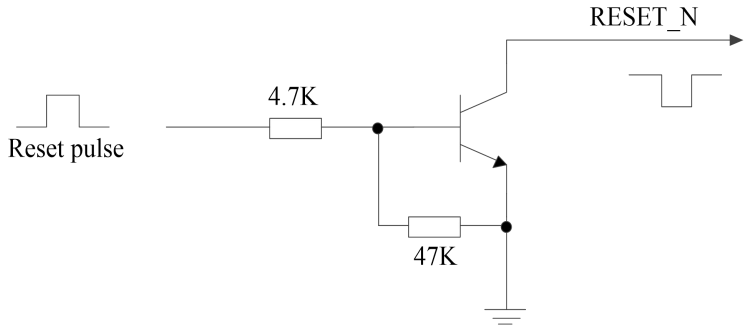


Figure 9. RESET_N reset the open set reference circuit

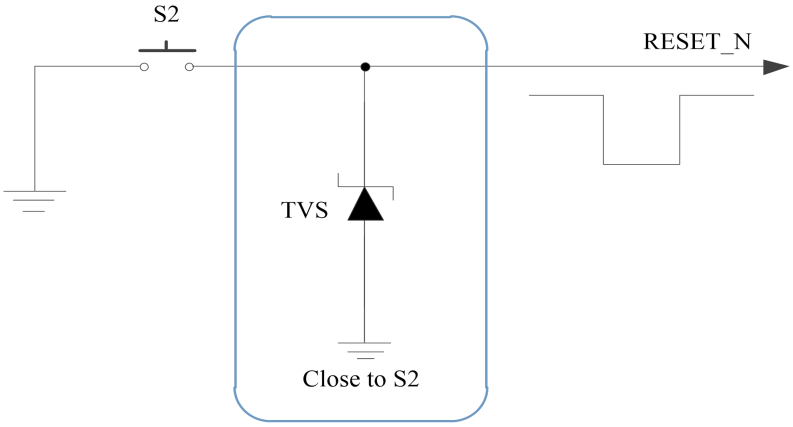


Figure 10 RESET_N reset button reference circuit

The reset sequence diagram is as follows:

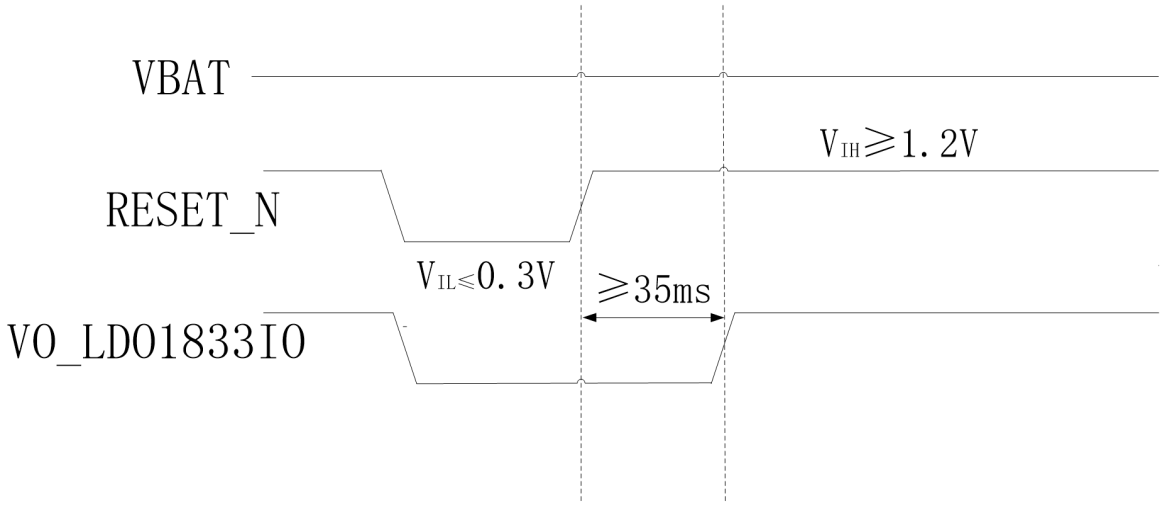


Figure 11 RESET_N reset sequence diagram

3.6.2 AT Command Reset

Through SLM336Q UART or USB AT port, enter AT+TRB command, make SLM336Q reset and restart.

3.7 USIM/SIM Port

SLM336Q supports 1.8V and 3.0V USIM/SIM CARDS.

Table9 USIM/SIM interface description

Pin Name	I/O	Pin	Pin Description
USIM_VDD	43/87	PO	(U)SIM1 Power
USIM1_DATA	45	DIO	(U)SIM1 data signal
USIM1_CLK	46	DO	(U)SIM1 clock signal
USIM1_RST	44	DO	(U)SIM1 reset signal
USIM1_DET	42	DI	(U)SIM1 Hot swap detection signal
USIM2_DATA	86	DIO	(U)SIM2 data signal
USIM2_CLK	84	DO	(U)SIM2 clock signal
USIM2_RST	85	DO	(U)SIM2 reset signal
USIM2_DET*	83*	DI	(U)SIM2 Hot swap detection signal

SLM336Q supports USIM/SIM card hot-plugging function through USIM_DET pin and supports low level detection. After USIM/SIM card is inserted in the figure, USIM_DET pin is at low level. When USIM_DET pin is at high level, no card is detected.

The USIM/SIM card hot swap function can be configured by the “AT+SIMHOTSWAP" command. The instructions of the AT command are shown in the following table:

Table 10 Description of USIM/SIM card hot-plug function setting

AT Command	USIM/SIM card hot swap detection	Function Description
AT+SIMHOTSWAP=1	open	By default, the USIM/SIM card hot-plug detection function is on, and the module detects whether the SIM card is inserted through the USIM_DET pin status
AT+SIMHOTSWAP=0	close	The USIM/SIM card hot-plug detection function is turned off. The USIM/SIM card will be read by the module when the machine is turned on. The USIM_DET status will not be detected

When the USIM_DET is low level, the module will execute the USIM/SIM card initializer when it detects the SIM card insertion. After reading the USIM/SIM card information, the module will register the network. When USIM_DET is high power, the module determines that the USIM/SIM card is pulled out and the USIM/SIM card will not be read. USIM_DET defaults to a low trigger level, which can be set using the AT command.

Table 11 Description of SLM336Q module 1.8V voltage output interface

AT Command	Function Description
AT+GTSET=1	High level detection
AT+GTSET=0	Default, low level detection

The circuit design shows in the follow figure, with USIM/SIM card hot swap function.

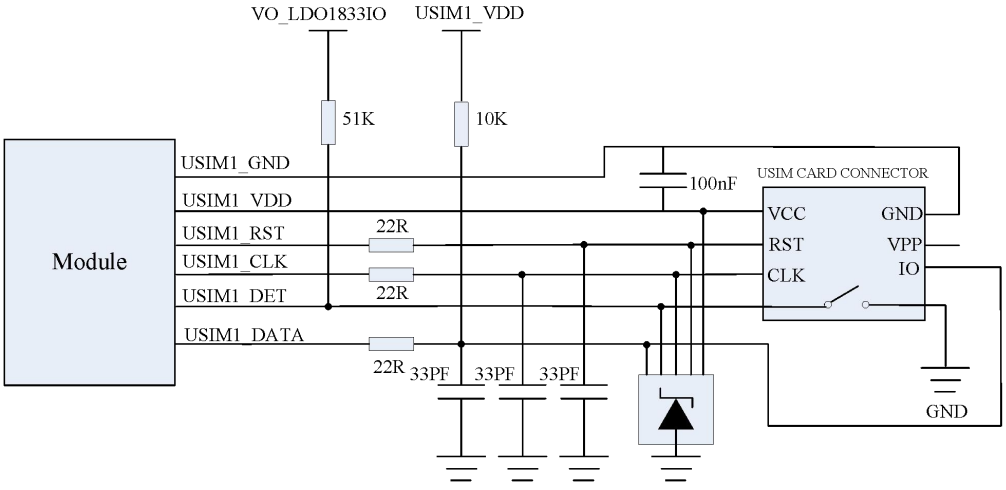


FIG. 12 Reference design drawing of the booth with hot-plug function

If you do not need USIM/SIM card hot-plug detection, keep the USIM1_DET pin dangling, log off the

USIM/SIM interrupt detection pin. The reference circuit is as follows::

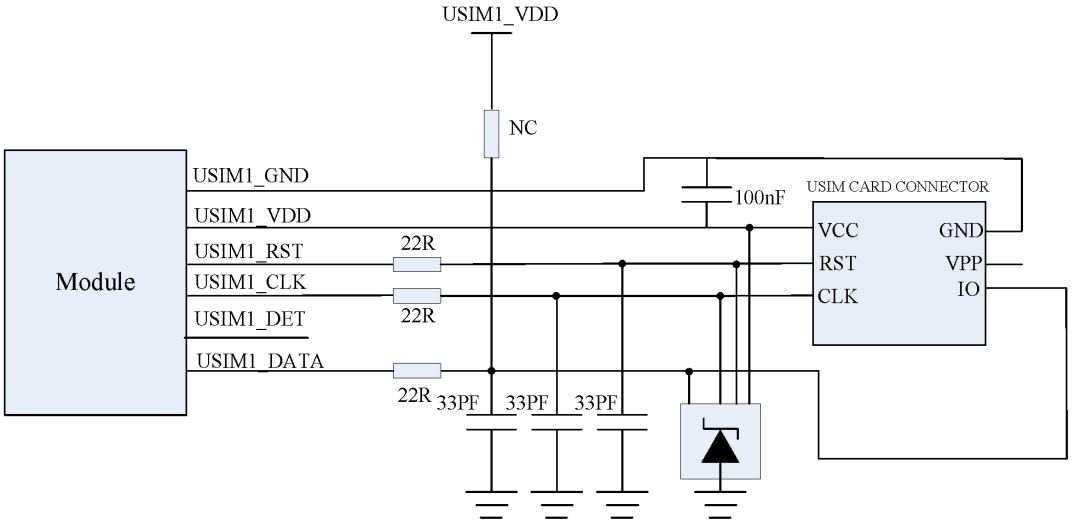


FIG. 13 Reference design drawing of the booth without hot-plugging function

In the circuit design of USIM card interface, in order to ensure the good performance and reliability of USIM card, the following design principles are recommended in the circuit design:

- In USIM_DATA USIM_CLK and USIM_RST lines on a 22Ω resistance, used to suppress the spurious EMI, enhance ESD protection, and convenient debugging;
- In order to improve the antistatic ability, TVS are added on USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST lines, ESD protection devices with parasitic capacitance no more than 15Pf;
- 33pF capacitors in parallel on USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST lines are used to filter out interference. The peripheral devices of the USIM card shall be placed as close as possible to the USIM booth;
- USIM booth is placed close to the module to ensure that the wiring length of USIM card signal line does not exceed 100mm;
- SIM card signal lines are wired away from RF lines and VBAT power lines;
- In order to prevent USIM_CLK signals from crosstalk with USIM_DATA, the two wires should not be too close together and an additional shielding should be added between the two wires.

3.8 USB Interface

The SLM336Q provides a USB interface conforming to the USB 2.0 standard. This interface is used for AT command interaction, data transfer, software debugging and version upgrading, etc.

3.8.1 USB Pin Description

The SLM336Q module provides a USB2.0 interface.

Table 12 DESCRIPTION of USB interface

Pin Name	I/O	Pin	Description
USB_VBUS	AI	8	USB Insert the test
USB_DP	AIO	9	USB Differential data +
USB_DM	AIO	10	USB Differential data -
GND	G	3,11,13,31,47,48,50,54,55,58,59,61,62,67~74 ,79~82,89~91,100~102	GND

3.8.2 USB Reference Circuit

The SLM336Q module USB interface application reference circuit is shown in the figure below.

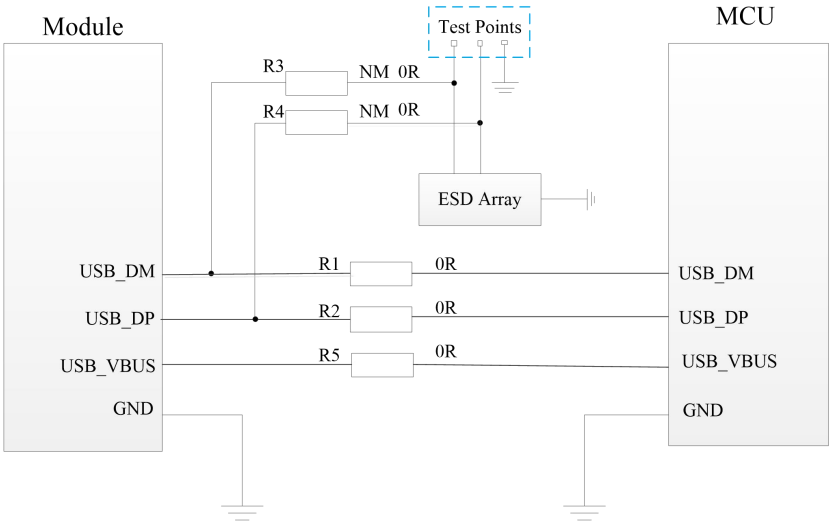


Figure 14. Refer to the design of the USB interface

In order to meet the signal integrity requirement of USB data line, R1/R2/R3/R4 resistors must be placed close to the module and between resistors close to each other. The branch connecting the test point must be as short as possible.

In USB interface circuit design, to ensure USB performance, the following principles are recommended in circuit design:

- The module USB_VBUS is not used to power the module, but to detect USB insertion and unplugging;
- In order to reduce the USB high speed data transmission of signal interference, in USB_DM USB_DP interface circuit and concatenated R1 and R2 can improve the accuracy

of data transmission, 0 Ω R1 and R2 are recommended;

- In order to improve the antistatic performance of USB interface, ESD protective devices are recommended to be added to USB_DP and USB_DM interface circuits, and ESD devices with junction capacitance less than 1pF are recommended. USB ESD protection device should be placed as close as possible to USB interface;
- In order to ensure the USB work reliable, the design still need more consideration to the protection of USB, such as the Layout of the protection of the USB, need to do to USB_DP and USB_DM 90 Ω impedance control, strictly in accordance with the requirements of the differential line, as far as possible away from the interference signal;
- Do not use USB cable under crystal oscillator, oscillator, magnetic device and RF signal. It is recommended to use inner differential wiring and wrap the ground left, right, up and down.

3.9 Serial Port

SLM336Q module has three serial ports: main serial port MAIN_UART, UART2, DEBUG UART. The main features of the main serial port MAIN_UART, UART2, DEBUG UART are described below.

- The main serial port supports 4800Bps, 9600bps, 19200Bps, 38400Bps, 57600bps, 115200Bps, 230400bps, 460800bps, 92160bps baud rate. The default baud rate is 115200bps for data transmission and AT command transmission.
- Debugging serial port support 115200bps baud rate, for r & D debugging use.
- UART2 is used as an auxiliary serial data communication.

Table 13 Main serial port pin description

Pin Name	I/O	Pin	Description
MAIN_RI	DO	39	Main serial port output ringing prompt
MAIN _DCD	DO	38	Main UART output carrier detection
MAIN _RTS	DI	37	Main UART Request to send data
MAIN _CTS	DO	36	Main UART clear send
MAIN _DTR	DI	30	The main serial data terminal is ready
MAIN _TXD	DO	35	Main UART TX
MAIN _RXD	DI	34	Main UART RX

Table 14 Description of UART2 port pin

Pin Name	I/O	PIN	Description
UART2_TXD	DO	27	UART2 TX
UART2_RXD	DI	28	UART2 RX

Table 15 Description of debugging serial port pin

Pin Name	I/O	PIN	Description
DBG_RXD	DI	22	DBG_UART RX
DBG_TXD	DO	23	DBG_UART TX

Table 16 Serial port logic level

Parameter	Min value	Max value	Units
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The serial port level of SLM336Q module is 1.8V. If the client host is 3.3V, the level converter needs to be added in the serial port application. TXB0104PWR of TI is recommended. The following picture is a reference design:

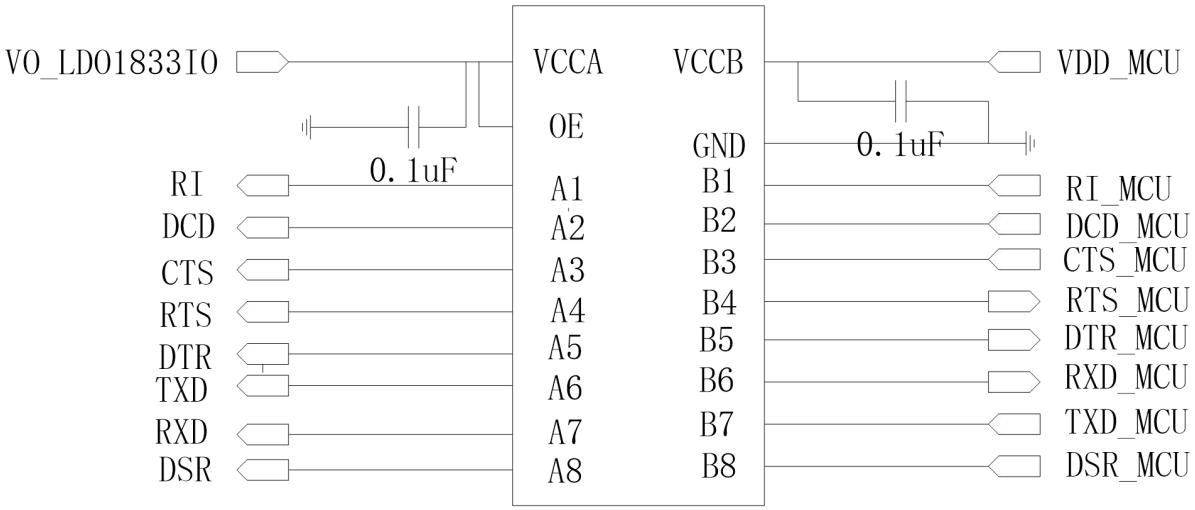


FIG. 15 Level conversion chip reference circuit

Another level conversion circuit is shown in the figure below. The input and output circuit design of the following dotted line section can refer to the solid line section, but pay attention to the connection direction. At the same time, this level conversion circuit is not suitable for applications with baud rate over 460Kbps.

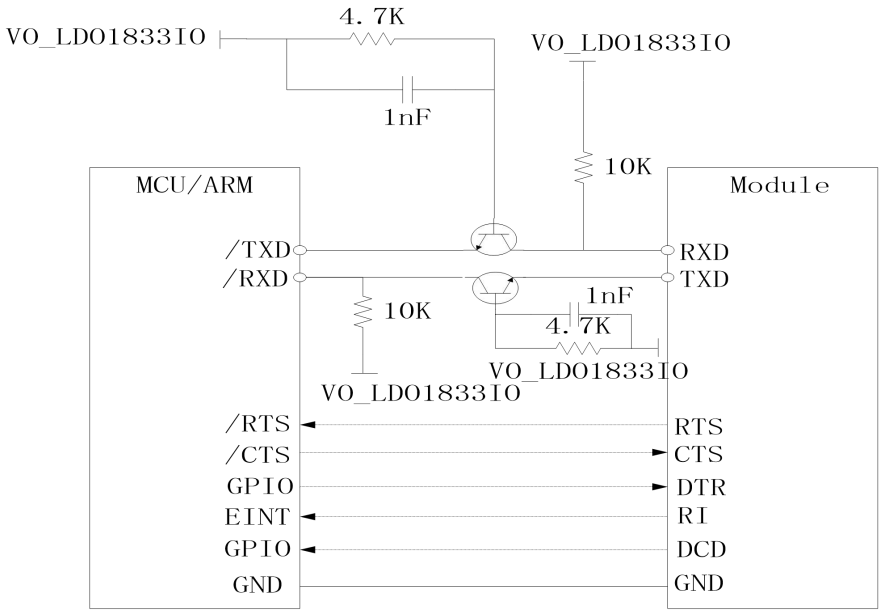


FIG. 16 UART signal connection

Note: During design, it is recommended to reserve 0R resistance and parallel capacitor positions on the main serial port and debug serial port circuit, which can be added to the baseplate to prevent RF interference.

3.10 Status Indication

The status indicator pin is mainly used to drive network status indicator light. SLM336Q module has NET_STATUS and STATUS two network STATUS pins. The following two tables describe the pin

definition and logic level changes in different network states.

Table 17 Description of network indicator pins

Pin Name	I/O	Pin	Description
STATUS	DO	20	Running status indication
NET_STATUS	DO	21	Network status indication

Table 18 Network indicates the working status of pins

Pin Name	Pin working state	Indicated working state
NET_STATUS	High level	Register LTE network status
	Low level	Else

The reference circuit is shown in the figure below:

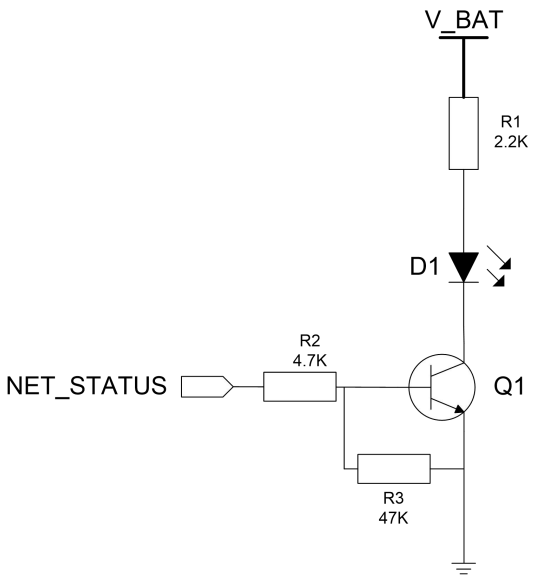


Figure 17 Network indication reference design drawing

NET_STATUS is used to indicate the working state of the module. The customer can connect this

pin to the pull-up GPIO on the device tape. When the module is turned on normally, the default high impedance state of NET_STATUS is.

3.11 Low Power Mode

3.11.1 Flight Mode

Table 19 W_DISABLE# pin descriptions:

Pin Name	I/O	Pin	Description
W_DISABLE#	DI	18	Flight mode control

SLM336Q module supports two ways to enter flight mode:

Table20 Description of flight mode Settings

1	Hardware I/O interface button control	W_DISABLE# for high or hovering (default is pull-up) is normal mode, and low is flight mode
2	AT command control	AT+CFUN=0-- go into airplane mode AT+CFUN=1-- go into normal mode

3.11.2 ULPS

Use AT instruction to put the module into ultra-low power mode (for power test)

3.12 ADC Mode

SLM336Q provides a two-way 12-bit analog-digital conversion interface, and the ADC voltage range is 0-1.2V.

Table 21 ADC pin description

Pin Name	I/O	Pin	Description
ADC1	AI	24	Analog to digital converter interface 1
ADC2	AI	2	Analog to digital converter interface 2

Remark:

1. In the case that VBAT is not powered, the ADC interface cannot directly connect any input

voltage

2. It is recommended that the ADC pin be input with voltage divider circuit.

3. It is suggested that ADC should be wrapped when wiring, which can improve the accuracy of ADC voltage measurement.

3.13 USB_BOOT Interface

SLM336Q supports USB_BOOT. The client can shorten USB_BOOT and VO_LDO1833IO before starting the module, and then the module will enter the forced download mode. In this mode, the module can be upgraded via USB interface.

Table 22 USB_BOOT pin definition

Pin Name	I/0	Pin	Description
USB_BOOT	DI	75	Short connect USB_BOOT and VO_LDO1833IO before starting the module, and then the module will enter the forced download mode
VO_LDO1833IO	PO	29	

3.14 PCM Interface

Table 23 PCM pin definition

Pin Name	I/0	Pin	Description
PCM_CLK	DI	4	PCM clock signal Leave empty if not used
PCM_SYNC	DI	5	PCM frame signal synchronization Leave empty if not used
PCM_DIN	DI	6	PCM data input signal Leave empty if not used
PCM_DOUT	DO	7	PCM data output signal Leave empty if not used
PCM_MCLK	DI	63	PCM master clock

			Leave empty if not used

3.15 I2C Interface

Table 24 I2C pin definition

Pin Name	I/0	Pin	Description
I2C_SCL	OD	40	I2C serial clock Leave empty if not used
I2C_SDA	OD	41	I2C serial data Leave empty if not used

3.16 SPI Port

SPI interface communicates with peripherals through synchronous duplex serial mode. The working voltage is 1.8V. When the universal 4-wire SPI interface is used to connect to Nor Flash, it supports basic operations such as reading, writing, erasing, etc., and needs to be erased and protected by itself. It does not support the file system and can only be stored.

Table 25 SPI pin definition

Pin Name	I/0	Pin	Description
SPI_CLK	DO	26	SPI CLK Leave empty if not used
SPI_CS	DO	25	SPI chip selection Leave empty if not used
SPI_DIN	DI	88	SPI input Leave empty if not used
SPI_DOUT	DO	64	SPI output

			Leave empty if not used

3.17 Function Multiplexing Interface

Table 26 Pin definition of multiplexing function

Pin Name	Pin	Default mode	Mode 0	Mode 1	Mode 2	Mode 3
PSM_IND	1	AGPIO7	GPIO27			
PCM_CLK	4	I2S0_BCLK	GPIO29	I2S0_BCLK		I2S0_BCLK
PCM_SYNC	5	I2S0_LRCK	GPIO30	I2S0_LRCK		I2S0_LRCK
PCM_DIN	6	I2S0_DIN	GPIO31	I2S0_DIN		I2S0_DIN
PCM_DOUT	7	I2S0_DOUT		I2S0_DOUT	I2S2_MCLK	I2S0_DOUT
W_DISABLE#	18	AGPIOWU0	GPIO20			
AP_READY	19	AGPIOWU2	GPIO22			
STATUS	20	AGPIO6	GPIO26			
NET_STATUS	21	AGPIO3	GPIO23			
DEBUG_RXD/ SPI_DIN	22/88	GPIO14	GPIO14	SPI1_MISO		UART0_RXD
DEBUG_TXD/SPI_CLK	23/26	GPIO15	GPIO15	SPI1_SCLK		UART0_TXD
SPI_CS	25	GPIO12	GPIO12	SPI1_SSn0	I2C0_SDA	UART0_RTSn
UART2_TXD	27	GPIO7	GPIO7/Counter3	I2S1_DOUT/ CAM_SPI_D		UART2_TXD
UART2_RXD/USIM2_DATA	28/86	GPIO6	GPIO6/Counter2	I2S1_DIN/CAM_SPI_DATA0		UART2_RXD
MAIN_DTR	30	GPIO2	GPIO2/Counter0		UART1_DTRn	

MAIN_RXD	34	GPIO18	GPIO18	UART1_RXD		
MAIN_TXD	35	GPIO19	GPIO19	UART1_TXD		
MAIN_CTS	36	GPIO16	GPIO16	UART1_RTSn	I2C0_SDA	UART0_RXD
MAIN_RTS	37	GPIO17	GPIO17	UART1_CTSn	I2C0_SCL	UART0_TXD
MAIN_DCD	38	GPIO3	GPIO3/Counter1	I2S1_MCLK/CAM_MCLK	UART1_DCDn	
MAIN_RI	39	AGPIO4	GPIO24			
I2C_SCL	40	SWCLK1	SWCLK1		I2C0_SCL	UART2_DTRn
I2C_SDA	41	SWDIO1	SWDIO1	I2S2_MCLK	I2C0_SDA	UART2_DCDn
USIM1_RST	44	USIM_RSTn	USIM_RSTn			
USIM1_DATA	45	USIM_IO	USIM_IO			
USIM1_CLK	46	USIM_CLK	USIM_CLK			
PCM_MCLK	63	I2S0_MCLK		I2S0_MCLK	I2S0_MCLK	
SPI_DOUT	64	GPIO13	GPIO13	SPI1_MOSI	I2C0_SCL	UART0_CTSn
USB_BOOT	75	GPIO0	GPIO0			
SPI_DIN	76	FEM3[1]	FEM3			
USIM2_CLK	84	GPIO5	GPIO5	I2S1_LRCK/CAM_CS	I2C1_SCL	
USIM2_RST	85	GPIO4	GPIO4	I2S1_BCLK/CAM_SPI_C	I2C1_SDA	ONEW

Remarks: "*" means under development.

4 Antenna Interface

SLM336Q module design interface, there are two antenna, the antenna impedance 50Ω.

Table 27 Definition of pin of antenna interface

Pin Name	Pin Number	Description	I/O	Remark
ANT_MAIN	60	main antenna port	IO	50Ω impedance
GPS_ANT	12	GPS antenna interface	IO	50Ω impedance

4.1 Antenna Interface

SLM336Q provides two antenna pins: ANT_MAIN and GPS_ANT to improve the product's FDD-LTE transceister performance. Recommend users to use with the module, RF connector match 50 Ω impedance of the antenna.

Remark:

In order to ensure the communication capability of all frequency bands, please connect all antennas.It is recommended that applications carefully select RF wiring. RF wiring needs to be selected with minimal loss. RF wiring for RF loss requirements is recommended as follows:

- FDD-LTE<1.2dB；
- GNSS<1.0dB.

4.2 RF Reference Circuit

4.2.1 Antenna Connection Reference Design

The reference circuit for antenna connection of ANT_MAIN, GPS_ANT is shown in the figure below. In order to obtain better RF performance, the following four points should be paid attention to when designing schematic diagram and PCB layout:

1. Schematic design, near the module RF port reserved π type matching circuit, capacitor default not attached;
2. Schematic design, redundant RF connectors between the RF port of the module and the antenna, used for certification test, RF connectors are not attached after mass production and delivery; (Reference: RF Connector C88P132-00001-H);
3. Schematic design, π type matching circuit is reserved near the antenna end, capacitor is not affixed by default;
4. PCB layout, Module RF port to the antenna between lines as short as possible, and need to plate factory for RF line do 50 Ω impedance control.

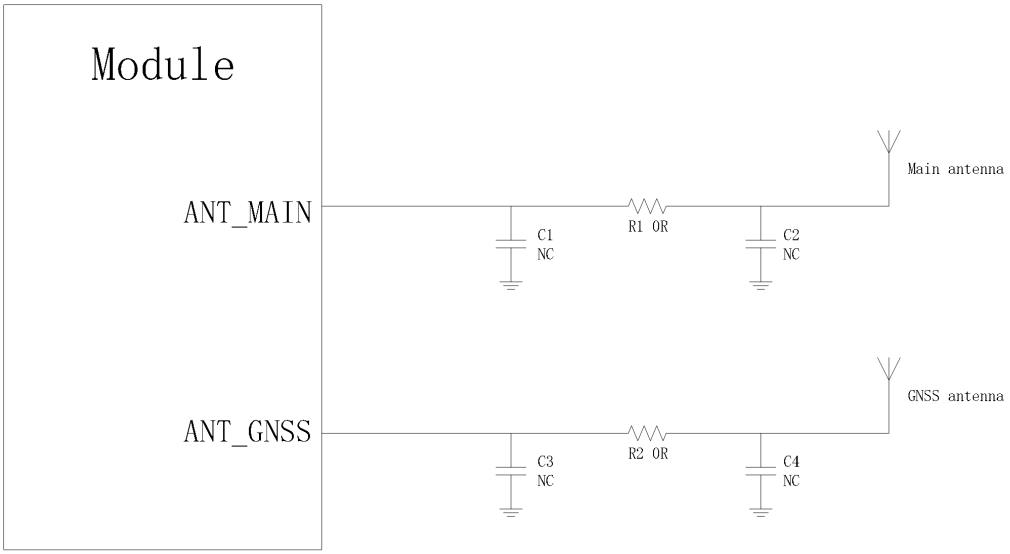


FIG. 19 Rf reference circuit

4.2.2 RF Signal Line Layout

For user PCB, the characteristic impedance of all RF signal lines should be controlled at 50ω. Generally, the impedance of RF signal line is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S), and the height (H) of the reference ground plane. The characteristic impedance of PCB is usually controlled by microstrip line and coplanar waveguide. In order to embody the design principle, the following figures show the structural design of microstrip line and coplanar waveguide when the impedance line is controlled to 50Ω.

Microstrip line complete structure

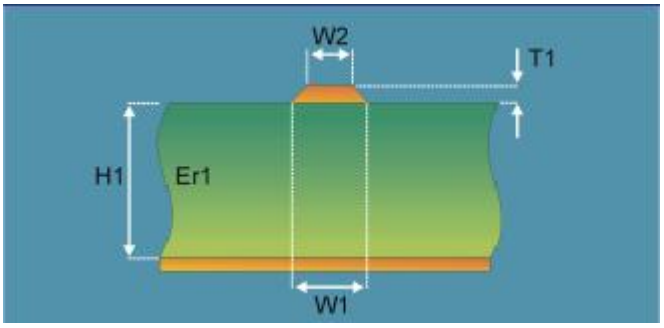


FIG. 20 Two-layer PCB microstrip line structure

Complete structure of coplanar waveguide

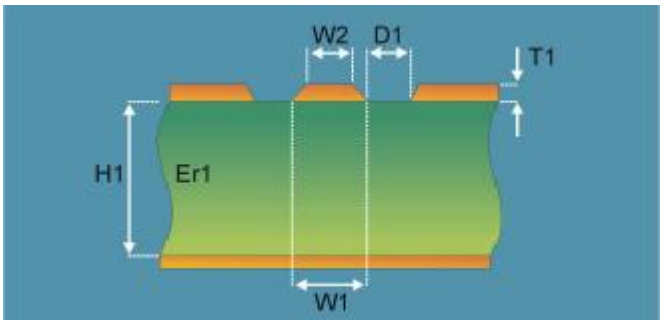


FIG. 21 Two-layer PCB coplanar waveguide structure

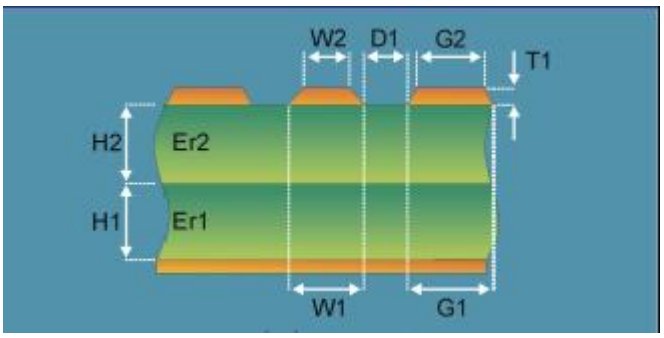


FIG. 22 Multi-layer PCB coplanar waveguide structure (the reference ground is the third layer)

In the circuit design of RF antenna interface, in order to ensure the good performance and reliability of RF signal, the following design principles are recommended:

- Precise 50Ω impedance control of the RF signal lines shall be performed using impedance simulation calculation tools.
- GND pin adjacent to the RF pin is not a hot pad, but should be fully contacted with the ground.
- The distance between RF pin and RF connector should be as short as possible; At the same time, avoid right-angle routing, and the recommended routing angle is 135.
- Pay attention to the connection device package when it is established, and keep a certain distance from the ground for the signal pin.
- The reference ground plane of RF signal line should be complete; Adding a certain amount of ground holes around the signal line and the reference ground can help improve the RF performance; The distance between the ground hole and the signal line should be at least 2 times the line width (2 × W).
- RF signal lines must be far away from interference sources, and avoid crossing or parallel with any signal lines in adjacent layers.

4.3 Antenna Installation

4.3.1 Antenna Requirements

The requirements of main antenna receiving antenna are shown in the following table:

Table 28 Antenna requirements

Type	Requirement
FDD-LTE	VSWR: < 2
	increase（dBi）: 1
	Maximum output power（W）: 2W
	input impedance（ohm）: 50
	Type of polarization: vertical direction
	Cable insertion loss: < 1.5dB (LTE B5/B12/B13/B14/B71)
	Cable insertion loss: < 2dB (LTE B2/B4/B66)
GNSS	VSWR: < 2
	increase（dBi）: 1
	Maximum output power（W）: 0.1W
	input impedance（ohm）: 50
	Type of polarization: vertical direction
	Cable insertion loss: < 1.5dB

4.3.2 RF output power

The RF output power of SLM336Q is shown in the following table.

Table 29 SLM336Q RF transmission power

Frequency	Max	Min
LTE-FDD B2	23dBm±2.7dB	<-39dBm
LTE-FDD B4	23dBm±2.7dB	<-39dBm
LTE-FDD B5	23dBm±2.7dB	<-39dBm
LTE-FDD B12	23dBm±2.7dB	<-39dBm
LTE-FDD B13	23dBm±2.7dB	<-39dBm
LTE-TDD B14	23dBm±2.7dB	<-39dBm
LTE-TDD B66	23dBm±2.7dB	<-39dBm
LTE-TDD B71	23dBm±2.7dB	<-39dBm

4.3.3 RF Frequency

Table 30 SLM336Q module RF reception sensitivity

Frequency	Reception sensitivity (typical value BW) -10M			
	Dominant set	Diversity	Dominant+Diversity	3GPP（Dominant+Diversity）
LTE-FDD B2	-98dBm	NA	NA	-94.3dBm
LTE-FDD B4	-98dBm	NA	NA	-96.3dBm
LTE-FDD B5	-96.5dBm	NA	NA	-94.3dBm
LTE-FDD B12	-96.5dBm	NA	NA	-93.3dBm

LTE-FDD B13	-96.5dBm	NA	NA	-93.3dBm
LTE-FDD B14	-97.5dBm	NA	NA	-93.3dBm
LTE-TDD B66	-98dBm	NA	NA	-95.8dBm
LTE-TDD B71	-97dBm	NA	NA	-93.5dBm

Remark:

Other sub-model and frequency information will be reflected in subsequent versions of the document.

4.3.4 Working Frequency

Table 31 SLM336Q operating frequency

3GPP Band	Send	Receive	unit
LTE-FDD B2	1850~1910	1930~1990	MHz
LTE-FDD B4	1710~1755	2110~2155	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B12	699~716	729~746	MHz
LTE-FDD B13	777~787	746~756	MHz
LTE-FDD B14	788~798	758~768	MHz
LTE-FDD B66	1710~1780	2110~2180	MHz
LTE-FDD B71	663~698	617~652	MHz
GPS	/	1575.42±1	MHz
Glonass	/	1597~1606	MHz
BeiDou	/	1559~1563	MHz
Galileo	/	1575.42±1	MHz

4.3.5 OTA Antenna Requirements

Table 32 Antenna index requirements

Network Mode	Band	VSWR	Gain		Effi.	SAR	TRP (dBm)	TIS (dBm)
			Peak	Avg.				
FDD-LTE	Band2	<2.5:1	>0dBi	>-4dBi	>40%	<1.6W/Kg	17	<-91
	Band4						17	<-91
	Band5						17	<-91
	Band12						17	<-91
	Band13						17	<-91
	Band14						17	<-91
	Band66						17	<-91
	Band71						17	<-91

5 Electrical Characteristics

5.1 Limited Voltage Range

Limited voltage range refers to the maximum voltage range that the module supply voltage and digital and analog input/output interfaces can withstand. Work outside this range may cause damage to the product.

The limited voltage range of SLM336Q is shown in the following table.

Table 33 Limited operating voltage range of modules

Parameters	Description	Min	Typical value	Max	units
VBAT	Power supply	-0.3	3.8	5	V
GPIO	Digital I/O level supply voltage	-0.3	1.8	2.0	V
USB_VBUS	USB Insert the test	-0.3	5.0	5.5	V

5.2 Ambient Temperature Range

The SLM336Q module is recommended to operate at -35~+75℃. It is suggested that temperature control measures should be considered at the application end under adverse environmental conditions. At the same time, the extended operating temperature range of the module is provided. When used at the extended temperature, the function is normal, and some RF indicators may deteriorate. It is also recommended that the module application terminal be stored at a certain temperature. Modules outside this range may not work properly or may be damaged.

Table34 Temperature range of module

Parameters	Min	Typical value	Max	Units
Operating temperature	-35	+25	+75	℃
Storage temperature	-40		+85	℃

5.3 Electrical Characteristics of Interface Working State

V_L: Logic low level;

V_H: Logic high level。

Table 35 The logic level of a normal digital IO signal

Signal	V_L		V_H		Units
	Min	Max	Min	Max	
digital input	-0.3	0.6	1.2	2.0	V
digital ouput		0.45	1.35		V

Table 36 Electrical characteristics of power supply operating state

Parameters	I/O	Min	Model	Max	Units
VBAT	I	3.5	3.8	4.2	V
VBUS	I	4.5	5.0	5.5	V
USIM_VDD	O	1.75/2.95	1.8/3	1.85/3.05	V

5.4 Power Consumption Range

Table 37 Power consumption

State of the module	Test item		Test Case	Result（mA）
Power off	Shutdown leakage current		Maintain normal voltage (3.8V) power supply in case of power failure	QE:3uA QA:8uA
Dormant	Real network	Insert the mobile card, the actual network standby, use the AT command to query the registration on the network, and record the average current of 10 minutes。		

	dormancy	Insert the unicom card, the actual network standby, use AT command to query and register the network, and record the 10-minute average current.		
		Insert the telecom card, the actual network standby, use AT command to query and register the network, and record the average current of 10 minutes.		
	FDD	The module is powered on, and the DRX monitoring period of the idle state on the network is 1.28s With no data transfer, the USB is in a suspended state	Band2 CH18900 1) The tested module was powered on, and the data network was successfully registered; 2) Set the module to sleep state through AT instruction (USB is in suspended state); 3) Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band4 CH20175 1) The tested module was powered on, and the data network was successfully registered; 2) Set the module to sleep state through AT instruction (USB is in suspended state); 3) Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band5 CH20525 1) The tested module was powered on, and the data network was successfully registered; 2) Set the module to sleep state through AT instruction (USB is in suspended state); 3) Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band12 CH23095 1) The tested module was powered on, and the data network was successfully registered;	

			2) Set the module to sleep state through AT instruction (USB is in suspended state); 3) Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band13 CH23230 1) The tested module was powered on, and the data network was successfully registered; 2) Set the module to sleep state through AT instruction (USB is in suspended state); 3) Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band14 CH23330 1) The tested module was powered on, and the data network was successfully registered; 2) Set the module to sleep state through AT instruction (USB is in suspended state); 3) Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band66 CH132322 1) The tested module was powered on, and the data network was successfully registered; 2) Set the module to sleep state through AT instruction (USB is in suspended state); 3) Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band71 CH133297 1) The tested module was powered on, and the data network was successfully registered; 2) Set the module to sleep state through AT instruction (USB is in suspended state);	

			3) Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
standby	FDD	The module is powered on, and the DRX monitoring period of the idle state on the network is 1.28s With no data transfer, USB is active	Band2 CH18900 Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band4 CH20175 Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band5 CH20525 Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band12 CH23095 Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band13 CH23230 Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band14 CH23330 Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
			Band66 CH132322 Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	

			Band71 CH133297 Under the condition of no data transmission, the tested module maintained for 10 minutes and recorded the average current for 10 minutes.	
	Real network data sleep	Unicom /Mobile	Keep the data connection sending 256-byte packets back to the server every 5 minutes	
Data transmission	FDD	1) Room temperature; 2) Dc power supply is used to supply the module, and the voltage is set at 3.8V;	Band2 0dBm CH18900 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band2 10dBm CH18900 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band2 23dBm CH18900 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band4 0dBm CH20175 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band4 10dBm CH20175 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band4 23dBm CH20175 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	

			Band5 0dBm CH20525 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band5 10dBm CH20525 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band5 23dBm CH20525 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band12 0dBm CH23095 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band12 10dBm CH23095 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band12 23dBm CH23095 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band13 0dBm CH23230 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band13 10dBm CH23230 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	

			Band13 23dBm CH23230 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band14 0dBm CH23330 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band14 10dBm CH23330 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band14 23dBm CH23330 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band66 0dBm CH132322 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band66 10dBm CH132322 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band66 23dBm CH132322 The tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band71 0dBm CH133297 Middle channel tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	

			Band71 10dBm CH133297 Middle channel tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	
			Band71 23dBm CH133297 Low channel tested module carries out data transmission and maintains for 5 minutes, and records the average current for 5 minutes	

6 Mechanical Characteristics

This section describes the mechanical dimensions of the module, all in millimeters; All dimensions not marked with tolerance, tolerance is ±0.05mm.

6.1 Module Dimension

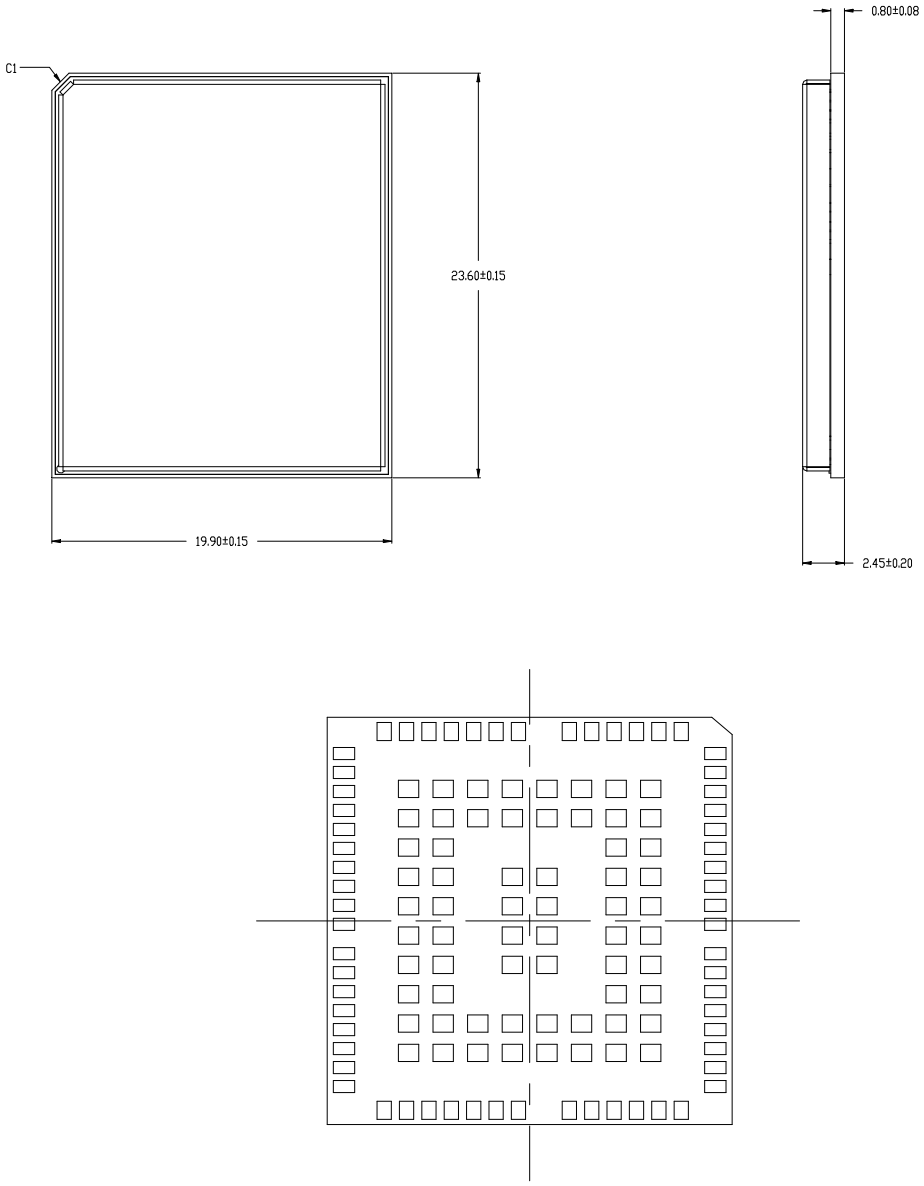


FIG. 23 Structural dimension drawing (unit: mm)

6.2 Recommended Package

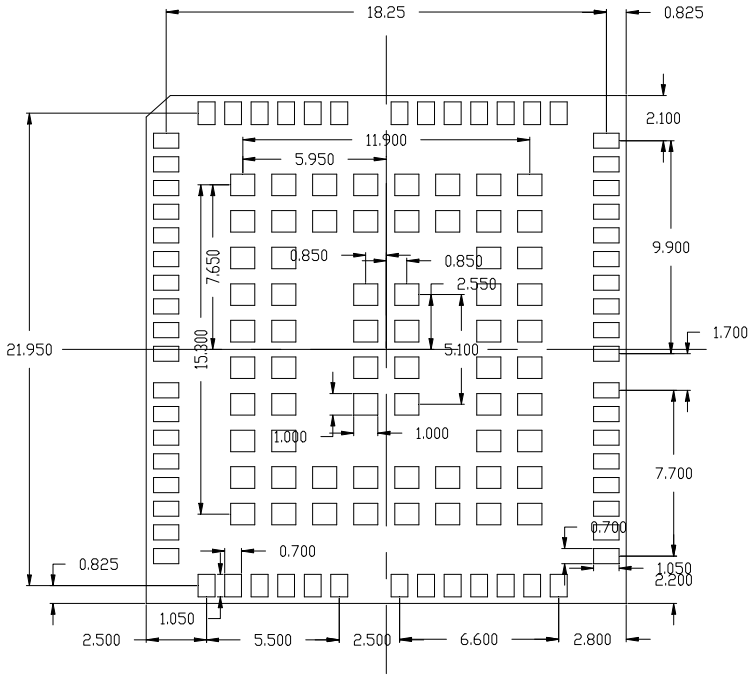


Figure 24 Recommended encapsulation (top view) (unit: mm)

6.3 Module Top View

Figure 25Top view of the module

6.4 Module Bottom View

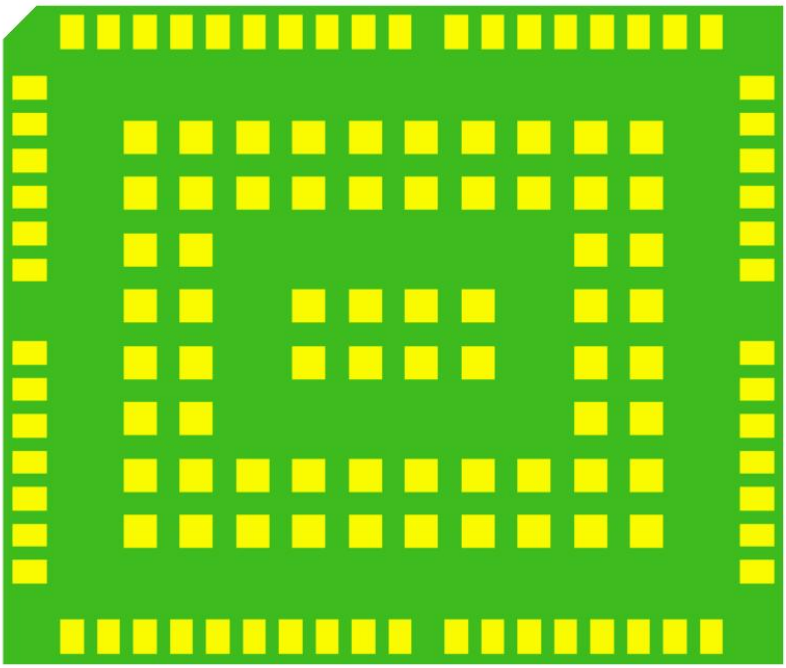


Figure 26. Bottom view of the module

7 Storage and Production

7.1 Storage

The SLM336Q is shipped in vacuum sealed bags. The storage of modules shall be subject to the following conditions:

1. When the ambient temperature is lower than 40° C and the air humidity is less than 90%, the module can be stored in a vacuum sealed bag for 12 months;
2. After the vacuum seal bag is opened, the module can directly carry out reflow welding or other high-temperature processes if the following conditions are met:
   - The module stores air humidity less than 10%;
   - The environment temperature of module is lower than 30℃, the air humidity is less than 60%, the factory finishes the patch within 72 hours.
   - If the module is under the following conditions, it needs to be baked before the patch;
   - When the ambient temperature is 23℃ (5℃ fluctuation is allowed), the humidity indicator card shows a humidity level greater than 10%;
   - When the vacuum seal bag is opened, the ambient temperature of the module is lower than 30℃ and the air humidity is less than 60%. However, the factory fails to complete the patch within 168 hours;
   - When the vacuum seal bag is opened, the module stores air humidity greater than 10%.
3. If the module needs to be baked, bake at 125℃ (fluctuation of 5℃ above and below) for 8 hours.

Remarks:

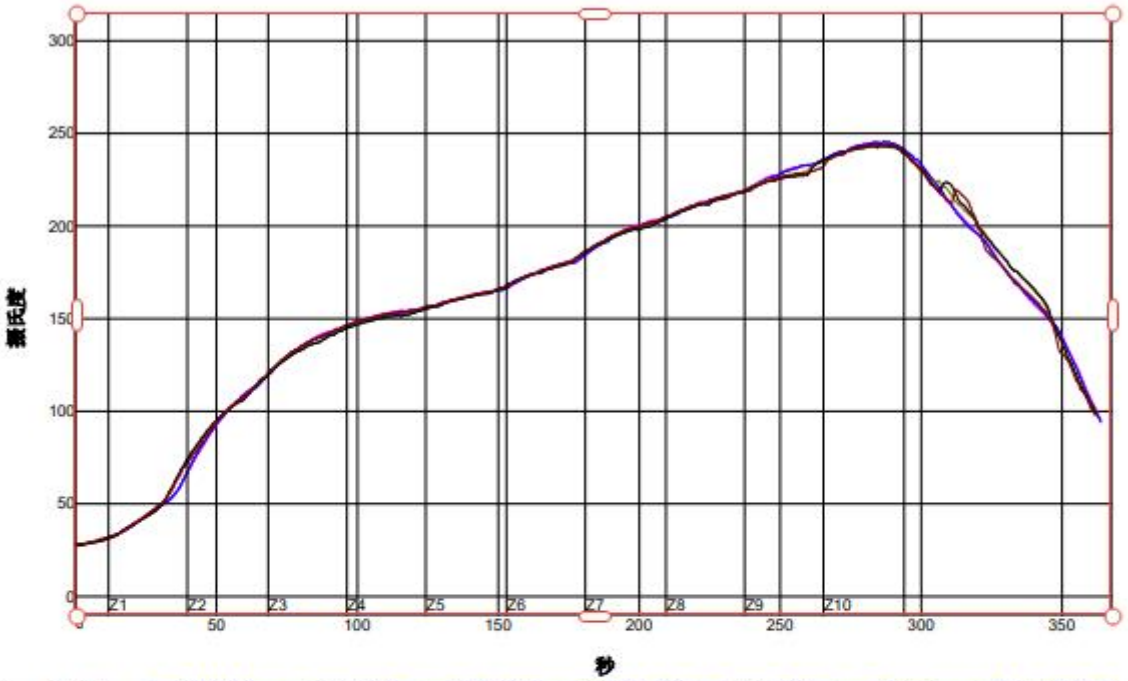
The module packaging cannot withstand such high temperature, please remove the module packaging before the module baking.

7.2 Manufacturing Welding

温度设置 (摄氏度)

温区	1	2	3	4	5	6	7	8	9	10
上温区	120	140	160	160	170	190	215	225	245	255
下温区	120	140	160	160	170	190	215	225	245	255

传送带速度 (公分/分): 80.0



PWI= 93%	最高上升斜率		最高下降斜率		预热130至165C		恒温时间165至217C		回流时间 /217C		峰值温度		总共时间 /230C	
U100	2.34	34%	-2.88	-28%	72.65	-58%	83.48	17%	76.40	40%	245.45	39%	49.07	93%
U201	2.35	35%	-2.95	-30%	73.07	-56%	84.04	20%	75.18	34%	245.68	42%	49.17	93%
U301	2.30	30%	-3.17	-45%	72.42	-59%	84.53	23%	77.78	46%	243.07	8%	40.36	23%
X300	2.33	33%	-3.22	-48%	72.00	-60%	85.14	26%	78.91	51%	243.62	15%	40.14	21%
C108	2.25	25%	-3.06	-37%	73.37	-55%	84.33	22%	77.04	42%	244.07	21%	38.00	4%
理想	0.10		0.34		1.37		1.66		3.73		2.61		11.17	

制程界限:

锡膏: MG-ROHS

统计项名称	最低界限	最高界限	单位
最高温度上升斜率 (目标=2.0) (计算斜率的时间距离= 20 秒)	0	3	度/秒
最高温度下降斜率 (计算斜率的时间距离= 20 秒)	-4	-1	度/秒
预热时间130-165摄氏度	60	120	秒
恒温时间165-217摄氏度	60	100	秒
回流以上时间 - 217摄氏度	45	90	秒
最高温度	235	250	度 摄氏度
在230摄氏度以上时间	25	50	秒

FIG. 27 Reflow temperature curve

8 Appendix A Reference and Term Abbreviation

8.1 Reference

- SLM336Q Module specifications;
- SLM336Q AT Commands;
- SLM336Q EVB user's manual
- SLM336Q Reference design circuit;
- SLM336Q Apply the business process manual.

8.2 Term Abbreviation

Table 39 Term abbreviations

Abbreviation	English Description	Chinese Description
AMR	Adaptive Multi-rate	自适应多速率
BER	Bit Error Rate	误码率
BTS	Base Transceiver Station	基站收发信台
PCI	Peripheral Component Interconnect	外设部件互连
CS	Circuit Switched (CS) domain	电路域
CSD	Circuit Switched Data	电路交换数据
DCE	Data communication equipment	数据电路终端设备
DTE	Data terminal equipment	数据终端设备
DTR	Data Terminal Ready	数据终端就绪
EDGE	Enhanced Data rates for GSM Evolution	增强型GPRS
EFR	Enhanced Full Rate	增强型全速率
EGSM	Enhanced GSM	增强型GSM
EMC	Electromagnetic Compatibility	电磁兼容性
ESD	Electrostatic Discharge	静电释放
FR	Frame Relay	帧中继
GMSK	Gaussian Minimum Shift Keying	高斯最小移频键控
GPIO	General Purpose Input Output	通用输入/输出
GPRS	General Packet Radio Service	通用分组无线系统
GSM	Global Standard for Mobile Communications	全球标准移动通信系统
HR	Half Rate	半速
HSDPA	High Speed Downlink Packet Access	高速下行分组接入
HSUPA	High Speed Uplink Packet Access	高速上行分组接入
HSPA	HSPA High-Speed Packet Access	高速分组接入
HSPA+	HSPA High-Speed Packet Access+	增强型高速分组接入
IEC	International Electro-technical Commission	国际电工技术委员会

IMEI	International Mobile Equipment Identity	国际移动设备标识
MEID	Mobile Equipment Identifier	CDMA终端的身份识别码
I/O	Input/Output	输入/输出
ISO	International Standards Organization	国际标准化组织
ITU	International Telecommunications Union	国际电信联盟
bps	bits per second	比特每秒
LED	Light Emitting Diode	发光二极管
M2M	Machine to machine	机器到机器
MO	Mobile Originated	移动台发起的
MT	Mobile Terminated	移动台终止的
NTC	Negative Temperature Coefficient	负温度系数
PC	Personal Computer	个人计算机
PCB	Printed Circuit Board	印制电路板
PCS	Personal Cellular System	个人蜂窝系统
PCM	Pulse Code Modulation	脉冲编码调制
PCS	Personal Communication System	GSM1900
PDU	Packet Data Unit	分组数据单元
PPP	Point-to-point protocol	点到点协议
PS	Packet Switched	分组交换
QPSK	Quadrate Phase Shift Keying	正交相位移频键控
SIM	Subscriber Identity Module	用户识别模组
TCP/IP	Transmission Control Protocol/ Internet Protocol	传输控制协议/互联网协议
UART	Universal asynchronous receiver-transmitter	通用异步收/发器（机）
USIM	Universal Subscriber Identity Module	通用用户识别模组
UMTS	Universal Mobile Telecommunications System	通用移动通信系统
USB	Universal Serial Bus	通用串行总线
WCDMA	Wideband Code Division Multiple Access	宽带码分多址
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access	时分同步码分多址
TDD-LTE	Time Division Long Term Evolution	时分长期演进
FDD-LTE	Frequency Division Duplexing Long Term Evolution	频分长期演进
Vmax	Maximum Voltage Value	最大电压值
Vnorm	Normal Voltage Value	典型电压值
Vmin	Minimum Voltage Value	最小电压值
V_{IH}max	Maximum Input High Level Voltage Value	输入高电平的最大电压
V_{IH}min	Minimum Input High Level Voltage Value	输入高电平的最小电压
V_{IL}max	Maximum Input Low Level Voltage Value	输入低电平的最大电压
V_{IL}min	Minimum Input Low Level Voltage Value	输入低电平的最小电压
V_{OH}max	Maximum Output High Level Voltage Value	输出高电平的最大电压
V_{OH}min	Minimum Output High Level Voltage Value	输出高电平的最小电压
V_{OL}max	Maximum Output Low Level Voltage Value	输出低电平的最大电压
V_{OL}min	Minimum Output Low Level Voltage Value	输出低电平的最小电压

9 FCC warning

According to the FCC KDB 996369 D03 OEM Manual v01r01 guidance, the following conditions must be strictly followed when using this certified module:KDB 996369 D03 OEM Manual v01r01

List of applicable FCC rules

This module has been tested for compliance with FCC Part 22/24/27/90R.

Summarize the specific operational use conditions.

The module is tested for standalone mobile RF exposure use conditions. Any other usage conditions such as co-location with other transmitter(s) or in a portable condition will need to be separate reassessment through a class II permissive change application or new certification.

Limited module procedures

Not applicable

Trace antenna designs

See the Section 4

RF exposure considerations

Exposure to Radio Frequency Radiation. This equipment must be installed and operated in accordance with provided instructions, and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be collocated or operating in conjunction with any other antenna or transmitter. End-users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

Antennas

External Antenna, Max Antenna Gain 5.75dBi，model number: 5Q004D.

Label and compliance information

if the host is marketed so that end users do not have straight forward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: Contains Transmitter Module FCC ID: 2APJ4-SLM336Q or Contains FCC ID: 2APJ4-SLM336Q must be used.

Information on test modes and additional testing requirements

Not applicable

Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B rule requirement applicable to the final host. The final host will sill need comply with Part 15 Subpart B rule requirement if applicable.