MT6177

Only PRX1-8 can be assigned to GSM HB

DRX

PRX

TXO

Power

DETIF

DRX(I/Q)

PRX(I/Q)

TX(I/Q)

BSI

U2502

RF_B28_DRX_RFIC
RF_B8_DRX_RFIC
RF_B20_DRX_RFIC
RF_B5_DRX_RFIC
RF_B12_13_DRX_RFIC
RF_B34/39_DRX_RFIC
RF_B3_DRX_RFIC
RF_B40/41_DRX_RFIC
RF_B1_DRX_RFIC
RF_B7_DRX_RFIC
RF_B2_DRX_RFIC

RF_B2_PRX_RFIC
RF_TDD_PRX_RFIC
RF_B7_PRX_RFIC
RF_B1_PRX_RFIC
RF_B4_PRX_RFIC
RF_TDD_PA_RX_RFIC
RF_B13_PRX_RFIC
RF_B3_PRX_RFIC
RF_B34/39/DCS/PCS_PRX_RFIC
RF_B5_PRX_RFIC
RF_B12_PRX_RFIC
RF_B20_PRX_RFIC
RF_B8_PRX_RFIC
RF_B28_PRX_RFIC

TX_UHB
TX_HB1
TX_HB2
TX_MB1
TX_MB2
TX_MB3
TX_LB1
TX_LB2
TX_LB3
TX_LB4
TXDET1

RF_HB2_TX_RFIC
RF_MB2_TX_RFIC
RF_MB3_TX_RFIC
RF_LB1_TX_RFIC
RF_LB3_TX_RFIC
RF_TXDET1_RFIC

VDD_TXHV
VDD_SXLF
VDD_SXLV
VDD_RXLV
VDD_RXHV
VIO

XOI
EN_BB
TMEAS
RCAL

PMIC_CLK_RF
SRCLKENA1

2K/1%/0201
R2720
U / MT6177W/ACA-E/H

D_GND

LTE_DET_BB_IP0
LTE_DET_BB_IN0
LTE_DET_BB_QP0
LTE_DET_BB_QN0

LTE_DRX_BB_Q1
LTE_DRX_BB_I1
LTE_DRX_BB_Q0
LTE_DRX_BB_I0

LTE_PRX_BB_Q1
LTE_PRX_BB_I1
LTE_PRX_BB_Q0
LTE_PRX_BB_I0

RFFE0_BSI_D1
RFFE0_BSI_D0
RFFE0_BSI_CK
RFFE0_BSI_EN

LTE_TX_BB_IP0
LTE_TX_BB_IN0
LTE_TX_BB_QP0
LTE_TX_BB_QN0

Attenuator for Detector

6dB Attenuator

RF_TXDET1_RFIC — R2712 150R/5%/0201 — R2711 36R/5%/0201 — R2713 150R/5%/0201 — RF_TXDET1

D_GND

Power For MT6177

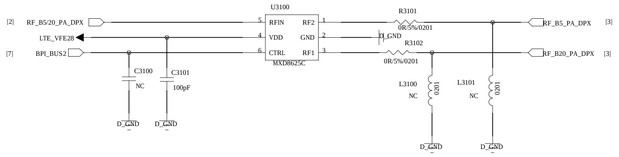
SH2616 NC/MMD-20MIL
SH2617 NC/MMD-20MIL
SH2618 NC/MMD-20MIL
SH2619 NC/MMD-20MIL
SH2620 NC/MMD-20MIL
SH2621 NC/MMD-20MIL

VRF18_TXH — VRF18_PMU — C5003 4.7uF/6.3V/0402
VRF18_RXH
VRF18_SXL
VRF12_RXL — VRF12_PMU — C10 4.7uF/6.3V/0402
VRF12_SXL
VIO18_RFIC — VIO18_PMU

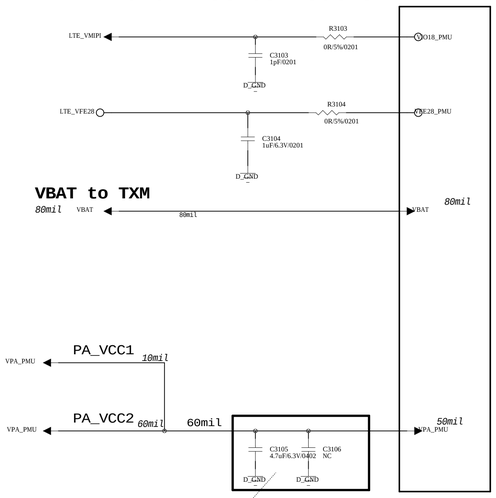
4.7uF close to RFIC

VIO18_RFIC — C5005 100nF/6.3V/0201
VRF18_TXHV — C9 100nF/6.3V/0201
VRF12_SXLV — C13 100nF/6.3V/0201
VRF12_SXLV — C11 100nF/6.3V/0201
VRF18_SXLF — C12 100nF/6.3V/0201
VRF18_RXHV — C5010 100nF/6.3V/0201

D_GND



Power Net Connection

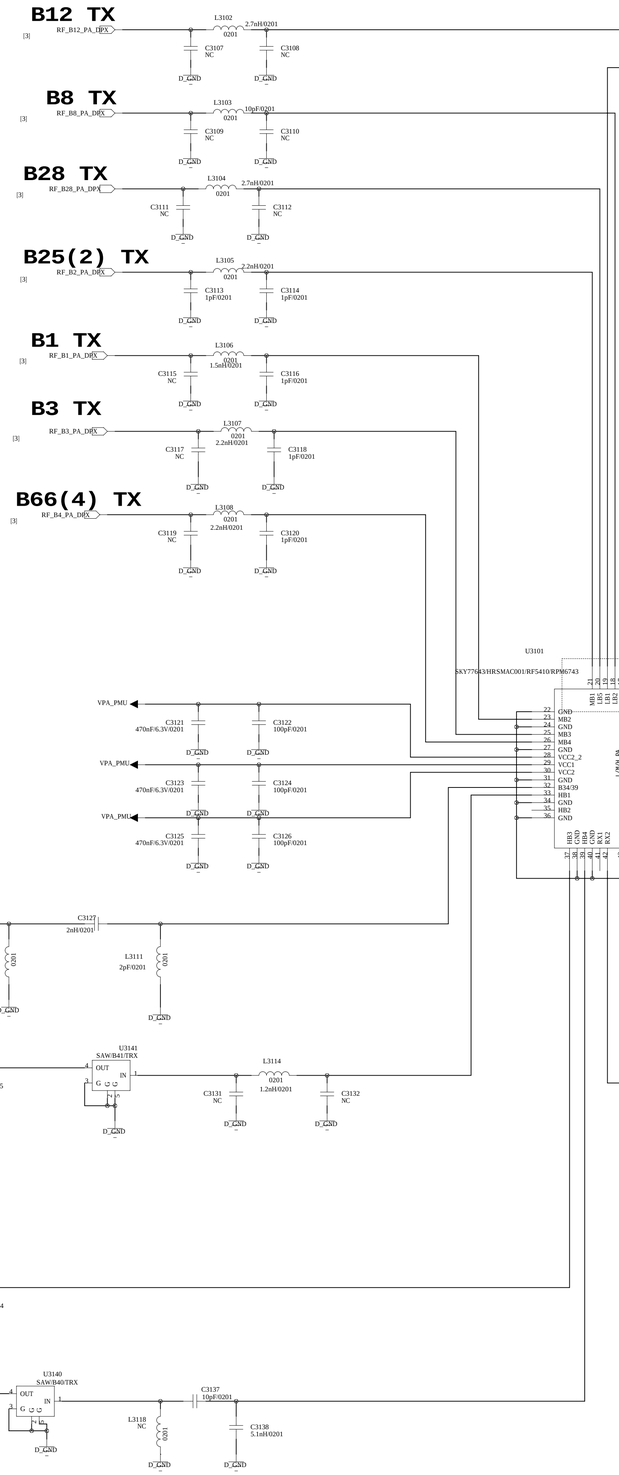


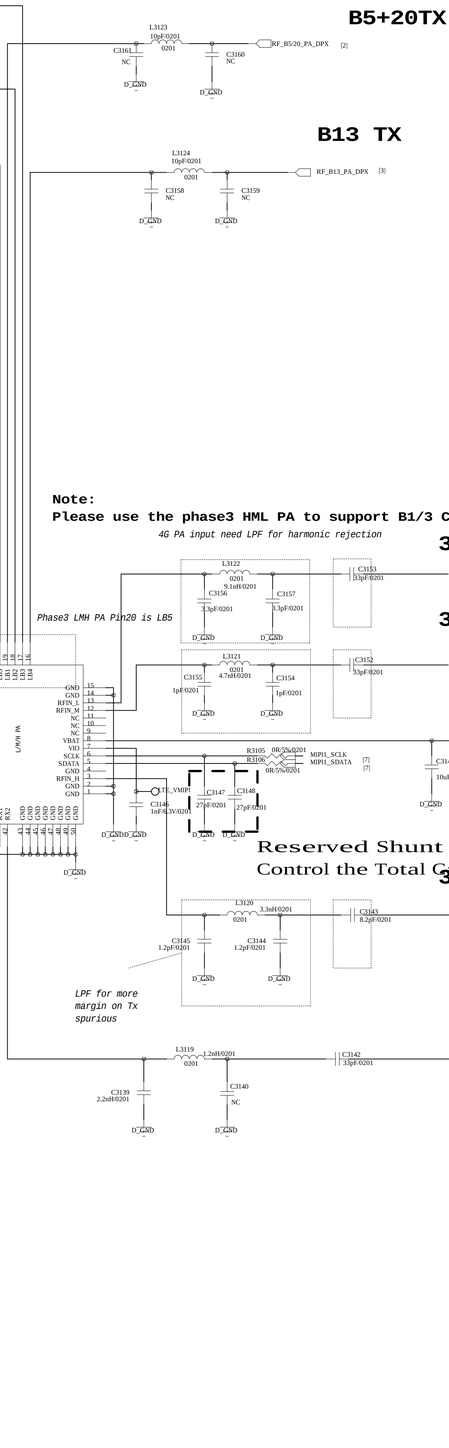
VBAT to TXM

From PMIC

Note:
Use 0603 for lower Capacitance drop

Note:
Reserve at least one tuning cap. For PMIC VPA total cap requirement, the total cap at RF side should be in 6.2uF +7/-5%.





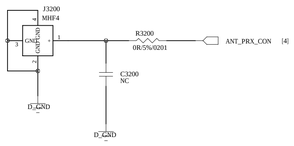
Note:
Please use the phase3 HML PA to support B1/3 CA

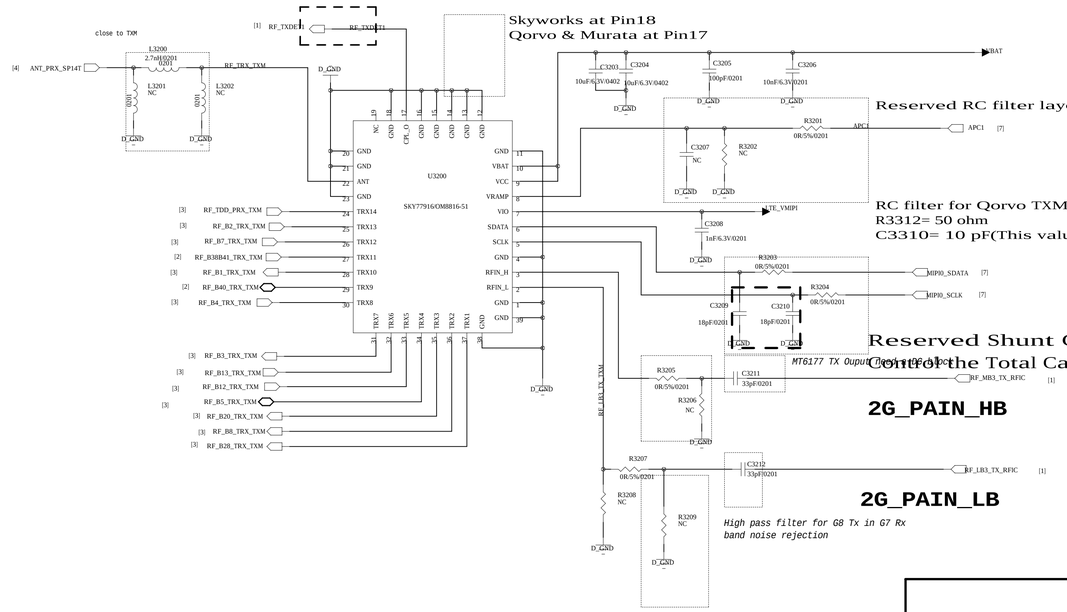
4G PA input need LPF for harmonic rejection

Phase3 LMH PA Pin20 is LB5

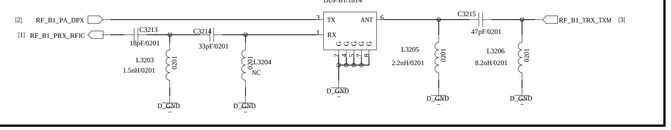
Reserved Shunt C for MIPI C-load Tuning
Control the Total Capacitance to 25pF+-3pF

HMLB_Primary-ANT

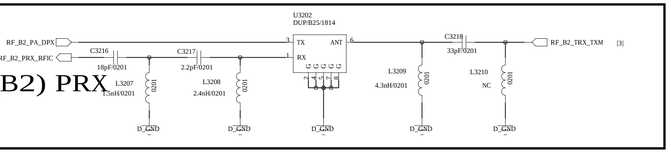




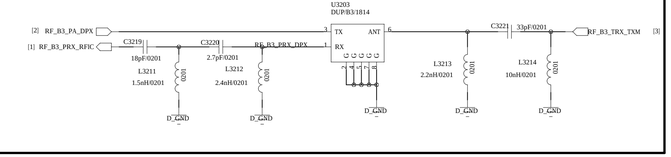
B1



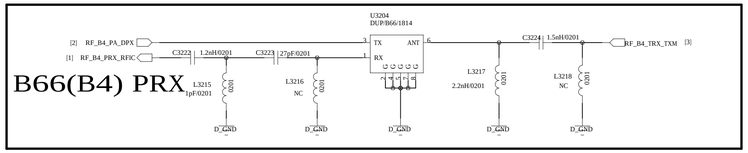
B25(B2) PRX



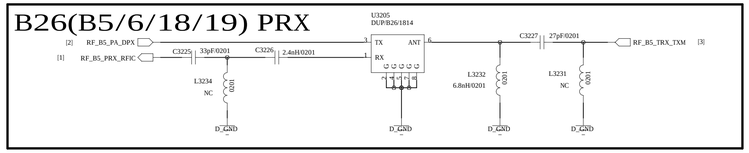
B3



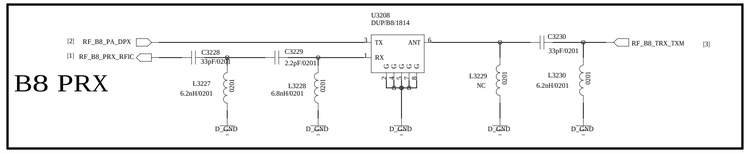
B66(B4) PRX



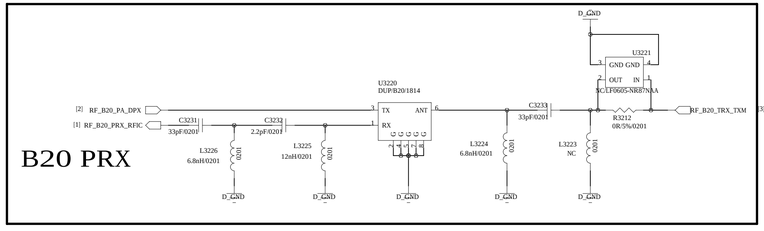
B26(B5/6/18/19) PRX



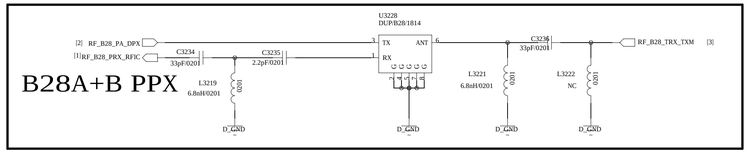
B8 PRX



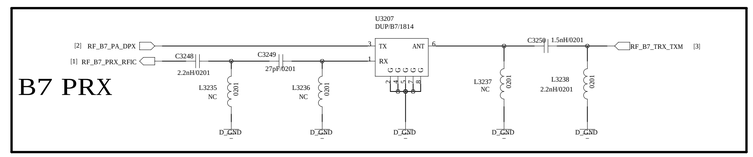
B20 PRX

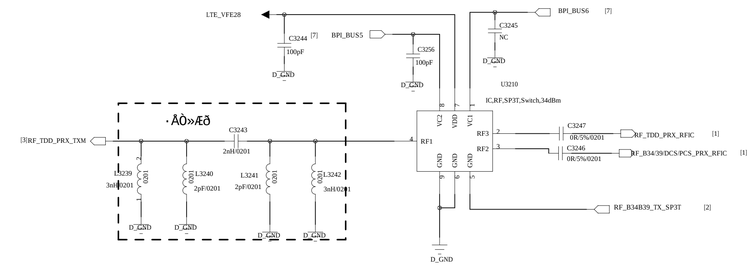


B28A+B PPX

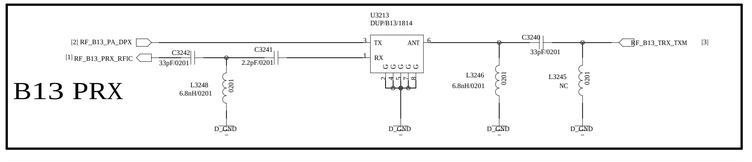


B7 PRX

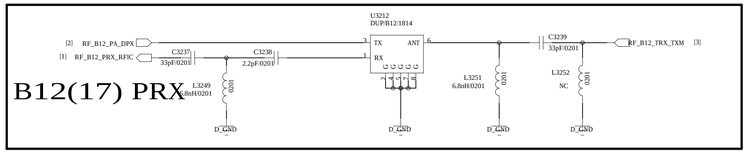




B13 PRX



B12(17) PRX



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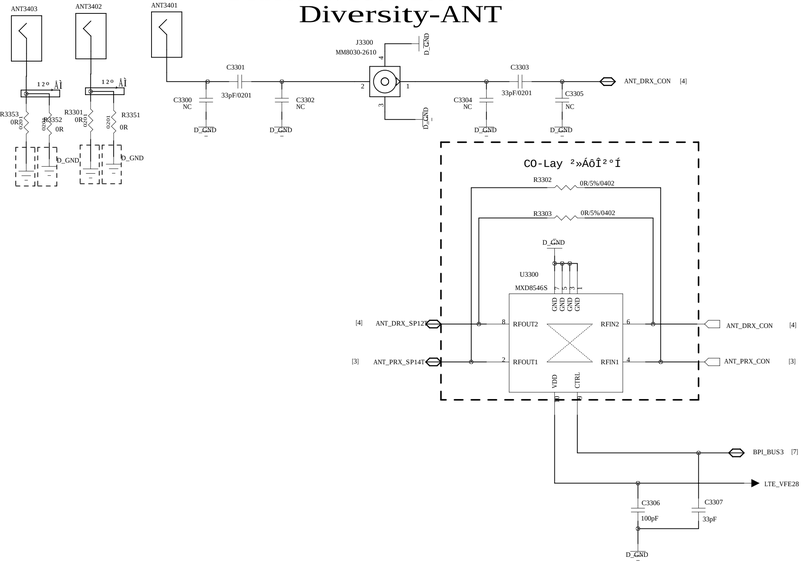
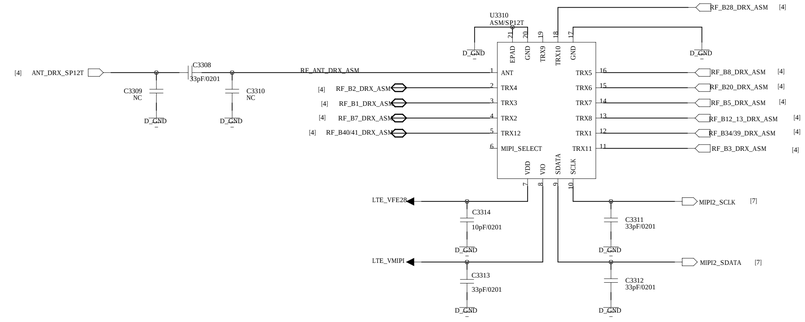
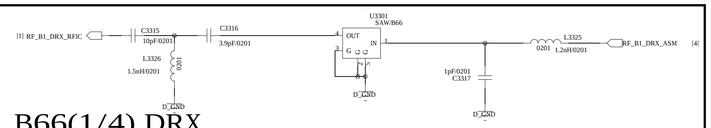
DRX ANT: 1805-2690MHz
Diversity-ANT

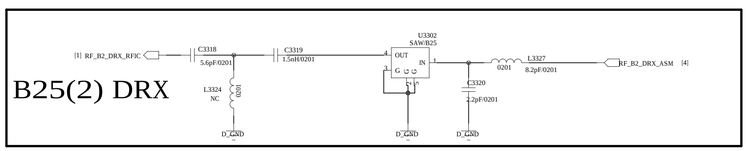




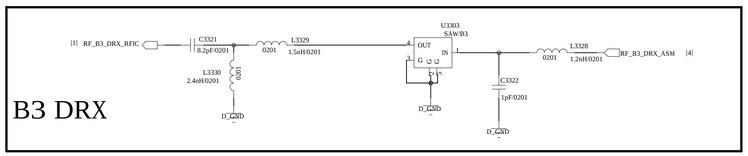
B66(1/4) DRX



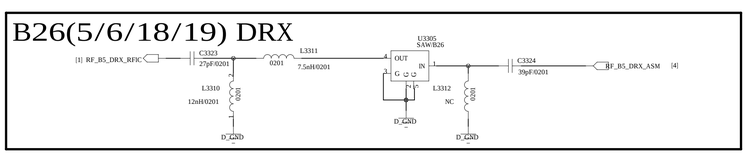
B25(2) DRX



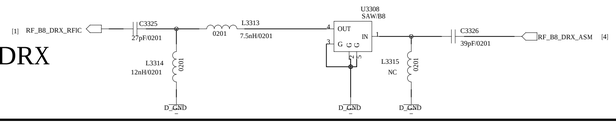
B3 DRX



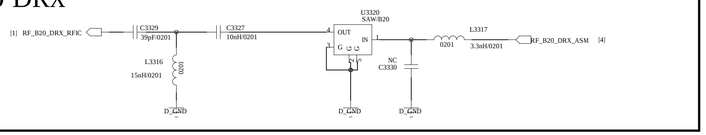
B26(5/6/18/19) DRX



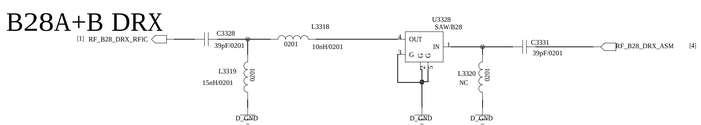
B8 DRX



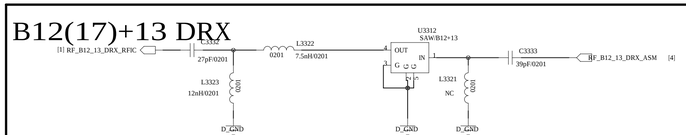
B20 DRX



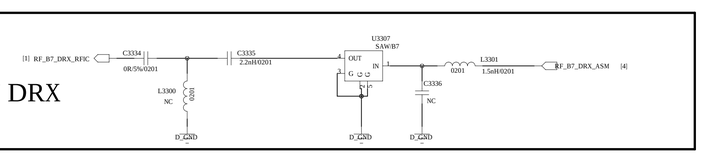
B28A+B DRX



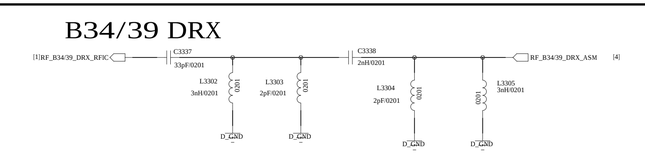
B12(17)+13 DRX



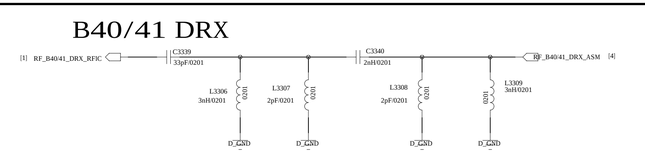
B7 DRX



B34/39 DRX



B40/41 DRX



Title	34_RF_MT6177M_RF_DRX
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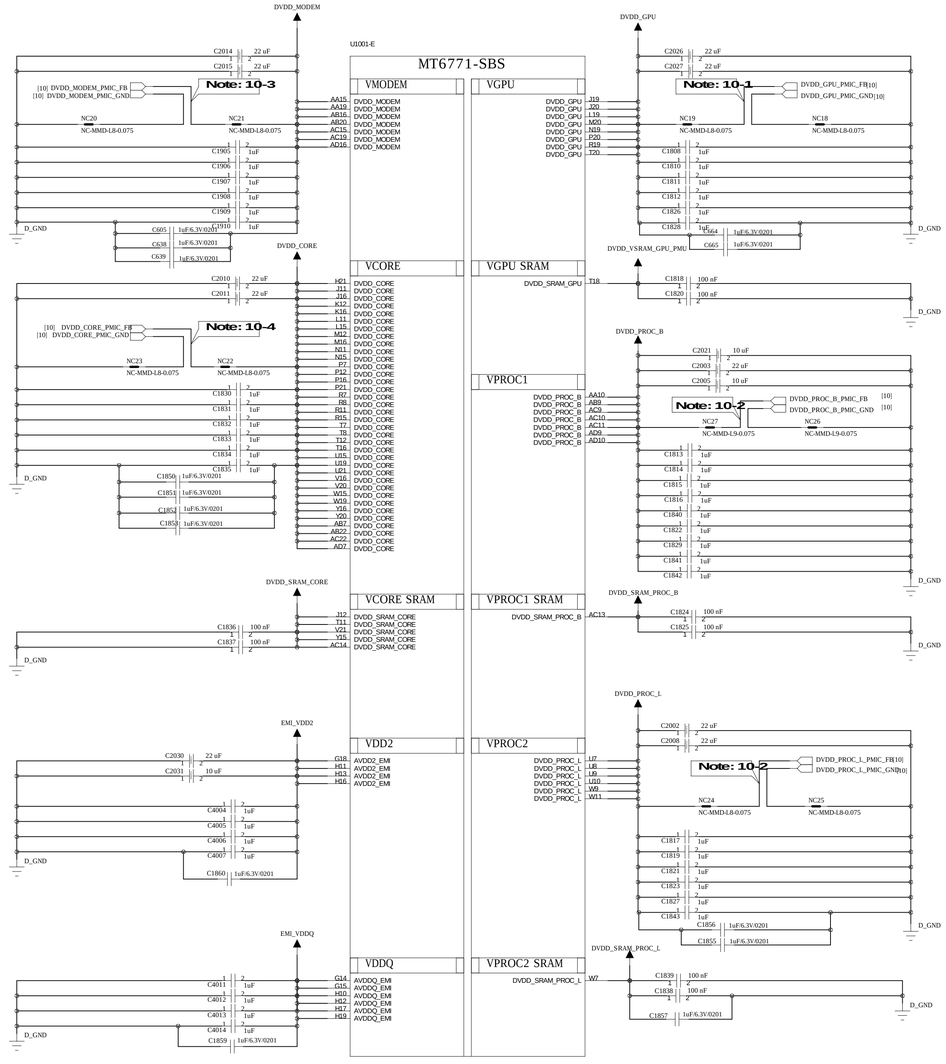


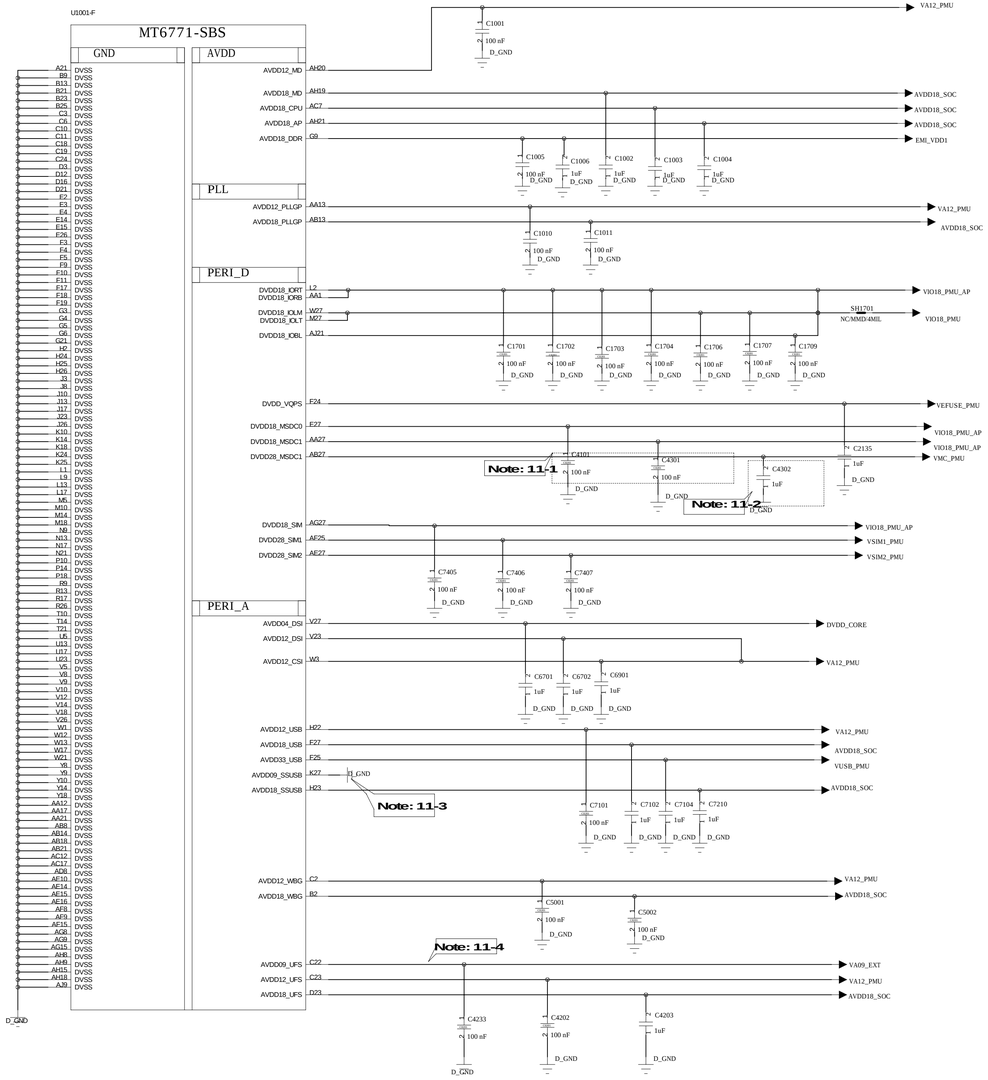
Schematic design notice of "10_BB_POWER_PDN" page.

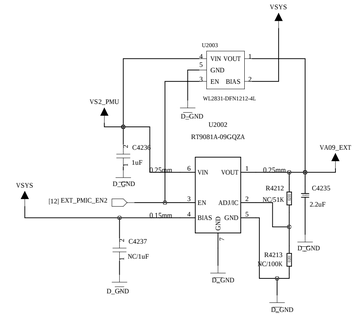
Note 10-1: Differential pair of DVDD_GPU remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)

Note 10-2: Differential pair of DVDD_PROC remote sense must be close to BB's ball Remote sense trace with GND shielding to PMIC (Differential)

Note 10-3: Differential pair of DVDD_MODEM remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)

Note 10-4: Differential pair of DVDD_CORE remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)





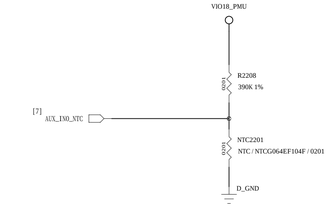
Schematic design notice of "11_BB_POWER_IO" page.

Note 11-1: C4101 closed DVDD18_MSDC0 150mil
C4301 closed DVDD18_MSDC1 150mil

Note 11-2: C4302 closed DVDD28_MSDC1 150mil

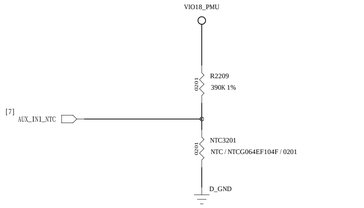
Note 11-3: Connects "AVDD09_SSUSB" to GND when USB3.0 is not used.

Note 11-4: Connects "AVDD09_UFS" to GND when UFS is not used.



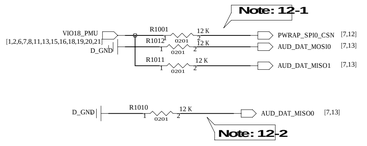
Thermistor to sense AP temperature

1. NTC1501 must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

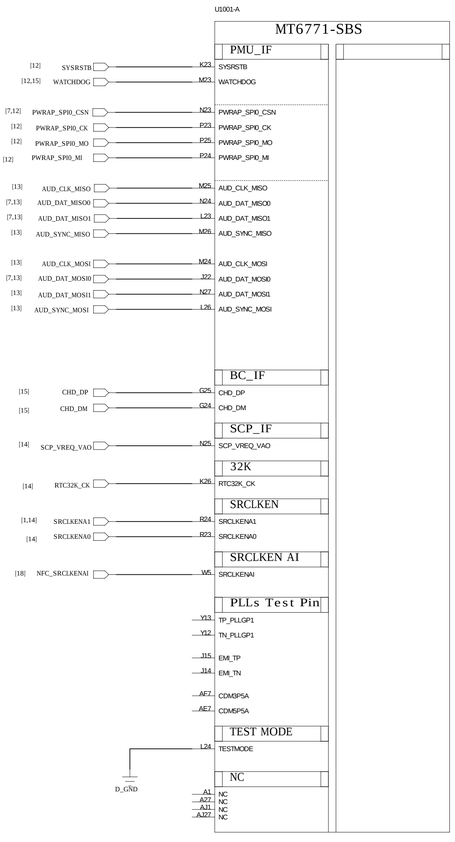


Thermistor to sense RF PA temperature

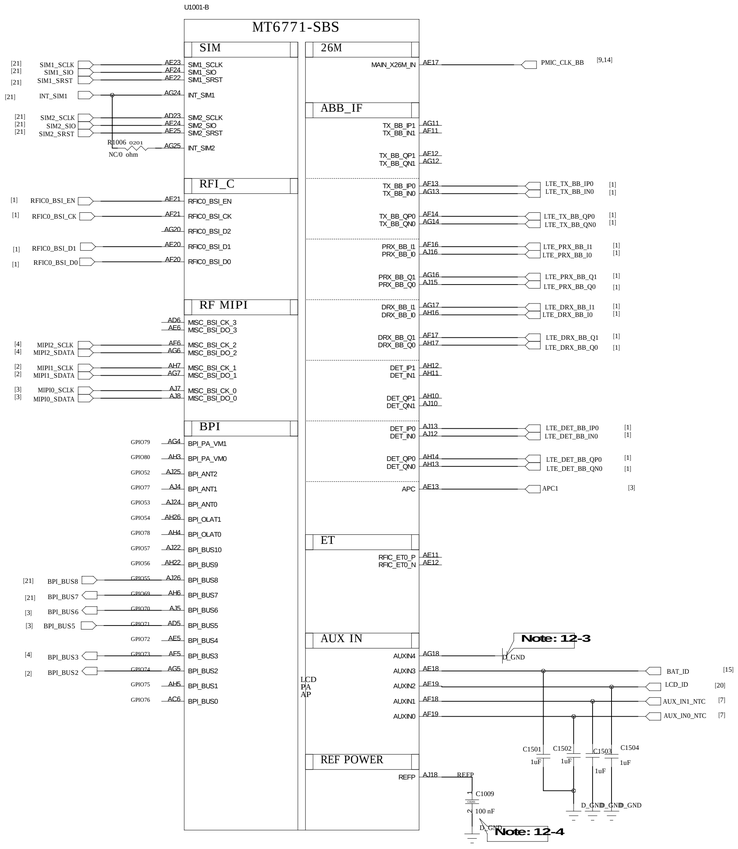
1. NTC1502 must close to LTE Band 7 PA or the hottest PA <2mm
2. The distance is the shortest distance from package edge to edge.



U1001-A



U1001-B



Schematic design notice of "12_BB_1" page.

Note 12-1: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP_JTAG	IO_JTAG
HI	LO	N/A	N/A
HI	HI	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	N/A
LO	LO	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	DPI_11/DPI_HSYNC/DPI_VSYNC/DPI_DE/ DPI_CK/DPI_D8/DPI_D9
LO	HI	MSDC1_CLK/CMD/ DAT0/DAT1/DAT2	N/A

Note 12-2: "AUD_DAT_MISO0" is bootstrap pin to enable serial JTAG output over USB2.0 interface or not.
When "AUD_DAT_MISO0" is pulled to high in system start up and then USB2.0 interface will be switched into serial JTAG mode.

"AUD_DAT_MISO1" is bootstrap pin to select system booting up from eMMC or UFS device.

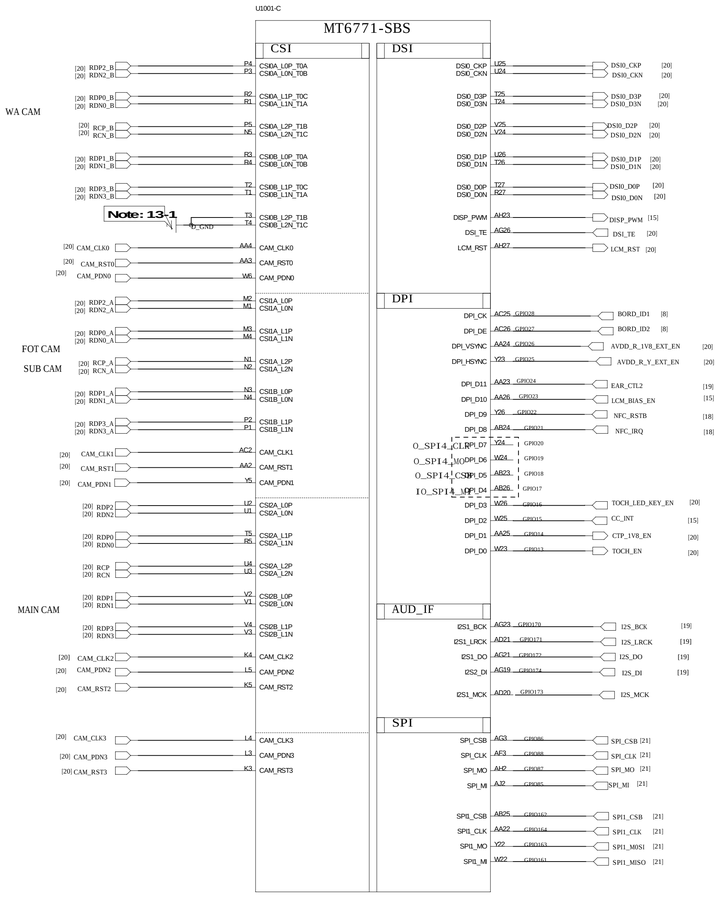
AUD_DAT_MISO1	Booting device
LO	eMMC
HI	UFS

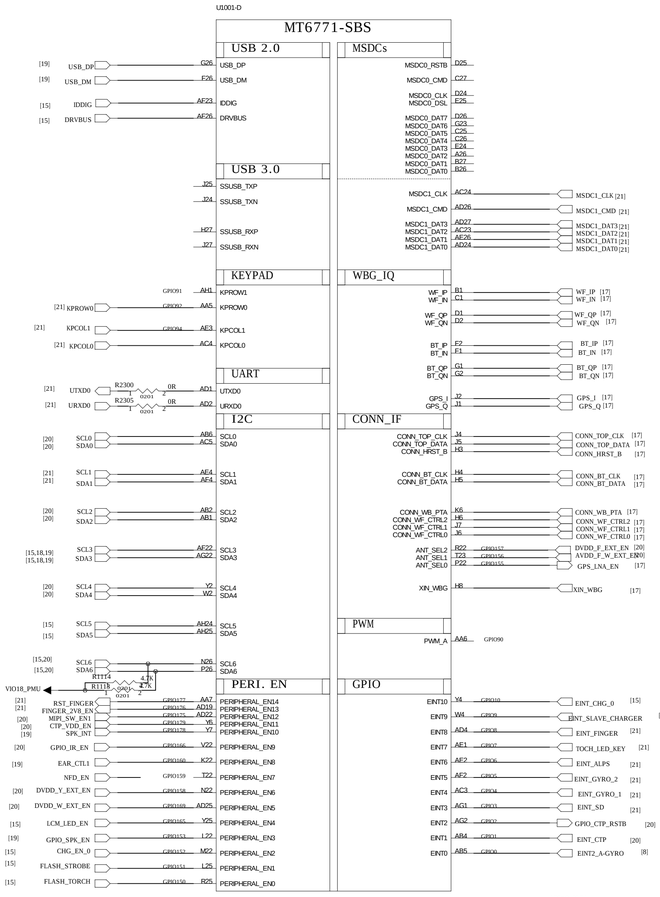
Note 12-3: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-4: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

Note 12-5: AUD_SYNC_MISO and AUD_CLK_MISO are DDR type feature in bootstrap

AUD_SYNC_MISO	AUD_CLK_MISO	DDR
LO	LO	LPDDR4X
LO	HI	LPDDR4X(Ext x 2 EN)
HI	LO	LPDDR3
HI	HI	LPDDR4X(Ext x 1 EN)



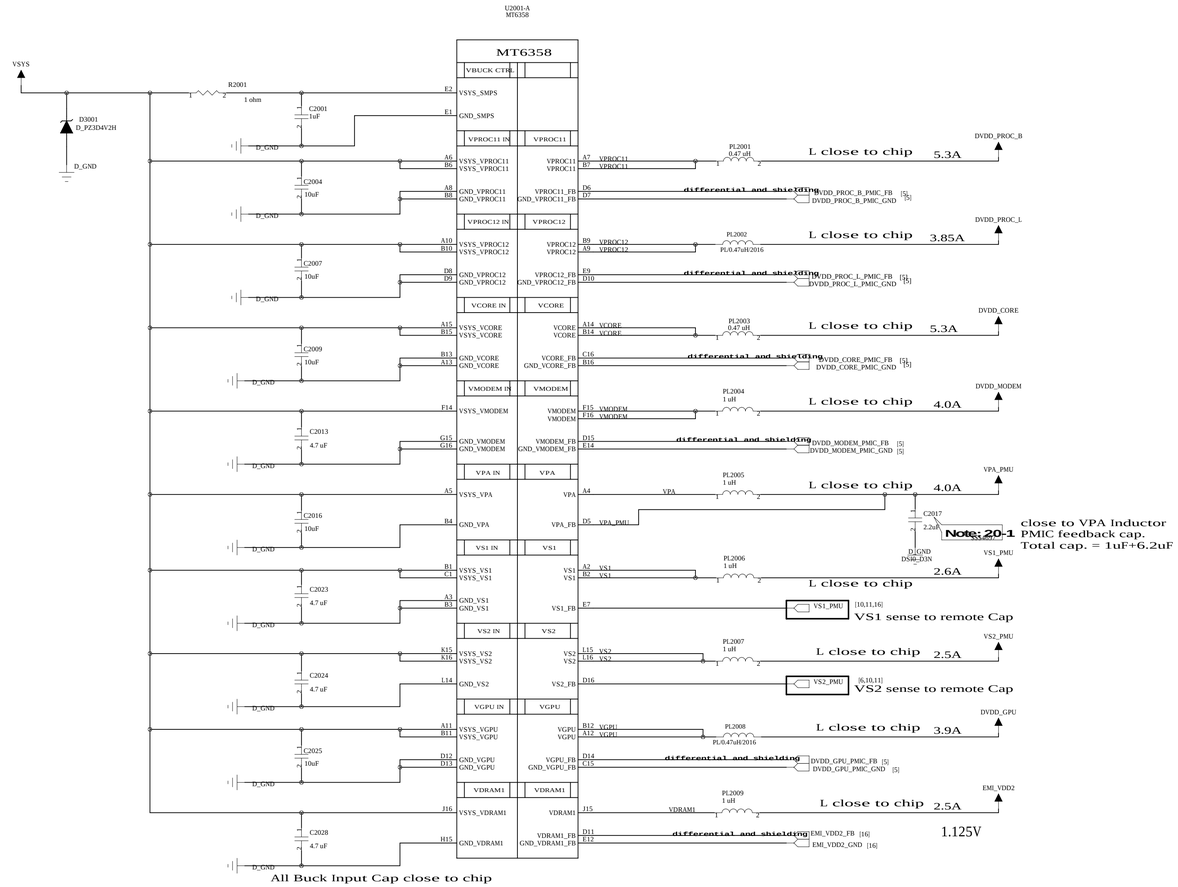


Note 13-1:

CSI ports which are no use could be connected to GND or set in NC.
For detail information, please refer to MT6771 Design Notice

Schematic design notice of "14_BB_3" page.

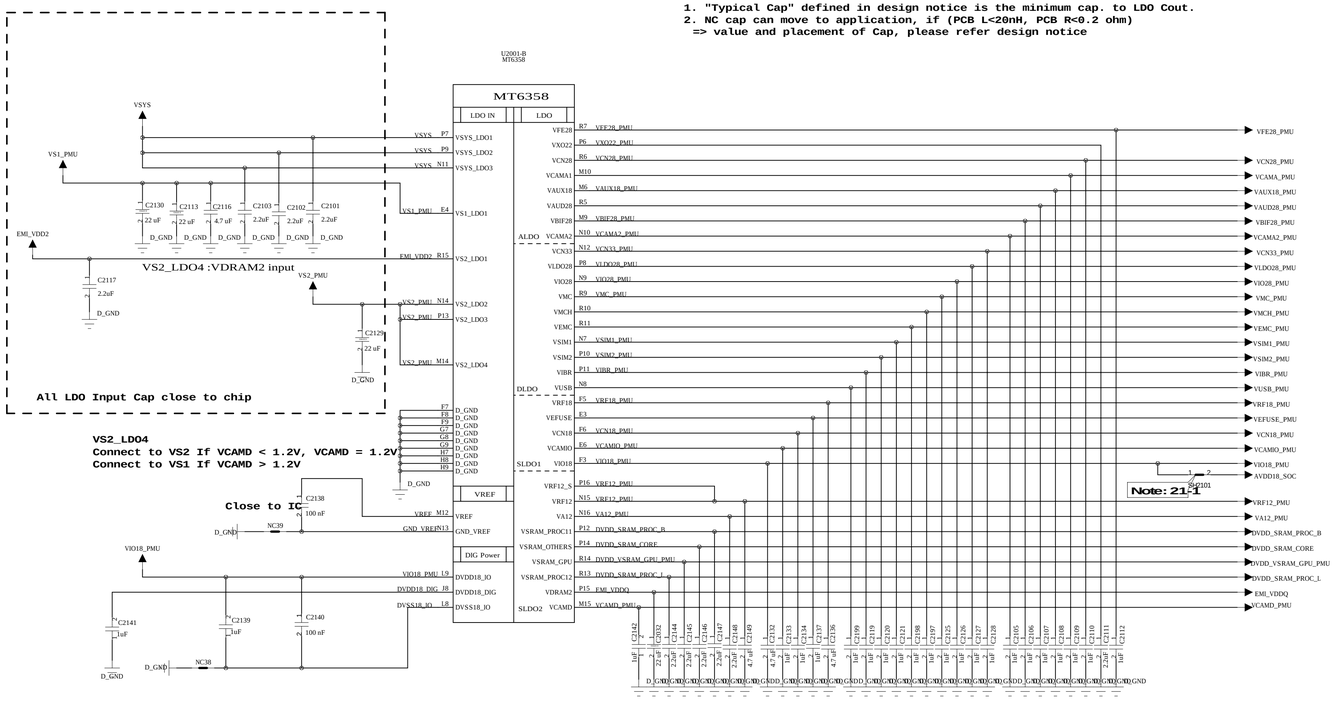
Note 14-1: The resistor of EMI_EXTR for DRAM has to be placed near to BB as close as possible
R4001, please select 60.4 ohm 1% resistor



Schematic design notice of "20_POWER_MT6358-Buck" page.

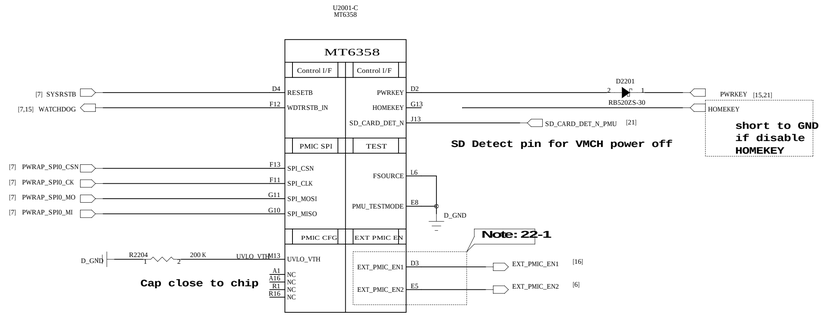
Note 20-1: Please select C2017 with 0402 size

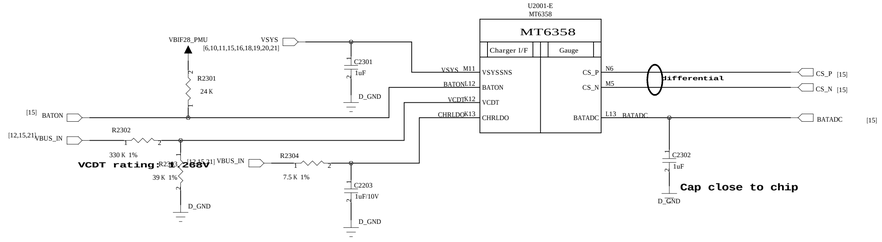
1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.
2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm)
   => value and placement of Cap, please refer design notice



Schematic design notice of "21_POWER_MT6358-LDO" page.

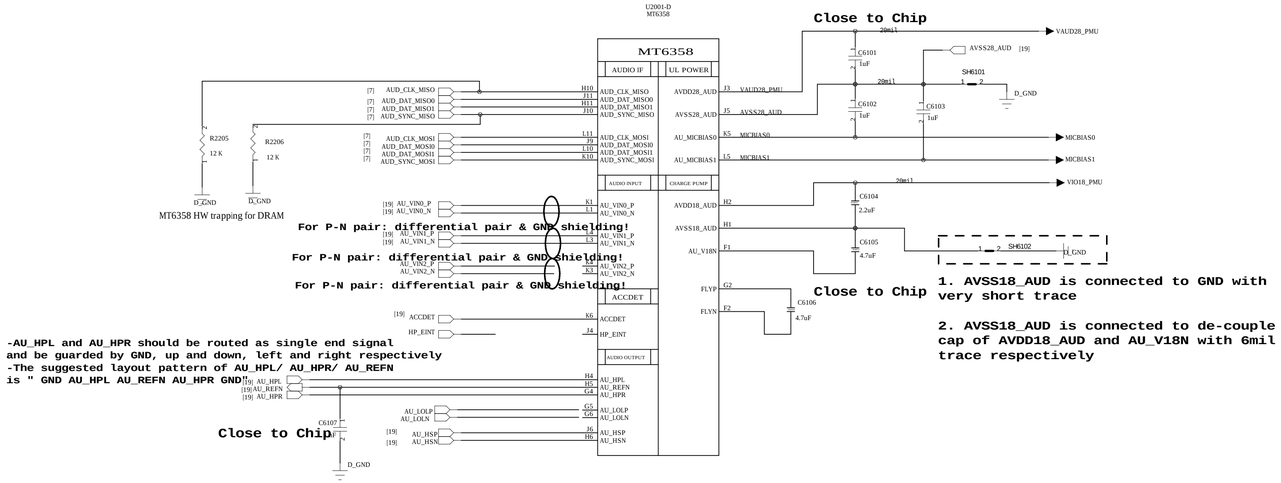
Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
Please also refer to MT6358 design notice for further detail design information





Schematic design notice of "22_POWER_MT6358-General"

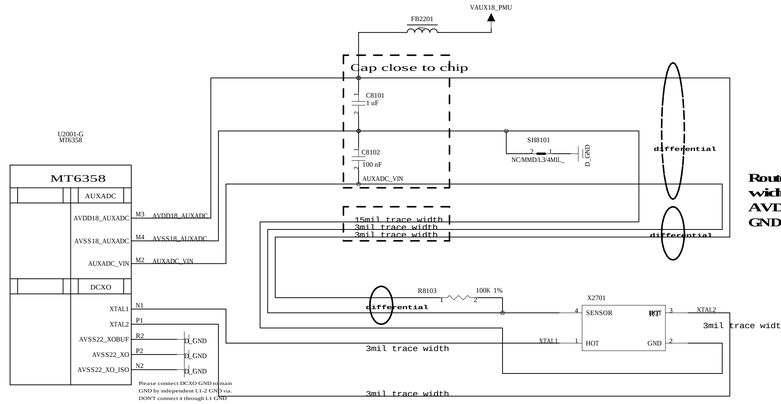
Note 22-1: EXT_PMIC_EN1 : For UFS_1V8, and keep floating if it is not used
EXT_PMIC_EN2 : For VA09 of SSUSB/UFS, and keep floating if it is not used



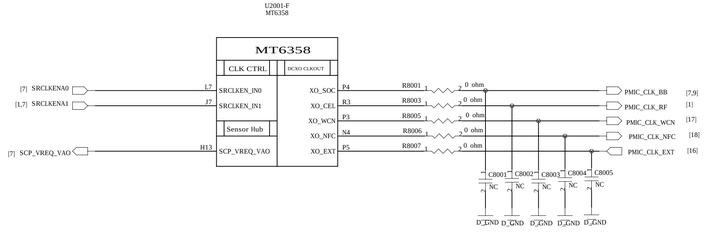
Schematic design notice of "23_POWER_MT6358-Audio"

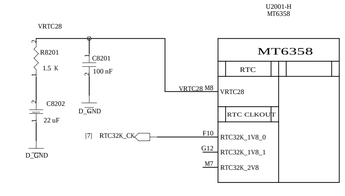
Note 23-1: VDRAM 2 / VDRAM1 output voltage vs. trap pin.

HW GPIO configuration		Trapping Option		DRAM type	VDRAM2 Power source (VS2_LDO1_ball)
AUD_SYNC_MISO	AUD_CLK_MISO	VDRAM1	VDRAM2		
0	0	1.125V	0.6V	LP4X	VDRAM1
0	1	OFF	1.8V	LP4X (Ext x 2 EN)	VS1
1	0	1.225V	OFF	LP3	VDRAM1
1	1	1.125V	1.8V	LP4X (Ext x 1 EN)	VS1

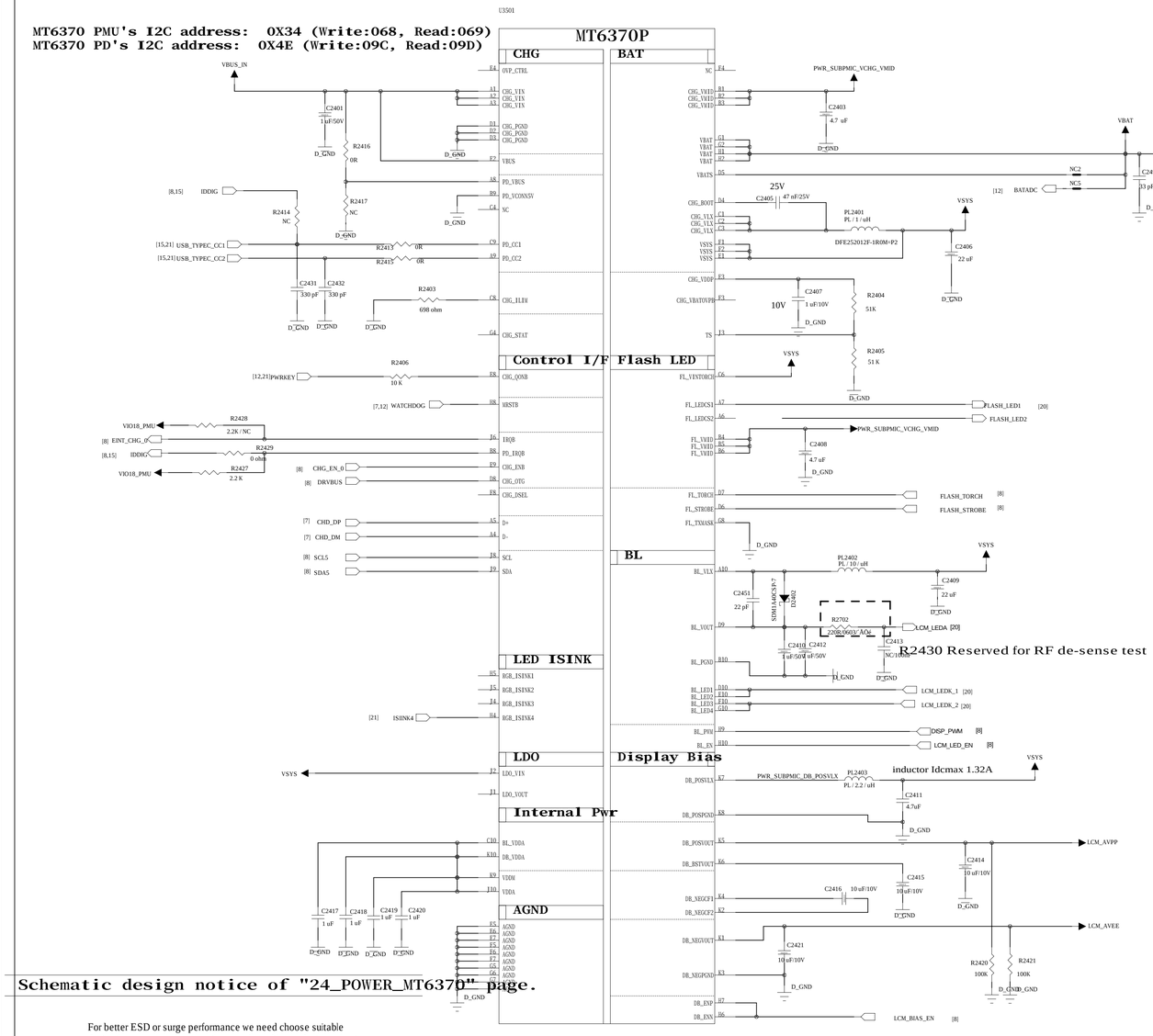


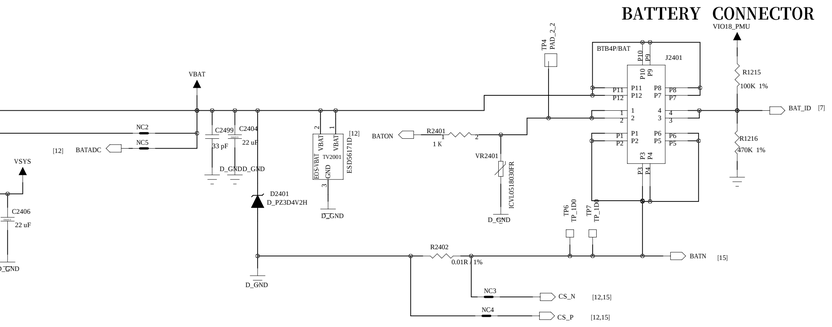
Route AVDD18_AUXADC/AUXADC_VIN with 3mil trace width and with well GND shielding. AVDD18_AUXADC/AUXADC_VIN need to be shielded with GND or AVSS18_AUXADC.

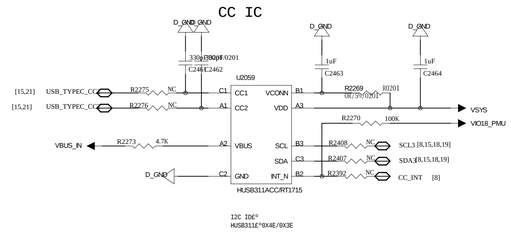


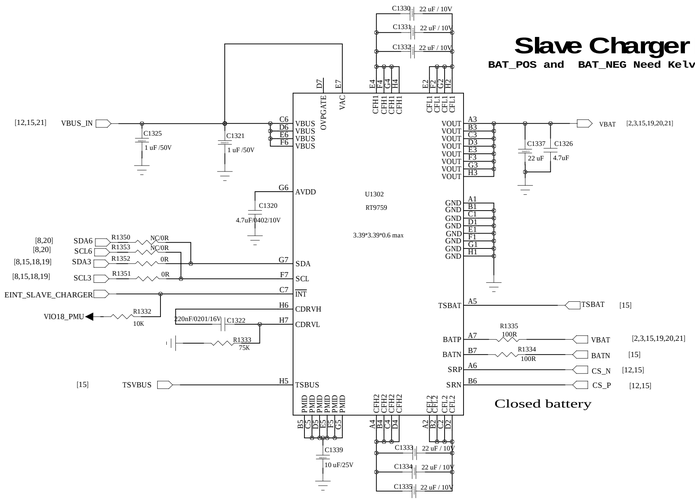


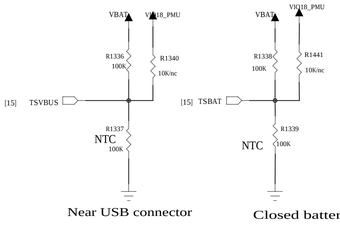
MT6370 PMU's I2C address: 0X34 (Write:068, Read:069)
MT6370 PD's I2C address: 0X4E (Write:09C, Read:09D)











Schematic design notice of "24_POWER_MT6370" page.

For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection

Note 24-1:

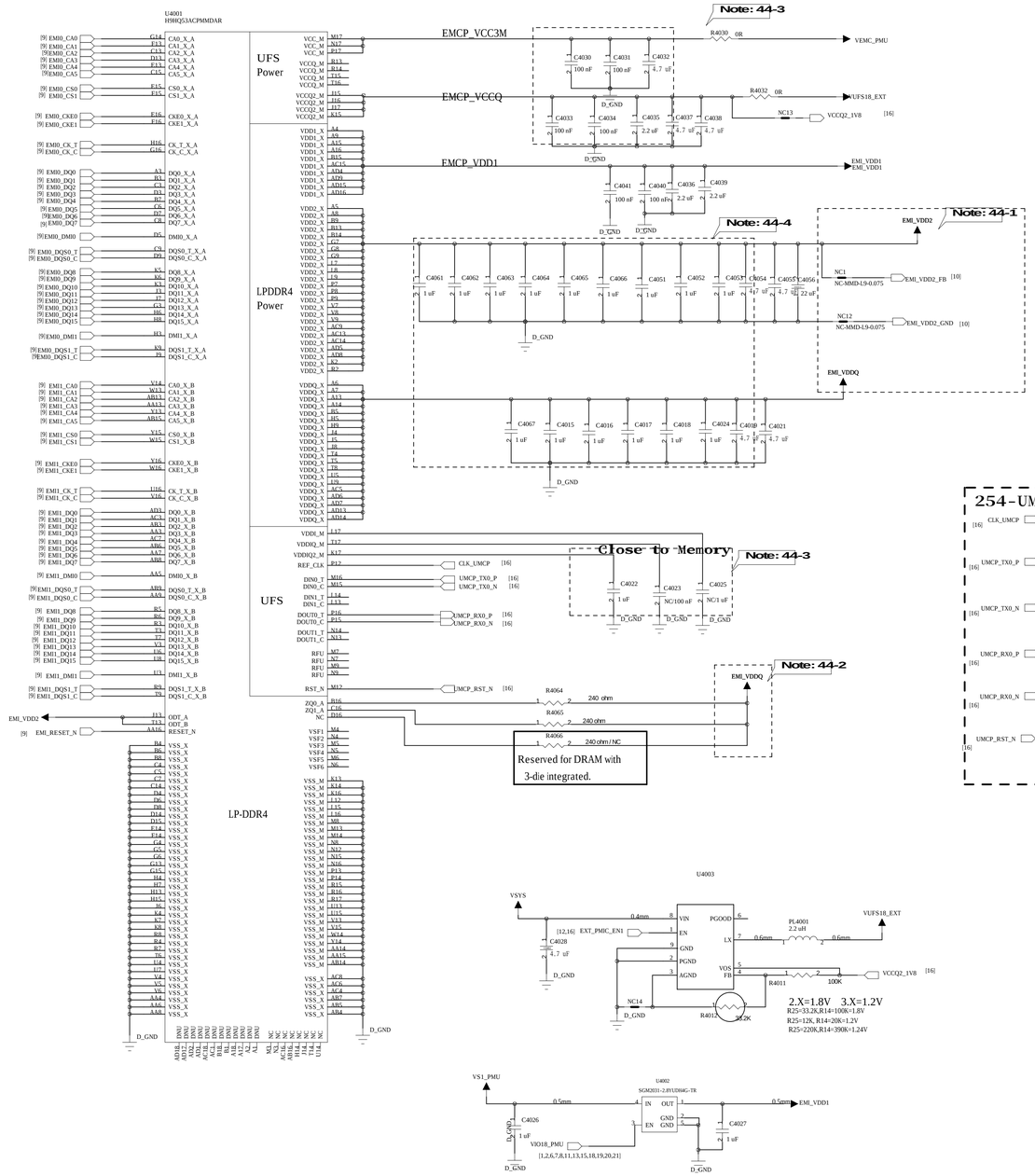
Schematic design notice of "27_POWER_SubPMIC-HV powers" page.

Note 27-1: It is recommended to reserve 0-ohm and cap. for BOM fine tune to minimize RF de-sense.

Note 27-2: It is recommended to reserve 0-ohm for BOM fine tune to minimize RF de-sense.

153-UFS

254B DDR4X/D4



254-UMCP / 153-UFS / SAM-PAD / CPU-1F

Schematic design notice of "44_Memory_eMMC_LPDDR4X"

Note 44-1: Please refer to power supply related page select VDRAM 2 / VDRAM1 output voltage properly for LPDDR4X

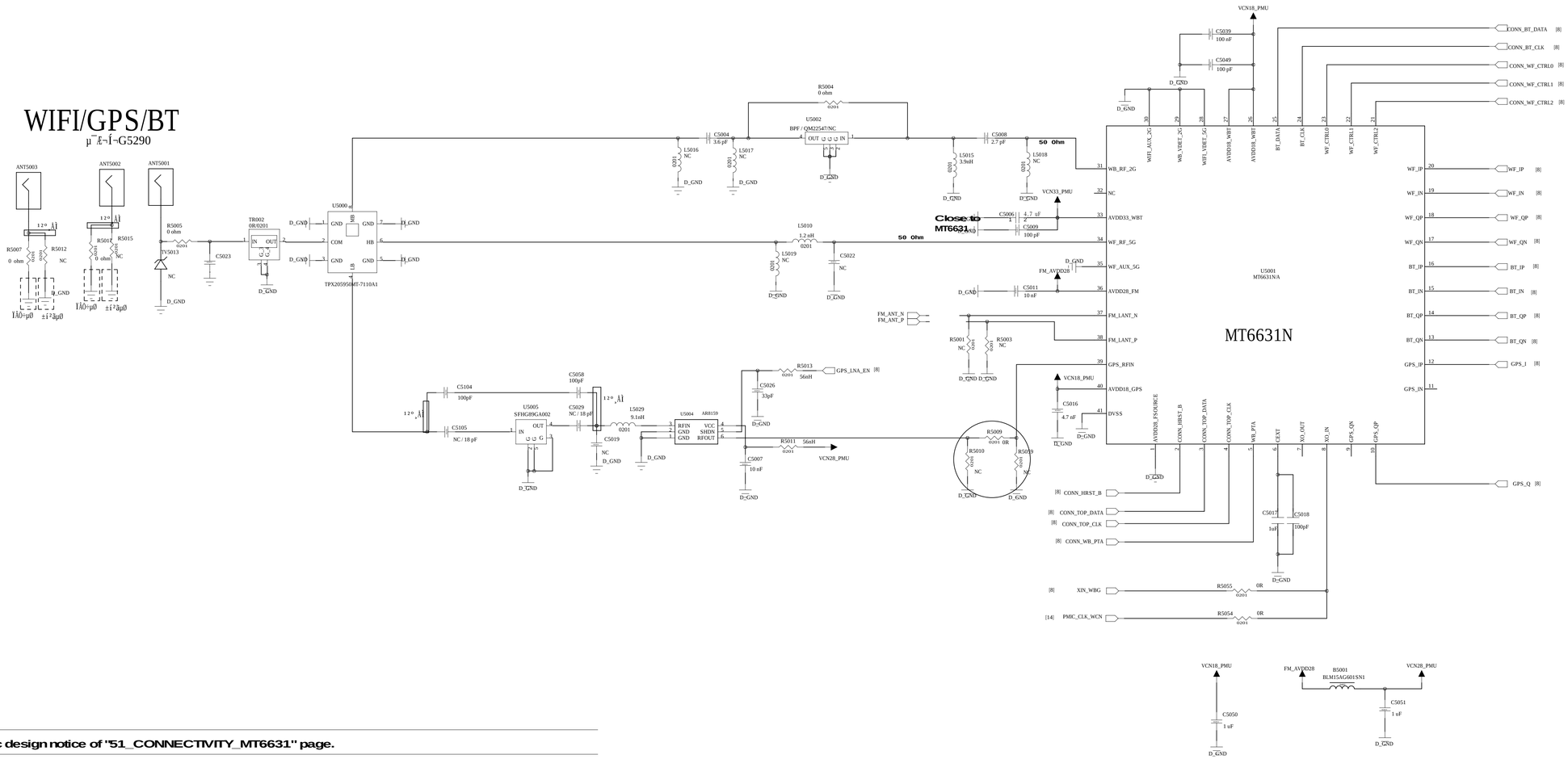
Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

WIFI/GPS/BT

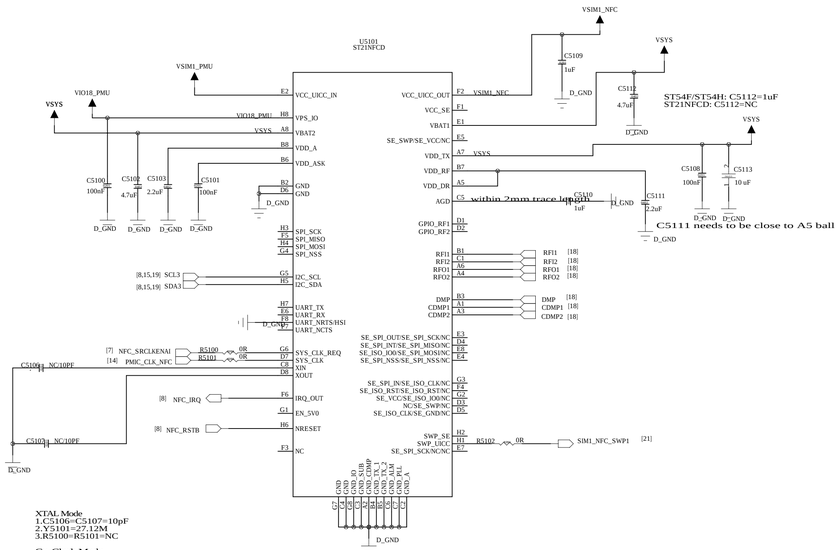
μ¯Æ¬Í¬G5290



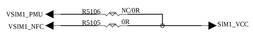
Schematic design notice of "51_CONNECTIVITY_MT6631" page.

Note 51-1:

Note 51-1: Add 3dB resistor attenuator at external LNA output for more AGC saturation margin. Please let total RF loss < 6dB from external LNA output to GPS chip-input.



ST21NFCD, ST54F and ST54H PCB footprint are the same.
ST21NFCD is NFC controller only; ST54F and ST54H are NFC controller with embeeded SE

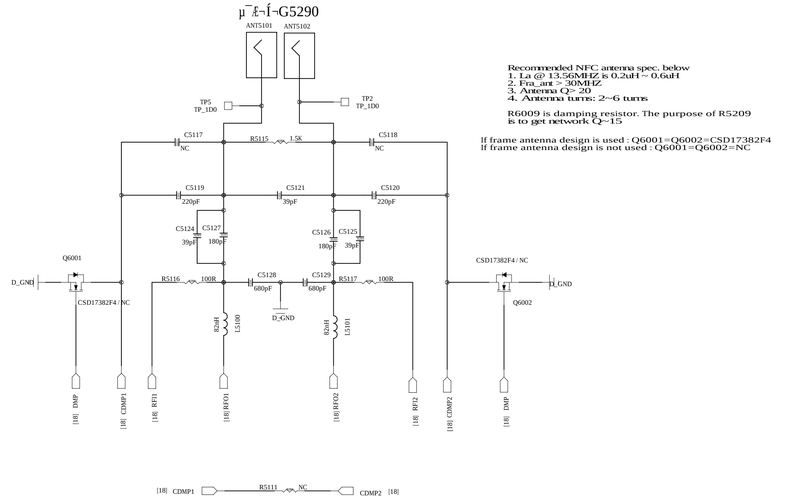


SE ball name definition for ST54F, ST54H, and ST21NFCD, respectively

Ball	ST21NFCD	ST54F	ST54H
D3	NC	SE_SWP	NC
D4	NC	SE_SPI_MISO	SE_SPI_INT
D5	NC	SE_GND	SE_ISO_CLK
E3	NC	SE_SPI_SCK	SE_SPI_OUT(MISO)
E4	NC	SE_SPI_NSS	SE_SPI_NSS
E5	NC	SE_VCC	SE_SWP
E7	NC	NC	SE_SPI_SCK
E8	NC	SE_SPI_MOSI	SE_ISO_IO0
F4	NC	SE_ISO_RST	SE_ISO_RST
G2	NC	SE_ISO_IO0	SE_VCC
G3	NC	SE_ISO_CLK	SE_SPI_IN(MOSI)

ANT CONN

µ¯g¬í¬G5290



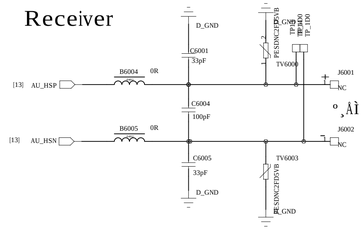
Recommended NFC antenna spec. below
1. La @ 13.56MHZ is 0.2uH ~ 0.6uH
2. Fra_ant > 30MHZ
3. Antenna Q> 20
4. Antenna turns: 2~6 turns

R6009 is damping resistor. The purpose of R5209 is to get network Q~15

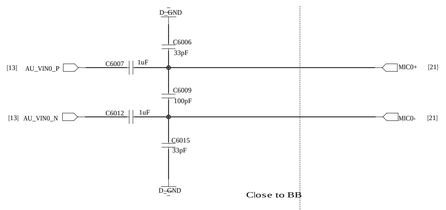
If frame antenna design is used : Q6001=Q6002=CSD17382F4
If frame antenna design is not used : Q6001=Q6002=NC

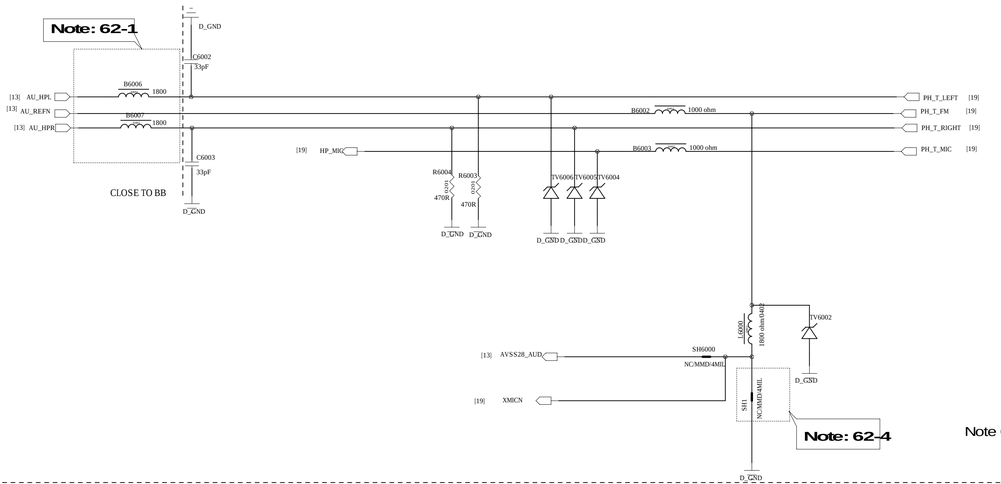
R5111 is reserved for RF network matching tuning

Receiver



MAIN MIC

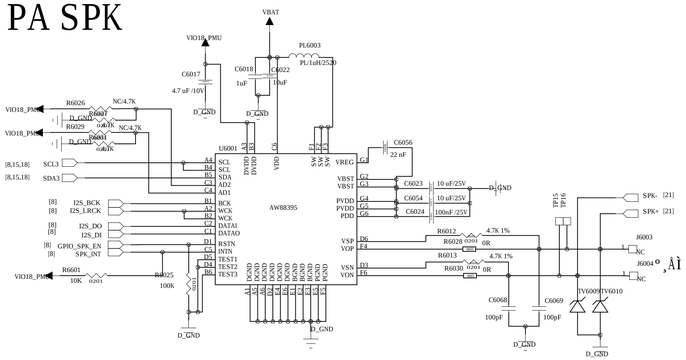




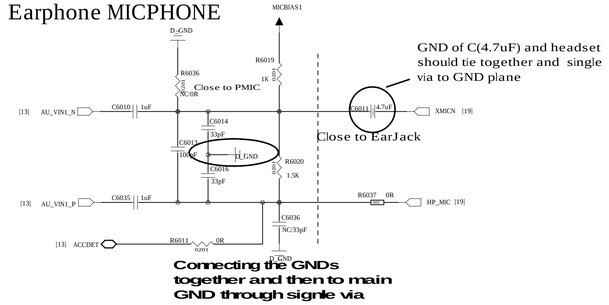
Note 62-4:

	Earphone Jack @ Main board	Earphone Jack @ Sub board
R6212	0 ohm	100nF

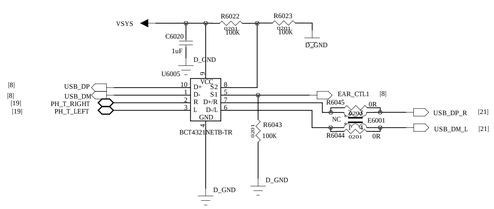
PA SPK

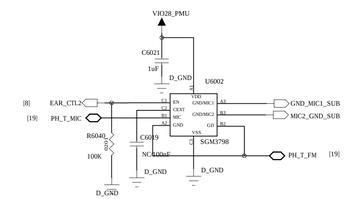


Earphone MICPHONE

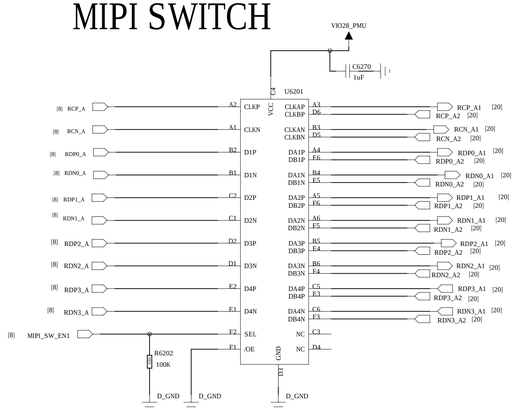


USB-DP/DM-AU-HPL/R-SWITCH-TYPE-C



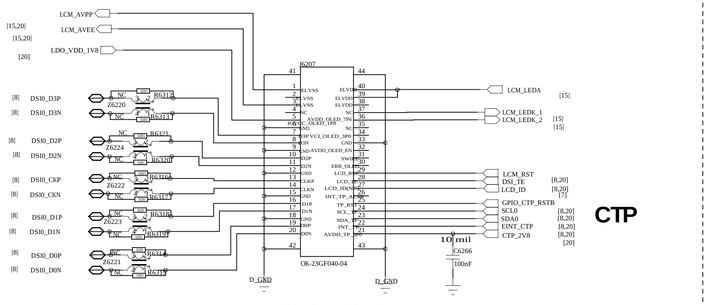


MIPI SWITCH



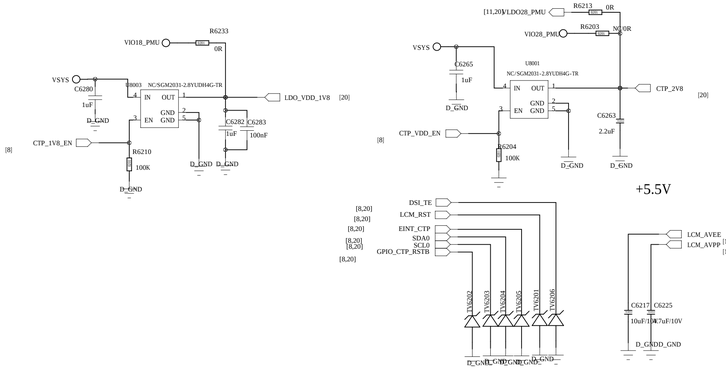
Main LCM

封装同G5290　定义有变动



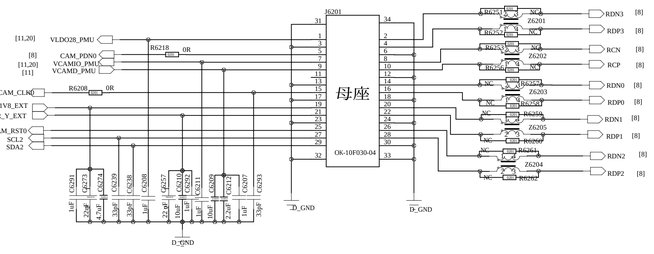
CTP

40pin　母座



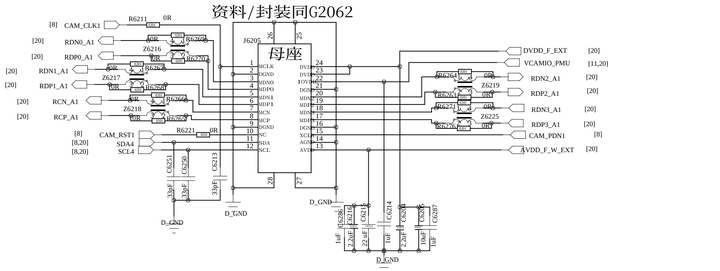
MAIN CAM

封装定义同G1929

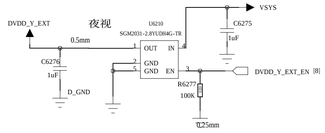


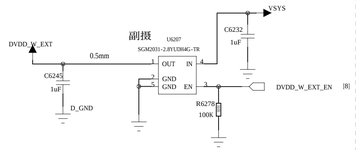
FOT CAM　前摄像头

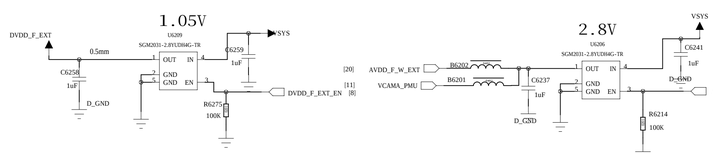
资料/封装同G2062



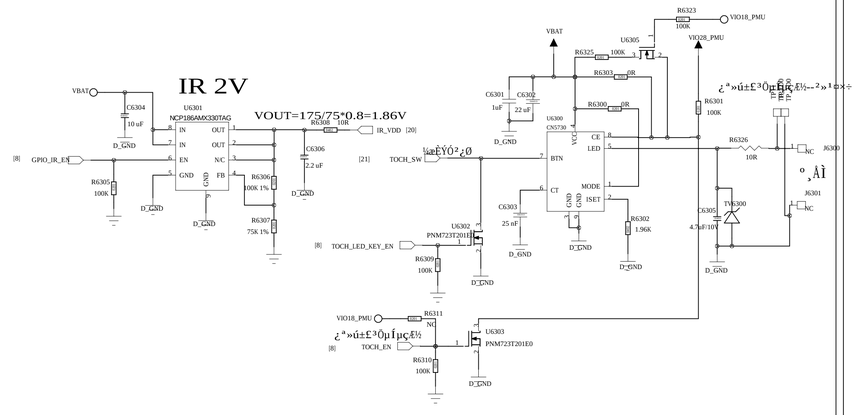
夜视



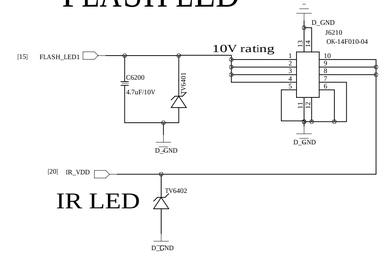


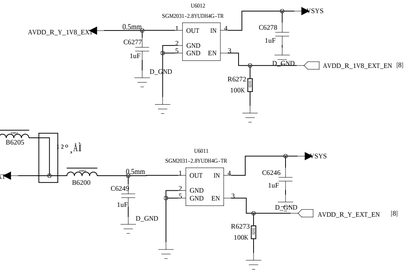


TOCH LED



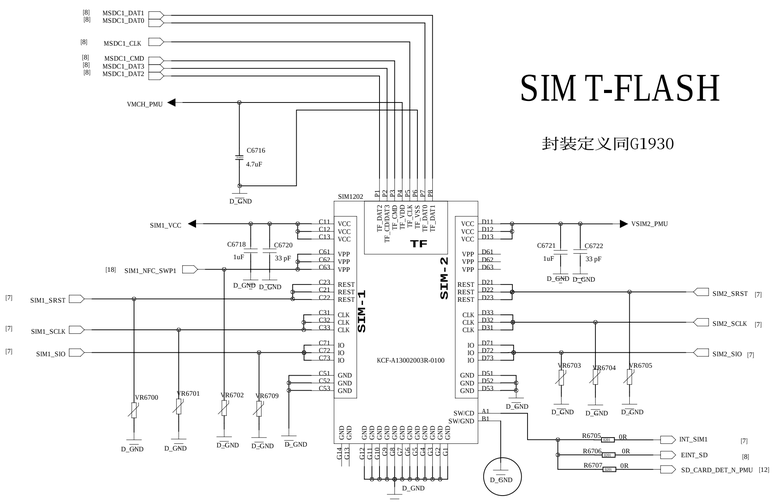
FLASH LED





SIM T-FLASH

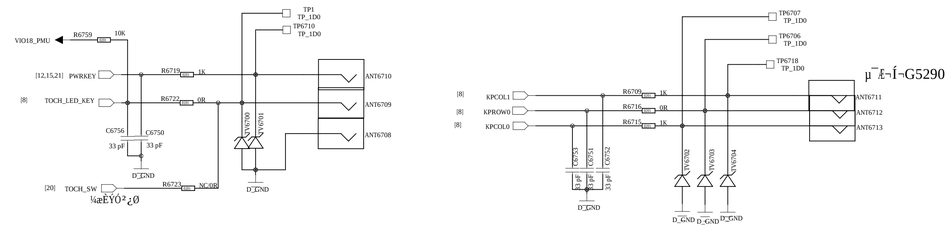
封装定义同G1930



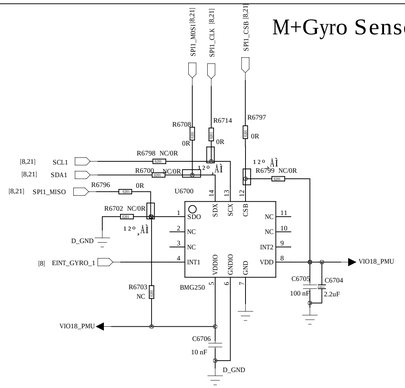
SIDE KEY

Volume Up ： KPROW0+KPCOL1

Volume Down : KPROW0 + KPCOL0



M+Gyro Sensor



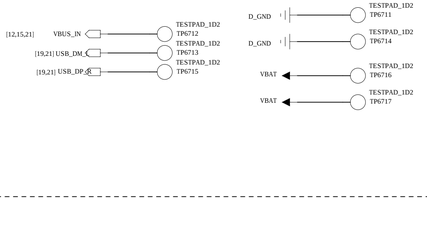
ALS & PS Sensor

封装定义同G2231

Finger Sensor

封装同G1970定义同G1915

LOG



SUB_CON

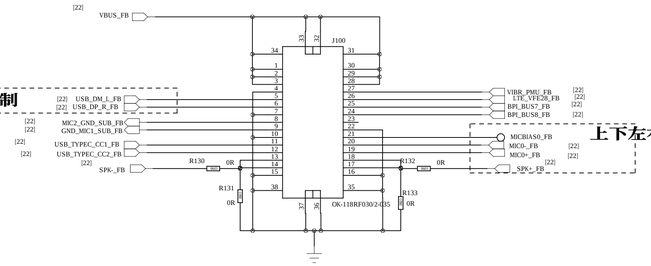
MOT+HOM+MIC+Fingerprint+SPK

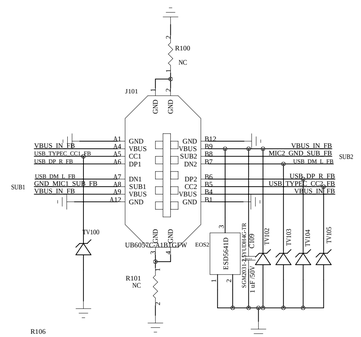
G-Sensor

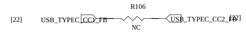
COMPASS

这两根要做阻抗控制

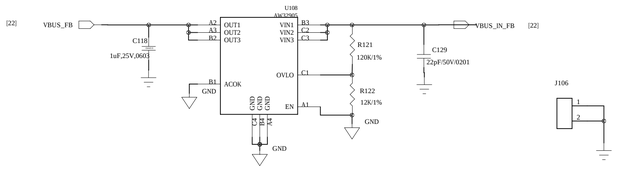
上下左右不包地，避开电源线



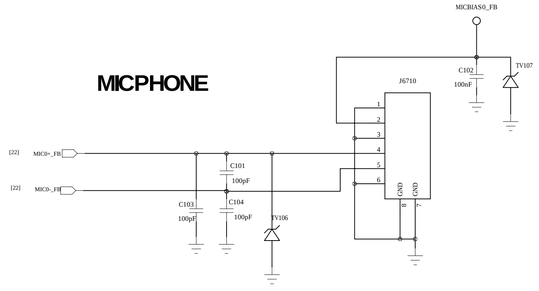




OVP



MICPHONE



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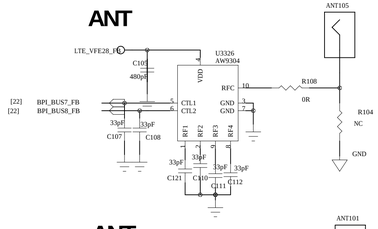

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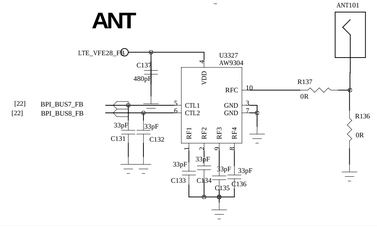

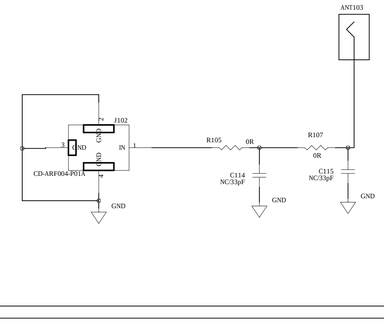

马达