Thundercomm

Empowering Every IoT Device with Our Technology

Qualcomm® Robotics RB5 Development Kit

Hardware User Manual

Rev. V1.1

Mar 12, 2021

Revision History

Revision	Date	Description
1.0	Sept 24, 2020	Initial release.
1.1	March 12, 2021	Fix typo in Top view in chapter 1.2.1. Remove description about ‘support headset jack’. Fix description for GPIO-B.

Table of Contents

1 Qualcomm® Robotics RB5 Development Kit

Qualcomm® Robotics RB5 Development Kit - the Company's most advanced, integrated, comprehensive offering designed specifically for robotics. Building on the successful Qualcomm® Robotics RB3 platform and its broad adoption in a wide array of robotics and drone products available today, the Qualcomm® Robotics RB5 Development Kit is comprised of an extensive set of hardware, software and development tools. The Qualcomm® Robotics RB5 Development Kit is the first of its kind to bring together the Company's deep expertise in 5G and AI to empower developers and manufacturers to create the next generation of high-compute, low-power robots and drones for the consumer, enterprise, defense, industrial and professional service sectors - and the comprehensive Qualcomm Robotics RB5 Development Kit helps ensure developers have the customization and flexibility they need to make their visions a commercial reality.

Based on the Qualcomm® QRB5165 Robotics SoC, the Qualcomm® Robotics RB5 Development kit contains a robotics-focused development board and compliant with the 96Boards open hardware specification which supports a broad range of mezzanine-board expansions for rapid prototyping.

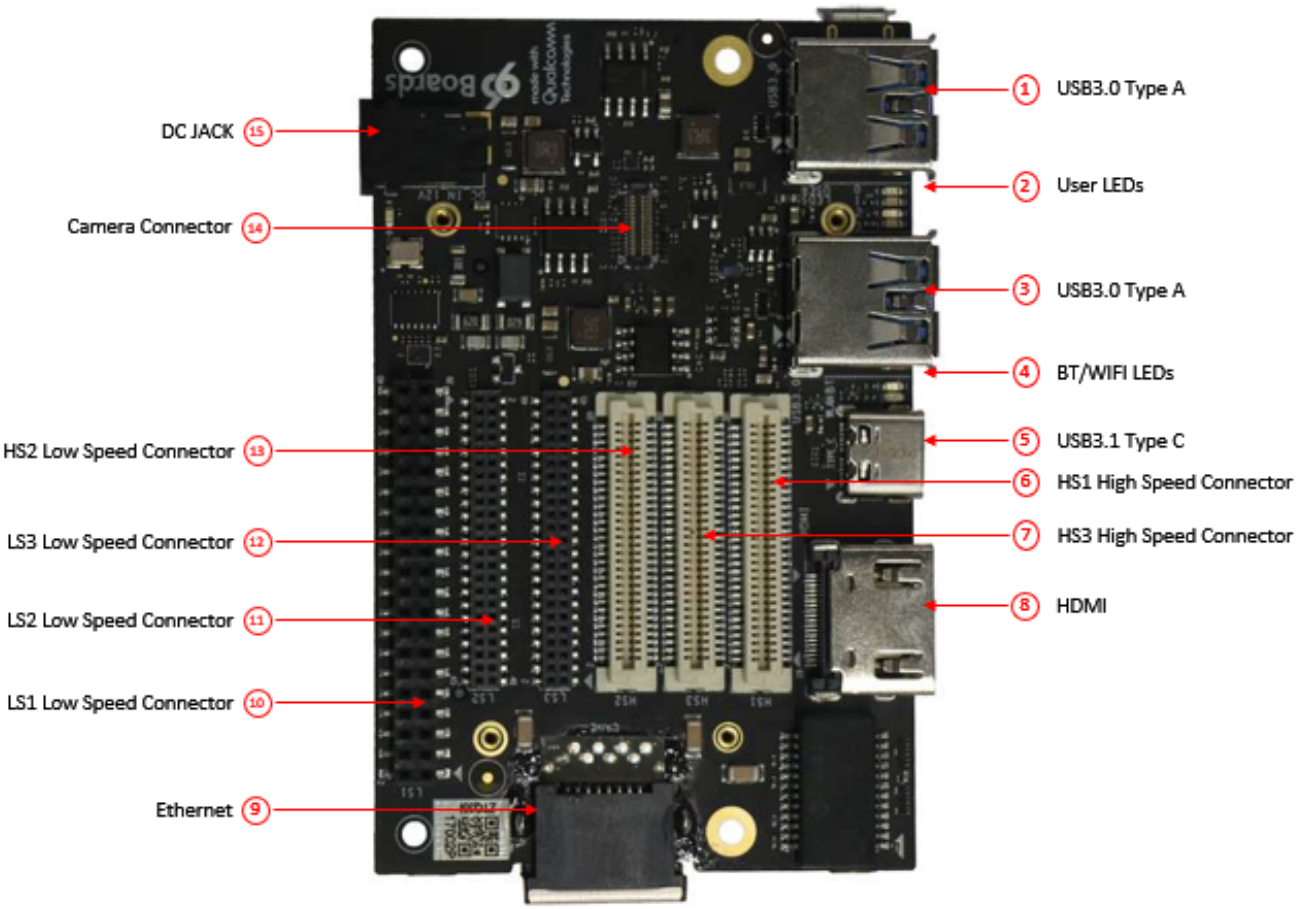
1.1 RB5 Development board Key Features

Component	Description
SOM Platform Feature	■ Snapdragon™ QRB5165 ■ LPDDR5(POP) + UFS, 8GB + 128GB ■ Wi-Fi/BT: QCA6391 (2x2 MIMO, 802.11 a/b/g/n/ac/ax & BT5.1) ■ LPDDR5(POP) + UFS, 8GB + 128GB
Ethernet	■ 1x GbE Ethernet
USB	■ 1 x USB 2.0 Micro B (Debug only) ■ 1 x USB 3.1 Type C (OTG mode) ■ 2 x USB 3.0 Type A (Host mode only)
Display	■ 1 x HDMI 1.4 (Type A - full)(support 4K60 output) on board connector
Camera	■ 1 x B2B connector with 4L-MIPI CSI D-PHY&C-PHY supported (on SOM)
Audio	■ 2 x Class-D on board speaker amplifier, WSA8815 ■ 1 x on board PDM MIC
Sensor	■ A+G sensor
FAN	■ FAN connector with 12V output and PWM control

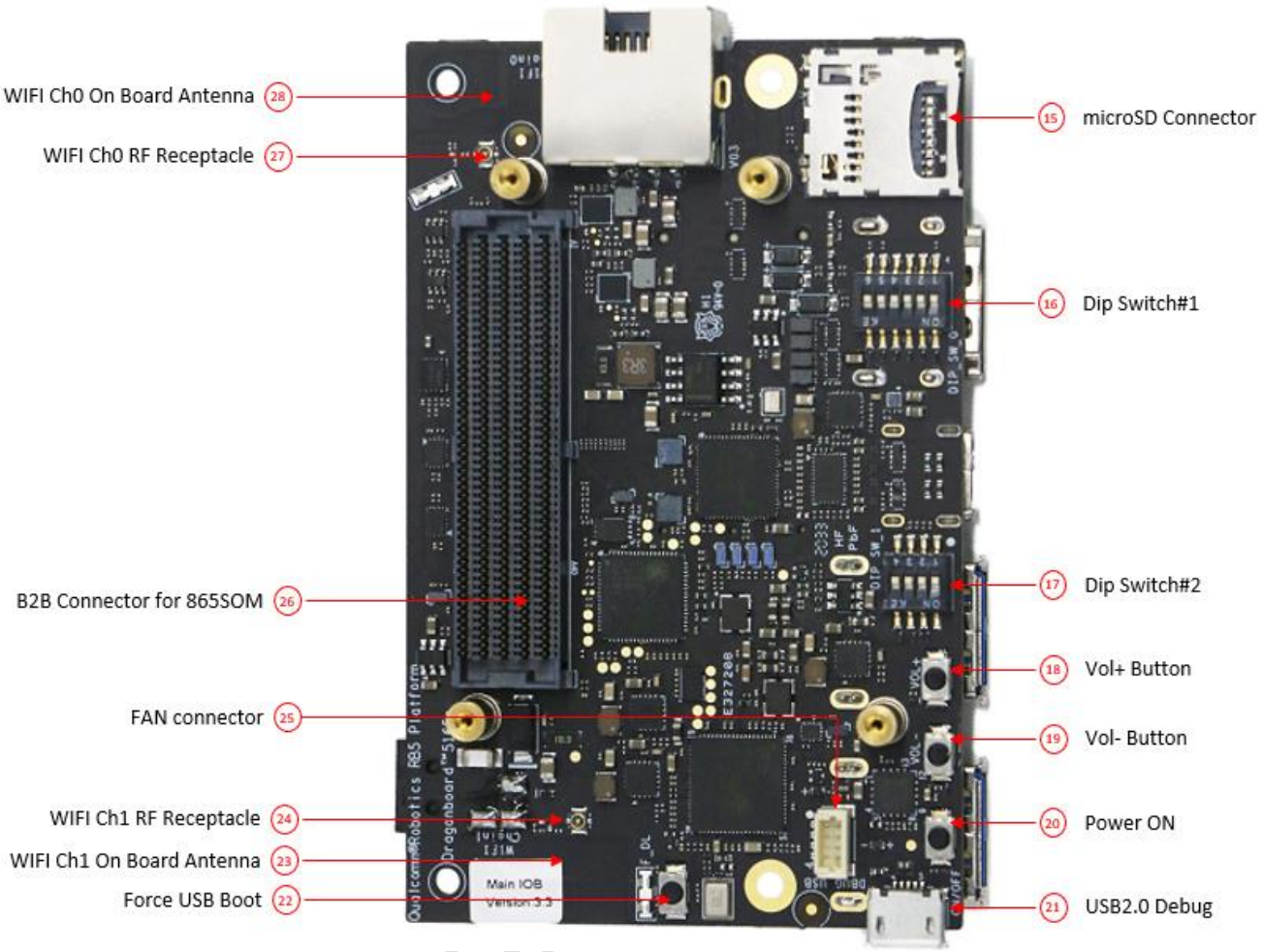
LED	■ 7 LED indicators: 4 x User controllable 2 x For radios (BT and WLAN activity) 1 x Power indicator
Button	■ Power ON ■ Volume Up/Down ■ Force USB Boot ■ DIP Switch x 2 (6pin+4pin)
Expansion interface	■ HS1:1 x 60 pin high-speed connector (SDC I/F, 1 x 4L MIPI DSI, USB 2.0, CCI I2C x2, 2L+4L-MIPI CSI) ■ HS2:1 x 60 pin high-speed connector (4L-MIPI CSI x 2, SPI x 1, PCIe 3.0 gen3 1L, USB 3.0 x1, GPIO x 8) ■ HS3:1 x 60 pin high-speed connector (4L-MIPI CSI x 2, 4L-MIPI CSI x1(plus 2L CSI in HS1), RF CLK x 2, 2L-PCIe 3.0 x 1, 2L-PCIe 3.0 x 1 (plus PCIe 1L in HS2), 4L-MIPI DSI x 1) ■ LS1:1 x 96boards 40 pin low-speed connector (UART x 2, SPI, I2S/PCM, I2C x 2, GPIO x 12, DC powers) ■ LS2:1 x 96boards 40 pin low-speed connector (Speaker x 2, DMIC I/F x 3, CAN, I2S, GPIOs, PWM, ADC, I2C, DC powers) ■ LS3:1 x 96boards 40 pin Low-Speed connector (SPI x 2, SSC I2C, sensor interrupt x 5, GPIOs, RTC clock, DC powers)
Operating Environment	■ Operation Temperature: -20℃ ~ 70℃ ■ Operation Humidity: 5%~95%, non-condensing **NOTE**: Tj<95℃ (compliant with QRB5165's working temperature requirement)
Power supply	■ 12V@2.5A adapter with a DC plug, with inner diameter as 1.75mm and outer diameter as 4.75mm
Dimension	■ 85mm x 54mm, meeting 96Boards Consumer Edition Standard form dimensions specifications

1.2 Board views

1.2.1 Top view



1.2.2 Back view



1.2.3 Terms and Definitions

Component	Description
QUP	Qualcomm Universal Peripheral The QUP engine provides a general-purpose data path that supports multiple mini cores, e.g., UART, I2C and SPI
CCI	Camera Control Interface
SPMI	System Power Management Interface

2 Start the board

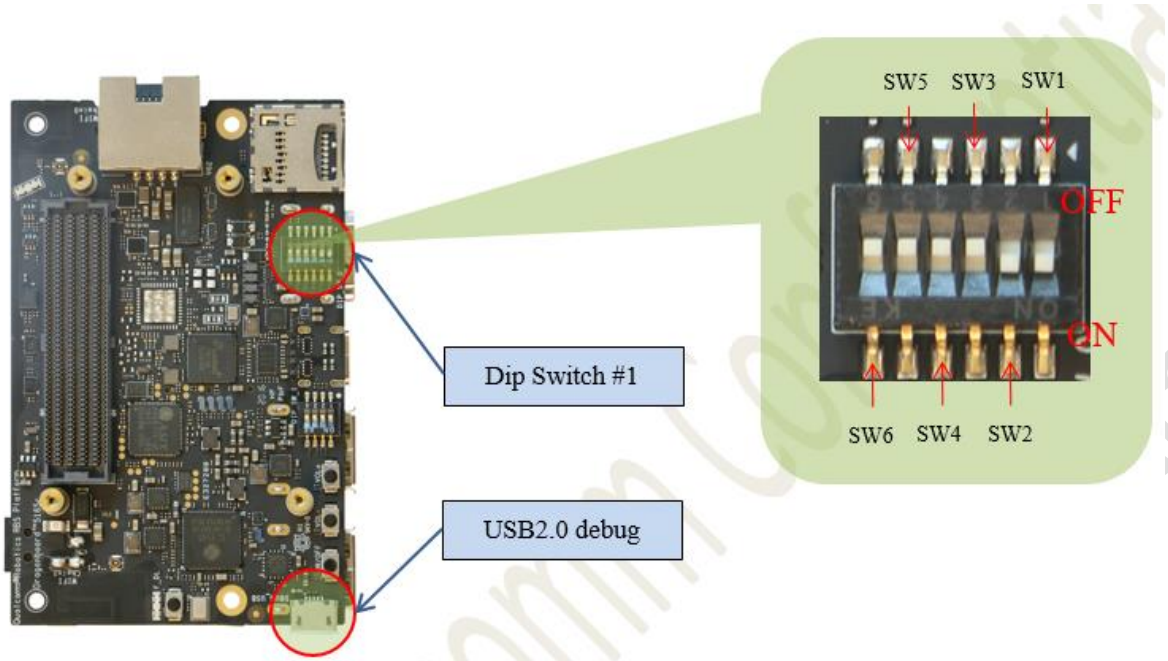
2.1 Required equipment

Equipment	Description
Qualcomm® Robotics RB5 Development Kit	SOM based on the Qualcomm® QRB5165 processor IO based on 96board requirement
Power adapter	12 V with 2500 mA required per 96Boards specification
USB to Micro USB cable	For serial console interface and ADB, Fastboot commands
USB to USB Type C cable	For connecting the USB3.0 Type C port and flashing images
Host PC	For connecting the board and installing Fastboot

2.2 Ubuntu Embedded OS startup process

Display is not supported in the LE OS.

1. Open the serial console tool on host PC (for example: minicom).
2. Turn on SW2 on the Dip Switch#1 (see section 1.2.2, #16) to enable the USB2.0 debug port (see Section 1.2.2, #21).
3. Turn on SW3 on the Dip Switch#1 (see section 1.2.2, #16) to enable the auto power up on (along with power connector).



4. Connect the USB cable Micro-B plug to the USB2.0 debug port (see section 1.2.2, #21), and connect the other end to an available USB port on the host PC.

NOTE: Set the Bps/Par/Bits to 115200 8N1

5. Connect the power supply to power connector (see section 1.2.1, #15).

6. Plug the power supply into a power outlet.

7. Press, and hold the power button on the device, and then release it. The green power-up LED should illuminate in a second.

8. The board will start the booting process. Login credentials will display on the host PC:

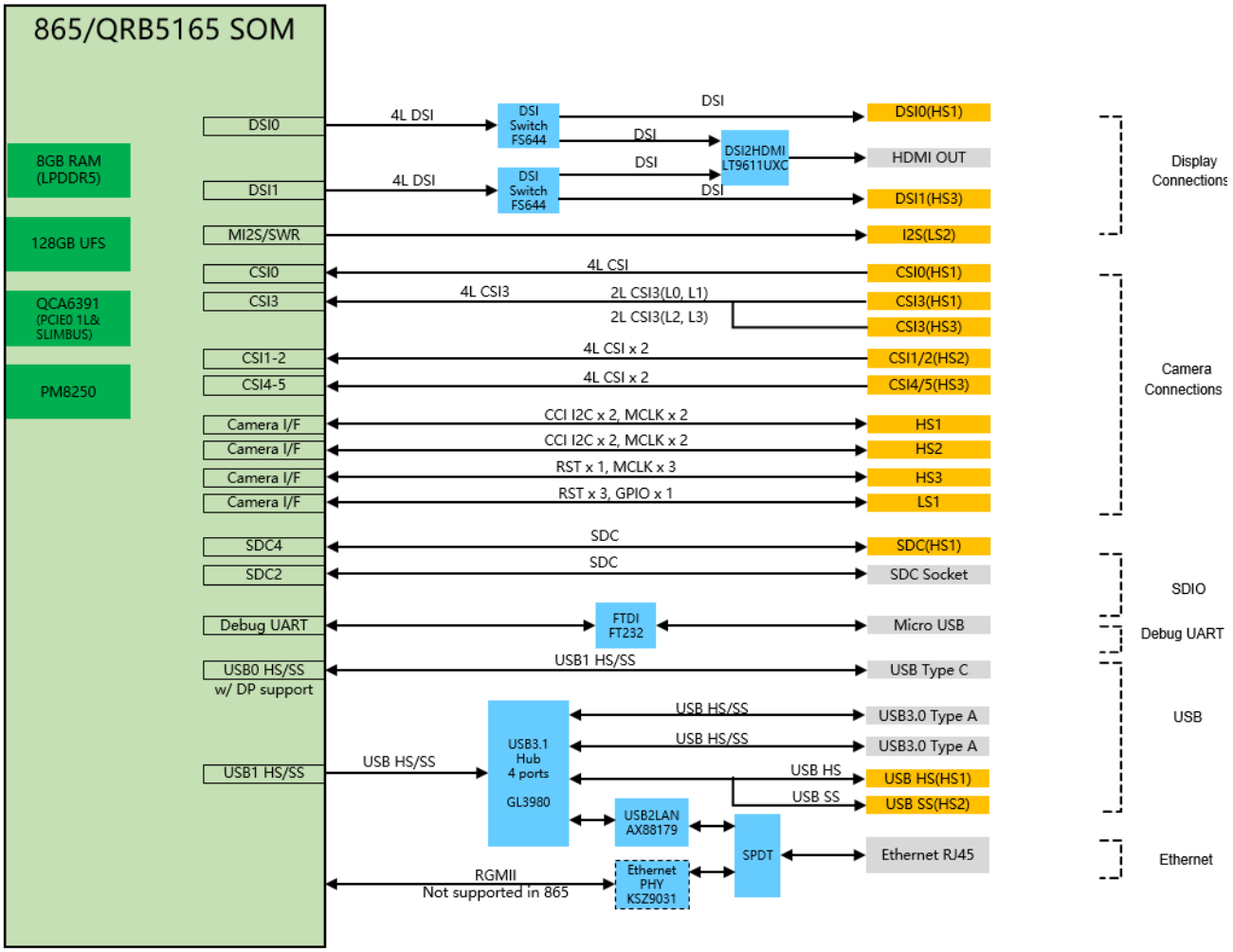
qrb5165-rb5 login: root

Password: oelinux123

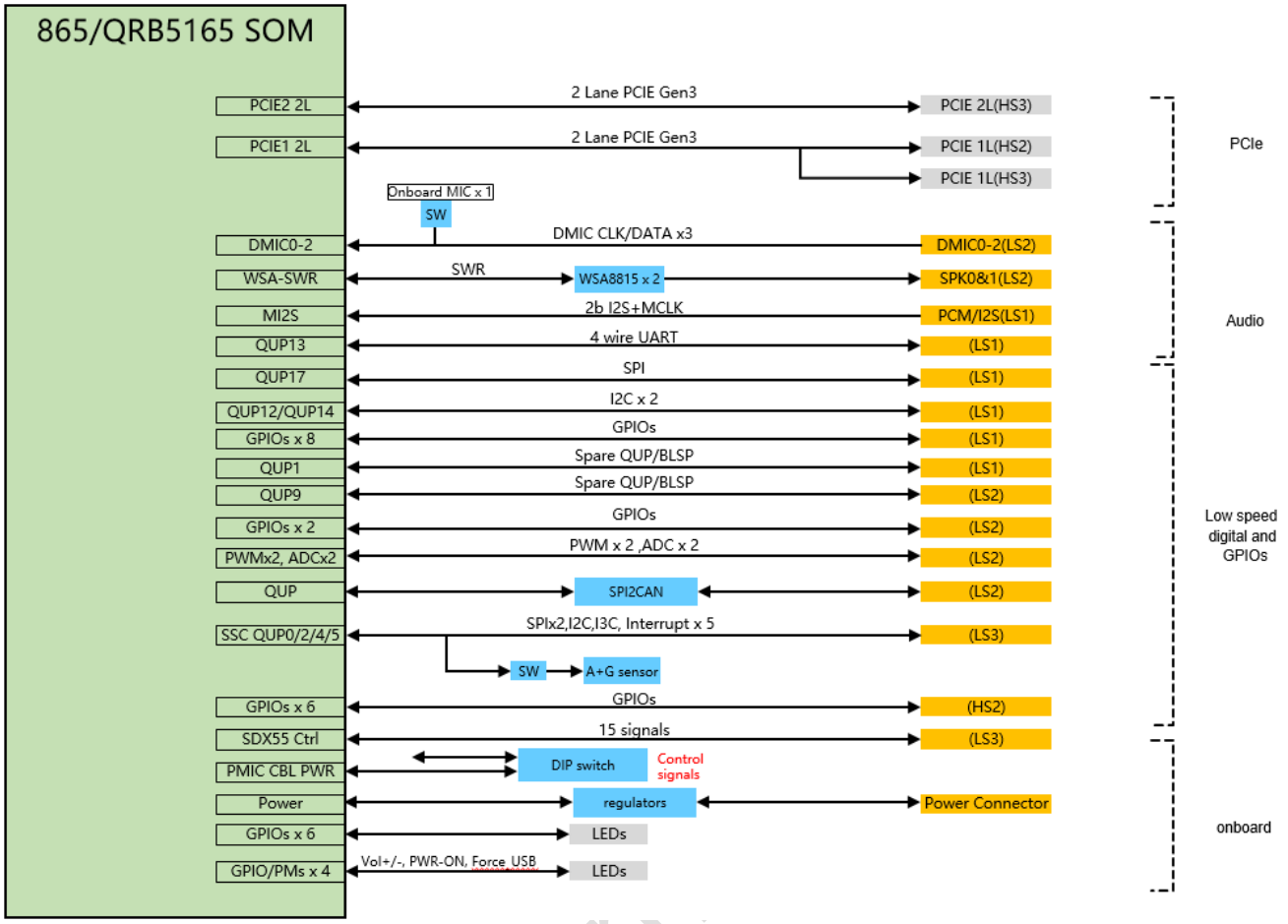
3 Qualcomm® Robotics RB5 Development Kit

3.1 System Block diagram

Block diagram part #1



Block diagram part #2



3.2 Processor

QRB5165 is the new generation Qualcomm® Snapdragon™ premium-tier processor with robotic application. It is designed with the 7 nm process, for superior performance and power efficiency.

3.3 Memory

The QRB5165 uses a package on package (PoP) LPDDR5 RAM configuration and discrete UFS3.0 flash memory.

- The LPDDR5 interface goes directly to the QRB5165 built-in LPDDR controller. The maximum DDR clock is 2750MHz.
- The UFS flash memory interfaces with QRB5165 over a dedicated UFS PHY bus supporting the UFS 3.0 specification.

3.4 MicroSD

MicroSD slot signals are routed directly to the QRB5165 SDC2 interface.

The slot is a push-push type with dedicated support for card detect signal (many microSD slots do not have dedicated CD pins, they use DATA3 state as the card detected signal). RB5 uses AP GPIO_77 as the SD_CARD_DET_N.

3.5 Wi-Fi/BT

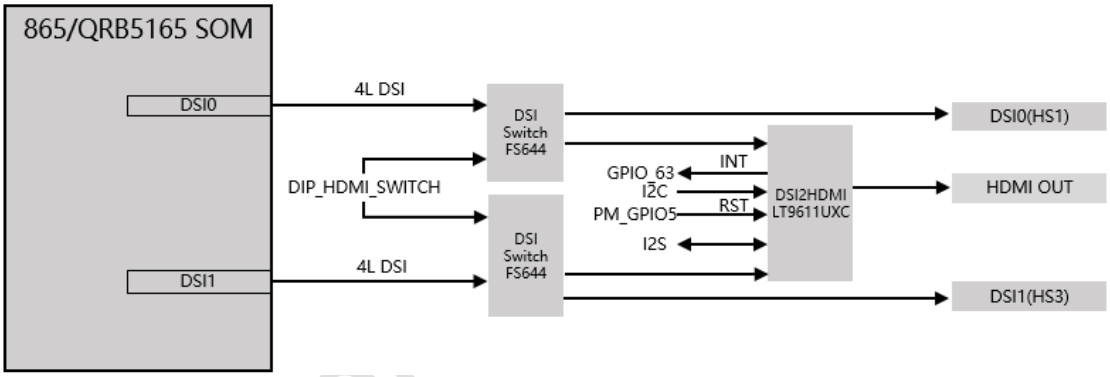
RB5 uses the Qualcomm RF chip QCA6391 solution that integrates two wireless connectivity technologies into a single device.

The interfaces are:

- WLAN-compliant with IEEE 802.11 b/g/n/ac/ax specifications, exceeding 96Boards minimum Wi-Fi requirements
- Bluetooth compliant with BT Milan and ANT+, supports BLE/BLE long range(BT specification version 5.1), meeting the 96Boards BT requirements

The antenna socket #27, for Wi-Fi chain 0 (and optionally BT) and antenna socket #24, for Wi-Fi chain1 are just backup solutions.

3.6 Display Interface



3.6.1 HDMI

The 96Boards specification calls for an HDMI port to be present on the board.

Because QRB5165 doesn't include a built-in HDMI interface, RB5 deploys the built-in MIPI-DSI 2x4 lanes interface as the source for the HDMI output. A DSI to HDMI Bridge (LONTIUM SEMICONDUCTOR LT9611UXC) performs this task and it supports a resolution from 1080p to 4K at 60Hz.

While the LT9611UXC supports automatic input video format timing detection (D-PHY1.2, DSI1.3/CSI-2 1.00 and DCS 1.02.00), an I2C channel from the QRB5165 also allows users to configure the operation of this bridge. It is QUP5 I2C interface from SoC.

This bridge supports audio as well (meeting the 96Boards requirements for providing audio via HDMI). The RB5 uses a 4 bit I2S2 interface from the QRB5165 for this task.

96Boards specification also calls for a MIPI-DSI interface to be routed to the High Speed Expansion connector. Since the QRB5165 has two MIPI-DSI interface for HDMI, two multiplexing devices (FSA644UCX) are used. Only one interface, HDMI, or the Expansion MIPI-DSI can be active at one time. Control signal, 'DIP_HDMI_SWITCH', comes from DIP switch#16. When this signal is set to OFF state, DIP_HDMI_SWITCH is logic HIGH '1', MIPI-DSI signals will be routed to DSI-HDMI Bridge. When the signal of DIP switch is set to ON state, DIP_HDMI_SWITCH as logic LOW '0', MIPI-DSI signals will be routed to the High Speed Expansion connector.

3.6.2 MIPI-DSI

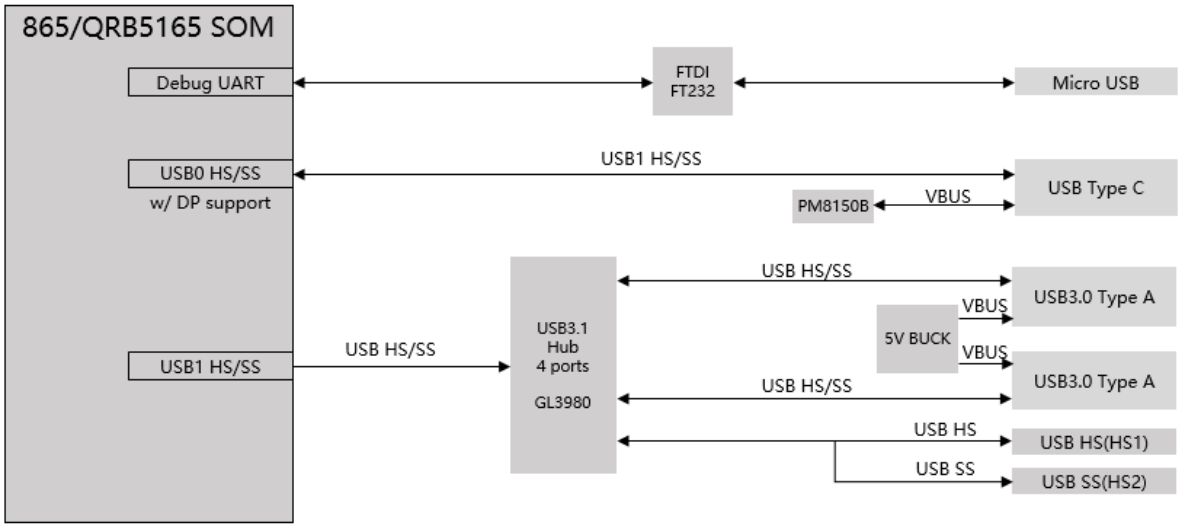
RB5 has 2x 4-lane MIPI_DSI interface. See below for details.

3.7 Camera Interfaces

RB5 has 6x 4L camera interfaces.

- 4-lane CSI0 camera on high-speed connector HS1 (section1.2.1 #6) ;
- 4-lane CSI1camera on high-speed connector HS2 (section1.2. #13)
- 4-lane CSI2 camera on high-speed connector HS2 (section1.2.1 #13)
- 4-lane CSI3 camera on high-speed connector HS1 (section1.2.1 #6) and high-speed connector (section1.2.1 #7)
- 4-lane CSI4 camera on high-speed connector HS3 (section1.2.1 #7)
- 4-lane CSI5 camera on high-speed connector HS3 (section1.2.1 #7)

3.8 USB Ports



3.8.1 USB-Host ports

The QRB5165 processor includes two USB channels:

- USB0 (section1.2.1 #5) is for USB Type C.
- USB1 (through a USB HUB to section1.2.1 #1&#3) is USB host only ports.
  RB5 supports below USB host ports by USB HUB mentioned above:
- Two Type A USB Host 3.0 (super-speed) connector, each with current limit 1.2A.
- USB 3.0 signals are also routed to high-speed expansion connector HS1&HS2.

3.8.2 USB TypeC port

RB5 implements a USB Type C port (section1.2.1#5)
This Type C port supports both device and host mode with different peripherals. The board can work in one mode at a time.
NOTE: There is a micro USB port section1.2.2#21. This micro B USB port is used only for debug-log-output from the QRB5165 with a debug UART to USB bridge.

3.9 Audio

The 96Boards specifications calls for a minimum of single channel audio through two interfaces, BT and HDMI/MHL/DisplayPort.
RB5 meets this requirement with HDMI, Display Port, and other audio channels.
Note that MHL is not supported.

3.9.1 BT Audio

The BT 5.1 implementation (including audio) on the Qualcomm® Robotics RB5 Development Kit is with QRB5165 and QCA6391.

3.9.2 HDMI Audio

A 4-bit (audio out only) I2S channel is routed directly from the QRB5165 SoC I2S interface pins to the DSI-HDMI bridge.

3.9.3 DisplayPort Audio

The DisplayPort audio is routed directly from the QRB5165 SoC eDP interface pins to the Type C USB connector.

3.10 DC-power and Battery Power

RB5 power is supplied in one of the following ways:

- 8 V to 18 V power from a dedicated DC jack
- 8 V to 18 V power from the DC12V pins on the low-speed expansion connector

See Section 6 for details on Robotics RB5 Development Kit DC power implementation.

3.11 DC power Measurements

The 96Boards specification calls for support for measuring board power consumption.
See Section 6 for details on Robotics RB5 Development Kit DC power measurement.

3.12 Buttons

The 96Boards specification calls for the presence of two buttons, a power on/sleep button and a reset button. RB5 meets these requirements.
See Section 7 for details on RB5 buttons.

3.13 External Fan connection

The 96Boards specification calls for support of an external fan. There is a on-board fan connector on main IO(see section 1.2.2, #25), fan power is 12V.

3.14 UART

RB5 supports one 4bit UART, and a 2bit UART (optional), and both of them are routed to the low-speed expansion connector.
The 4bit UART comes directly from SoC pins to low-speed expansion connector. The 2bit UART is optional an on-board UART debug log port via Micro USB port#21, or to be routed to low-speed expansion connector. To use the port for log output, switch DIP_DEBUG_UART_SWITCH on DIP switch (section 1.2.2#16) to ON.

3.15 JTAG (NA)

NA

3.16 System and user LEDs

RB5 supports seven LEDs on the board. LEDs color and mechanical location on the board are designed based on 96Boards specification.

Two activity LEDs

- Wi-Fi activity LED – RB5 drives this Yellow LED via GPIO_9 from the PMIC (PM8250).
- BT activity LED – RB5 drives this Blue LED via GPIO_7 from the PMIC (PM8250).

Four user LEDs

The four user LEDs are surface mount LEDs in 0603 size located next to the two USB Type A connectors and labeled with ‘USER LEDS 3 2 1 0’ .
RB5 drives three of them by the red, green and blue LED drivers from power management IC PM8150L.
The fourth one is driven by the PM8250 via GPIO_10.

Power indicator LED

A Green LED

3.17 Expansion Connector

The 96Boards specification calls for two expansion connectors, a low-speed connector and a high-speed connector.
RB5 meets this requirement. See Section 4 for details about the low-speed expansion connector and Section 5 for high speed expansion connectors.

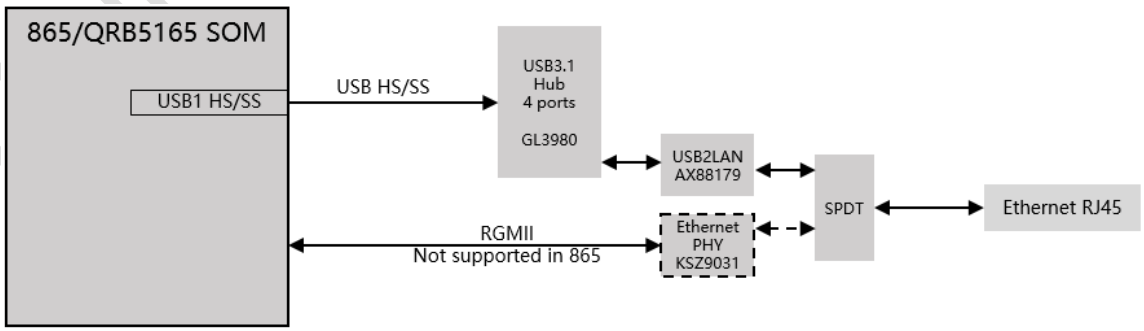
3.18 Additional Functionality

The 96Boards specification permits additional functionality provided:

- All mandatory functionality is available
- No impact to the physical footprint specification (including height)
- No impact to the use of 96Boards CE low-speed and high-speed expansion facilities

RB5 implements a few additional functions as described from Sections 3.17.1 to 3.17.4

3.18.1 Ethernet Connector



RB5 has the translation from USB1, a USB HUB and a USB to Gigabit Ethernet controller. RB5 uses an RJ45 (see Section1.2.1, #9) as the physical interface.

3.18.2 Inertial Sensors

RB5 includes the following inertial sensors.

- 6-axis accelerometer/gyroscope: INVENSENSE ICM-42688

The SPI interface for ICM-42688 is multiplexing to LS3 by a SPDT, controlled by DIP_SENSOR_SWITCH_IMU. Setting DIP_SENSOR_SWITCH_IMU of DIP switch (section1.2.2 #16) to OFF will enable ICM-42688's SPI communication.

3.18.3 DIP Switch

RB5 has two DIP switches (see Section 1.2.2, #16&#17).

DIP switch (section1.2.2 #16)

- Switch 1 – DIP_MIC_SWITCH: When set to ON, will enable on board MIC; when set to OFF, will enable DMIC1 on LS2
- Switch 2 – DIP_DEBUG_UART_SWITCH: When set to ON position, will enable on board debug UART; when set to OFF, will enable UART1 on LS1.
- Switch 3 – CBL_PWR_N: When set to ON, the QRB5165 system will power on automatically when main power is asserted; when set to OFF, the QRB5165 system will power on by ON-KEY manual press.
- Switch 4 – DIP_HDMI_SWITCH: When set to ON, will enable DSI0 to HS1 and DSI1 to HS3; when set to OFF, will enable DSI1&2 to LT9611UXC and on board HDMI.
- Switch 5 – DIP_SENSOR_SWITCH_IMU: When set to ON, will enable SPI to LS3; when set to OFF, will enable SPI to on board sensor ICM_42688.
- Switch 6 – IMU_EXT_CLK_TOGGLE: When set to ON, the onboard ICM-42688 sensor will use the external CLK of GPIO3 from PM8250; when set to OFF, the onboard ICM-42688 sensor will output interrupt to SoC GPIO113. These GPIOs need the software configure setting.

DIP switch (section1.2.2 #17)

- Switch 1 – BOOT_CONFIG(1)
- Switch 2 – BOOT_CONFIG(2).
- Switch 3 – BOOT_CONFIG(3)
- Switch 4 – BOOT_CONFIG(0)

3.18.4 Extra Low Speed Expansion Connector

RB5 has 3 extra low-speed expansion connectors. See Section 4 for detail.

3.18.5 Extra High Speed Expansion Connectors

RB5 has 3 high-speed expansion connector. See Section 5 for detail

4 Low speed Expansion connector

4.1 Primary Low Speed Expansion Connector: LS1

PIN	RB5 Signal	Additional Info
1	GND	
3	UART0_CTS	QUP13
5	UART0_TXD	QUP13
7	UART0_RXD	QUP13
9	UART0_RTS	QUP13
11	UART1_TXD	QUP12
13	UART1_RXD	QUP12
15	I2C0_SCL	QUP4
17	I2C0_SDA	QUP4
19	I2C1_SCL	QUP15
21	I2C1_SDA	QUP15
23	GPIO-A/QUP-A0	QUP1
25	GPIO-C/QUP-A1	QUP1
27	GPIO-E/QUP-A2	QUP1
29	GPIO-G	DISPLAY_VSYNC
31	GPIO-I	CAM0_RST_N
33	GPIO-K	CAM1_RST_N
35	+1V8	From PM8250 BUCK
37	+5V	From on board DCDC
39	GND	

PIN	RB5 Signal	Additional Info
2	GND	
4	PWR_BTN_N	PHONE_ON
6	RST_BTN_N	Default volume down;
8	SPI0_SCLK	QUP17
10	SPI0_MISO	QUP17
12	SPI0_CS	QUP17
14	SPI0_MOSI	QUP17
16	PCM_FS/I2S0_WS	
18	PCM_CLK/I2S0_CLK	
20	PCM_DO/I2S0_D1	
22	PCM_DI/I2S_D0	
24	GPIO-B	PCM0_MCLK / MI2S0_MCLK
26	GPIO-D/QUP_A3	QUP1

28	GPIO-F	DISPLAY MIPI_ERR_ FG / QUP15
30	GPIO-H	DISP_RST_N
33	GPIO-J	CAM0_PWDN
34	GPIO-L	CAM1_PWDN
36	DC12V	
38	DC12V	
40	GND	

4.1.1 UART

The 96Boards specification calls for a 4-wire UART implementation, UART0 and an optional second 2-wire UART, UART1 on the low-speed expansion connector.

RB5 implements UART0 as a 4-wire UART that connects directly to the QRB5165 SoC. These signals are driven at 1.8 V.

RB5 implements UART1 as a 2-wire UART that connects directly to the QRB5165 SoC. These signals are driven at 1.8 V.

4.1.2 I2C

The 96Boards specification calls for two I2C interfaces to be implemented on the low-speed expansion connector.

RB5 has both I2C0 and I2C1 interfaces. The interfaces connect directly to the QRB5165 SoC. A resistor is needed to provide pull-up for each of the I2C lines per the I2C specifications. These pull-ups are connected to the 1.8 V voltage rail.

4.1.3 GPIO

The 96Boards specification calls for twelve GPIO lines to be implemented on the low-speed expansion connector.

RB5 implements this requirement. Twelve GPIOs are routed from the QRB5165 SoC. The GPIOs are 1.8V voltage rail.

- GPIO A/QUP_A0: Connects to GPIO_4 of QRB5165 SoC. Can be configured to be an IRQ line.
- GPIO B: Connects to GPIO_136 of QRB5165 SoC. Can be configured to be an IRQ line and MI2S master clock.
- GPIO C/QUP_A1: Connects to GPIO_5 of QRB5165 SoC.
- GPIO D/QUP_A3: Connects to GPIO_7 of QRB5165 SoC.
- GPIO E/QUP_A2: Connects to GPIO_6 of QRB5165 SoC.
- GPIO F: Connects to GPIO_46 of QRB5165 SoC.

- GPIO G: Connects to GPIO_6 of QRB5165 SoC.
- GPIO H: Connects to GPIO_116 of QRB5165 SoC.
- GPIO I: Connects to GPIO_93 of QRB5165 SoC.
- GPIO J: Connects to GPIO_114 of QRB5165 SoC.
- GPIO K: Connects to GPIO_92 of QRB5165 SoC.
- GPIO L: Connects to GPIO_109 of QRB5165 SoC.

4.1.4 SPI

The 96Boards specification calls for one SPI bus master to be provided on the low-speed expansion connector.

RB5 implements a full SPI master with 4 wires: CLK, CS, MOSI, and MISO. All signals go directly to the QRB5165 SoC. These signals are driven at 1.8 V.

4.1.5 PCM/I2S

The 96Boards specification calls for one PCM/I2S bus to be provided on the low-speed expansion connector.

The CLK, FS, and DO signals are required while the DI is optional.

RB5 implements a PCM/I2S with 4 wires: CLK, FS, D0~D1. The I2S signals are connected directly to the QRB5165 SoC. These signals are driven at 1.8 V.

4.1.6 Power and Reset

The 96Boards specification calls for a signal on the low-speed expansion connector that can power on/off the board and a signal that serves as a board reset signal.

RB5 routes the PWR_BTN_N signal to the KYP_DPWR_N pin of the PM8250 PMIC. This signal is available on the onboard Power ON button switch (see Section 1.2.2, #20). The button only provides an ON/Sleep function and not OFF functionality.

A mezzanine implementation of this signal should not drive it with any voltage, the only allowed operation is to force it to GND to start the board from a sleep mode. A board shutdown will occur when this signal is held to ground for more than 15 seconds.

RB5 routes the RST_BTN_N (named PM_RESIN_N on the Robotics RB5 Development Kit schematic) signal to the RESIN_N pin of the PM8250 PMIC. This signal is driven by SW1302, the onboard reset switch (see Section 1.2.2, #17). This signal is dual purpose, the default purpose is Volume down, and the second purpose is the Reset function which needs the software configure setting.

4.1.7 Power Supplies

The 96Boards specification calls for three power rails to be present on the low-speed expansion connector:

- +1.8 V: Max of 100mA
- +5 V: Able to provide a minimum of 5 W of power (1A).
- SYS_DCIN: 9-18 V input with enough current to support all the board functions or the output DCIN from onboard DC connector able to provide a minimum of 7 W of power.
- RB5 supports these requirements as follows:
- +1.8 V: Driven by PMIC PM8250 VREG_S4A_1P8, which can provide 100mA.
- +5 V: Driven by the 4A 5.0 V DC to DC converter. The buck can provide at least current of 2A to the low-speed expansion connector to meets the 96Boards requirements.
- DC12V: DC jack input can serve as the main power source.

4.2 Secondary Low Speed Connector: LS2

PIN	RB5 Signal	Additional Info
1	GPIO_U	CAM3_RST_N
3	DMIC_CLK1_LS2	
5	DMIC_DATA1_LS2	
7	GPIO_V	I2S1_DATA2/ext codec/CAM0_STROBE_N
9	DMIC_CLK2	
11	DMIC_DATA2	
13	GPIO_W	I2S1_DATA3/ext codec/CAM5_RST_N
15	DMIC_CLK3	
17	DMIC_DATA3	
19	PM_GPIO-F	PM8250_GPIO3
21	CCI_I2C_SCL2	
23	CCI_I2C_SDA2	
25	CCI_I2C_SCL3	
27	SPK0_P	
29	SPK0_M	
31	SPK1_P	
33	SPK1_M	
35	CCI_I2C_SDA3	
37	PM_GPIO-E	PM8250 AMUX1/MDM SKIN THERM

39	VBAT	
41	GND	
43	GPIO_X	CAM5_RST_N
45	GPIO_Y	CAM4_PWDN

PIN	RB5 Signal	Additional Info
2	GPIO_Z	CAM4_RST_N
4	CAN_H	
6	CAN_L	
8	VREG_IO_1P8	
10	GND	
12	PM_GPIO-A	PM8150L GPIO6
14	PM_GPIO-B	PM8150L GPIO10
16	GPIO-M/QUP-B0	QUP9
18	GPIO-N/QUP-B1	QUP9
20	GPIO-O/QUP-B2	QUP9/PWM
22	GPIO-P/QUP-B3	QUP9/BOOT_CONFIG 0
24	GPIO-Q	GPIO 147
26	GPIO-R	GPIO 148
28	GPIO-S	GPIO 148
30	GPIO-T	GPIO 149
33	PM_AMUX1	PM8150L
34	PM_AMUX2	PM8150L
36	BATT_THERM	
38	BATT_ID	
40	USB_VBUS	
42	GND	
44	GPIO-AA	CAM4_PWDN
46	GPIO-BB	CAM5_PWDN/BOOT_CONFIG 1

4.2.1 Audio

RB5 provide below interface for audio.

- One 4 data bit PCM/I2S with 6 wires: CLK, FS, D0~D3, are connected directly to the QRB5165 SoC. These signals are driven at 1.8 V
- 2 WSA8815 amplifiers are on-board and 2 pairs of speaker signals are routed to LS2.
- 1 digital mic on development board
- 3 pairs of DMIC signals are routed to LS

4.2.2 Stereo speaker

The speaker signals are routed from the 2 on board WSA8815. The signals are:

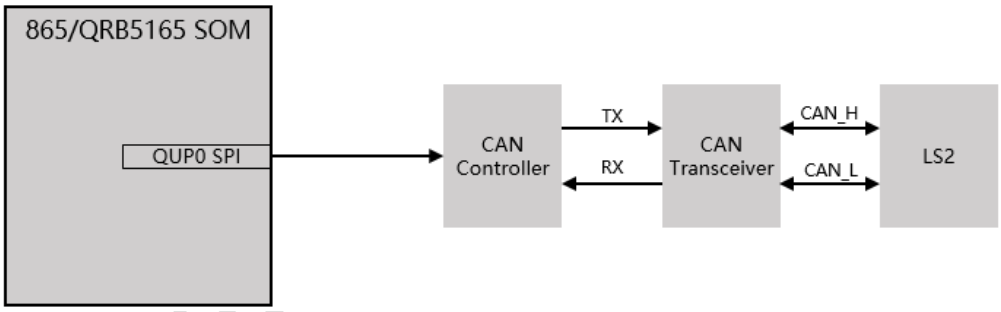
- SPK0_P - Class-D speaker amplifier output+
- SPK0_M - Class-D speaker amplifier output-
- SPK1_P - Class-D speaker amplifier output+
- SPK1_M - Class-D speaker amplifier output-

4.2.3 Digital Microphones

The expansion connector supports 3 additional default digital microphone inputs, support maximum 6 DMICs:

- DMIC_CLK1_LS2
- DMIC_DATA1_LS2
- DMIC_CLK1/DATA1_LS2 are multiplexing with on board MIC, see Section 3.18.3, switch1 of DIP switch#16
- DMIC_CLK2
- DMIC_DATA2
- DMIC_CLK3
- DMIC_DATA3

4.2.4 CAN



The CAN signals are rounded from CAN transceiver which is from SPI translation. The signals are:

- CAN_H: CAN High-Level Voltage I/O
- CAN_L: CAN Low-Level Voltage I/O

4.2.5 I2C

Two dedicated CCI (Camera Control Interface) I2C signal pairs are routed from QRB5165 SoC. 2.2k resistors are used in SOM to pull signals up for each of the I2C lines per the I2C specifications. The signals are:

- CCI_I2C_SDA2: Connects to CCI2 of QRB5165 SoC, Be configured to I2C SDA.
- CCI_I2C_SCL2: Connects to CCI2 of QRB5165 SoC. Be configured to I2C SCL
- CCI_I2C_SDA3: Connects to CCI3 of QRB5165 SoC, Be configured to I2C SDA.

- CCI_I2C_SCL3: Connects to CCI3 of QRB5165 SoC. Be configured to I2C SCL

4.2.6 GPIOs

RB5 implements more GPIOs for low-speed expansion connector. The GPIOs are 1.8V voltage rail.

- GPIO-M/QUP-B0: Connects to GPIO_125 of QRB5165.
- GPIO-N/QUP-B1: Connects to GPIO_126 of QRB5165.
- GPIO-O/QUP-B2: Connects to GPIO_127 of QRB5165.
- GPIO-P/QUP-B3: Connects to GPIO_128 of QRB5165.
- GPIO-Q/I2S1_WS_LS2: Connects to GPIO_147 of QRB5165. Can be configured as I2S WS
- GPIO-R/I2S1_CLK_LS2: Connects to GPIO_146 of QRB5165. Can be configured as I2S CLK
- GPIO-S/I2S1_DATA0_LS2: Connects to GPIO_148 of QRB5165. Can be configured as I2S DATA
- GPIO-T/I2S1_DATA1_LS2: Connects to GPIO_149 of QRB5165. Can be configured as I2S DATA
- GPIO-U: Connects to GPIO_144 of QRB5165.
- GPIO-V/I2S1_DATA2_LS2: Connects to GPIO_150 of QRB5165. Can be configured as I2S DATA.
- GPIO-W/I2S1_DATA3_LS2: Connects to GPIO_144 of QRB5165. Can be configured as I2S DATA.
- GPIO-X: Connects to GPIO_14 of QRB5165.
- GPIO-Y: Connects to GPIO_145 of QRB5165.
- GPIO-Z: Connects to GPIO_25 of QRB5165
- GPIO-AA: Connects to GPIO_64 of QRB5165.
- GPIO-BB: Connects to GPIO_27 of QRB5165.
- PM GPIO A: Connects to GPIO_6 of PM8150L. Can be configured as PWM signal.
- PM GPIO B: Connects to GPIO_10 of PM8150L. Can be configured as PWM signal.
- PM_AMUX1: Connects to AMUX1 of PM8150L.
- PM_AMUX2: Connects to AMUX1 of PM8150L.

4.2.7 Other signals on Secondary Low Speed Connector

The RB5 board implements more source voltage at the Lowe Speed Expansion Connector. The signals are:

- USB_VBUS: Connects to VBUS of PM8250 PMIC, Can be configured as an OTG USB

VBUS.

- VBAT: Connects to a DC-DC buck of board power, be configured as output 4.2V source.

4.3 Tertiary Low Speed Connector: LS3

PIN	RB5 Signal	Additional Info
1	GPIO-KK	CAM2_STROBE
3	SLEEP_CLK	
5	GPIO-LL	CAM3_STROBE
7	GPIO-MM	QUP19
9	GPIO-NN	QUP19
11	GPIO-OO	QUP19
13	QCA_GPIO-A	QUP7
15	QCA_GPIO-B	QUP7
17	QCA_GPIO-C	
19	GPIO-PP	QUP19
21	GPIO-QQ	QUP18
23	SPI2_CLK_LS3	SSC QUP2
25	SPI2_MOSI_LS3	SSC QUP2
27	SPI2_MISO_LS3	SSC QUP2
29	SPI2_ACCEL_CS_LS3	SSC QUP2
31	SPI2_CS1	SSC QUP2
33	SPI3_CS1	SSC QUP5
35	VREG_L8C_1P8	
37	VDC_5V	A board DC buck power 5V
39	VBAT	A board DC buck power 4.2V
41	GND	
43	GPIO-RR	QUP18
45	GPIO-SS	SSC QUP4/I2C SDA

PIN	RB5 Signal	Note
2	GPIO-TT	CAM4_STROBE
4	PMK8002_PMIC_CLK	
6	GPIO-UU	CAM5_STROBE/WCD_RESET
8	QCA_GPIO-D	DISP_RST_N
10	QCA_GPIO-E	
12	GPIO-VV	
14	GPIO-WW	
16	SPI3_MISO	SSC QUP5
18	SPI3_MOSI	SSC QUP5
20	SPI3_CLK	SSC QUP5

22	SPI3_CS	SSC QUP5
24	PS_INT	
26	ACCEL_INT	
28	GYRO_INT	
30	MAG_INT	
32	MAG_DRDY_INT	
34	I2C4_SDA	SSC QUP0
36	I2C4_SCL	SSC QUP0
38	VREG_L5C_1P8	
40	GND	
42	GND	
44	SPI3_CS2	SSC QUP5
46	GPIO-XX	SSC QUP4

4.3.1 SSC SPI

RB5 implements 2 SSC SPI interfaces for different sensors that connect to QRB5165 processor sensor core. Each SPIs can support 2 CS signals.

The signals are:

- SPI2_CLK_LS3: Connects to SSC QUP2 of QRB5165 SoC, to be configured to CLK.
- SPI2_MOSI_LS3: Connects to SSC QUP2 of QRB5165 SoC, to be configured to MOSI.
- SPI2_MISO_LS3: Connects to SSC QUP2 of QRB5165 SoC, to be configured to MISO.
- SPI2_ACCEL_CS_LS3: Connects to SSC QUP2 of QRB5165 SoC, to be configured to CS.
- SPI2_CS1: Connects to SSC QUP2 of QRB5165 SoC, to be configured to gyroscope CS.
- SPI3_CLK: Connects to SSC QUP5 of QRB5165 SoC, to be configured to CLK.
- SPI3_MOSI: Connects to SSC QUP5 of QRB5165 SoC, to be configured to MOSI.
- SPI3_MISO: Connects to SSC QUP5 of QRB5165 SoC, to be configured to MISO.
- SPI3_CS: Connects to SSC QUP5 of QRB5165 SoC, to be configured to CS.
- SPI3_CS1: Connects to SSC QUP5 of QRB5165 SoC, to be configured to gyroscope CS.

The DIP switch (see Section 1.2.2, #16) pin5 is used to select between the onboard 6-axis sensor ICM-42688 and expansion connector. When set to ON, will enable SPI to LS3; when set to OFF, will enable SPI to on board sensor ICM_42688.

4.3.2 SSC I2C

The RB5 implements a SSC I2C interface for different sensors that connect to QRB5165 sensor core. 2.2k resistors are used in SOM to pull signals up for each of the I2C lines per the I2C specifications. The signals are:

- I2C4_SDA: Connects to SSC QUP0 of QRB5165 SoC, Be configured to I2C SDA.
- I2C4_SCL: Connects to SSC QUP0 of QRB5165 SoC. Be configured to I2C SCL

4.3.3 Sensor interrupt

The RB5 implements a SSC interrupt for sensor interrupts that is the 1.8V voltage rail. The signals are:

- ACCEL_INT: Connects to GPIO_112 of QRB5165 SoC, Be configured to Accelerometer INT.
- GYRO_INT: Connects to GPIO_113 of QRB5165 SoC, Be configured to Gyroscope INT.
- MAG_DRDY_INT: Connects to GPIO_123 of QRB5165 SoC, Be configured to Magnetometer data INT.
- MAG_INT: Connects to GPIO_122 of QRB5165 SoC, Be configured to Magnetometer INT.
- PS_INT: Connects to GPIO_129 of QRB5165 SoC, Be configured to Proximity INT.

4.3.4 Other signals on Tertiary Low Speed Connector

The RB5 board implements more source voltage at the Lowe Speed Expansion Connector. The signals are:

- VREG_L5C_1P8: Connects to L5 LDO of PM8250 PMIC, Can be as sensor IO voltage source.
- VREG_L8C_1P8: Connects to L8 LDO of PM8250 PMIC, Can be as sensor IO voltage source.
- VDC_5V: Connects to a board DC buck power 5V, Can be as a 5V voltage source.
- VBAT: Connects to a board DC buck power 4.2V, Can be as a 4.2V voltage source.

5 High speed expansion connectors

5.1 Primary high speed expansion connector: HS1

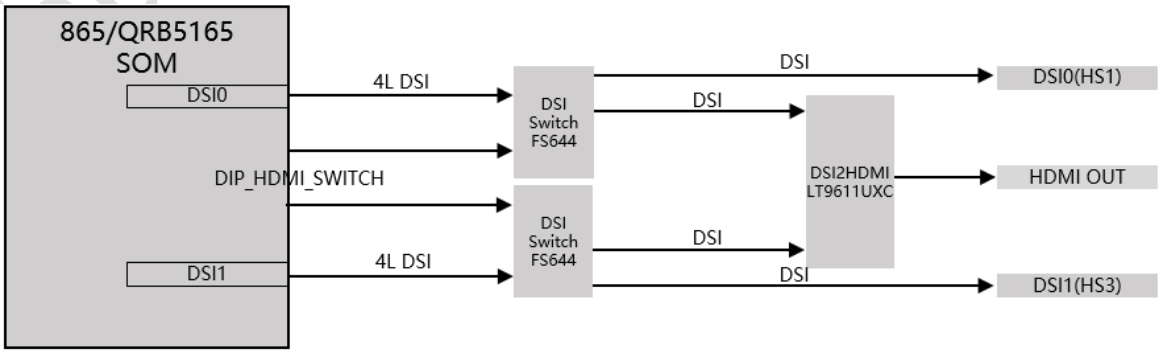
The following table shows the High Speed Expansion Connector pin out:

PIN	96Boards Signals	Note
1	SD_DAT0	SDC4_DATA0
3	SD_DAT1	SDC4_DATA1
5	SD_DAT2	SDC4_DATA2
7	SD_DAT3	SDC4_DATA4
9	SD_SCLK	SDC4_SCLK
11	SD_CMD	SDC4_CMD
13	GND	
15	CLK0/CSI0_MCLK	
17	CLK3/CSI3_MCLK	
19	GND	
21	DSI0_CLK_P_HS1	
23	DSI0_CLK_M_HS1	
25	GND	
27	DSI0_D0_P_HS1	
29	DSI0_D0_M_HS1	
31	GND	
33	DSI0_D1_P_HS1	
35	DSI0_D1_M_HS1	
37	GND	
39	DSI0_D2_P_HS1	
41	DSI0_D2_M_HS1	
43	GND	
45	DSI0_D3_P_HS1	
47	DSI0_D3_M_HS1	
49	GND	
51	USB1_HS_DP_HS1	
53	USB1_HS_DM_HS1	
55	GND	
57	NC	
59	NC	

PIN	RB5 Signals	Note
2	CSI0_C_P	

4	CSI0_C_M	
6	GND	
8	CSI0_D0_P	
10	CSI0_D0_M	
12	GND	
14	CSI0_D1_P	
16	CSI0_D1_M	
18	GND	
20	CSI0_D2_P	
22	CSI0_D2_M	
24	GND	
26	CSI0_D3_P	
28	CSI0_D3_M	
30	GND	
32	CCI_I2C_SCL0	
34	CCI_I2C_SDA0	
36	CCI_I2C_SCL1	
38	CCI_I2C_SDA1	
40	GND	
42	CSI3_D0_P	
44	CSI3_D0_M	
46	GND	
48	CSI3_D1_P	
50	CSI3_D1_M	
52	GND	
54	CSI3_C_P	
56	CSI3_C_M	
58	GND	
60	RESERVED	Can be pull-up to 1.8V by adding a serial resistor.

5.1.1 MIPI DSI



The 96Boards specification calls for a MIPI-DSI to be present on the high-speed expansion connector. A minimum of one lane is required and up to four lanes can be accommodated on the connector.

RB5 implementation supports a full 4-lane MIPI-DSI interface that is routed to HS1. A DSI switch, FS644, is used to support on board DSI-to-HDMI bridging. DSI switch is controlled via DIP switch #16, pin4, DIP_HDMI_SWITCH. When set to ON, it will enable DSI0 to HS1 and DSI1 to HS3; when set to OFF, will enable DSI1&2 to LT9611UXC and on board HDMI.

5.1.2 MIPI CSI

The 96Boards specification calls for two MIPI-CSI interfaces to be present on the high-speed expansion connector. Both interfaces are optional. CSI0 interface can be up to four lanes while CSI1 is up to two lanes.

The current Robotics RB5 Development Kit implementation supports a full 4-lane MIPI-CSI interface on CSI0 and two lanes of MIPI-CSI on CSI3. All MIPI-CSI signals are routed directly to and from the QRB5165 processor.

5.1.3 I2C

The 96Boards specification calls for two I2C interfaces to be present on the high-speed expansion connector. Both interfaces are optional unless a MIPI-CSI interface has been implemented. In this case, an I2C interface shall be implemented.

Robotics RB5 Development Kit have two CCI I2C interface, I2C0&I2C1, in HS1.

NOTE: Both interfaces, I2C0 and I2C1 are pull-up to 1.8V via 2.2K resistor in 865SOM.

5.1.4 HSIC

The 96Boards specification calls for an optional MIPI-HSIC interface to be present on the High Speed Expansion Connector.

The RB5 board implementation doesn't support this optional requirement.

5.1.5 Reserved

The 96Boards specification calls for a 10K pull-up to 1.8V to be connected to pin 60 of the High Speed Expansion Connector.

In RB5, a NC resistor is used in HS1 to connect pin60 of HS1 to 1.8V.

5.1.6 SD/SPI

The 96Boards specification calls for an SD interface or a SPI port to be part of the High

Speed Expansion Connector.

The RB5 provides a full SD master with SDIO (CLK/CMD/D0~D3) from QRB5165 SoC. All signals are driven at 1.8V and 1.8V only.

5.1.7 Camera Clocks

The 96Boards specification calls for one or two programmable clock interfaces to be provided on the High Speed Expansion Connector. These clocks may have a secondary function of being CSI0_MCLK and CSI1_MCLK. If these clocks can't be supported by the SoC than an alternative GPIO or No-Connect is allowed by the specifications.

HS1 in RB5 implements two CSI clocks, CLK0/CSI0_MCLK, GPIO_94 for CSI0 and CLK3/CSI3_MCLK, GPIO_97 for CSI3. These signals are driven at 1.8V.

5.1.8 USB

The 96Boards specification calls for a USB data line interface to be present on the high-speed expansion connector.

RB5 implements this requirement. In HS1, USB HS DP/DM signals are routing from a USB HUB.

5.2 Secondary High Speed Connector: HS2

PIN	RB5 Signals	Note
1	PCIE_REFCLK_M	
3	PCIE_REFCLK_P	
4	PCIE_RX_M	
7	PCIE_RX_P	
9	PCIE_TX_M	
11	PCIE_TX_P	
13	GPIO-CC	PCIE1_RST_N
15	GPIO-DD	PCIE1_CLK_REQ_N
17	GPIO-EE	PCIE1_WAKE_N
19	GPIO-FF	PCIE2_RST_N
21	GPIO-GG	PCIE2_CLK_REQ_N
23	GPIO-HH	PCIE2_WAKE_N
25	GND	
27	CLK1/CSI1_MCLK	
29	CLK2/CSI2_MCLK	
31	GND	
33	CSI2_C_P	
35	CSI2_C_M	
37	GND	

39	CSI2_D0_P	
41	CSI2_D0_M	
43	GND	
45	CSI2_D1_P	
47	CSI2_D1_M	
49	GND	
51	CSI2_D2_P	
53	CSI2_D2_M	
55	GND	
57	CSI2_D3_P	
59	CSI2_D3_M	

PIN	RB5 Signals	Note
2	CSI1_C_P	
4	CSI1_C_M	
6	GND	
8	CSI1_D0_P	
10	CSI1_D0_M	
12	GND	
14	CSI1_D1_P	
16	CSI1_D1_M	
18	GND	
20	CSI1_D2_P	
22	CSI1_D2_M	
24	GND	
26	CSI1_D3_P	
28	CSI1_D3_M	
30	GND	
32	SPI1_CLK	QUP14
34	SPI1_CS	QUP14
36	SPI1_MOSI	QUP14
38	SPI1_MISO	QUP14
40	CLK4/CSI4_MCLK	
42	CLK5/CSI5_MCLK	
44	GPIO-II	CAM2_RST_N
46	GPIO-JJ	CAM2_PWDN
48	PMIC_SPMI_CLK	
50	PMIC_SPMI_DATA	
52	GND	
54	USB1_SS_TX_P_HS2	
56	USB1_SS_TX_M_HS2	
58	USB1_SS_RX_P_HS2	

60	USB1_SS_RX_M_HS2	

5.2.1 MIPI CSI

The Secondary High Speed Expansion Connector supports 2 4-lane MIPI-CSI bus (MIPI-CSI1/MIPI-CSI2). All MIPI-CSI signals are routed directly to/from the QRB5165.

5.2.2 Clock

The RB5 implements another 4 CSI clocks on the Secondary High Speed Expansion Connector, CLK1/CSI1_MCLK, GPIO_95 for CSI1; CLK2/CSI2_MCLK, GPIO_96 for CSI2; CLK4/CSI4_MCLK, GPIO98 for CSI4 and CLK5/CSI5_MCLK, GPIO99 for CSI5. These signals are driven at 1.8V.

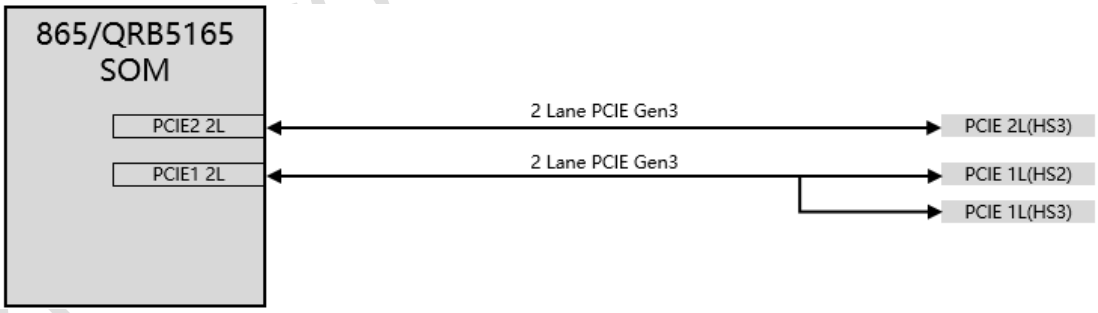
5.2.3 SPI

The RB5 implements another SPI interface on the Secondary High Speed Expansion Connector that connect to QRB5165 QUP14. These signals are driven at 1.8V.

- SPI1_CLK : Connects to QUP 14 of QRB5165 SoC, Be configured as CLK
- SPI1_CS : Connects to QUP 14 of QRB5165 SoC. Be configured to CS.
- SPI1_MOSI : Connects to QUP 14 of QRB5165 SoC. Be configured to MOSI.
- SPI1_MISO : Connects to QUP 14 of QRB5165 SoC. Be configured to MISO.

5.2.4 PCIe1

The RB5 has 2 2-lane PCIe interfaces. PCIe1 1-lane is available on the Secondary High Speed Expansion Connector.



5.2.5 USB

The RB5 implements one USB Supper speed interface on the Secondary High Speed Expansion Connector.

The Supper Speed USB of HS2 and High Speed USB of HS1 can be combined to one USB3.0 port.

5.2.6 Other signals on Secondary High Speed Connector

The Robotics RB5 Development Kit implements more GPIOs on the secondary high-speed expansion connector. The GPIOs are 1.8 V voltage rail.

- GPIO-CC: Connects to GPIO_82 of QRB5165 SoC. Can be configured as PCIE1 Reset.
- GPIO-DD: Connects to GPIO_83 of QRB5165 SoC. Can be configured as PCIE1 Clock Request.
- GPIO-EE: Connects to GPIO_84 of QRB5165 SoC. Can be configured as PCIE1 Wake.
- GPIO-FF: Connects to GPIO_85 of QRB5165 SoC. Can be configured as PCIE2 Reset.
- GPIO-GG: Connects to GPIO_86 of QRB5165 SoC. Can be configured as PCIE2 Clock Request.
- GPIO-HH: Connects to GPIO_87 of QRB5165 SoC. Can be configured as PCIEI2 Wake.
- GPIO-II: Connects to GPIO_78 of QRB5165 SoC. Can be configured as Camera2 Reset.
- GPIO-JJ: Connects to GPIO_47 of QRB5165 SoC. Can be configured as Camera2 power down, QUP 14 CS or BOOT CONFIG 2.
- PMIC_SPMI_CLK: Can be connected to SDX55 module.
- PMIC_SPMI_DATA: Can be connected to SDX55 module.

5.3 Tertiary High Speed Connector: HS3

PIN	RB5 Signals	Note
1	CSI4_C_P	
3	CSI4_C_M	
5	CSI4_D0_P	
7	CSI4_D0_M	
9	GND	
11	CSI4_D1_P	
13	CSI4_D1_M	
15	CSI4_D2_P	
17	CSI4_D2_M	
19	CSI4_D3_P	
21	CSI4_D3_M	
23	GND	
25	CSI3_D2_P	
27	CSI3_D2_M	
29	CSI3_D3_P	
31	CSI3_D3_M	
33	GND	
35	CSI5_C_P	
37	CSI5_C_M	

39	CSI5_D0_P	
41	CSI5_D0_M	
43	CSI5_D1_P	
45	CSI5_D1_M	
47	CSI5_D2_P	
49	CSI5_D2_M	
51	CSI5_D3_P	
53	CSI5_D3_M	
55	GND	
57	PMK8002_RF_CLK1	
59	PMK8002_RF_CLK2	

PIN	RB5 Signals	Note
2	GND	
4	PCIE1_RX1_M	
6	PCIE1_RX1_P	
8	PCIE1_TX1_M	
10	PCIE1_TX1_P	
12	GND	
14	PCIE2_REFCLK_M	
16	PCIE2_REFCLK_P	
18	PCIE2_RX0_M	
20	PCIE2_RX0_P	
22	PCIE2_RX1_M	
24	PCIE2_RX1_P	
26	PCIE2_TX0_M	
28	PCIE2_TX0_P	
30	PCIE2_TX1_M	
32	PCIE2_TX1_P	
34	GND	
36	DSI1_CLK_P	
38	DSI1_CLK_M	
40	DSI1_D0_P	
42	DSI1_D0_M	
44	DSI1_D1_P	
46	DSI1_D1_M	
48	GND	
50	DSI1_D2_P	
52	DSI1_D2_M	
54	DSI1_D3_P	
56	DSI1_D3_M	
58	GND	

60	GPIO_DDD(GPIO_26)	

5.3.1 MIPI CSI

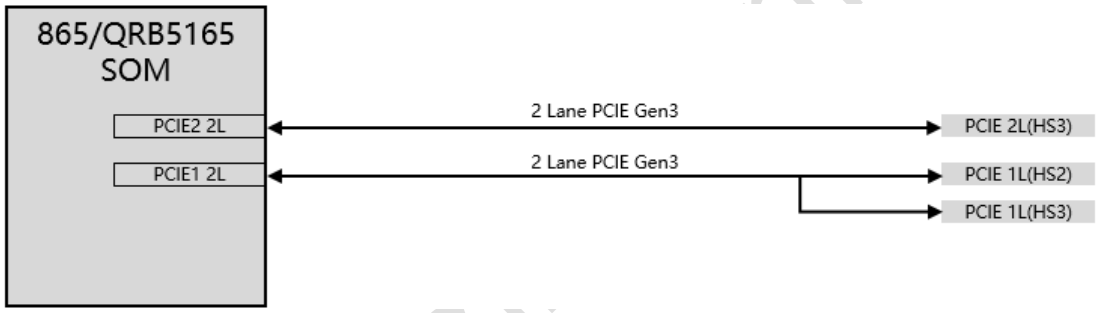
The Tertiary High Speed Expansion Connector supports 2 4-lane MIPI-CSI bus (MIPI-CSI4/MIPI-CSI5) and 2 data lane on MIPI-CSI3. All MIPI-CSI signals are routed directly to/from the QRB5165.

5.3.2 Clock

The RB5 implements another 2 RF clocks on the Tertiary High Speed Expansion Connector, PM8002_RF_CLK1 and PM8002_RF_CLK2.

5.3.3 PCIe1&2

The RB5 has 2 2-lane PCIe interfaces. Another PCIe1 1-lane and PCIe2 2-lane are available on the Tertiary High Speed Expansion Connector.



5.3.4 MIPI-DSI1

RB5 implementation supports another full 4-lane MIPI-DSI interface that is routed to HS3. See more detail on 5.1.1.

5.3.5 Other signals on Tertiary High Speed Connector

GPIO_26 is available in Tertiary High Speed Connector.

6 Power management

The 96Boards specification defines how power arrives to the board and the supplies that the board needs to provide. The onboard power requirement for each 96Boards implementation depends on the SoC and the set of peripherals that are specific to that implementation.

RB5 uses five buck regulators: U0700, U0701, U0800, U0801 as the main power suppliers for RB5, provide 4.2V for 865 SOM, 4.2V, 5V and 3.3V for peripherals in RB5.

- U0700 and U0701 generate 4.2 V at 4A. U0700 feeds the 4.2V power for peripherals in RB5. U0701 feeds the 865 SOM power.
- U0800 generates 3.3 V at 4A.
- U0801 generates 5 V at 4A.

6.1 DC Power Input

The 96Boards specification calls for power to be provided to the board in one of the following ways:

- 8 V to 18 V power from a dedicated DC jack
  □RB5 supports this requirement through the use of #15 (see Section 1.2.1).
- 8 V to 18 V power from the DC12V pins on the low-speed expansion connector
- llA USB Type C port at 5 V
  □The Robotics RB5 Development Kit supports the 5 V from USB Type C port. It cannot support system bring up power on.

6.2 Power Source Selection

The 96Boards specification calls for only one power source to be applied to the board at any given time.

Following this requirement, RB5 user should never apply power to the board from #15 (see Section 1.2.1) and the low-speed expansion connector at the same time.

There is no active or passive mechanism on RB5 to prioritize one source over the other.

6.3 Power Sequencing

Upon applying power to the DC12V of Robotics RB5 Development Kit (from either one of the two sources), some power will be automatically enable, some will waiting S/W to enable.

- 4.2V for 865 SOM: will enable after DC12V is asserted. 865 SOM will power on once

power-on button is pressed.

- 4.2V for IO peripheral: will not enable, S/W can enable it after 865 SOM is powered on.
- 3.3V/5V for IO peripheral: same as 4.2V for IO peripheral. These 3 power rails are controlled via one same signal.

6.4 Power Measurements

The 96Boards specification calls for a minimum of one current sense resistor to be placed on the board permitting basic power measurement functions.
RB5 implements two different power measurements.

6.4.1 DC-In measurement

A 0.01ohm resistor R0700 is placed in line of the DC12V on the DC input. Placing a probe over the resistor pins will provide a voltage measurement of the voltage drop across the resistor. Dividing this measurement by 0.01 will give you the amount of the current flowing into the DC.

6.4.2 PMIC Power-In measurement (VPH_PWR measurement)

A 0.01ohm resistors are used on output path of these two 4.2V, 3.3V and 5V for current measurement, i.e. R0709 for 4.2V of SOM, R0703 for 4.2 V of IO, R0801 for 3.3V of IO and R0805 for 5V of IO.
Placing a probe over the resistor pins will provide a voltage measurement of the voltage drop across the resistor. Dividing this measurement by 0.01 will give you the amount of the current.

7 Buttons and status LED’s

7.1 Buttons

7.1.1 Volume up

The Volume up button (see Section 1.2.2, #18) is used to control the audio volume of RB5.

7.1.2 Volume down

The Volume down button (see Section 1.2.2, #19) is used to control the audio volume of the Robotics RB5 Development Kit.

7.1.3 Power Button

The push-button (see Section 1.2.2, #20) serves as the power ON/OFF/Sleep button.
Sleep/Suspend

- Set the device to sleep by pressing this button momentarily.
- Wake the device from sleep by pressing this button momentarily.
- Power ON/OFF
- Option 1: Long press/hold
  - While the device is awake, press and hold the Power button #20 (see Section 1.2.2) for longer than 15 seconds to Power OFF the device.
  - Once OFF, press and hold the Power button #20 (see Section 1.2.2) for longer than 3 seconds to Power ON the device.
- Option 2: Short press/hold
  - While the device is awake, press and hold the Power button #20 (see Section 1.2.2) for 2~3 seconds to display the Power OFF notice. Using a mouse, click the notice to Power OFF the device.
  - Once OFF, press and hold the Power button #20 (see Section 1.2.2) for longer than 3 seconds to Power ON the device.

7.1.4 Reset Button

The onboard (see Section 1.2.2, #19) push-button has two functions, it serves as a reset button and as a Volume button.
The reset function needs to be a software-configured setting.

7.1.5 Force_USB_BOOT button

The onboard (see Section 1.2.2, #22) push-button is used for emergency USB boot for during development.

7.2 LED's

There are one power indication LED, two status LEDs and four user LEDs on RB5.
The status LEDs report the status of the Bluetooth and Wi-Fi devices onboard.
The user LEDs are driven directly by the SoC.

7.2.1 User LED 1-4

The four user LEDs are surface mount green LEDs, 0603 size, located between two USB Type A connectors and labeled USER LEDS 3 2 1 0.

7.2.2 Wi-Fi status

Wi-Fi LED is located next to the USB OTG connector. The Wi-Fi LED reflects the status of the Wi-Fi device.

7.2.3 Bluetooth status

BT LED is located next to the WI-FI LED. The BT LED reflects the status of the Bluetooth device.

7.2.4 Power Indicator LED

Power indicator is located beside the DC jack. The power indicator LED notifies the user that the power is applied.

8 Boot configurations

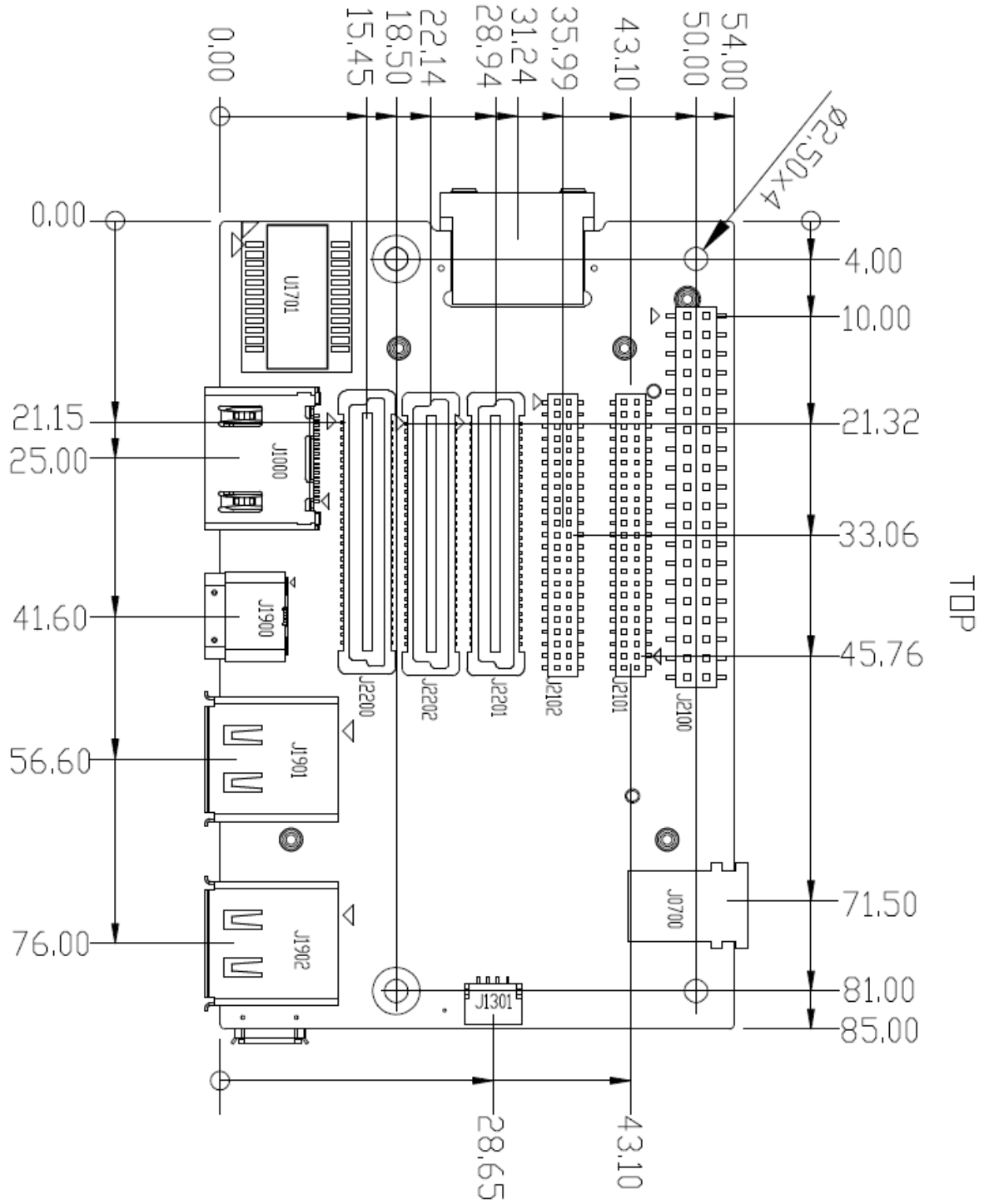
A DIP switch is located on the top of the development board (see Section 1.2.2, #17):

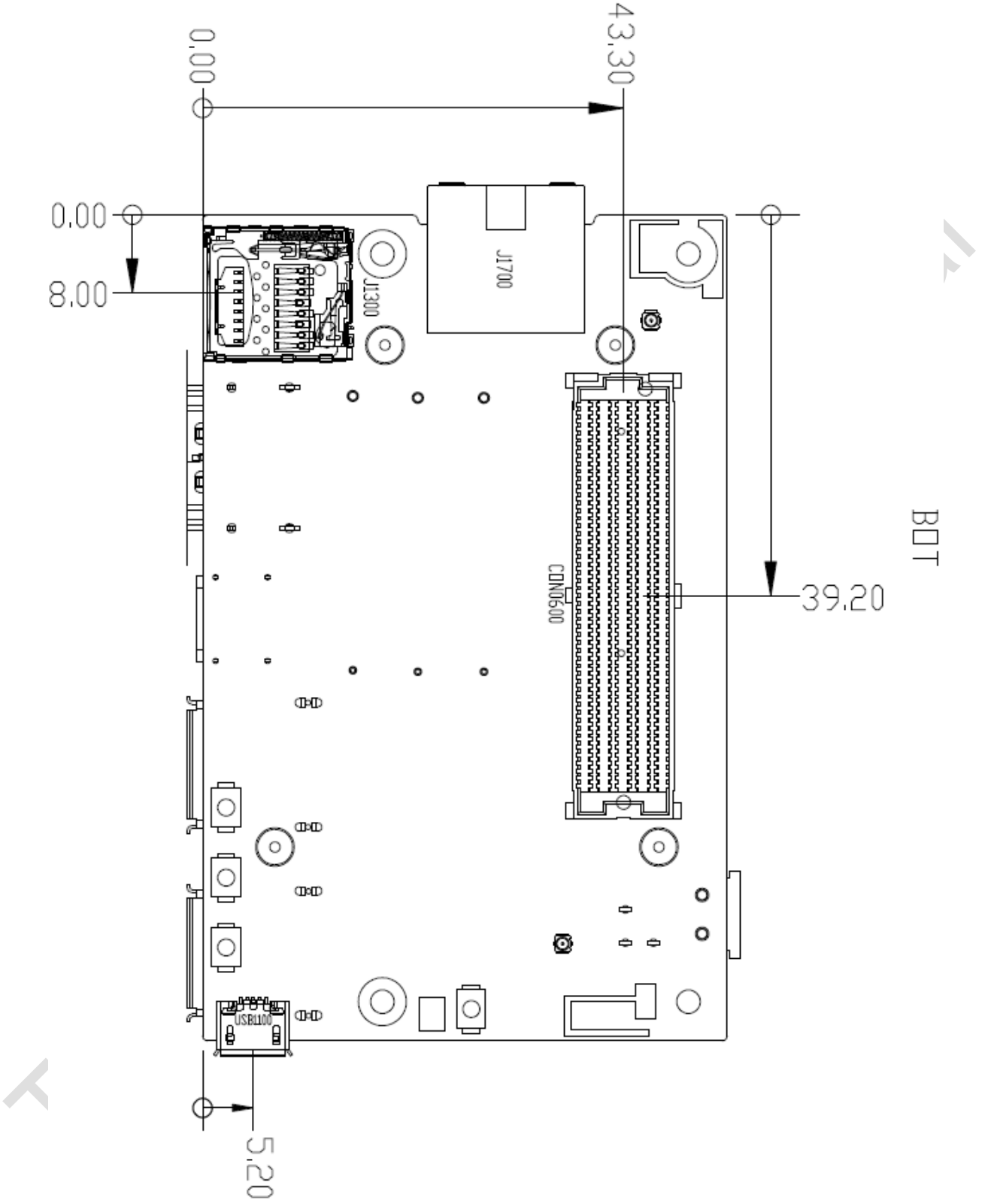
DIP_SW_1	Name	Details	Default
1	BOOT_CONFIG_1 [GPIO_27]	Selects external boot devices	OFF
2	BOOT_CONFIG_2 [GPIO_47]		OFF
3	BOOT_CONFIG_3 [GPIO_76]		OFF
4	BOOT_CONFIG_0 [GPIO_128]	ON – Disables WDOG OFF – Enables WDOG	OFF

GPIO details:

GPIO				Boot device
FAST_BOOT GPIO bit (3:0)	76	47	27	Default: UFS0 → SDC2 → USB0 → EDL(USB0)
0000	0	0	0	
Other	Reserved			

9 Mechanical specification





Connector Part Number

Connector	MPN	MPN of Mate

High Speed Conn. 1&2&3	FCI: 61082-061409LF	FCI: 61083-064402LF
Low Speed Conn.1(LS1)	Molex: 87381-4063	FCI: 57202-G52-20LF
Low Speed Conn.2&3(LS2&3)	Samtec: CLP-123-02-L-D-P-K-TR	Samtec: FTSH-123-05-L-DV-A-P-TR

10 Appendix

10.1 Navigation Mezzanine

The RB5 Navigation Mezzanine development board can be used to connect different cameras directly by MIPI CSI interface from QRB5165: 5 generic CSI camera ports with identical pinouts (to allow for 7 camera concurrency testing in next phase and support for open community camera development with CSI0 splitting into CAM0A and CAM0B), 2 GMSL camera inputs, 4 on-board DMIC and 3 sensors. It is ideal for developers to enable rapid development of embedded vision applications.

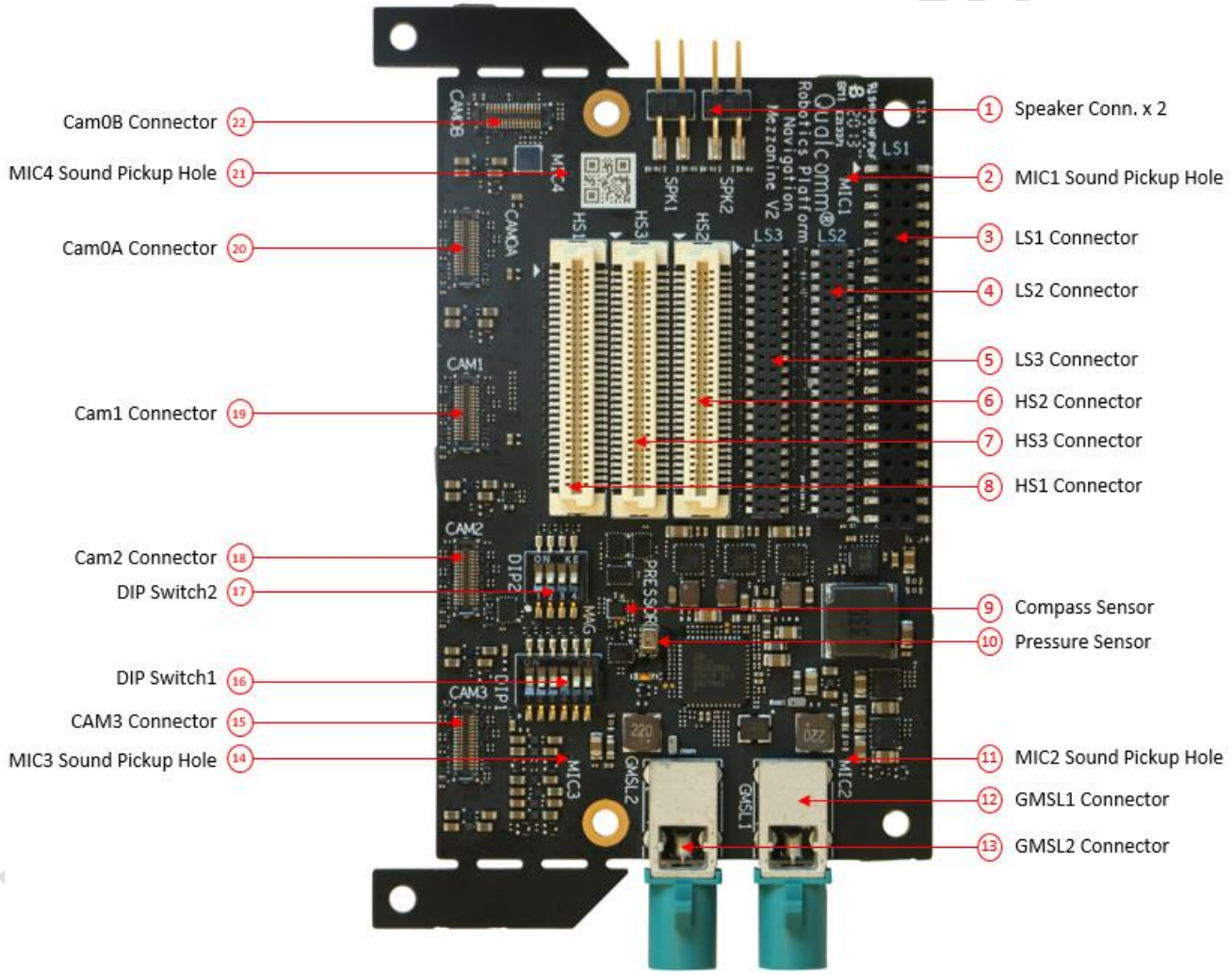
10.1.1 Technical specifications

Component	Description
Expansion interface	■ HS1:1 x 60 pin high-speed connector (SDC I/F, 1 x 4L MIPI DSI, USB 2.0, CCI I2C x2, 2L+4L-MIPI CSI) ■ HS2:1 x 60 pin high-speed connector (4L-MIPI CSI x 2, SPI x 1, PCIe 3.0 gen3 1L, USB 3.0 x1, GPIO x 8) ■ HS3:1 x 60 pin high-speed connector (4L-MIPI CSI x 2, 4L-MIPI CSI x1(plus 2L CSI in HS1), RF CLK x 2, 2L-PCIe 3.0 x 1, 2L-PCIe 3.0 x 1 (plus PCIe 1L in HS2), 4L-MIPI DSI x 1) ■ LS1:1 x 96boards 40 pin low-speed connector (UART x 2, SPI, I2S/PCM, I2C x 2, GPIO x 12, DC powers) ■ LS2:1 x 96boards 40 pin low-speed connector (Speaker x 2, DMIC I/F x 3, CAN, I2S, GPIOs, PWM, ADC, I2C, DC powers) ■ LS3:1 x 96boards 40 pin Low-Speed connector (SPI x 2, SSC I2C, sensor interrupt x 5, GPIOs, RTC clock, DC powers)
Other Interfaces	Cameras Dual GMSL camera inputs Tracking cameras: OV9282 modules, CAM0A/CAM0B/CAM1 Main Cameras: IMX577, CAM2, includes a SPI interface for future plug in module with a IMU + camera

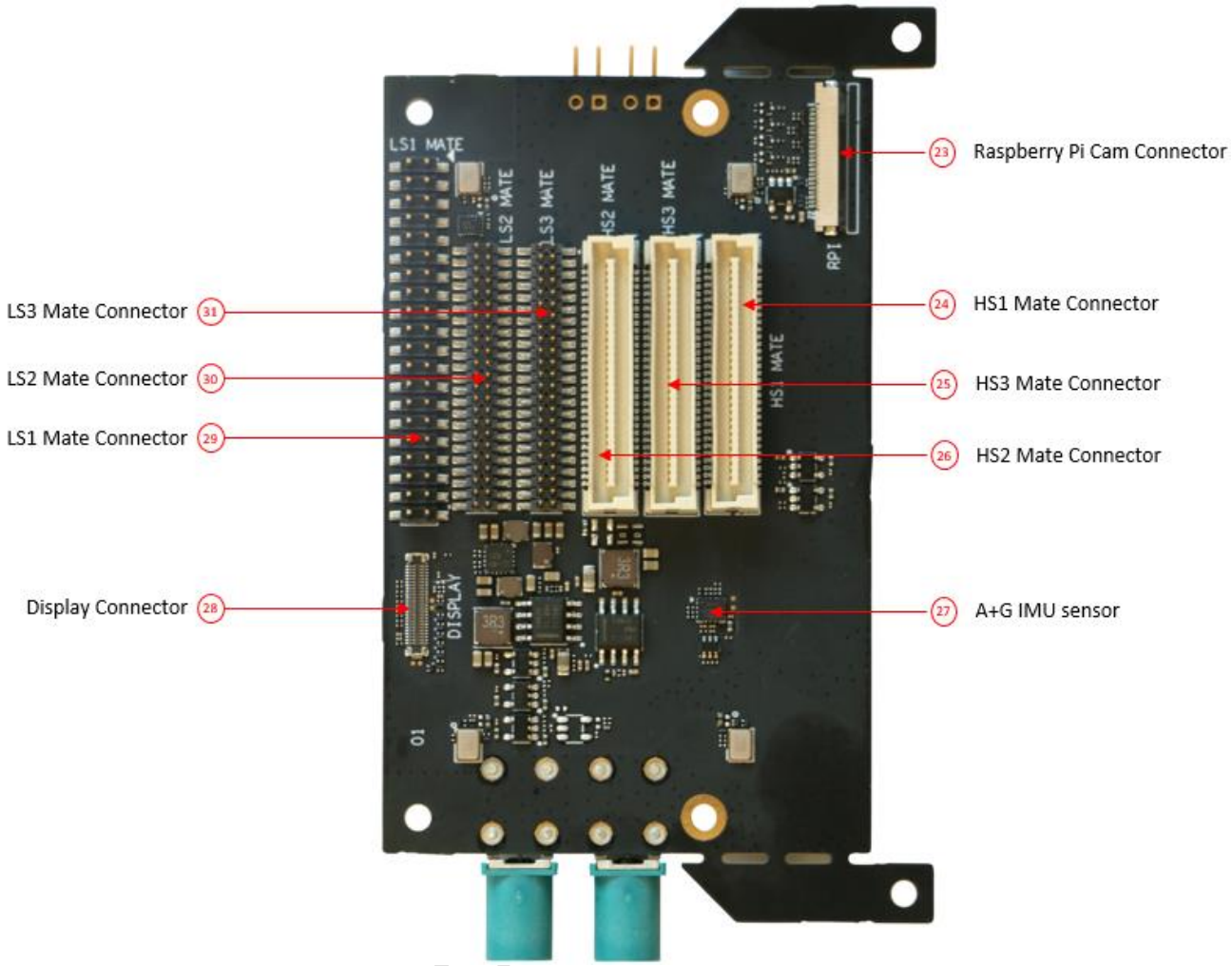
	TOF camera: higher supply voltage is added to support Panasonic TOF camera module with a switch board Raspberry Pi Camera: duplicated with CAM0B
Sensors	TDK ICM-42688-P with footprint compatible for Bosch BMI160 AKM compass AK09918C TDK Pressure sensor (ICP-10111)
Audio	4 digital PDM mics that interface directly to QRB5165 chipset Speaker connectors

10.1.2 Board views

Top view



Bottom view



10.2 Machine Communication Mezzanine

Machine Communication Mezzanine is designed to connect the cellular networks, adopts 5G M.2 key B modules which offers 5G (sub6 or mmWave) coverage.

10.2.1 Technical specifications

Component	Description
■ Expansion interface	■ HS1:1 x 60 pin high-speed connector (SDC I/F, 1 x 4L MIPI DSI, USB 2.0, CCI I2C x2, 2L+4L-MIPI CSI)

	■ HS2:1 x 60 pin high-speed connector (4L-MIPI CSI x 2, SPI x 1, PCIe 3.0 gen3 1L, USB 3.0 x1, GPIO x 8) ■ HS3:1 x 60 pin high-speed connector (4L-MIPI CSI x 2, 4L-MIPI CSI x1(plus 2L CSI in HS1), RF CLK x 2, 2L-PCIe 3.0 x 1, 2L-PCIe 3.0 x 1 (plus PCIe 1L in HS2), 4L-MIPI DSI x 1) ■ LS1:1 x 96boards 40 pin low-speed connector (UART x 2, SPI, I2S/PCM, I2C x 2, GPIO x 12, DC powers) ■ LS2:1 x 96boards 40 pin low-speed connector (Speaker x 2, DMIC I/F x 3, CAN, I2S, GPIOs, PWM, ADC, I2C, DC powers) ■ LS3:1 x 96boards 40 pin Low-Speed connector (SPI x 2, SSC I2C, sensor interrupt x 5, GPIOs, RTC clock, DC powers)
Other Interfaces	■ 2 x SIM holders ■ 1 x M.2 key B connector ■ 8 x RF Connectors ■ 4 B2B connectors
Cellular Components	

FCC Caution:

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IMPORTANT NOTE:

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM

Manual v01

2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C&E has been investigated. It is applicable to the modular.

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

2.4 Limited module procedures

Not applicable

2.5 Trace antenna designs

Not applicable

2.6 RF exposure considerations

To maintain compliance with FCC's RF Exposure guidelines, This equipment should be installed and operated with minimum distance of 20cm from your body.

2.7 Antennas

This radio transmitter FCC ID: **2AOHH-TURBOXC865** has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Internal Identification	Antenna Description	Antenna type	Maximum antenna gain
Antenna 0	BT Antenna & Wi-Fi Antenna 0	PCB Antenna	BT/2.4G Wi-Fi: -3.0dBi, 5G Wi-Fi: 0dBi
Antenna 1	Wi-Fi Antenna 1	PCB Antenna	2.4G Wi-Fi: -3.0dBi, 5G Wi-Fi: -3dBi

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains FCC ID: **2AOHH-TURBOXC865**"

2.9 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B