Thundercomm TurboX™ C845 System on Module Datasheet

Thundercomm

Thundercomm TurboX™ C845 System on Module

A high performance embedded platform based on Qualcomm® Snapdragon™ 845 processor

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Description

Thundercomm TurboX™ C845 System on Module (SOM) is an intelligent high-performance module, integrating Android or Linux system, based on Qualcomm SDA845 processor. It integrates the advanced 10 nm Fin FET process, a customized 64-bit ARM v8-compliant Octacore Qualcomm Kryo 385 applications processor.

TurboX C845 SOM supports short-range wireless communication through Wi-Fi 802.11 a/b/g/n/ac and BT5.0. This SOM supports 3840*2400@60fps display, it can connect 4 x camera modules, and integrating multiple audio and video input/output interfaces. This SOM provides a variety of GPIO, I2C, UART and SPI standard interfaces. In addition, it supports two MIPI-DSI, four MIPI-CSI and SOM common standard protocol interfaces such as USB3.1, PCIE2.1/3.0, I2S and SLIMBUS.

TurboX C845 SOM provides convenient and stable system solution for IOT field, it can be embedded into the device on VR/AR, Drone, Robot, Smart Camera, AI devices, and any other connecting fields. The size of module is 37mm x 60mm x 7.1mm, weight 10.3g, with 336PINs.

Features

The following table shows the detailed features and performance on TurboX C845 SOM.

Processors	
Applications Processor	64-bit applications processor (Kryo 385) with 2 MB L3 cache Quad high-performance Kryo cores at 2.649 GHz - Kryo Gold cluster with 256 kB L2 cache per core Quad low-power Kryo cores at 1.766 GHz - Kyro Silver cluster with 128 kB L2 cache per core
Digital signal processing	Compute DSP with Qualcomm Hexagon Vector Extensions (dual-HVX512) processor

Sensor core	Snapdragon™ sensor core with dedicated sensor DSP and 1.0 MB memory (512 kB TCM + 512 kB L2) to support always-on low-power use cases
Operating System	Android OS 10
Memory	64GB UFS + LPDDR4x 4GB / 64GB UFS + LPDDR4x 8GB Four-channel PoP high-speed memory – LPDDR4x SDRAM (4 x 16-bit) designed for a 1866 MHz clock.
Multimedia	
Display support	2 x 4-lane DSI DPHY 1.2 and DisplayPort 1.4 data concurrency over USB Maximum concurrency configurations 3840x2400 at 60Hz primary + 3840 x 2160 or 4096 x 2160 at 60Hz DP 2 x 2560 x 1600 at 60 fps primary + 3840 x 2160 or 4096 x 2160 at 60fps DP
Camera support	Support 3 x 4-lane MIPI_CSI + 1 x 2-lane MIPI_CSI Dual 14-bit ISP + one Lite ISP Real-time sensor input resolution: 16 + 16 +2 MP 32 MP 30 fps ZSL with a dual ISP 16 MP 30 ZSL with single ISP
Video	
Encode	4K60 encode for H.264 High Profile, H265 Main 10 Profile 4K30 encode for VP8
Decode	4K60 decode for H.264 High Profile, H265 Main 10 Profile and VP9 Profile 2
Graphics	Adreno 630 - 4K 60 fps UI or 2x 2k x 2k 90 fps UI

	OpenGL ES 3.2 + AEP, DX next, Vulkan 2 OpenCL 2.0 full profile, RenderScript
Audio ***(build in TurboX C845 Carrier Board)***	
Codec	Five DACs, five outputs five differential analog inputs; four ADCs Six digital microphones Open DSP CPE voice activation subsystem for ultra low-power voice wake-up Native DSD (WCD9341 only), MBHC, and ANC 130 dB dynamic range, 32-bit DAC
Low-power audio	Low-power, low-complexity; 7.1 surround sound
Voice codec support	QCELP, EVS, EVRC, EVRC-B, EVRC-WB; G.7 Gen, G.729A/AB; GSM-FR, GSM-EFR and GSM-HR; AMR-NB and AMR-WB
Enhanced audio	Surround sound: advanced multichannel Fluence™ Pro noise cancellation; enhanced speaker protection Qualcomm enhance 3D audio solution, Qualcomm stereo audio expansion feature, and Qualcomm intelligent mixing algorithm
Wireless connectivity	
WLAN	2.4G/5G, support 802.11 a/b/g/n/ac, 2 X 2 MIMO
Bluetooth	Support Bluetooth 5.0 + HS BLE
Connectivity	

USB	2x USB 3.1, one can support Type-C with DisplayPort
PCIe	2x PCIe, one Gen 2 1-lane with PHY 2.1 and one Gen 3 1-lane with PHY 3.0
SDIO	SD V3.0 4-bit for SD card
QUP	4 bit each; Multiplexed serial interface functions, can be configured as UART, I2C, SPI
SLIMbus	One, highly multiplexed, high-speed, baseline WCD9340/WCD9341
MI2S	Full duplex stereo or up to quad channel Tx/Rx MI2S (x3) Up to eight channels for multi-channel Tx/Rx audio applications (x1)
GPIO	12+ GPIO ports
Others	
ADC Interface	Support ADC interfaces used for input voltage sense, battery temperature detection and general purpose ADC
Touchscreen support	Capacitive panels via ext IC (I2C, and interrupts)
Physical size	Size: 37mm x 60mm x7.1mm Weight: approx. 10.3g Interface: Connector
Operating temperature	-20~70℃
RoHS	All hardware components are fully compliant with EU RoHS directive

Applications

TurboX C845 SOM is ideal for many applications including (but not limited to): AI, Robotics, Virtual Reality (VR), Augmented Reality (AR), Drones and Medical Devices.

Revision History

Version	Date	Description
V1.0	Jan 19, 2022	Initial release.

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1 Physical Description

1.1 Major Components Location

Refer to the figure below for the major components of TurboX C845 SOM.

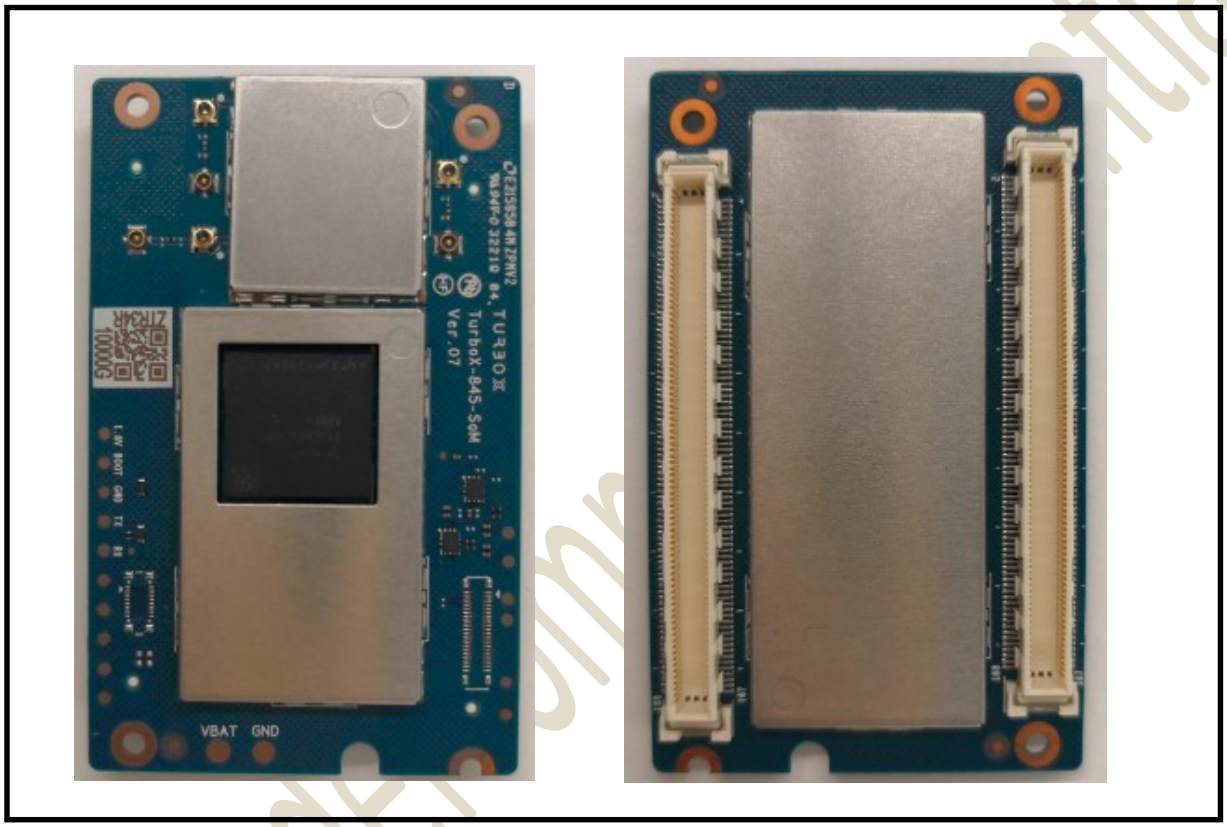


Figure 1.2-1 TurboX C845 SOM Key component Location

1.2 Connectors Function and Part Number

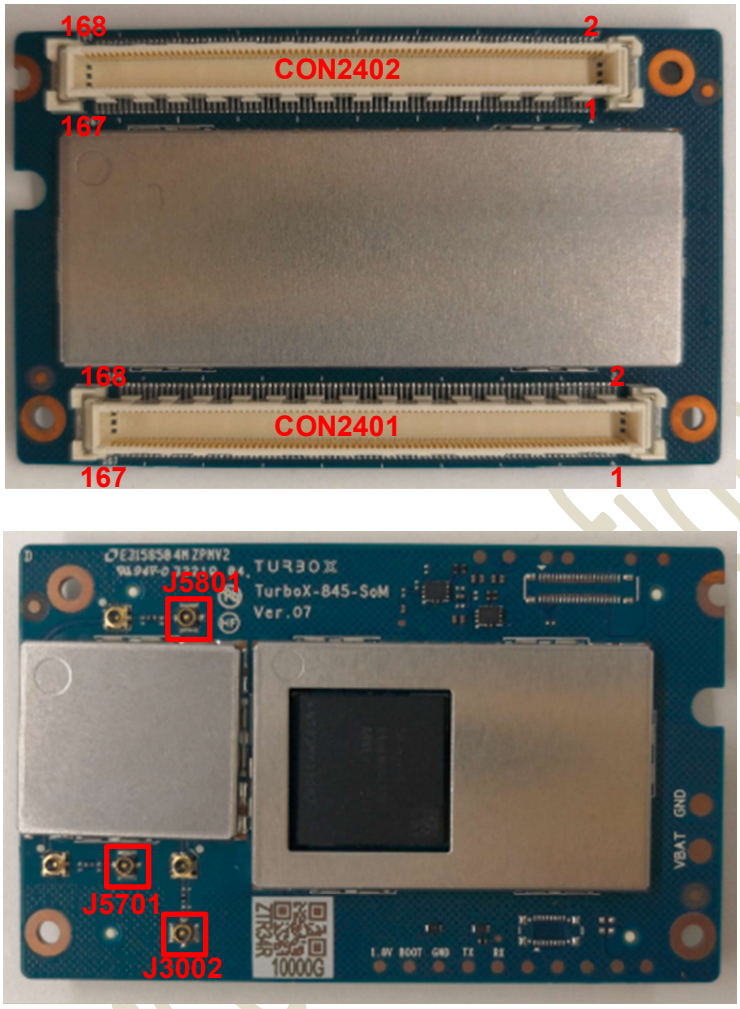


Figure 1.2-1 TurboX C845 SOM Connector PIN Location

Below table indicates connectors detail information.

Part Reference	Description	Manufacturer Part Number	Manufacturer
CON2401,CON2402	BTB connectors, used for connecting to Carrier Board.	FX10A-168P-SV	HIROSE
J3002,J5701,J5801	RF antenna connector, J3002 is no use.	818000500	ECT

Table 1.2-1 Connector part number and information

1.3 Package Drawing and Dimensions

Figure 1.3-1 Top View

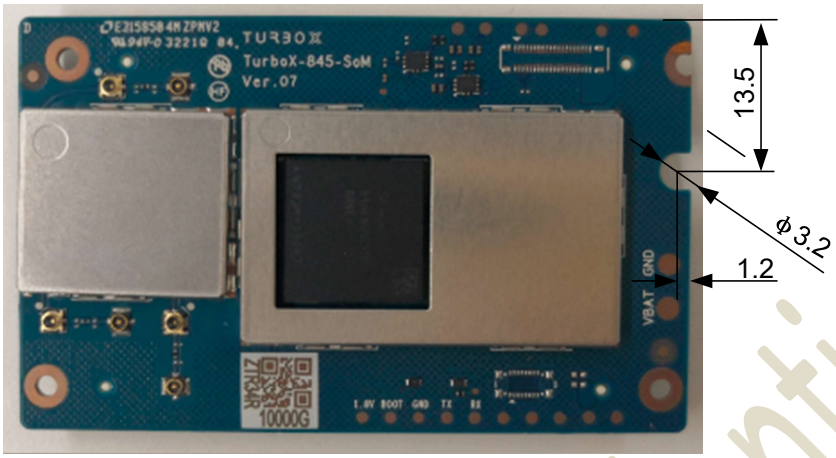
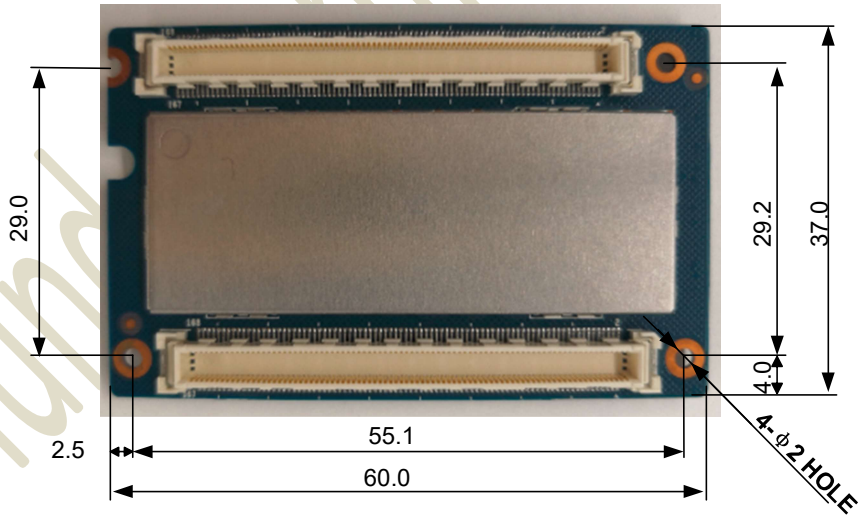


Figure 1.3-2 Side View

Figure 1.3-3 Bottom View



2 Functional Overview

2.1 DSP (Hexagon v65)

- Hexagon Coprocessor (HCP) and VMA1.0
- Universal Bandwidth Compression (UBWC) and DMA1.0
- Vector TCM (VTCM)
- Scatter-Gather support
- HVX contexts and concurrency
- Migrating to 128-byte mode for future forward compatibility
- dspCV_init is deprecated
- New HAP DCVS v2 APIs for clock and bus voting
- dspCV_concurrency is deprecated
- Session restart
- SDK 3.x
- Camera streaming – four tap points
- Dedicated bus for camera streaming on the cDSP
- Dedicated high-speed bus for data transfer from the DDR to the cDSP
- FastCV software development kit with HVX acceleration

2.2 Visual Processing Subsystem

- Improved GPGPU
  - Enhanced image processing for GPGPU use cases
  - Native MIPI and Bayer texture format support
  - Enhanced mathematics for machine learning (matrix Mul)
- Architectural improvements for performance and power

- Efficient multiview rendering for VR/AR
- More efficient, wider Shader microarchitecture
- Significant resource (ALU) increase in Shader Processors
- Increased texture performance

- Memory bandwidth reduction and efficiency improvements
  - Improved UI with updated 2D rasterization patterns
  - Improved hidden surface removal to reduce work
  - Better lossless compression to reduce memory bandwidth and power
- Improvements for Vulkan support
  - Reduced overhead in hardware and driver

2.3 Secure Processing Unit (SPU)

- Qualcomm Trusted Execution Environment
  - Isolates secure and non-secure software operations
  - Small code base, rigorously reviewed
  - Based on ARM's TrustZone architecture
- Secure Boot
  - Deters unauthorized code execution
  - Tamper resistant root of trust in ROM or e-fuses
- Hardware Crypto
  - FIPS certifiable cryptographic engines and HW keys for more robust and fast encrypt/decrypt operations
- Secure Storage and Key Provisioning
  - OTP e-fuse memory for storage of keys and configurations
  - Secure file system for encrypted storage of DRM keys and certificates
  - Provisioning of Keys
- Secure Debug
  - Prevents JTAG debugger connection in commercial products and reverse engineering

- Set by e-fuse, with support for secure RMA

2.4 ISP(ISP280)

- IFE: Image front-end engine
  - Bayer process for preview/video only
  - Stats for 3A
  - Muti-pass outputs feeding to IPE
- IPE: Image processing engine, consists of 2 parts
  - NPS: Noise processing segment
  - PPS: Post processing segment
- BPS: Bayer processing segment
  - Bayer process and noise reduction for snapshot only
  - Simple stats for special offline processing
  - Muti-pass outputs feeding to IPE

2.5 Connection

- 2 x 2 802.11ac with MU-MIMO(Beamforming function is not supported)
- 160 MHz & DBS support
- Bluetooth 5.0
- Optional dedicated BT antenna support concurrent operation for WLAN and BT with and without dedicated BT antenna
- RF performance meets all carrier requirments
  - Industry leading throughput
  - Low power island on MSM for lowest Wi-Fi power consumption (up to 61% improvement)
  - BT/BTLE integration within WCN3990 for lowest BT power consumption (up to 87% improvement)

3 Interfaces Description

This chapter introduces all the interfaces definition, purpose to guide developer easy to design and verification on Thundercomm TurboX™ C845 SOM.

3.1 Interfaces Parameter Definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O; (1.8 V only)
DI	Digital input(CMOS)
DSI	Supply voltage for MIPI_DSI I/O; (1.8 V only)
DO	Digital output(CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output

PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3, it is 1.8V.
P2	SDC Power group 3, it is 1.8V or 2.96V.
P12	SSC Power group 12, it is 1.8V.

Table 3.1-1 Interfaces parameter definitions

3.2 Interfaces Detail Description

3.2.1 Power Supply Interface

Below table describes all interfaces of SOM Power Supply. For the detail parameter request, please refer the chapter on Electrical specifications.

Power Supply					
PIN Name	**Location**	**PIN**	**Type**	**Description**	**Notes**
VBATT	CON2401	159,160,161,162,163,164,165,166,167,168	PI	Power supply in for SOM all operations.	
USB_VBUS	CON2402	159,161,163,165,167	PO	USB output during USB-OTG operation.	
VREG_LVS2A_1P8	CON2402	147	PO	Low voltage switch supply output for sensor	
VREG_S4A_1P8	CON2402	123,125,127	PO	SMPS power output for external CODEC ; Also can used for 1.8V IO pull up voltage;	
VREG_L21A_2P95	CON2401	152,154,156	PO	Power output for SD card	
VREG_L19A_3P0	CON2402	149	PO	Power output for Sensor	
VREG_LVS1A_1P8	CON2401	150	PO	Cameras IO power supply	
VREG_BOB	CON2402	139,141	PO	For Codec VDD input	
GND	CON2401	1,7,8,13,14,19,20,25,26,31,32,37,38,42,43,49,55,60,61,66,67,72,73,78,79,84,90,93,94,98,102,106,114,120,126,132,155,157,158	GND		

	CON2402	11,12,17,18,23,24,29,30,35,36,41,42,46,54,97,103,104,109,110,115,116,121,122,128,156,157,162,168	GND		
	J2	8	GND		

Table 3.2-1 Power Supply Definition

3.2.2 Touchscreen Interface

Touchscreen panels are supported using I2C buses and GPIOs configured as discrete digital inputs.

Touchscreen						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
TP_I2C_SDA	CON2402	45	PX3	OD	QUP5 I2C signals	
TP_I2C_SCL	CON2402	43	PX3	OD	QUP5 I2C signals	
TP_INT_N	CON2402	47	PX3	DO	TP interrupt signals	
TP_RST_N	CON2402	49	PX3	DI	TP reset signals	

Table 3.2-2 Touchscreen interfaces definition

3.2.3 Display Interface

The SOM supports dual 4-lane MIPI_DSI interfaces. 60fps, Up to 3840 x 2400.

Display						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
MIPI_DSI0_LANE3_N	CON2402	13	DSI	AO	MIPI0 signals for MIPI LCM. Compliant with MIPI Alliance Specification for Display Serial Interface	
MIPI_DSI0_LANE3_P	CON2402	15	DSI	AO		
MIPI_DSI0_LANE2_N	CON2402	19	DSI	AO		
MIPI_DSI0_LANE2_P	CON2402	21	DSI	AO		
MIPI_DSI0_CLK_N	CON2402	25	DSI	AO		
MIPI_DSI0_CLK_P	CON2402	27	DSI	AO		
MIPI_DSI0_LANE1_N	CON2402	31	DSI	AO		
MIPI_DSI0_LANE1_P	CON2402	33	DSI	AO		
MIPI_DSI0_LANE0_N	CON2402	37	DSI	AO		
MIPI_DSI0_LANE0_P	CON2402	39	DSI	AO		
MIPI_DSI1_LANE0_N	CON2402	14	DSI	AO	MIPI1 Signals for MIPI LCM	
MIPI_DSI1_LANE0_P	CON2402	16	DSI	AO		

MIPI_DSI1_CLK_P	CON2402	20	DSI	AO	Compliant with MIPI Alliance Specification for Display Serial Interface	
MIPI_DSI1_CLK_N	CON2402	22	DSI	AO		
MIPI_DSI1_LANE2_P	CON2402	26	DSI	AO		
MIPI_DSI1_LANE2_N	CON2402	28	DSI	AO		
MIPI_DSI1_LANE3_N	CON2402	32	DSI	AO		
MIPI_DSI1_LANE3_P	CON2402	34	DSI	AO		
MIPI_DSI1_LANE1_N	CON2402	38	DSI	AO		
MIPI_DSI1_LANE1_P	CON2402	40	DSI	AO		
LCD_RST_N	CON2402	61	PX3	DO	LCD reset signal	
LCD_TE0	CON2402	59	PX3	DI	LCD TE signal input	

Table 3.2-3 Display interfaces definition

3.2.4 Camera Interfaces

The SOM supports 3 x 4-lane + 1 x 2-lane camera interfaces.

Camera0 Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
CCI_I2C_SDA0	CON2401	143	PX3	OD	CCI0 Date signal, already pull up on SOM	
CCI_I2C_SCL0	CON2401	141	PX3	OD	CCI0 Clock signal, already pull up on SOM	
CAM0_PWDN	CON2401	113	PX3	DO	Camera power down signal	
CAM0_RSTN	CON2401	99	PX3	DO	Camera reset signal	
CAM0_STROBE	CON2401	121	PX3	DI	Camera STROBE signal	
CAM0_DVDD_EN	CON2401	131	LV	DO	Camera DVDD LDO enable signal	
CAM0_AVDD_EN	CON2401	101	PX3	DO	Camera AVDD LDO enable signal	
CAM_MCLK0	CON2401	92	PX3	DO	Camera main clock output	
MIPI_CSI0_LANE3_P	CON2401	3	CSI	AI	MIPI Signals of Camera0 Compliant with MIPI Alliance Standard Specification	
MIPI_CSI0_LANE3_N	CON2401	5	CSI	AI		
MIPI_CSI0_LANE2_N	CON2401	9	CSI	AI		
MIPI_CSI0_LANE2_P	CON2401	11	CSI	AI		
MIPI_CSI0_LANE1_N	CON2401	15	CSI	AI		
MIPI_CSI0_LANE1_P	CON2401	17	CSI	AI		
MIPI_CSI0_LANE0_N	CON2401	21	CSI	AI		
MIPI_CSI0_LANE0_P	CON2401	23	CSI	AI		

MIPI_CSI0_CLK_P	CON2401	27	CSI	AI		
MIPI_CSI0_CLK_N	CON2401	29	CSI	AI		

Camera1 Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
CCI_I2C_SDA0	CON2401	143	PX3	OD	CCI0 Date signal, already pull up on SOM	
CCI_I2C_SCL0	CON2401	141	PX3	OD	CCI0 Clock signal, already pull up on SOM	
CAM1_PWDN	CON2401	119	PX3	DO	Camera power down signal	
CAM1_RSTN	CON2401	95	PX3	DO	Camera reset signal	
CAM1_STROBE	CON2401	115	PX3	DI	Camera STROBE signal	
CAM1_DVDD_EN	CON2401	129	LV	DO	Camera DVDD LDO enable signal	
CAM1_AVDD_EN	CON2401	97	PX3	DO	Camera AVDD LDO enable signal	
CAM_MCLK1	CON2401	96	PX3	DO	Camera main clock output	
MIPI_CSI1_LANE3_N	CON2401	33	CSI	AI	MIPI Signals of Camera1 Compliant with MIPI Alliance Standard Specification	
MIPI_CSI1_LANE3_P	CON2401	35	CSI	AI		
MIPI_CSI1_LANE2_P	CON2401	39	CSI	AI		
MIPI_CSI1_LANE2_N	CON2401	41	CSI	AI		
MIPI_CSI1_LANE1_N	CON2401	45	CSI	AI		
MIPI_CSI1_LANE1_P	CON2401	47	CSI	AI		
MIPI_CSI1_LANE0_N	CON2401	51	CSI	AI		
MIPI_CSI1_LANE0_P	CON2401	53	CSI	AI		
MIPI_CSI1_CLK_N	CON2401	57	CSI	AI		
MIPI_CSI1_CLK_P	CON2401	59	CSI	AI		

Camera2 Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
CCI_I2C_SDA1	CON2401	145	PX3	OD	CCI0 Date signal, already pull up on SOM	
CCI_I2C_SCL1	CON2401	147	PX3	OD	CCI0 Clock signal, already pull up on SOM	
CAM2_PWDN	CON2401	105	PX3	DO	Camera power down signal	
CAM2_RSTN	CON2401	123	PX3	DO	Camera reset signal	
CAM2_STROBE	CON2401	117	PX3	DI	Camera STROBE signal	
CAM2_DVDD_EN	CON2401	109	PX3	DO	Camera DVDD LDO enable signal	
CAM2_AVDD_EN	CON2401	103	PX3	DO	Camera AVDD LDO	

					enable signal	
CAM_MCLK2	CON2401	100	PX3	DO	Camera main clock output	
MIPI_CSI2_LANE1_P	CON2401	63	CSI	AI	MIPI Signals of Camera2 Compliant with MIPI Alliance Standard Specification	
MIPI_CSI2_LANE1_N	CON2401	65	CSI	AI		
MIPI_CSI2_LANE2_P	CON2401	69	CSI	AI		
MIPI_CSI2_LANE2_N	CON2401	71	CSI	AI		
MIPI_CSI2_LANE3_P	CON2401	75	CSI	AI		
MIPI_CSI2_LANE3_N	CON2401	77	CSI	AI		
MIPI_CSI2_CLK_P	CON2401	62	CSI	AI		
MIPI_CSI2_CLK_N	CON2401	64	CSI	AI		
MIPI_CSI2_LANE0_N	CON2401	68	CSI	AI		
MIPI_CSI2_LANE0_P	CON2401	70	CSI	AI		
Camera3 Interface						
MIPI_CSI3_LANE1_N	CON2401	74	CSI	AI	MIPI Signals of Camera3 Compliant with MIPI Alliance Standard Specification	
MIPI_CSI3_LANE1_P	CON2401	76	CSI	AI		
MIPI_CSI3_LANE0_P	CON2401	80	CSI	AI		
MIPI_CSI3_LANE0_N	CON2401	82	CSI	AI		
MIPI_CSI3_CLK_N	CON2401	86	CSI	AI		
MIPI_CSI3_CLK_P	CON2401	88	CSI	AI		
CAM_MCLK3	CON2401	104	PX3	DO	Camera main clock output	
CAM3_PWDN	CON2401	111	PX3	DO	Camera power down signal	
CAM3_RSTN	CON2401	125	PX3	DO	Camera reset signal	
CAM3_DVDD_EN	CON2401	127	PX3	DO	Camera DVDD LDO enable signal	
CAM3_AVDD_EN	CON2401	107	PX3	DO	Camera AVDD LDO enable signal	

Table 3.2-4 Camera interface definition

3.2.5 Audio Interface

The SOM provide SLIMBUS and I2S interfaces for audio. SLIMBUS interface is dedicate for external codec IC, which can build system's audio functions. I2S interface can connect audio devices.

Audio Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
CODEC_SLIMBUS_DATA0	CON2402	48	PX3	IO	Slimbus, connect to COEDC Compliant with MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	
CODEC_SLIMBUS_DATA1	CON2402	50	PX3	IO		
CODEC_SLIMBUS_CLK	CON2402	52	PX3	DO		
CODEC_INT1_N	CON2402	92	PX3	DI	CODEC interrupt signal	
CODEC_INT2_N	CON2402	94	PX3	DI		
CODEC_RST_N	CON2402	89	PX3	DO	CODEC reset signal	
LN_BB_CLK2_WCD	CON2402	44	PX3	DO	CODEC clock	
CODEC_SPI_CLK	CON2402	91	PX3	DO	SPI interface for faster code download and IPC to the integrated DSP	
CODEC_SPI_MOSI	CON2402	93	PX3	DO		
CODEC_SPI_CS_N	CON2402	95	PX3	DO		
CODEC_SPI_MISO	CON2402	90	PX3	DI		
MI2S1_WS	CON2402	80	PX3	IO	I2S1 signals Compliant with Philips I2S Bus Specifications	
MI2S1_MCLK	CON2402	82	PX3	DO		
MI2S1_SCK	CON2402	84	PX3	IO		
MI2S1_DATA1	CON2402	86	PX3	IO		
MI2S1_DATA0	CON2402	88	PX3	IO		
MI2S2_WS	CON2402	56	PX3	IO	I2S2 signals Compliant with Philips I2S Bus Specifications	
MI2S2_SCK	CON2402	58	PX3	IO		
MI2S2_DATA0	CON2402	60	PX3	IO		
MI2S2_DATA1	CON2402	62	PX3	IO		
MI2S3_WS	CON2402	64	PX3	IO	I2S3 signals Compliant with Philips I2S Bus Specifications	
MI2S3_DATA1	CON2402	66	PX3	IO		
MI2S3_DATA2	CON2402	68	PX3	IO		
MI2S3_DATA0	CON2402	70	PX3	IO		
MI2S3_DATA3	CON2402	72	PX3	IO		
MI2S3_SCK	CON2402	74	PX3	IO		

Table 3.2-5 Audio interface definition

3.2.6 USB & DisplayPort Interface

The SOM support 2 x USB 3.1, one can support Type-C with DisplayPort. USB mode and DisplayPort mode can be simultaneously operation at USB 3 (5 Gbps) and DP (8.1 Gbps).

SS/HS USB (3.0/2.0) & DisplayPort Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
USB1_SS_TX0_M	CON2402	124		DO	USB 3.0 Signals Compliant with USB 3.1 standard specification	Require differential impedance of 90Ω.
USB1_SS_TX0_P	CON2402	126		DO		
USB1_SS_RX0_M	CON2402	117		DI		
USB1_SS_RX0_P	CON2402	119		DI		
USB1_SS_TX1_M	CON2402	112		DO		
USB1_SS_TX1_P	CON2402	114		DO		
USB1_SS_RX1_P	CON2402	111		DI		
USB1_SS_RX1_M	CON2402	113		DI		
USB1_HS_DP	CON2402	120		IO	USB 2.0 Signals Compliant with USB 2.0 standard specification	
USB1_HS_DM	CON2402	118		IO		
USB_VBUS	CON2402	159,161, 163,165, 167		PO	USB VBUS OTG output	
USB_CC1	CON2402	142		IO	CC pin for Type-C USB connector	
USB_CC2	CON2402	140		IO		
EDP_AUX_P	CON2402	130	PX3	IO	DP AUX signals	
EDP_AUX_N	CON2402	132	PX3	IO		
SBU_SW_OE	CON2402	2	PX3	IO	DP AUX signals switch chipset enable	
SBU_SW_SEL	CON2402	4	PX3	IO	DP AUX signal switch select indicate	
USB2_SS_RX_M	CON2402	99		DI	USB 3.0 Signals Compliant with USB 3.1 standard specification	Require differential impedance of 90Ω.
USB2_SS_RX_P	CON2402	101		DI		
USB2_SS_TX_P	CON2402	105		DO		
USB2_SS_TX_M	CON2402	107		DO		
USB2_HS_DP	CON2402	106		IO	USB 2.0 Signals Compliant with USB 2.0 standard specification	
USB2_HS_DM	CON2402	108		IO		

Table 3.2-6 USB &DP interface definition

3.2.7 PCIe Interface

The SOM support one Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

PCIE Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PCIE0_REFCLK_P	CON2401	16		AO	PCIe Signals Compliant with PCI Express Specification Revision 2.1	
PCIE0_REFCLK_M	CON2401	18		AO		
PCIE0_RX_P	CON2401	22		AI		
PCIE0_RX_M	CON2401	24		AI		
PCIE0_TX_M	CON2401	10		AO		
PCIE0_TX_P	CON2401	12		AO		
PCIE_0_CLK_REQ	CON2401	6	PX3	DI	PCIe clock require signal, need to reserve pull up resistor	
PCIE_0_RST_N	CON2401	2	PX3	DO	PCIe reset signal	
PCIE_0_WAKE_N	CON2401	4	PX3	DI	PCIe wake up signal	
PCIE1_REFCLK_P	CON2401	122		AO	PCIe Signals Compliant with PCI Express Specification Revision 3.0	
PCIE1_REFCLK_M	CON2401	124		AO		
PCIE1_RX_P	CON2401	116		AI		
PCIE1_RX_M	CON2401	118		AI		
PCIE1_TX_M	CON2401	128		AO		
PCIE1_TX_P	CON2401	130		AO		
PCIE_1_CLK_REQ	CON2401	110	PX3	DI	PCIe clock require signal, need to reserve pull up resistor	
PCIE_1_RST_N	CON2401	108	PX3	DO	PCIe reset signal	
PCIE_1_WAKE_N	CON2401	112	PX3	DI	PCIe wake up signal	

Table 3.2-4 PCIe interface definition

3.2.8 SSC Interface

The SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the MSM device is in sleep mode. The SSC has a dedicated 1.0MB L2/TCM cache.

The SSC core has dedicated I/O to communicate with the sensors. The I/O scan support I2C and SPI interfaces.

SSC Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SSC_I2C1_SDA	CON2402	7	PX12	OD	These I2C signals are dedicated to Sensor	
SSC_I2C1_SCL	CON2402	9	PX12	OD		
SSC_SPI1_MISO	CON2401	149	PX12	DI	Snapdragon™ Sensor Core SPI signals	
SSC_SPI1_MOSI	CON2401	151	PX12	DO		
SSC_SPI1_CLK	CON2401	153	PX12	DO		
SSC_MAG_CS_L	CON2401	135	PX12	DO		
SSC_GYRO_CS_L	CON2401	137	PX12	DO		
SSC_ACCEL_CS_L	CON2401	139	PX12	DO		
SSC_SPI2_CS_L	CON2401	142	PX12	DO	Snapdragon™ Sensor Core SPI signals	
SSC_SPI2_MOSI	CON2401	144	PX12	DO		
SSC_SPI2_CLK	CON2401	146	PX12	DO		
SSC_SPI2_MISO	CON2401	148	PX12	DI		

Table 3.2-8 SSC interface definition

3.2.9 SDIO Interface

The SOM support dual 4-laneSDIO, SDC2 connect to SD-card.
The SDIO is high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 200 MHz.
- The signals routing should be 50ohm ±10% impedance control.
- CLK to DATA/CMD length matching less than 1mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

SDIO (SDC2) Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SDC2_CLK	CON2401	46	PX2	DO	SD card signals; SD_CARD_DET_N need pull up to PX3	
SDC2_CMD	CON2401	48	PX2	IO		
SDC2_DATA3	CON2401	56	PX2	IO		
SDC2_DATA2	CON2401	58	PX2	IO		
SDC2_DATA1	CON2401	54	PX2	IO		
SDC2_DATA0	CON2401	52	PX2	IO		
SD_CARD_DET_N	CON2401	50	PX3	DI		
SDIO (SDC4) Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SDC4_DATA0	CON2401	81	PX3	IO	SDIO Signals Compliant with SDIO standard specification.	
SDC4_DATA1	CON2401	83	PX3	IO		
SDC4_DATA2	CON2401	87	PX3	IO		
SDC4_DATA3	CON2401	89	PX3	IO		
SDC4_CLK	CON2401	85	PX3	DO		
SDC4_CMD	CON2401	91	PX3	IO		

Table 3.2-5 SDIO interface definition

3.2.10 QUP Interface

These GPIOs are available as Qualcomm universal peripheral (QUP) interface ports that can be configured for UART, SPI, or I2C operation.
I2C is a two-wire bus that can be routed to multiple devices; each line of each bus need to supplement by a 2.2kΩ pull-up resistor

QUP Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
BLSP_SPI0_MISO	CON2402	83	PX3	IO	QUP0 can be configured to GPIO or UART or SPI or I2C	
BLSP_SPI0_MOSI	CON2402	81	PX3	IO		
BLSP_SPI0_CLK	CON2402	85	PX3	IO		
BLSP_SPI0_CS_L	CON2402	79	PX3	IO		
BLSP_SPI2_MISO	CON2402	55	PX3	IO	QUP2 can be configured to GPIO or UART or SPI or I2C	
BLSP_SPI2_MOSI	CON2402	57	PX3	IO		
BLSP_SPI2_CLK	CON2402	51	PX3	IO		
BLSP_SPI2_CS_L	CON2402	53	PX3	IO		
BLSP_SPI11_MISO	CON2402	98	PX3	IO	QUP11 can be configured to GPIO or UART or SPI or I2C	
BLSP_SPI11_MOSI	CON2402	96	PX3	IO		
BLSP_SPI11_CLK	CON2402	100	PX3	IO		
BLSP_SPI11_CS_L	CON2402	102	PX3	IO		
BLSP_I2C4_SDA	CON2402	3	PX3	IO	QUP4 can be configured to GPIO or UART or SPI or I2C	
BLSP_I2C4_SCL	CON2402	5	PX3	IO		
SDC4_CMD	CON2401	91	PX3	IO		
SDC4_DATA3	CON2401	89	PX3	IO		
SDC4_CLK	CON2401	85	PX3	IO	QUP7 can be configured to GPIO or UART or SPI or I2C	
SDC4_DATA2	CON2401	87	PX3	IO		
SDC4_DATA1	CON2401	83	PX3	IO		
SDC4_DATA0	CON2401	81	PX3	IO		
APPS_I2C10_SDA	CON2402	78	PX3	IO	QUP10 can be configured to GPIO or I2C	
APPS_I2C10_SCL	CON2402	76	PX3	IO		
TP_I2C_SDA	CON2402	45	PX3	IO	QUP5 can be configured to GPIO or I2C	
TP_I2C_SCL	CON2402	43	PX3	IO		

Table 3.2-6 QUP interface definition

3.2.11 Power on Interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device's available power sources, enable the correct source. It is longer than 1s with pressing power-on key, for power on event. And it is suggested for 3s powering on system. Power on/off key signal can be connected to ground through CON2402.6; the other power on method is: when using CBL_PWR_N pin connect to ground, insert battery or power supply，SOM will power on automatically.

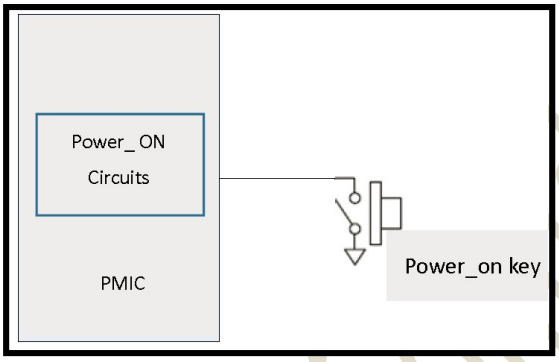


Figure 3.2-1 Power on signal

Power on Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
CBL_PWR_N	CON2401	133	pulled up internally through a 200K resistor to 1.8V	DI	Signal use for auto power on when you plug in a battery, active low, internal pull up	

Table 3.2-11 Power on interface definition

3.2.12 Reset Interface

Extended press of volume key will initiate a shutdown or reset (software selectable)

- Stage 1 reset – software-configurable bark

PMIC generates interrupt, giving the MSM device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark: Over temperature indicates system is getting too hot. PMIC watchdog indicates that it has not kicked.

- Stage 2 –software-configurable bite

If reset is ignored, PMIC will force a reset event (selectable by software).

- Stage 3 –hardware mandatory bite

The user can generate a mandatory reset by a long press of PM_RESIN_N, or PHONE_ON_N, or PM_RESIN_N + PHONE_ON_N in combination.

The standalone or combination of reset triggers can also be selected as SBL by directly writing to the appropriate registers

Reset Pin						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PM_RESIN_N	CON2402	8	pulled up internally to 1.8V	DI	Volume down/Reset key signal, Low active	

Table 3.2-12 Reset interface definition

3.2.13 Keys Interface

This is interface dedicate for key.

KEYs PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PHONE_ON_N	CON2402	6	PX3	DI	Power on key signal, Low active	
PM_RESIN_N	CON2402	8	PX3	DI	Volume down/Reset key signal, Low active	
VOL_UP_N	CON2402	10	PX3	DI	Volume up key signal, Low active	

Table 3.2-7 Keys interface definition

3.2.14 Sensor Interrupt Interface

All these interfaces dedicate to below sensors.

Sensor Interrupt PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
MAG_INT	CON2401	134	PX3	DI	Magnetometer sensor interrupt	
MAG_DRDY_INT	CON2401	136	PX3	DI	Magnetometer data ready interrupt	
GYRO_INT	CON2401	138	PX3	DI	Gyroscope sensor interrupt	
ACCEL_INT	CON2401	140	PX3	DI	Accelerometer Sensor interrupt	

Table 3.2-8 Sensor interrupt definition

3.2.15 Debug UART Interface

This is interface dedicate for debug.

Debug UART PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
MSM_UART_RX	CON2402	136	PX3	DI	QUP8 UART signals, can use for debug	
MSM_UART_TX	CON2402	138	PX3	DO		

Table 3.2-9 Debug UART interface definition

3.2.16 Battery Interface

This is dedicate for battery interface, major for monitoring battery status, inserting and voltage detect.

Battery PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
VBATT_CONN_VSENSE_P	CON2402	164	VBATT	AI	Battery voltage sense positive input signal	
VBATT_CONN_VSENSE_M	CON2402	166	VBATT	AI	Battery voltage sense negative input signal	
IBATT_SENSE_P	CON2402	158	VBATT	AI	Battery current sense positive input signal	
IBATT_SENSE_M	CON2402	160	VBATT	AI	Battery current sense negative input signal	
BATT_THERM	CON2402	144	BATT_THERM _BIAS=2.7V	AI	Battery temperature sense input signal	

Table 3.2-10 Battery interface definition

3.2.17 ADCs Interface

The ADC input signal use as analog multiplexer function.

ADCs PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
ADC_IN_5V	CON2402	152	MV	AI	ADC input, can be configured as 1.8V or 5V	
ADC_IN_1P8V	CON2402	154	LV	AI	ADC input, can be configured as 1.8V	

Table 3.2-1711 MPPs interface definition

3.2.18 PWMs and LED Current Driver Interface

The SOM support dual PWM output and dual LED Current Driver, all PWM output by Light Pulse Generators.

LED Current Driver PINs can be used for different events, they are separate controller. Independently programmable duty cycle and period via LPGs (6-or 9-bit resolution) for digital dimming.

Flash or blinking with register-selectable durations of ON-time from 0 to 1 second, in ≤ 0.05-second steps, and flashing periods from 0 to 12 seconds in steps of ≤ 0.5 seconds (or always on).

PWMs PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PWM_OUTPUT1	CON2402	145	P3	LV	Can be configured as GPIO and PWM(max 19.2MHz)	LPG_OUT_2
PWM_OUTPUT2	CON2402	143	P3	MV		LPG_OUT_6
LED Driver PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
R_LED	CON2402	151		AO	Custom indicator light, connect to positive port	LPG_OUT_5
B_LED	CON2402	153		AO	Custom indicator light, connect to positive port	LPG_OUT_3
G_LED	CON2402	155		AO	Custom indicator light, connect to positive port	LPG_OUT_4

Table 3.2-12 PWMs and LED Current Driver interface definition

3.2.19 Antenna Interface

The SOM provides the fully-integrated WLAN and Bluetooth function.
The WLAN and Bluetooth share the antenna port with 50ohm impedance.

- WLAN supports 2 × 2 multiple input, multiple output (MIMO) with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards.
- Supports Bluetooth 5.0 + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.
- Optional dedicated BT antenna support -concurrent operation for WLAN and BT with and without dedicated BT antenna

Antenna interface						
Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
Antenna 1	J5701			IO	Antenna 1 supports WIFI 2.4G/5G &BT	Chain0
Antenna 2	J5801			IO	Antenna 2 supports WIFI 2.4G/5G	Chain1
Antenna 3	J3002			IO	Antenna 3 support dedicated BT antenna(Optional)	Chain2

Table 3.2-13 Antenna interface definition

4 Connector PIN Summary

4.1 CON2401 BTB Connector

Pin	Signal Name		Pin	Signal Name
1	GND		2	PCIE_0_RST_N
3	MIPI_CSI0_LANE3_P		4	PCIE_0_WAKE_N
5	MIPI_CSI0_LANE3_N		6	PCIE_0_CLK_REQ
7	GND		8	GND
9	MIPI_CSI0_LANE2_N		10	PCIE0_TX_M
11	MIPI_CSI0_LANE2_P		12	PCIE0_TX_P
13	GND		14	GND
15	MIPI_CSI0_LANE1_N		16	PCIE0_REFCLK_P
17	MIPI_CSI0_LANE1_P		18	PCIE0_REFCLK_M
19	GND		20	GND
21	MIPI_CSI0_LANE0_N		22	PCIE0_RX_P
23	MIPI_CSI0_LANE0_P		24	PCIE0_RX_M
25	GND		26	GND
27	MIPI_CSI0_CLK_P		28	UFS2_L0_RX_M
29	MIPI_CSI0_CLK_N		30	UFS2_L0_RX_P
31	GND		32	GND
33	MIPI_CSI1_LANE3_N		34	UFS2_L0_TX_P
35	MIPI_CSI1_LANE3_P		36	UFS2_L0_TX_M
37	GND		38	GND
39	MIPI_CSI1_LANE2_P		40	UFS2_REF_CLK
41	MIPI_CSI1_LANE2_N		42	GND
43	GND		44	UFS_CARD_DET_N
45	MIPI_CSI1_LANE1_N		46	SDC2_CLK
47	MIPI_CSI1_LANE1_P		48	SDC2_CMD

49	GND		50	SD_CARD_DET_N
51	MIPI_CSI1_LANE0_N		52	SDC2_DATA0
53	MIPI_CSI1_LANE0_P		54	SDC2_DATA1
55	GND		56	SDC2_DATA3
57	MIPI_CSI1_CLK_N		58	SDC2_DATA2
59	MIPI_CSI1_CLK_P		60	GND
61	GND		62	MIPI_CSI2_CLK_P
63	MIPI_CSI2_LANE1_P		64	MIPI_CSI2_CLK_N
65	MIPI_CSI2_LANE1_N		66	GND
67	GND		68	MIPI_CSI2_LANE0_N
69	MIPI_CSI2_LANE2_P		70	MIPI_CSI2_LANE0_P
71	MIPI_CSI2_LANE2_N		72	GND
73	GND		74	MIPI_CSI3_LANE1_N
75	MIPI_CSI2_LANE3_P		76	MIPI_CSI3_LANE1_P
77	MIPI_CSI2_LANE3_N		78	GND
79	GND		80	MIPI_CSI3_LANE0_P
81	SDC4_DATA0		82	MIPI_CSI3_LANE0_N
83	SDC4_DATA1		84	GND
85	SDC4_CLK		86	MIPI_CSI3_CLK_N
87	SDC4_DATA2		88	MIPI_CSI3_CLK_P
89	SDC4_DATA3		90	GND
91	SDC4_CMD		92	CAM_MCLK0
93	GND		94	GND
95	CAM1_RSTN		96	CAM_MCLK1
97	CAM1_AVDD_EN		98	GND
99	CAM0_RSTN		100	CAM_MCLK2
101	CAM0_AVDD_EN		102	GND
103	CAM2_AVDD_EN		104	CAM_MCLK3
105	CAM2_PWDN		106	GND
107	CAM3_AVDD_EN		108	PCIE_1_RST_N

109	CAM2_DVDD_EN		110	PCIE_1_CLK_REQ
111	CAM3_PWDN		112	PCIE_1_WAKE_N
113	CAM0_PWDN		114	GND
115	CAM1_STROBE		116	PCIE1_RX_P
117	CAM2_STROBE		118	PCIE1_RX_M
119	CAM1_PWDN		120	GND
121	CAM0_STROBE		122	PCIE1_REFCLK_P
123	CAM2_RSTN		124	PCIE1_REFCLK_M
125	CAM3_RSTN		126	GND
127	CAM3_DVDD_EN		128	PCIE_TX_M
129	CAM1_DVDD_EN		130	PCIE1_TX_P
131	CAM0_DVDD_EN		132	GND
133	CBL_PWR_N		134	MAG_INT
135	SSC_MAG_CS_L		136	MAG_DRDY_INT
137	SSC_GYRO_CS_L		138	GYRO_INT
139	SSC_ACCEL_CS_L		140	ACCEL_INT
141	CCI_I2C_SCL0		142	SSC_SPI2_CS_L
143	CCI_I2C_SDA0		144	SSC_SPI2_MOSI
145	CCI_I2C_SDA1		146	SSC_SPI2_CLK
147	CCI_I2C_SCL1		148	SSC_SPI2_MISO
149	SSC_SPI1_MISO		150	VREG_LVS1A_1P8
151	SSC_SPI1_MOSI		152	VREG_L21A_2P95
153	SSC_SPI1_CLK		154	VREG_L21A_2P95
155	GND		156	VREG_L21A_2P95
157	GND		158	GND
159	VBAT		160	VBAT
161	VBAT		162	VBAT
163	VBAT		164	VBAT
165	VBAT		166	VBAT
167	VBAT		168	VBAT

4.2 CON2402 BTB Connector

Pin	Signal Name		Pin	Signal Name
1	GPIO_25		2	SBU_SW_OE
3	BLSP_I2C4_SDA		4	SBU_SW_SEL
5	BLSP_I2C4_SCL		6	PHONE_ON_N
7	SSC_I2C1_SDA		8	PM_RESIN_N
9	SSC_I2C1_SCL		10	VOL_UP_N
11	GND		12	GND
13	MIPI_DSI0_LANE3_N		14	MIPI_DSI1_LAN0_N
15	MIPI_DSI0_LANE3_P		16	MIPI_DSI1_LANE0_P
17	GND		18	GND
19	MIPI_DSI0_LANE2_N		20	MIPI_DSI_CLK_P
21	MIPI_DSI0_LANE2_P		22	MIPI_DSI_CLK_N
23	GND		24	GND
25	MIPI_DSI0_CLK_N		26	MIPI_DSI1_LANE2_P
27	MIPI_DSI0_CLK_P		28	MIPI_DSI1_LANE2_N
29	GND		30	GND
31	MIPI_DSI0_LANE1_N		32	MIPI_DSI1_LANE3_N
33	MIPI_DSI0_LANE1_P		34	MIPI_DSI1_LANE3_P
35	GND		36	GND
37	MIPI_DSI0_LANE0_N		38	MIPI_DSI1_LANE1_N
39	MIPI_DSI0_LANE0_P		40	MIPI_DSI1_LANE1_P
41	GND		42	GND
43	TP_I2C_SCL		44	LN_BB_CLK2_WCD
45	TP_I2C_SDA		46	GND
47	TP_INT_N		48	CODEC_SLIMBUS_DATA0
49	TP_RST_N		50	CODEC_SLIMBUS_DATA1
51	BLSP_SPI2_CLK		52	CODEC_SLIMBUS_CLK

53	BLSP_SPI2_CS_L		54	GND
55	BLSP_SPI2_MISO		56	MI2S2_WS
57	BLSP_SPI2_MOSI		58	MI2S2_SCK
59	LCD_TE0		60	MI2S2_DATA0
61	LCD_RST_N		62	MI2S2_DATA1
63	GPIO_42		64	MI2S3_WS
65	GPIO_44		66	MI2S3_DATA1
67	GPIO_52		68	MI2S3_DATA2
69	GPIO_50		70	MI2S3_DATA0
71	GPIO_134		72	MI2S3_DATA3
73	GPIO_122		74	MI2S3_SCK
75	GPIO_124		76	APPS_I2C10_SCL
77	GPIO_49		78	APPS_I2C10_SDA
79	BLSP_SPI0_CS_L		80	MI2S1_WS
81	BLSP_SPI0_MOSI		82	MI2S1_MCLK
83	BLSP_SPI0_MISO		84	MI2S1_SCK
85	BLSP_SPI0_CLK		86	MI2S1_DATA1
87	CC_DIR		88	MI2S1_DATA0
89	CODEC_RST_N		90	CODEC_SPI_MISO
91	CODEC_SPI_CLK		92	CODEC_INT1_N
93	CODEC_SPI_MOSI		94	CODEC_INT2_N
95	CODEC_SPI_CS_N		96	BLSP_SPI11_MOSI
97	GND		98	BLSP_SPI11_MISO
99	USB2_SS_RX_M		100	BLSP_SPI11_CLK
101	USB2_SS_RX_P		102	BLSP_SPI11_CS_L
103	GND		104	GND
105	USB2_SS_TX_P		106	USB2_HS_DP
107	USB2_SS_TX_M		108	USB2_HS_DM
109	GND		110	GND
111	USB1_SS_RX1_P		112	USB1_SS_TX1_M

113	USB1_SS_RX1_M		114	USB1_SS_TX1_P
115	GND		116	GND
117	USB1_SS_RX0_M		118	USB1_HS_DM
119	USB1_SS_RX0_P		120	USB1_HS_DP
121	GND		122	GND
123	VREG_S4A_1P8		124	USB1_SS_TX0_M
125	VREG_S4A_1P8		126	USB1_SS_TX0_P
127	VREG_S4A_1P8		128	GND
129	FORCE_USB_BOOT		130	EDP_AUX_P
131	GPIO_128		132	EDP_AUX_N
133	GPIO_135		134	VCOIN
135	GPIO_129		136	MSM_UART_RX
137	NC		138	MSM_UART_TX
139	VREG_BOB		140	USB_CC2
141	VREG_BOB		142	USB_CC1
143	PWM_OUTPUT2		144	BATT_THERM
145	PWM_OUTPUT1		146	HOME_KEY
147	VREG_LVS2A_1P8		148	PM845_GPIO10
149	VREG_L19A_3P0		150	PM845_GPIO13
151	R_LED		152	ADC_IN_5V
153	B_LED		154	ADC_IN_1P8V
155	G_LED		156	GND
157	GND		158	IBATT_SENSE_P
159	USB_VBUS		160	IBATT_SENSE_M
161	USB_VBUS		162	GND
163	USB_VBUS		164	VBATT_CONN_VSENSE_P
165	USB_VBUS		166	VBATT_CONN_VSENSE_M
167	USB_VBUS		168	GND

4.3 J2 BTB Connector

Pin	Signal Name		Pin	Signal Name
1	MSM_JTAG_TMS		9	MSM_JTAG_SRST_N
2	MSM_JTAG_TCK		10	MSM_UART_TX
3	MSM_JTAG_TDO		11	MSM_UART_RX
4	MSM_JTAG_TDI		12	VREG_S4A_1P8
5	MSM_JTAG_TRST_N		13	MSM_PS_HOLD
6	PHONE_ON_N		14	FORCE_USB_BOOT
7	PM_RESIN_N		15	WDOG_DISABLE
8	GND		16	MSM_RESOUT_N

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

The SOM needs to be desinged in the operatin conditions which is shown as below table.

Parameter	Min	Max	Units
Input Power voltage			
USB_VBUS	-0.3	28	V
VBAT	-0.5	6	V
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M, RSENSE_EXT_M, RSENSE_EXT_P	-0.5	6	V
ESD			
ESD-HBM model rating		±2k	KV
ESD-CDM model rating		±4k	KV

Table 5.1-1 Absolute rating condition

***Notes**: for the ESD, it will be valid and available only when the module is fully tested and approved in the Initial Production stage.*

5.2 Operating Conditions

The SOM needs to be desinged in the operatin conditons which is shown as below table.

Parameters	Min	Typical	Max	Units
Input Power voltage				
USB_VBUS	+3.6	5	+13.2	V
VBAT	+3.6	3.8	+4.8	V
VBAT	3			A
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M,	+3.6	3.8	+4.8	V

RSENSE_EXT_M, RSENSE_EXT_P				
Thermal conditions				
Operating temperature	-20	25	70	°C
Storage temperature	-40	-	70	°C

Table 5.2-1 Operating condition

Note: *For the thermal conditons, operatin and storage min and max temperature is only when the module is fully tested and approved in the Initial Production stage.*

5.3 Output Power

The SOM provide power supply for external device, like camera module, SD card, Sensor, and so on. Below map show the details.

Function	Default voltage(V)	Programble range(V)	Rated current(mA)	Expected use
VREG_LVS1A_1P8	+1.8	NA	300	supply output for camera DOVDD
VREG_LVS2A_1P8	+1.8	NA	100	Supply output for sensor
VREG_L19A_3P0	+3.0	+1.62--+3.7	300	Power output for Sensor
VREG_S4A_1P8	+1.8	NA	900	SMPS power output for extra position CODEC, and 1.8V IO pull up voltage;
VREG_BOB	+3.7	+3.6-- +4.0	600	for Codec VDD input Each Pin is 300mA
VREG_L21A_2P95	+2.95	+1.66--+3.7	800	Power output for SD card

Table 5.3-1 Output power

5.4 Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage.The SOM IO voltage level is the same with VDDPX_3 except the SD card and analog input/output. The I2C, USB,MIPI and UART comply with the standards.

5.4.1 Digital GPIO characteristics

The follow-int table shows the digital GPIO characteristics:

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt,	0.7 x VDDPX_3	VDDPX_3+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt,	-0.3	0.3 x VDDPX_3	V
VSHYS	Schmitt hysteresis voltage	300	-	mV
VOH	High-level output voltage, CMOS	VDDPX_3 - 0.45	VDDPX_3	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V
RPULL-UP	Pull-up resistance	20 K	60 K	Ω
RPULL-DOWN	Pull-down resistance	60 K	20 K	Ω

Table 5.4-1 Digital IO voltage performance

5.4.2 SD card digital I/O characteristics

The SD card is powered by P2 supply; the power is 1.8V and 2.96V.the following table shows the SD card digital I/O characteristics:

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27/0.625 x VDDPX_2	-	2/VDDPX_2 + 0.3	V
VIL	Low-level input voltage	-0.3/-0.3	-	0.58/0.25 x VDDPX_2	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/0.75 x VDDPX_2	-	-/VDDPX_2	V
VOL	Low-level output voltage	0/0	-	0.45/0.125 x VDDPX_2	V

Table 5.4-2 SD digital IO voltage performance (1.8V/2.96V)

5.5 MIPI

The SOM supports the MIPI interface and comply with MIPI standards.

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

Table 5.5-1 MIPI_DSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	The maximum supported data rate is 1.5Gsps

Table 5.5-2 MIPI_CSI

5.6 USB

The SOM supports USB standards and exceptions.

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None

Table 5.6-1 USB

5.7 PCIe

The SOM supports PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI Express Specification, Revision 3.0	None

Table 5.7-1 PCIe

5.8 DisplayPort

The SOM supports DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	HBR3

Table 5.8-1 DP

5.9 SLIMbus

The SOM supports SLIMbus HDMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

Table 5.9-1 SLIMbus

5.10 SDIO

The SOM Supports SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

Table 5.100-1 SDIO

5.11 I2S

The SOM I2S standards and exceptions:

- Legacy I2S interfaces for primary and secondary microphones and speakers.
- The multiple I2S (MI2S) interface for microphone and speaker functions.

It is supports both master and slave mode.
Supports 16, 24, or 32-bit resolution audio samples
Supports 8, 16, 32, 48, 96 and192 kHz sampling rate in Master mode, and all standard sample rates in Slave mode. Supports 16-bit and 24-bit data formats in standard I2S mode, and 24-bit left-justified (24-bit data in 32-bit frame left-justified, LSBs are padded with 0s).
Maximum clock frequency supported 12.288 MHz.
An additional pin can be used for a master clock, supplied by the MSM device, the master clock is often used

in the external devices to drive their oversampling logic. The LPASS clock controller can provide master clocks from independent clock dividers to the I2S bit-clock dividers.

Applicable standard	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996	None

Table 5.111-1 I2S

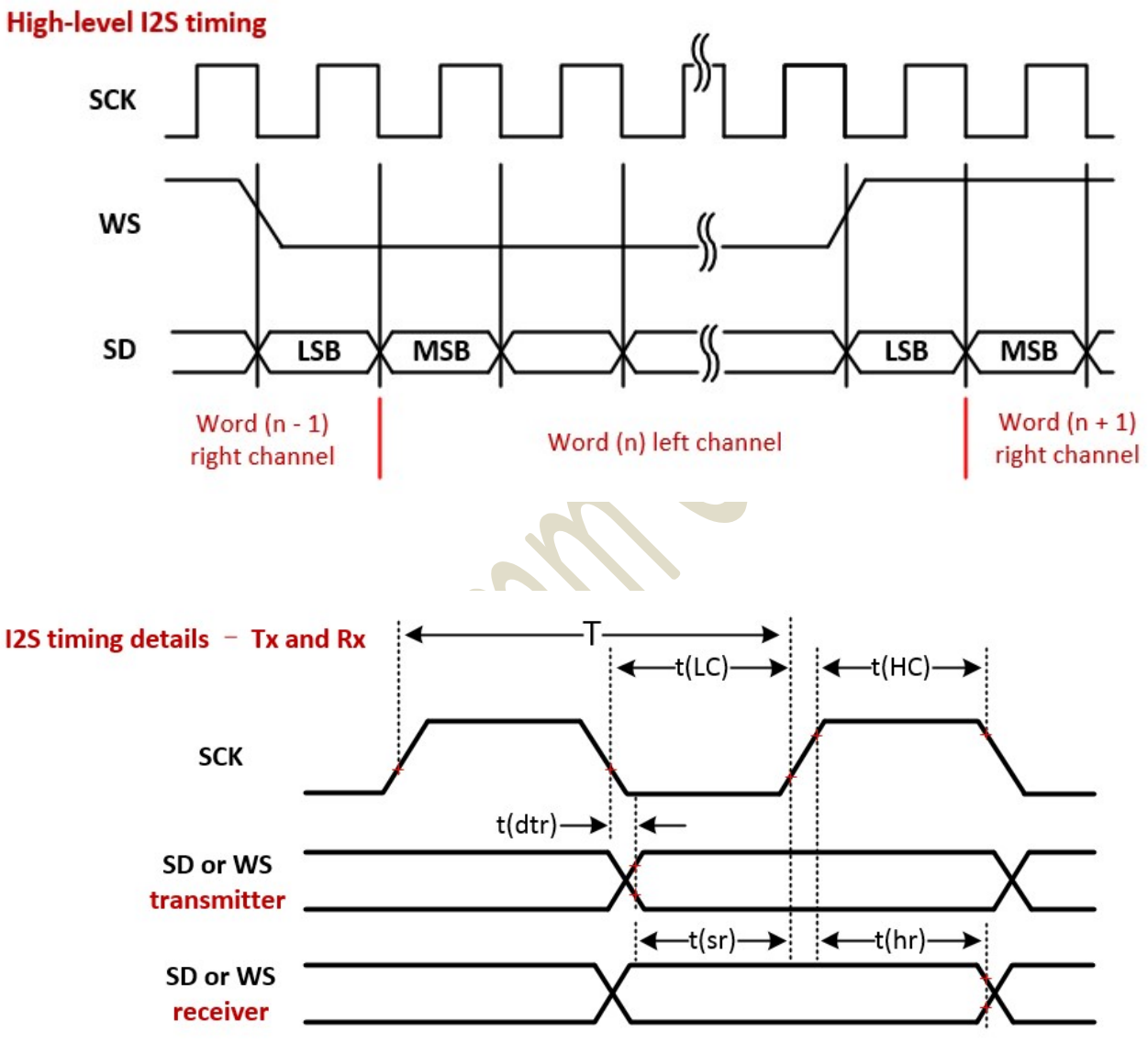


Figure 5.111-1 I2S timing diagram

The word-select signal is a 50% duty cycle signal. Data is delayed 1 bit-clock, relative to the word select. Data outputs are launched on the falling edge of the clock, and inputs data are captured on the rising edge of the clock by the receiver.

I2S samples are 2's complement values, and the MSB is transmitted first allowing the transmitter and

receiver to support different number of bits per sample.
The left channel is transmitted when the word select is low, and the right channel is transmitted when the word select is high

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
Using external SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns

Table 5.111-2 I2S Timing

5.12 I2C

The SOM I2C standards and exceptions:

Applicable standard	Feature exceptions
I2C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.

Table 5.122-1 I2C

5.13 SPI

The SOM supports **SPI** standards as a master only.

5.14 Fuel gauge

The fuel gauge module offers a hardware-based algorithm that is able to accurately estimate the Battery's state of charge by using current monitoring and voltage-based techniques. This hybrid approach ensures both excellent short-term linearity and long-term accuracy. Furthermore, neither full battery charge cycling, nor zero-current-load conditions, are required to maintain the accuracy.
The fuel gauge measures the battery pack temperature by sensing the voltage across an external thermistor. Missing battery detection is also incorporated to accurately monitor battery insertion and removal scenarios, while properly updating the state of charge when a battery is reconnected.
Using precise measurements of battery voltage, current, and temperature, the fuel gauging algorithm compensates for the variation in battery characteristics across temperature changes and aging effects. This provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions.

Function	Min	Type	Max	Units	Expected use
VBATT_CONN_VSENSE_P & VBATT_CONN_VSENSE_M, RSENSE_EXT_M & RSENSE_EXT_P					
ADC resolution			15	bits	***Voltage ADC***
			9	bits	***ID ADC***
			15	bits	***Current ADC***
ADC clock conversion frequency		200		kHz	

Table 5.144-1 Fuel Gauge

5.15 LED Current Driver

Red, green, and blue (RGB) drivers, which operate off a dedicated supply voltage, are available.

Function	Min	Type	Max	Units	Expected use
RGB_LED					
Current per channel (I out)			8	mA	
Dimming PWM frequency	0.1		18.75	KHZ	
Dimming Resolution	6		9	bit	

Table 5.155-1 LED current Driver

5.16 ADC

ADC performance specifications are listed in Table 5.166-1

Specification	Test condition	Min	Typ	Max	Units	Expected use
1/1 channel end-to-end accuracy	Calibrated data result	-11	±6	11	mV	
1/1 channel end-to-end accuracy with internal pull-up	Calibrated data result	-12.5	±7	12.5	mV	
1/3 channel end-to-end accuracy	Calibrated data result	-20	±10	20	mV	
ADC resolution (LSB)		-	114.441	-	μV	
ADC conversion time	1K decimation ratio, 4.8MHz sample clock	-	515	-	μs	
Current consumption	VADC active	-	450	500	μA	

Table 5.166-1 ADC

5.17 Power Consumption

Power Consumption				
S/N	Test Items and Test Condition		UNIT	DUT average value
1	**Normal Operation Current (Play Movie)** -Play mp4 4K -Loudspeaker	4K60	mA	335.9
		1080P		104
2	**Normal Operation Current (Camera mode)** - HDMI Output	Take photo	mA	357.5
		video	mA	408.2
3	**Normal Operation Current (Sleep Mode)** - No LCD. No camera	WIFI ON	mA	13.74
		WIFi OFF	mA	13.71
4	**Leakage current（SOM）**	-	mA	0.049

Table 5.177-1 Power Consumption

5.18 Thermal

This chart records thermal test data, to make sure the SOM working on highest performance, strong suggest make solution for heat sink. Table 5.188-1 describes SOM thermal test point.

Thermal Test Condition		
1	Test case	The test script of CPU + HDMI Out + WIFI/BT open + Play Game
2	HW Version	TurboX-845-SOM-V02,TurboX-845-IO-V02
3	Test points	CPU +LPDDR4x , UFS , PM845 , PMI8998 , PM8005
4	Ambient temperature	25℃

Table 5.188-1 Thermal Test

Thermal Test Result			
	Test Location	Temperature(Max)	△T
1	Environment Temperature	25	
2	UFS	34.6	9.6
3	PM845	38.6	13.6
4	DDR	33.9	8.9
5	PMI8998	35.5	10.5
6	WIFI	33.8	8.8
7	PCB	29.7	4.7

Figure 5.188-1 Thermal Data Heat Sink Design

5.19. Antenna Design Guideline（for reference）

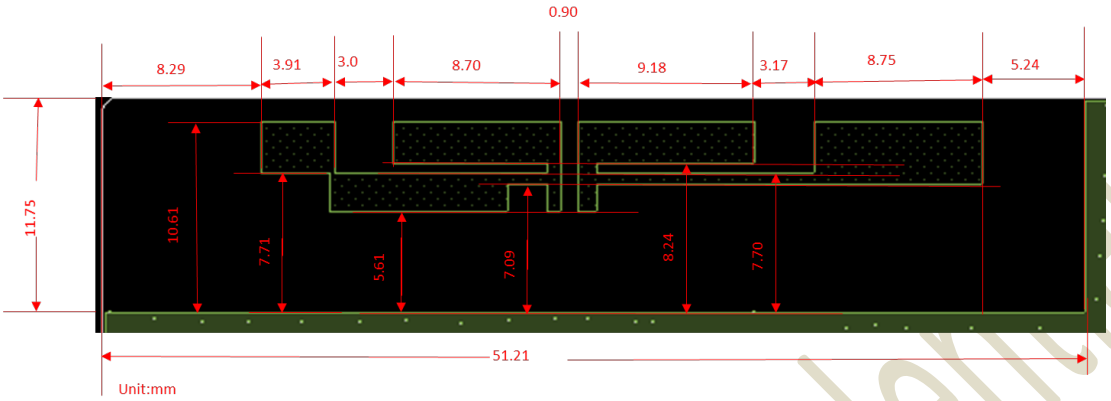


Figure 5.193-1 PCB Antenna Design Size

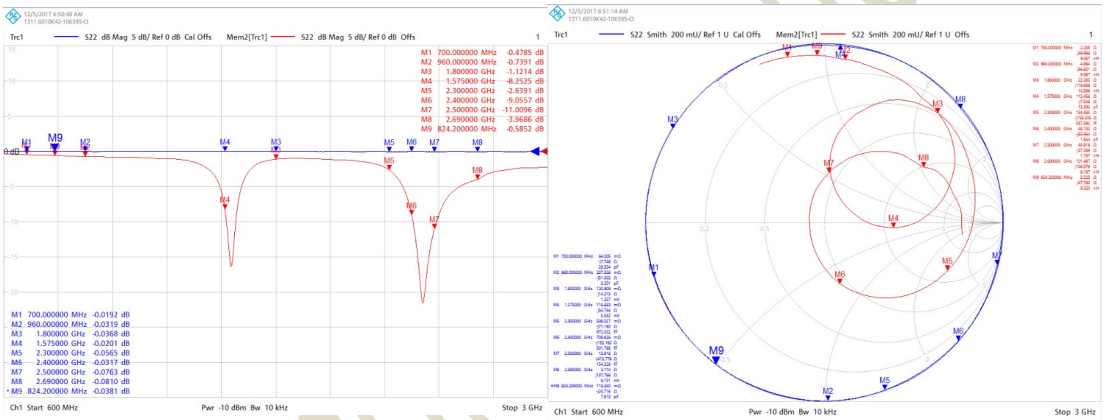
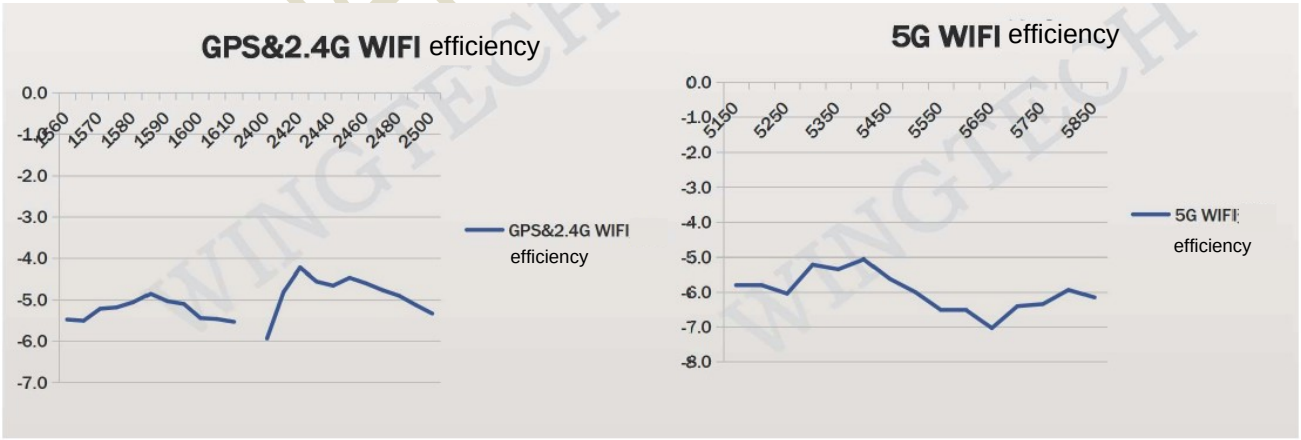


Figure 5.19-2 PCB Antenna Smith Chart



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FCC Caution:

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IMPORTANT NOTE:

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM

Manual v01

2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C&E has been investigated. It is applicable to the modular.

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

2.4 Limited module procedures

Not applicable

2.5 Trace antenna designs

See user manual section 5.19.

2.6 RF exposure considerations

To maintain compliance with FCC's RF Exposure guidelines, This equipment should be installed and operated with minimum distance of 20cm from your body.

2.7 Antennas

This radio transmitter FCC ID: 2AOHHTURBOXC845SOM has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Internal Identification	Antenna Description	Antenna type	Maximum antenna gain
Antenna 1	Bluetooth/Wi-Fi Antenna on I/O Board	PCB Antenna	Bluetooth/2.4G Wi-Fi: 2.8dBi, 5G Wi-Fi: 3.0dBi
Antenna 2	Wi-Fi Antenna on I/O Board	PCB Antenna	2.4G Wi-Fi: 2.8dBi, 5G Wi-Fi: 3.0dBi

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains FCC ID: 2AOHHTURBOXC845SOM"

2.9 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B