Thundercomm
AIOT ENABLER

Thundercomm TurboX C7230C SOM Datasheet

Smart Module

Rev. V0.1
Sep 15, 2023

Revision History

Version	Date	Description
V0.1	Sep 15, 2023	Preliminary draft.

Table List

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Chapter 1. Overview

TurboX C7230C SOM (System on Module) is a high-performance intelligent module, integrating Linux Android, based on Qualcomm QCS7230 processor. It also includes the advanced 7nm Fin FET process, a customized 64-bit Octa-core Qualcomm Kryo 585 application processor.

➲ **NOTE:** "TurboX" referred to herein is the English text of our registered trademark TURBOX.

C7230C SOM supports wide-range Wi-Fi, Wi-Fi 6 (Wi-Fi 802.11 a/b/g/n/ac/ax) and BT5.1. It supports one 4K@60FPS or two 4K@30FPS displays, as well as up to multi-camera concurrency. It also integrates multiple audio and video input/output interfaces. C7230C SOM provides a variety of GPIO, I2C, UART and SPI standard interfaces. In addition, it supports four 4-lane MIPI-CSIs (D-PHY) and one 3-trio MIPI-CSI (C-PHY) together with SOM common standard protocol interfaces such as USB3.1, PCIE2.1/3.0 and I2S.

C7230C SOM provides convenient and stable system solutions for IoT (Internet of Things) field. It can be embedded into devices including VR/AR, Robot, Smart Camera, AI devices, drones and medical devices.

The module uses LCC (Leadless Chip Carrier) packaging, which hides the pins beneath the chip, as opposed to traditional pin packaging. In the production process, SMT (Surface Mount Technology) is used to solder the module onto the mainboard.

During SMT soldering, the module is accurately placed on the designated location of the mainboard. The solder paste is melted by heating, allowing the pins of the module to connect with the solder pads on the mainboard. Depending on the design and manufacturing quality, SMT soldering should not significantly affect the RF (Radio Frequency) performance indicators.

Although the pins of the LCC package are hidden beneath the chip, their design usually takes into account the requirements for RF performance, aiming to minimize interference with signal transmission. Additionally, measures are taken in the module's design and layout to reduce interference or loss of RF signals.

Laser engraving the FCC ID on the shielding cover of the C7230C module effectively demonstrates its compliance with FCC regulations and its successful completion of relevant testing and certification. Such identification provides a credible proof of product compliance for users, regulatory authorities, and other stakeholders.

//TSR-End

1.1. Key features

Table 1-1. Key features and performance of QCS7230 and C7230C SOM

QCS7230	
Application processor	Kryo 585-64-bit application processor with a 4MB L3 cache • Quad high-performance Kryo Gold cores • Quad low-power Kryo Silver cores
Digital signal processing	• Compute Hexagon DSP with quad Hexagon Vector eXtensions (quad-HVX) and Hexagon Co-processor (Hexagon CP) 2.0 • Audio Hexagon DSP dedicated to audio subsystem • Sensor Hexagon DSP in the Qualcomm All-Ways Aware Hub to support always-on, low-power use cases • All Hexagon DSP are cache-based processors with full access to DDR
Graphics	• Adreno GPU 650 - 4K 60 fps UI or 2x 2k 60 fps UI • OpenGL ES 3.2, Vulkan 1.1, DX12 FL 12_1 • OpenCL 2.0 full profile
Display support	2 x 4-lane DSI D-PHY 1.2 and DisplayPort 1.4 data concurrency over USB. Maximum concurrency configurations: • 5040 × 2160 at 60 Hz 30bpp primary + 3840 × 2160 at 60 Hz 30bpp DisplayPort or 3840 × 2160 at 60 Hz 30bpp Wi-Fi display • 5040 × 2160 at 60Hz 30bpp primary + 7680 × 4320 at 30 Hz 24bpp DisplayPort

QCS7230	
	• 5040 × 2160 at 60Hz 30bpp primary + 2 × 3840 ×2160 at 60 Hz DisplayPort
Video encode	4K120/8K30 encode for H.265 Main 10, H.265 Main, H.264 High, and VP8 codecs
Video decode	4K240/8k30 decode for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, VP8, and MPEG-2 codecs
Camera support	• Qualcomm Spectra 480 Camera ISP • Support 6 x 4 Lane MIPI CSI • Real-time sensor input resolution: 25 + 25 + 2 + 2 + 2 + 2 + 2 MP • 64 MP 30 fps ZSL with a dual ISP
WLAN	2.4G/5G, support 802.11 a/b/g/n/ac/ax, 2 x 2 MIMO
Bluetooth	• Support Bluetooth 5.1 + HS • BLE
ADC Interface	• Support ADC interfaces • Used for input voltage sense, battery temperature detection and general-purpose ADC
C7230C SOM	
Processor	Snapdragon™ QCS7230
Memory [1)]	LPDDR5(POP) + UFS3.1, 8GB + 128GB
Connectivity	Wi-Fi/BT: QCA6391 (2x2 MIMO, 802.11 a/b/g/n/ac/ax & BT5.1)
Display interfaces	2 x MIPI-DSI 4-lane, 5040 x 2160@60fps
Camera interfaces	• 4x MIPI-CSI D-PHY, 4-lane, 2.5 Gbps per lane • Up to 25 MP sensors • 1x MIPI-CSI C-PHY, 3-trio, 10.26 Gbps/trio on three trios per port • Up to 64MP sensor
Audio interface	• SoundWire interface for smart speaker amplifier • 4x MI2S with two data lanes to support full duplex stereo • 3 DMIC ports supports up to 6 DMICs • 2x Analog MIC, comes from AUDIO CODEC, WCD9385
USB	2x USB 3.1 GEN2, one can support Type-C with DisplayPort
PCIe	1x 2-lane PCIe Gen3.0+1x 1-lane PCIe Gen3.0
Other Interfaces	• 2x RF connector for Wi-Fi /BT, 1 x UART, 1 x SDC for SD card • 12x 4pin QUPs (can be set as 4pin SPI or 2pin I2C) • Another 3x QUPs can be set as 2pin I2C • Another 2x QUPs can be set as 2pin UART • 4x camera dedicated I2Cs • 1x sensor dedicated I2C • 1x sensor dedicated I3C
Operating Environment	• Operation temperature: -25℃ ~ 75℃[2)] • Operation humidity: 5%~95%, non-condensing
Power supply	3.2V ~ 4.35V
Dimensions	36.5mm x 52mm x 4.55mm
RoHS	All hardware components are fully compliant with EU RoHS 2.0 directive.

[1)] Please note that storage devices such as UFS, eMMC, NAND, etc. have a limit to the total amount of data that can be written. Exceeding this limit can cause damage to the storage device.

[2)] To guarantee thermal dissipation, make sure that Tj (Junction Temperature) of processor does not exceed 95℃.

1.2. Hardware block diagram

NA

1.3. Major component location

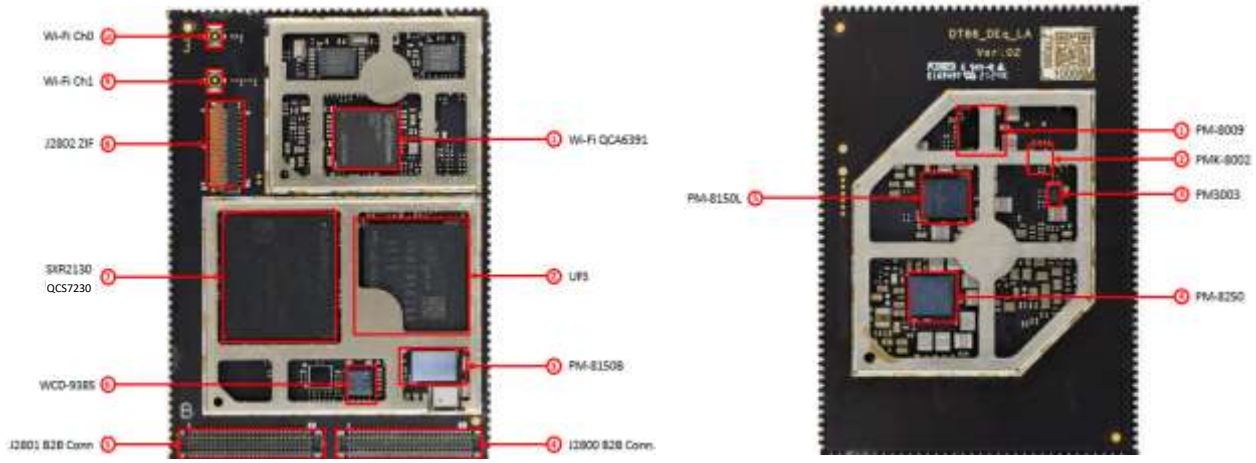

Figure 1-1.C7230C SOM Major Component Location

1.4. Mechanical size

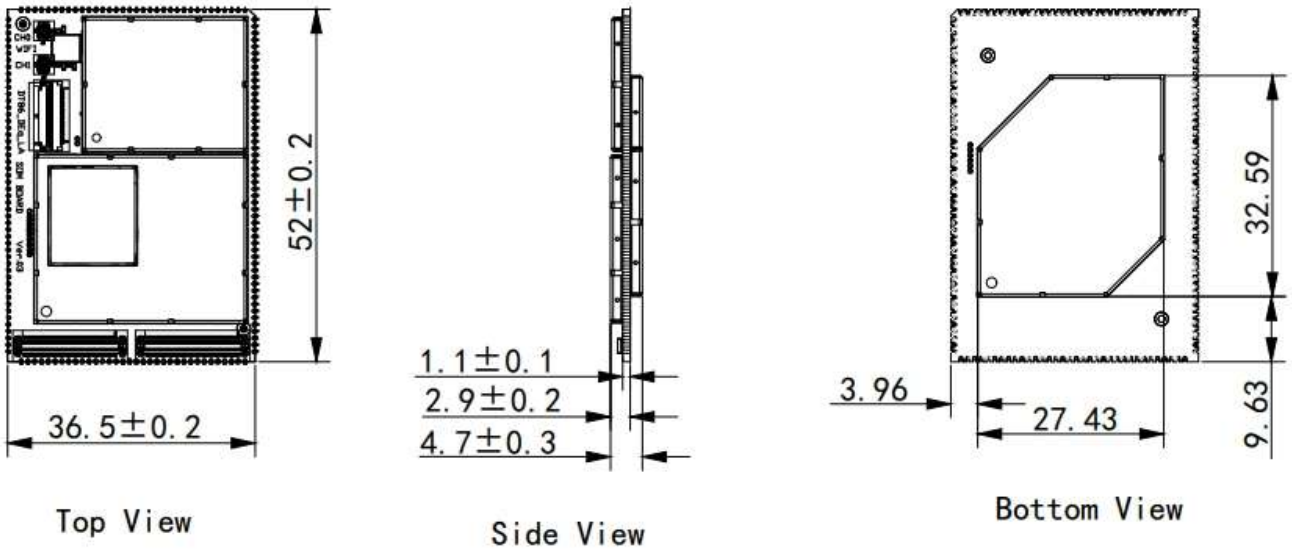

Figure 1-2.Mechanical Size

1.5. Package dimensions

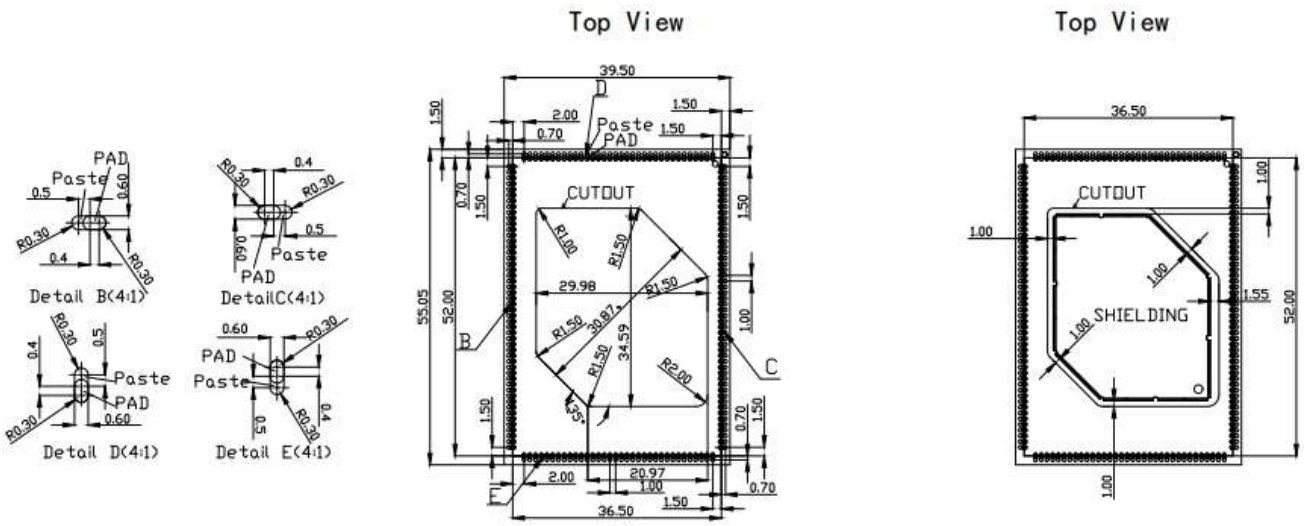

Figure 1-3.Package Dimensions

1.6. Stencil design and aperture

To supply sufficient soldering paste and keep reliable soldering joints, add the thickness of stencil partly on the top surface. The stencil aperture for single sheet cannot be greater than 3.0mm×4.0mm and the exceeded part should be divided into smaller apertures with applicable shelves. A clearance of over 2.0mm should be kept between the outward end of the aperture and the component if there are components around the module.

➲ **NOTES**:

- For the convenience of heating and repairing, it is recommended that no components should be placed in the area at the backside of the module on PCB.
- In order to avoid reverse polarity of the module, it is recommended to use asymmetric pads at the bottom of the module to identify the module polarity during module placement.
- It is not recommended to add any silkscreen in the area where the module is mounted to avoid the height that may influence the solder paste printing and soldering quality.
- When there is a need to step-up the stencil, all 01005/0201, 0.4mm-pitch and 0.5mm-pitch components should be kept over 5.0mm away from the stepped-up area to avoid solder bridging that is caused by thicker solder paste.

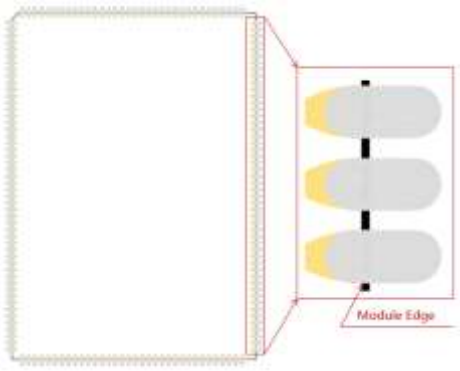

Figure 1-4.Stencil Aperture Diagram

Requirements on stencil aperture

- **Stencil thickness**

  Area of the module should be partly stepped-up to 0.15mm-0.18mm.
- **LCC pads on four sides**

  The surrounding edge of the stencil aperture for each LCC pad should be shifted outward by 0.20mm and the outermost edge should be shifted outward by 1.2mm at maximum while the width should be reduced at a ratio of 1:0.85 if necessary, and the stencil aperture should be designed in rectangle with round chamfers (as shown in Figure 1-5).

1.7. Module laser marking

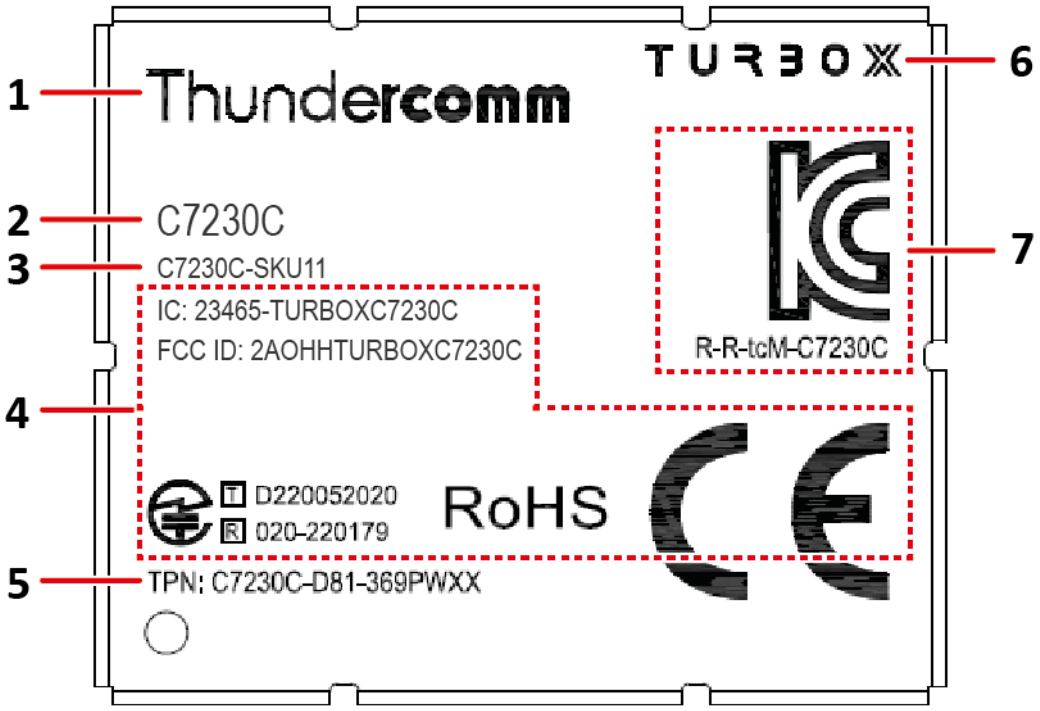

Figure 1-5.Example: C7230C

Table 1-2. SOM ID description

1. Thundercomm Logo	5. Part number
2. Production code	6. SOM brand
3. Hardware code	7. Certification information
4. Certification information	-

➲ **NOTES**:

- Figure 1-6 is for reference only and may vary with the specific module.
- The part number may be updated. Please confirm with the supplier about the accurate information.

1.8. SMT assembly guide

To reduce module trial cost and improve project implementation efficiency, it is **strongly recommended** to comprehend TurboX Common SMT Assembly Guidelines and TurboX LCC/LGA Module Carrier Board Design Guidelines for DFM before the early stage of module layout design.

Additionally, if necessary, you can contact us at service@thundercomm.com for assistance in review of PCBA placement design.

Chapter 2. Interface Description

This chapter introduces all the interfaces to guide developers to easily design and verify on C7230C SOM module.

2.1. Pin description

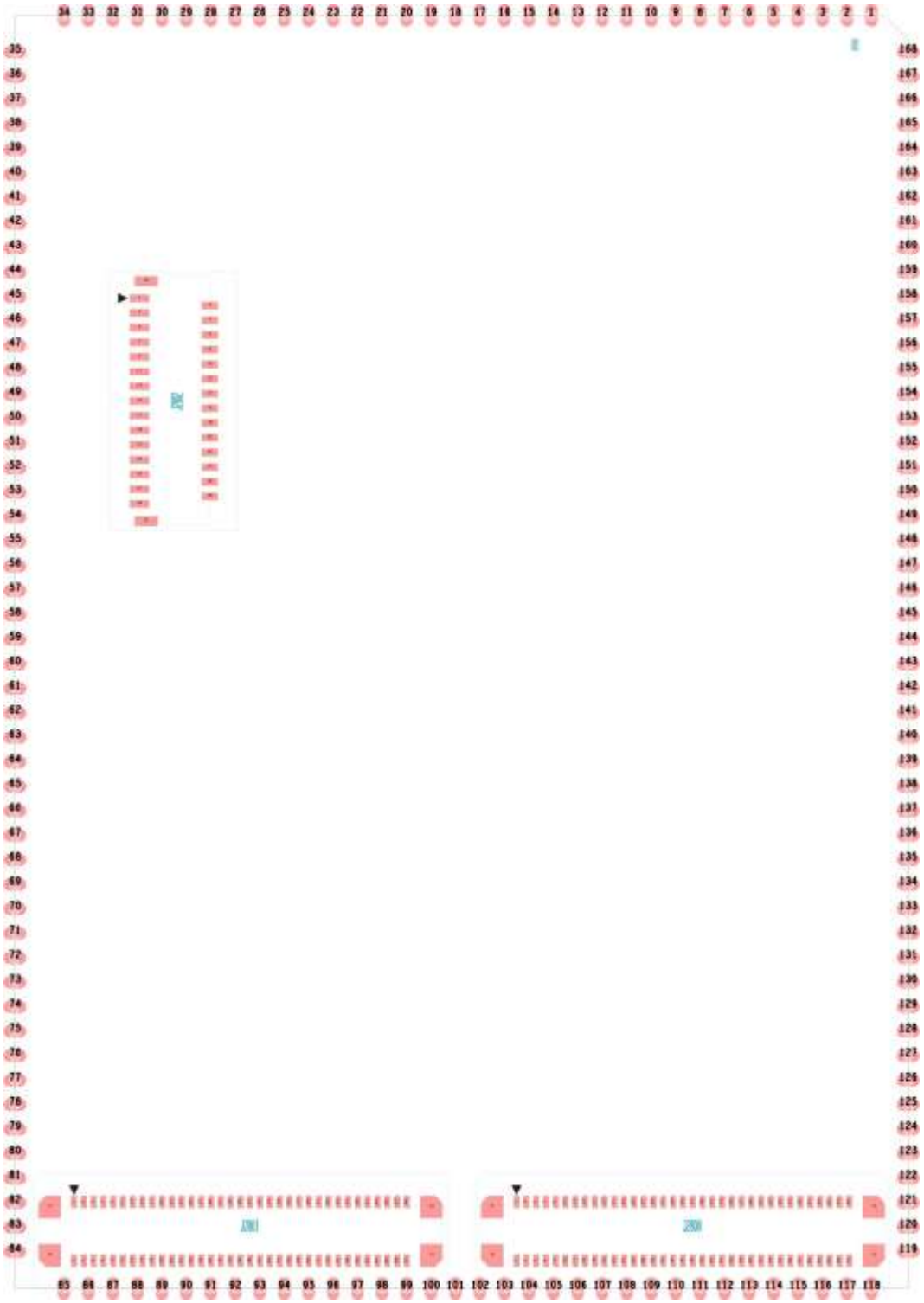

Figure 2-1.TurboX C7230C Pin Map

2.1.1. Pads

Table 2-1. Pin list

Pin#	Function	Description
1	GND	Grounding
2	VREG_L9C_2P96	LDO, 2.96V@600mA
3	SDC2_CLK_CONN	Secure digital controller 2 clock
4	SDC2_DATA_2	Secure digital controller 2 data bit 2
5	SDC2_DATA_3	Secure digital controller 2 data bit 3
6	SDC2_CMD	Secure digital controller 2 command
7	SDC2_DATA_0	Secure digital controller 2 data bit 0
8	SDC2_DATA_1	Secure digital controller 2 data bit 1
9	GND	Grounding
10	CAM_MCLK0	Camera master clock 0
11	CSI0_NC_CLK_P	MIPI CSI 0 (DPHY), differential clock – plus
12	CSI0_A0_CLK_M	MIPI CSI 0 (DPHY), differential clock – minus
13	CSI0_B0_LN0_P	MIPI CSI 0 (DPHY), differential lane 0 – plus
14	CSI0_C0_LN0_M	MIPI CSI 0 (DPHY), differential lane 0 – minus
15	CSI0_A1_LN1_P	MIPI CSI 0 (DPHY), differential lane 1 – plus
16	CSI0_B1_LN1_M	MIPI CSI 0 (DPHY), differential lane 1 – minus
17	CSI0_C1_LN2_P	MIPI CSI 0 (DPHY), differential lane 2 – plus
18	CSI0_A2_LN2_M	MIPI CSI 0 (DPHY), differential lane 2 – minus
19	CSI0_B2_LN3_P	MIPI CSI 0 (DPHY), differential lane 3 – plus
20	CSI0_C2_LN3_M	MIPI CSI 0 (DPHY), differential lane 3 – minus
21	GND	Grounding
22	CAM_MCLK2	Camera master clock 2
23	CSI2_C2_LN3_M	MIPI CSI 2 (DPHY), differential lane 3 – minus
24	CSI2_B2_LN3_P	MIPI CSI 2 (DPHY), differential lane 3 – plus
25	CSI2_A2_LN2_M	MIPI CSI 2 (DPHY), differential lane 2 – minus
26	CSI2_C1_LN2_P	MIPI CSI 2 (DPHY), differential lane 2 – plus
27	CSI2_B1_LN1_M	MIPI CSI 2 (DPHY), differential lane 1 – minus
28	CSI2_A1_LN1_P	MIPI CSI 2 (DPHY), differential lane 1 – plus
29	CSI2_C0_LN0_M	MIPI CSI 2 (DPHY), differential lane 0 – minus
30	CSI2_B0_LN0_P	MIPI CSI 2 (DPHY), differential lane 0 – plus
31	CSI2_A0_CLK_M	MIPI CSI 2 (DPHY), differential clock – minus
32	CSI2_NC_CLK_P	MIPI CSI 2 (DPHY), differential clock – plus
33	FLASH_LED1	Flash high-side current source for LED1
34	VREG_L7F_1P8	LDO, 1.8V@600mA
35	FLASH_LED2	Flash high-side current source for LED2
36	GND	Grounding
37	CAM_MCLK4	Camera master clock 4
38	CSI4_C2_LN3_M	MIPI CSI 4 (DPHY), differential lane 3 – minus

Pin#	Function	Description
39	CSI4_B2_LN3_P	MIPI CSI 4 (DPHY), differential lane 3 – plus
40	CSI4_A2_LN2_M	MIPI CSI 4 (DPHY), differential lane 2 – minus
41	CSI4_C1_LN2_P	MIPI CSI 4 (DPHY), differential lane 2 – plus
42	CSI4_C0_LN0_M	MIPI CSI 4 (DPHY), differential lane 0 – minus
43	CSI4_B0_LN0_P	MIPI CSI 4 (DPHY), differential lane 0 – plus
44	CSI4_A0_CLK_M	MIPI CSI 4 (DPHY), differential clock – minus
45	CSI4_NC_CLK_P	MIPI CSI 4 (DPHY), differential clock – plus
46	CSI4_B1_LN1_M	MIPI CSI 4 (DPHY), differential lane 1 – minus
47	CSI4_A1_LN1_P	MIPI CSI 4 (DPHY), differential lane 1 – plus
48	GND	Grounding
49	CSI3_C0_LN0_M	MIPI CSI 3 (DPHY), differential lane 0 – minus
50	CSI3_B0_LN0_P	MIPI CSI 3 (DPHY), differential lane 0 – plus
51	CSI3_A0_CLK_M	MIPI CSI 3 (DPHY), differential clock – minus
52	CSI3_NC_CLK_P	MIPI CSI 3 (DPHY), differential clock – plus
53	CSI3_C2_LN3_M	MIPI CSI 3 (DPHY), differential lane 3 – minus
54	CSI3_B2_LN3_P	MIPI CSI 3 (DPHY), differential lane 3 – plus
55	CSI3_A2_LN2_M	MIPI CSI 3 (DPHY), differential lane 2 – minus
56	CSI3_C1_LN2_P	MIPI CSI 3 (DPHY), differential lane 2 – plus
57	CSI3_B1_LN1_M	MIPI CSI 3 (DPHY), differential lane 1 – minus
58	CSI3_A1_LN1_P	MIPI CSI 3 (DPHY), differential lane 1 – plus
59	CAM_MCLK3	Camera master clock 3
60	GND	Grounding
61	DSI1_A2_LN2_P	MIPI DSI 1 (DPHY), differential lane 2 – plus
62	DSI1_B2_LN2_M	MIPI DSI 1 (DPHY), differential lane 2 – minus
63	DSI1_B1_CLK_P	MIPI DSI 1 (DPHY), differential clock – plus
64	DSI1_C1_CLK_M	MIPI DSI 1 (DPHY), differential clock – minus
65	DSI1_A0_LN0_P	MIPI DSI 1 (DPHY), differential lane 0 – plus
66	DSI1_B0_LN0_M	MIPI DSI 1 (DPHY), differential lane 0 – minus
67	DSI1_C0_LN1_P	MIPI DSI 1 (DPHY), differential lane 1 – plus
68	DSI1_A1_LN1_M	MIPI DSI 1 (DPHY), differential lane 1 – minus
69	DSI1_C2_LN3_P	MIPI DSI 1 (DPHY), differential lane 3 – plus
70	DSI1_NC_LN3_M	MIPI DSI 1 (DPHY), differential lane 3 – minus
71	GND	Grounding
72	DSI0_A0_LN0_P	MIPI DSI 0 (DPHY), differential lane 0 – plus
73	DSI0_B0_LN0_M	MIPI DSI 0 (DPHY), differential lane 0 – minus
74	DSI0_B1_CLK_P	MIPI DSI 0 (DPHY), differential clock – plus
75	DSI0_C1_CLK_M	MIPI DSI 0 (DPHY), differential clock – minus
76	DSI0_C0_LN1_P	MIPI DSI 0 (DPHY), differential lane 1 – plus
77	DSI0_A1_LN1_M	MIPI DSI 0 (DPHY), differential lane 1 – minus
78	DSI0_A2_LN2_P	MIPI DSI 0 (DPHY), differential lane 2 – plus
79	DSI0_B2_LN2_M	MIPI DSI 0 (DPHY), differential lane 2 – minus

Pin#	Function	Description
80	DSI0_C2_LN3_P	MIPI DSI 0 (DPHY), differential lane 3 – plus
81	DSI0_NC_LN3_M	MIPI DSI 0 (DPHY), differential lane 3 – minus
82	GND	Grounding
83	SDM_DEBUG_UART_TX	Uart TX for system debug
84	SDM_DEBUG_UART_RX	Uart RX for system debug
85	PHONE_ON_N	Power on
86	SDM_FORCE_USB_BOOT	Force USB boot
87	USB1_HS_DM	USB1 high-speed data – minus
88	USB1_HS_DP	USB1 high-speed data – plus
89	USB1_SS_TX_M	USB1 super-speed transmit – minus
90	USB1_SS_TX_P	USB1 super-speed transmit – plus
91	GND	Grounding
92	USB1_SS_RX_M	USB1 super-speed receive – minus
93	USB1_SS_RX_P	USB1 super-speed receive– plus
94	GND	Grounding
95	PCIE2_TX0_P	PCIe 2 Gen 3 transmit 0 – plus
96	PCIE2_TX0_M	PCIe 2 Gen 3 transmit 0 – minus
97	PCIE2_RX0_M	PCIe 2 Gen 3 receive 0 – minus
98	PCIE2_RX0_P	PCIe 2 Gen 3 receive 0 – plus
99	PCIE2_REFCLK_M	PCIe 2 Gen 3 reference clock minus
100	PCIE2_REFCLK_P	PCIe 2 Gen 3 reference clock – plus
101	GND	Grounding
102	USB0_SS_RX1_P	USB0 super-speed receive 1 – plus
103	USB0_SS_RX1_M	USB0 super-speed receive 1 – minus
104	USB0_SS_RX0_M	USB0 super-speed receive 0 – minus
105	USB0_SS_RX0_P	USB0 super-speed receive 0 – plus
106	GND	Grounding
107	USB0_SS_TX0_P	USB0 super-speed transmit 0 – plus
108	USB0_SS_TX0_M	USB0 super-speed transmit 0 – minus
109	USB0_SS_TX1_M	USB0 super-speed transmit 1 – minus
110	USB0_SS_TX1_P	USB0 super-speed transmit 1 – plus
111	GND	Grounding
112	USB0_CC2	CC2 of Type C, USB0
113	USB0_CC1	CC1 of Type C, USB0
114	USB0_SBU1	SBU1 of Type C, USB0
115	USB0_SBU2	SBU1 of Type C, USB0
116	GND	Grounding
117	USB0_HS_DP_CONN	USB0 high-speed data – plus
118	USB0_HS_DM_CONN	USB0 high-speed data – minus
119	GND	Grounding
120	GND	Grounding

Pin#	Function	Description
121	VBAT	VBAT
122	VBAT	VBAT
123	VBAT	VBAT
124	VBAT	VBAT
125	GND	Grounding
126	GND	Grounding
127	USB_IN_MID	Mid point of the charger
128	USB_IN_MID	Mid point of the charger
129	USB_IN_MID	Mid point of the charger
130	GND	Grounding
131	USB_VBUS	VBUS
132	USB_VBUS	VBUS
133	USB_VBUS	VBUS
134	USB_VBUS	VBUS
135	GND	Grounding
136	VPH_PWR	Vsystem. Power supply for function module
137	VPH_PWR	Vsystem. Power supply for function module
138	VPH_PWR	Vsystem. Power supply for function module
139	VPH_PWR	Vsystem. Power supply for function module
140	VBATT_CONN_VSENSE_M	Battery current sense negative
141	VBATT_CONN_VSENSE_P	Battery current sense positive
142	ISNS_SMB_P	Current sense plus from external parallel charger
143	ISNS_SMB_M	Current sense minus from external parallel charger
144	VREG_S4A_1P8	S4 SMPS 1.8V output
145	VREG_BOB	Regulated BOB output
146	GND	Grounding
147	PCIE1_TX0_M	PCIe 1 Gen 3 transmit 0 – minus
148	PCIE1_TX0_P	PCIe 1 Gen 3 transmit 0 – plus
149	PCIE1_TX1_M	PCIe 1 Gen 3 transmit 1 – minus
150	PCIE1_TX1_P	PCIe 1 Gen 3 transmit 1 – plus
151	PCIE1_REFCLK_M	PCIe 1 Gen 3 reference clock minus
152	PCIE1_REFCLK_P	PCIe 1 Gen 3 reference clock – plus
153	PCIE1_RX1_M	PCIe 1 Gen 3 receive 1 – minus
154	PCIE1_RX1_P	PCIe 1 Gen 3 receive 1 – plus
155	PCIE1_RX0_P	PCIe 1 Gen 3 receive 0 – minus
156	PCIE1_RX0_M	PCIe 1 Gen 3 receive 0 – plus
157	GND	Grounding
158	CAM_MCLK1	Camera master clock 1
159	CSI1_C2_LN3_M	MIPI CSI 1 (DPHY), differential lane 3 – minus
160	CSI1_B2_LN3_P	MIPI CSI 1 (DPHY), differential lane 3 – plus
161	CSI1_A2_LN2_M	MIPI CSI 1 (DPHY), differential lane 2 – minus

Pin#	Function	Description
162	CSI1_C1_LN2_P	MIPI CSI 1 (DPHY), differential lane 2 – plus
163	CSI1_B1_LN1_M	MIPI CSI 1 (DPHY), differential lane 1 – minus
164	CSI1_A1_LN1_P	MIPI CSI 1 (DPHY), differential lane 1 – plus
165	CSI1_C0_LN0_M	MIPI CSI 1 (DPHY), differential lane 0 – minus
166	CSI1_B0_LN0_P	MIPI CSI 1 (DPHY), differential lane 0 – plus
167	CSI1_A0_CLK_M	MIPI CSI 1 (DPHY), differential clock – minus
168	CSI1_NC_CLK_P	MIPI CSI 1 (DPHY), differential clock – plus

2.1.2. BTB connectors

Table 2-2. J2800 pin list

J2800			
Pin	**Signal name**	**Pin**	**Signal name**
1	CON_AMICR_M CON_AMICL_M	2	GPIO_126
3	CON_AMICR_P	4	GPIO_22
5	CON_AMICL_P	6	GPIO_9
7	KYPD_VOLP_N	8	GPIO_23
9	GND	10	SEN1_GYRO_INT2
11	PM_RESIN_N	12	SEN1_ACCL_INT1
13	CBL_PWR_N	14	SNS_I2C4_SDA
15	PM8150L_GPIO_6	16	SNS_I2C4_SCL
17	PM8150L_GPIO_10	18	GPIO_141
19	PM8150L_GPIO_7	20	GPIO_135
21	USB_CONN_THERM	22	GND
23	BATT_ID	24	GPIO_137
25	BATT_THERM	26	GPIO_136
27	SMB_THERM	28	GPIO_134
29	VBATT_PACK_SNS_M	30	GPIO_133
31	GND	32	GPIO_4
33	SMB_EN_CHG	34	GPIO_5
35	SMB_STAT	36	GPIO_28
37	DC_IN_PON	38	GPIO_8
39	DC_IN_EN	40	GPIO_121
41	SNS_I3C0_SCL	42	GPIO_122
43	SNS_I3C0_SDA	44	GND
45	GPIO_140	46	GPIO_123
47	GPIO_138	48	CAM0_RST_N
49	GPIO_139	50	CAM1_RST_N
51	SPI2_MISO_IMU	52	CAM3_RST_N
53	SPI2_CLK_IMU	54	CCI_I2C_SCL3
55	SPI2_CS_IMU	56	CCI_I2C_SDA3

J2800			
Pin	**Signal name**	**Pin**	**Signal name**
57	GND	58	CCI_I2C_SCL2
59	SPI2_MOSI_IMU	60	CCI_I2C_SDA2
61	PCIE1_RST_N	62	CCI_I2C_SCL1
63	PCIE1_CLK_REQ_N	64	CCI_I2C_SDA1
65	PCIE1_WAKE_N	66	CCI_I2C_SCL0
67	DC_IN_PSNS	68	CCI_I2C_SDA0
69	PM8150L_GPIO_5	70	GND

Table 2-3. J2801 pin list

J2801			
Pin	**Signal name**	**Pin**	**Signal name**
1	SD_UFS_CARD_DET_N	2	GPIO_10
3	CAM2_RST_N	4	GPIO_11
5	GPIO_40	6	GPIO_26
7	DISP0_RESET_N	8	GPIO_62
9	GND	10	SDM_FAST_BOOT_1
11	GPIO_7	12	GPIO_88
13	GPIO_31	14	GPIO_89
15	GPIO_6	16	GPIO_100
17	GPIO_30	18	GPIO_119
19	GPIO_29	20	GPIO_120
21	GPIO_43	22	GND
23	GPIO_59	24	CAM_MCLK5
25	GPIO_58	26	GPIO_42
27	GPIO_57	28	GPIO_41
29	GPIO_56	30	GPIO_37
31	GND	32	GPIO_36
33	GPIO_52	34	GPIO_49
35	GPIO_55	36	GPIO_48
37	GPIO_53	38	GPIO_125
39	GPIO_54	40	SDM_RESOUT_N
41	GPIO_2	42	GPIO_25

J2801			
Pin	**Signal name**	**Pin**	**Signal name**
43	GPIO_3	44	GND
45	PCIE2_WAKE_N	46	GPIO_24
47	PCIE2_RST_N	48	APPS_I2C_SCL
49	PCIE2_CLK_REQ_N	50	APPS_I2C_SDA
51	GPIO_1	52	GPIO_127
53	GPIO_39	54	WSA_SWR_CLK
55	GPIO_51	56	WSA_SWR_DATA
57	GND	58	DMIC45_DATA
59	GPIO_38	60	DMIC45_CLK
61	GPIO_50	62	DMIC23_DATA
63	GPIO_0	64	DMIC23_CLK
65	GPIO_130	66	DMIC01_DATA
67	GPIO_129	68	DMIC01_CLK
69	SDM_FAST_BOOT_0	70	GND

Table 2-4. J2802 pin list

J2802	
Pin	**Signal name**
1	GND
2	GPIO_12
3	GPIO_13
4	GPIO_14
5	GPIO_15
6	GPIO_46
7	B_LED
8	G_LED
9	R_LED
10	LAA_TXEN_GPIO [1] (To SDR865 GRFC2 Pull Down with 10K when unused)
11	GPIO_64
12	GPIO_66
13	GPIO_67
14	GPIO_68

J2802	
Pin	**Signal name**
15	GND
16	GPIO_60
17	GPIO_61
18	PM8250_GPIO1
19	GPIO_110
20	GPIO_111
21	CTRL_PA_MULT [1] (To X55 GPIO_41 PD with 10K when unused)
22	CTRL_LAA_RX [1] (To X55 GPIO_26 PD with 10K when unused)
23	WLAN_COEX_MDMUART_TX [1] (To X55 GPIO_44 PD with 10K when unused)
24	WLAN_COEX_MDMUART_RX [1] (To X55 GPIO_45 PD with 10K when unused)
25	LAA_AS_EN [1] (To X55 GPIO_40 PD with 10K when unused)
26	WL_TXEN_GPIO [1] (To 5G RFFE Pull Down with 10K when unused)
27	PM8150L_GPIO_3
28	PM8150L_GPIO_4
29	GND

[1] indicates QCA6391 Wi-Fi module control signals used for radio frequency coexistence control.

2.2. Interfaces parameter definitions

Table 2-5. Interfaces parameter definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O
DI	Digital input (CMOS)
DSI	Supply voltage for MIPI_CSI circuits and I/O
DO	Digital output (CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: • NP: pdpukp = default no-pull with programmable options following the colon (:) • PD: nppukp = default pull-down with programmable options following the colon (:) • PU: nppdkp = default pull-up with programmable options following the colon (:) • KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3, 1.8V
P2	SDC Power group 2, 1.8V or 2.95V

2.3. Interfaces detail description

2.3.1. Power supply interfaces

Table 2-2 describes all interfaces of SOM Power Supply. For detailed parameter request, refer to Chapter 3. Electrical Characteristics.

Table 2-6. Power supply definition

PIN name	Conn.	PIN location	Type	Description
VBAT	Pad	121,122,123,124	PI	Power supply for SOM
USB_VBUS	Pad	131,132,133,134	PO	USB output during USB-OTG operation.
USB_IN_MID	Pad	127,128,129	PO	Mid point of the charger; input for charger buck
VREG_L9C_2P96	Pad	2	PO	LDO, 2.96V@600mA
VREG_L7F_1P8	Pad	34	PO	LDO, 1.8V@600mA
VREG_S4A_1P8	Pad	144	PO	BUCK, 1.8V 1000mA
VREG_BOB	Pad	145	PO	Buck-boost output, 3.0V to 3.8V 1000mA
GND	-	Pads:1,9,21,36,48,60,71,82,91,94,101,106, 111,116,119,120,125,126,130,135,146,157 J2800: 9,22,31,44,57,70 J2801: 9,22,31,44,57,70 J2802: 1.15,29	GND	GND

2.3.2. Display interfaces

C7230C SOM supports dual 4-lane MIPI_DSI interfaces, 60fps, 5040 x 2160.

Table 2-7. Display interface definition

PIN name	Location	PIN	Voltage	Type	Description
DSI0_A0_LN0_P	Pad	72	DSI	AO	MIPI0 signals for MIPI LCM, compliant with MIPI Alliance Specification for Display Serial Interface.
DSI0_B0_LN0_M	Pad	73	DSI	AO	
DSI0_C0_LN1_P	Pad	76	DSI	AO	
DSI0_A1_LN1_M	Pad	77	DSI	AO	
DSI0_B1_CLK_P	Pad	74	DSI	AO	
DSI0_C1_CLK_M	Pad	75	DSI	AO	
DSI0_A2_LN2_P	Pad	78	DSI	AO	
DSI0_B2_LN2_M	Pad	79	DSI	AO	
DSI0_C2_LN3_P	Pad	80	DSI	AO	
DSI0_NC_LN3_M	Pad	81	DSI	AO	
DSI1_A0_LN0_P	Pad	65	DSI	AO	MIPI1 signals for MIPI LCM, compliant with MIPI Alliance Specification for Display Serial Interface.
DSI1_B0_LN0_M	Pad	66	DSI	AO	
DSI1_C0_LN1_P	Pad	67	DSI	AO	
DSI1_A1_LN1_M	Pad	68	DSI	AO	
DSI1_B1_CLK_P	Pad	63	DSI	AO	
DSI1_C1_CLK_M	Pad	64	DSI	AO	
DSI1_A2_LN2_P	Pad	61	DSI	AO	
DSI1_B2_LN2_M	Pad	62	DSI	AO	
DSI1_C2_LN3_P	Pad	69	DSI	AO	
DSI1_NC_LN3_M	Pad	70	DSI	AO	

2.3.3. Camera interfaces

C7230C SOM supports 5 x 4-lane camera interfaces.

Table 2-8. Camera interface definition

Camera0 interfaces					
PIN name	**Location**	**PIN**	**Voltage**	**Type**	**Description**
CCI_I2C_SDA0	J2800	68	P3	OD	CCI0 Date signal, already pulled up on SOM
CCI_I2C_SCL0	J2800	66	P3	OD	CCI0 Clock signal, already pulled up on SOM
CAM_MCLK0	Pad	10	P3	DO	Camera main clock output
CSI0_NC_CLK_P	Pad	11	CSI	AI	MIPI Signals of Camera0, compliant with MIPI Alliance Standard Specification.
CSI0_A0_CLK_M	Pad	12	CSI	AI	
CSI0_B0_LN0_P	Pad	13	CSI	AI	
CSI0_C0_LN0_M	Pad	14	CSI	AI	
CSI0_A1_LN1_P	Pad	15	CSI	AI	
CSI0_B1_LN1_M	Pad	16	CSI	AI	
CSI0_C1_LN2_P	Pad	17	CSI	AI	
CSI0_A2_LN2_M	Pad	18	CSI	AI	
CSI0_B2_LN3_P	Pad	19	CSI	AI	
CSI0_C2_LN3_M	Pad	20	CSI	AI	
Camera1 interfaces					
PIN name	**Location**	**PIN**	**Voltage**	**Type**	**Description**
CCI_I2C_SDA1	J2800	64	P3	OD	CCI1 Date signal, already pulled up on SOM
CCI_I2C_SCL1	J2800	62	P3	OD	CCI1 Clock signal, already pulled up on SOM
CAM_MCLK1	Pad	158	P3	DO	Camera main clock output
CSI1_NC_CLK_P	Pad	168	CSI	AI	MIPI Signals of Camera1, compliant with MIPI Alliance Standard Specification.
CSI1_A0_CLK_M	Pad	167	CSI	AI	
CSI1_B0_LN0_P	Pad	166	CSI	AI	
CSI1_C0_LN0_M	Pad	165	CSI	AI	
CSI1_A1_LN1_P	Pad	164	CSI	AI	
CSI1_B1_LN1_M	Pad	163	CSI	AI	
CSI1_C1_LN2_P	Pad	162	CSI	AI	
CSI1_A2_LN2_M	Pad	161	CSI	AI	
CSI1_B2_LN3_P	Pad	160	CSI	AI	
CSI1_C2_LN3_M	Pad	159	CSI	AI	

Camera2 interfaces					
PIN name	**Location**	**PIN**	**Voltage**	**Type**	**Description**
CCI_I2C_SDA2	J2800	60	P3	OD	CCI2 Date signal, already pulled up on SOM
CCI_I2C_SCL2	J2800	58	P3	OD	CCI2 Clock signal, already pulled up on SOM
CAM_MCLK2	Pad	22	P3	DO	Camera main clock output
CSI2_NC_CLK_P	Pad	32	CSI	AI	MIPI Signals of Camera2 Compliant with MIPI Alliance Standard Specification
CSI2_A0_CLK_M	Pad	31	CSI	AI	
CSI2_B0_LN0_P	Pad	30	CSI	AI	
CSI2_C0_LN0_M	Pad	29	CSI	AI	
CSI2_A1_LN1_P	Pad	28	CSI	AI	
CSI2_B1_LN1_M	Pad	27	CSI	AI	
CSI2_C1_LN2_P	Pad	26	CSI	AI	
CSI2_A2_LN2_M	Pad	25	CSI	AI	
CSI2_B2_LN3_P	Pad	24	CSI	AI	
CSI2_C2_LN3_M	Pad	23	CSI	AI	
Camera3 interfaces					
PIN name	**Location**	**PIN**	**Voltage**	**Type**	**Description**
CCI_I2C_SDA3	J2800	56	P3	OD	CCI3 Date signal, already pulled up on SOM
CCI_I2C_SCL3	J2800	54	P3	OD	CCI3 Clock signal, already pulled up on SOM
CSI3_NC_CLK_P	Pad	52	CSI	AI	MIPI Signals of Camera3, compliant with MIPI Alliance Standard Specification.
CSI3_A0_CLK_M	Pad	51	CSI	AI	
CSI3_B0_LN0_P	Pad	50	CSI	AI	
CSI3_C0_LN0_M	Pad	49	CSI	AI	
CSI3_A1_LN1_P	Pad	58	CSI	AI	
CSI3_B1_LN1_M	Pad	57	CSI	AI	
CSI3_C1_LN2_P	Pad	56	CSI	AI	
CSI3_A2_LN2_M	Pad	55	CSI	AI	
CSI3_B2_LN3_P	Pad	54	CSI	AI	
CSI3_C2_LN3_M	Pad	53	CSI	AI	
CAM_MCLK3	Pad	59	P3	DO	Camera main clock output

Camera4 interfaces					
PIN name	Location	PIN	Voltage	Type	Description
CSI4_NC_CLK_P	Pad	45	CSI	AI	MIPI Signals of Camera4, compliant with MIPI Alliance Standard Specification.
CSI4_A0_CLK_M	Pad	44	CSI	AI	
CSI4_B0_LN0_P	Pad	43	CSI	AI	
CSI4_C0_LN0_M	Pad	42	CSI	AI	
CSI4_A1_LN1_P	Pad	47	CSI	AI	
CSI4_B1_LN1_M	Pad	46	CSI	AI	
CSI4_C1_LN2_P	Pad	41	CSI	AI	
CSI4_A2_LN2_M	Pad	40	CSI	AI	
CSI4_B2_LN3_P	Pad	39	CSI	AI	
CSI4_C2_LN3_M	Pad	38	CSI	AI	
CAM_MCLK4	Pad	37	P3	DO	Camera main clock output

2.3.4. Audio interfaces

C7230C SOM provides Soundwire, DMIC, AMIC, MI2S and analog audio via USB for audio.

- Soundwire interface is dedicate for QUALCOMM speaker amplifier, WSA serial IC.
- DMIC interface can be used to directly connect up to 6 PDM MICs.
- An Audio Codec IC is also embedded in SOM to provide analog MIC I/F on B2B connector and analog audio I/F via USB interface.
- MI2S I/Fs are also available on SOM pads.

Table 2-9. Audio interface definition

Audio Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Alt Function
WSA_SWR_DATA	J2801	56	P3	IO	AUDIO PA Soundwire	LPI_MI2S2_WS
WSA_SWR_CLK	J2801	54	P3	IO		LPI_MI2S2_CLK
DMIC01_CLK	J2801	68	P3	DO	DMIC I/F	LPI_MI2S1_CLK
DMIC01_DATA	J2801	66	P3	IO		LPI_MI2S1_WS
DMIC23_CLK	J2801	64	P3	DO		LPI_MI2S1_DATA0
DMIC23_DATA	J2801	62	P3	IO		LPI_MI2S1_DATA1
DMIC45_CLK	J2801	60	P3	DO		LPI_MI2S2_DATA0
DMIC45_DATA	J2801	58	P3	IO		LPI_M2S2_DATA1
CON_AMICR_M	J2800	1	--	AI	Analog mic 4 negative input	To WCD9385
CON_AMICL_M			--	AI	Analog mic 5 negative input	
CON_AMICR_P	J2800	3	--	AI	Analog mic 4 positive input	

Audio Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Alt Function**
CON_AMICL_P	J2800	5	--	AI	Analog mic 5 positive input	
MI2S0_MCLK	J2800	26	P3	--	MI2S0 master clock	GPIO_136
MI2S0_SCK	J2800	47	P3	--	MI2S0 clock	GPIO_138
MI2S0_DATA0	J2800	49	P3	--	MI2S0 serial data channel 0	GPIO_139
MI2S0_DATA1	J2800	45	P3	--	MI2S0 serial data channel 1	GPIO_140
MI2S0_WS	J2800	18	P3	--	MI2S0 serial data word select	GPIO_141
MI2S2_SCK	J2800	30	P3	--	MI2S2 clock	GPIO_133
MI2S2_DATA0	J2800	28	P3	--	MI2S2 serial data channel 0	GPIO_134
MI2S2_WS	J2800	20	P3	--	MI2S2 serial data word select	GPIO_135
MI2S2_DATA1	J2800	24	P3	--	MI2S2 serial data channel 1	GPIO_137
LPI_MI2S1_CLK	J2801	68	P3	--	LPI MI2S1 clock	GPIO_152
LPI_MI2S1_WS	J2801	66	P3	--	LPI MI2S1 serial data word select	GPIO_153
LPI_MI2S1_DATA0	J2801	64	P3	--	LPI MI2S1 serial data channel 0	GPIO_154
LPI_MI2S1_DATA1	J2801	62	P3	--	LPI MI2S1 serial data channel 1	GPIO_155
LPI_MI2S2_CLK	J2801	54	P3	--	LPI MI2S2 clock	GPIO_156
LPI_MI2S2_WS	J2801	56	P3	--	LPI MI2S2 serial data word select	GPIO_157
LPI_MI2S2_DATA0	J2801	60	P3	--	LPI MI2S2 serial data channel 0	GPIO_158
LPI_MI2S2_DATA1	J2801	58	P3	--	LPI MI2S2 serial data channel 1	GPIO_159

2.3.5. USB & DisplayPort interfaces

C7230C SOM includes 2 x USB 3.1 GEN2 interfaces, which can support Type-C with DisplayPort. USB mode and DisplayPort mode can be simultaneously operated at USB 3.1 GEN2 (10 Gbps) and DP 1.4(8.1 Gbps).

Table 2-10. USB & DP interface definition

PIN Name	Location	PIN	Type	Description
USB0_SS_RX0_M	Pad	104	DO	USB 3.0 signals, compliant with USB 3.1 standard specification.
USB0_SS_RX0_P	Pad	105	DO	
USB0_SS_RX1_M	Pad	103	DI	
USB0_SS_RX1_P	Pad	102	DI	
USB0_SS_TX0_M	Pad	108	DO	
USB0_SS_TX0_P	Pad	107	DO	
USB0_SS_TX1_M	Pad	109	DI	
USB0_SS_TX1_P	Pad	110	DI	
USB0_HS_DM	Pad	118	IO	USB 2.0 signals, compliant with USB 2.0 standard specification.
USB0_HS_DP	Pad	117	IO	
USB_VBUS	Pad	131,132,133,134	PO	USB VBUS OTG output
USB_CC1	Pad	113	IO	CC pin for Type-C USB connector
USB_CC2	Pad	112	IO	
PM855_USB_SBU1	Pad	114	IO	DP AUX signals
PM855_USB_SBU2	Pad	115	IO	
USB1_SS_RX_M	Pad	92	DI	USB 3.0 signals, compliant with USB 3.1 standard specification.
USB1_SS_RX_P	Pad	93	DI	
USB1_SS_TX_M	Pad	89	DO	
USB1_SS_TX_P	Pad	90	DO	
USB1_HS_DM	Pad	87	IO	USB 2.0 signals, compliant with USB 2.0 standard specification.
USB1_HS_DP	Pad	88	IO	

2.3.6. PCIe interfaces

C7230C SOM supports one 2-lane PCIe (Peripheral Component Interconnect Express) gen3 interface and one 1lane PCIe gen3 interface.

Table 2-11. USB & DP interface definition

PIN name	Location	PIN	Type	Description	Notes
PCIE1_REFCLK_M	Pad	151	AO	PCIe signals, compliant with PCI Express Specification Revision 3.0.	
PCIE1_REFCLK_P	Pad	152	AO		
PCIE1_RX0_M	Pad	156	AI		
PCIE1_RX0_P	Pad	155	AI		
PCIE1_RX1_M	Pad	153	AI		
PCIE1_RX1_P	Pad	154	AI		
PCIE1_TX0_M	Pad	147	AO		
PCIE1_TX0_P	Pad	148	AO		
PCIE1_TX1_M	Pad	149	AO		
PCIE1_TX1_P	Pad	150	AO		
PCIE1_CLK_REQ_N	J2800	63	DI	PCIE1 Clock request	GPIO 83
PCIE1_RST_N	J2800	61	DO	PCIe1 reset signal	GPIO 82
PCIE1_WAKE_N	J2800	65	DI	PCIe1 wake up signal	GPIO 84
PCIE2_REFCLK_M	Pad	99	AO	PCIe signals, compliant with PCI Express Specification Revision 3.0.	
PCIE2_REFCLK_P	Pad	100	AO		
PCIE2_RX0_M	Pad	97	AI		
PCIE2_RX0_P	Pad	98	AI		
PCIE2_TX0_M	Pad	96	AI		
PCIE2_TX0_P	Pad	95	AI		
PCIE2_CLK_REQ_N	J2801	49	DI	PCIE1 clock request	GPIO 86
PCIE2_RST_N	J2801	47	DO	PCIe1 reset signal	GPIO 85
PCIE2_WAKE_N	J2801	45	DI	PCIe1 wake up signal	GPIO 87

2.3.7. SSC interfaces

C7230C SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the MSM device is in sleep mode. The SSC has a dedicated 1.5MB L2/TCM cache.

The SSC core has dedicated I/O to communicate with the sensors.

➲ **NOTE:** It is not recommended to use SSC pins as GPIO.

Table 2-12. SSC interface definition

PIN name	Location	PIN	Voltage	Type	Description
SNS_I2C4_SDA	J2800	14	P3	IO	I2C signals are dedicated to Sensor.
SNS_I2C4_SCL	J2800	16	P3	IO	

SNS_I3C0_SCL	J2800	41	P3	IO	I3C (Improved Inter Integrated Circuit) signals dedicated to Sensor.
SNS_I3C0_SDA	J2800	43	P3	IO	

2.3.8. SDIO interfaces

C7230C SOM supports one 4-lane SDIO, SDC2 connected to SD card.

The SDIO is a high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF, etc.).

- The clock can be up to 200 MHz.
- The signals routing should be 50ohm ±10% impedance control.
- CLK to DATA/CMD length matching should be less than 1mm.
- The spacing to all other signals should be 2 x line width.
- Maximum bus capacitance should be less than 1.0pF.
- Each trace needs to be next to a ground plane.

Table 2-13. SDIO interface definition

PIN name	Location	PIN	Voltage	Type	Description
SDC2_CLK_CONN	Pad	3	P2	DO	SD card signals; SD_UFS_CARD_DET_N need to be pulled up to P3.
SDC2_CMD	Pad	6	P2	IO	
SDC2_DATA_3	Pad	5	P2	IO	
SDC2_DATA_2	Pad	4	P2	IO	
SDC2_DATA_1	Pad	8	P2	IO	
SDC2_DATA_0	Pad	7	P2	IO	
SD_UFS_CARD_DET_N	J2801	1	P3	DI	

2.3.9. QUP interfaces

These GPIOs are available as QUP (Qualcomm Universal Peripheral) interface ports that can be configured for UART, SPI, I2C or I3C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus needs to be supplemented by a 2.2kΩ pull-up resistor.

Table 2-14. QUP lane to function mapping

QUP lane to function mapping							
	L0	**L1**	**L2**	**L3**	**L4**	**L5**	**L6**
(HS) UART	CTS	RFR	TX	RX	-	-	-
I2C/I3C	SDA	SCL	-	-	-	-	-
SPI	MISO	MOSI	SCLK	CS_0	CS_1	CS_2	CS_3

Table 2-15. QUP interface definition

QUP Interface						
PIN name	**Location**	**PIN**	**Voltage**	**Typ.**	**Description**	**Notes**
GPIO0	J2801	63	P3	IO	QUP19	
GPIO1	J2801	51	P3	IO		
GPIO2	J2801	41	P3	IO		
GPIO3	J2801	43	P3	IO		
GPIO4	J2800	32	P3	IO	QUP1	
GPIO5	J2800	34	P3	IO		
GPIO6	J2801	15	P3	IO		
GPIO7	J2801	11	P3	IO		
GPIO8	J2800	38	P3	P3	QUP4	
GPIO9	J2800	6	P3	P3		
GPIO10	J2801	2	P3	P3		
GPIO11	J2801	4	P3	P3		
GPIO12	J2802	2	P3	IO	QUP5	
GPIO13	J2802	3	P3	IO		
GPIO14	J2802	4	P3	IO		
GPIO15	J2802	5	P3	IO		
GPIO24	J2801	46	P3	IO	QUP8	
GPIO25	J2801	42	P3	IO		
GPIO26	J2801	6	P3	IO		
SDM_FAST_BOOT_0	J2801	69	P3	IO		GPIO27
GPIO28	J2800	36	P3	IO	QUP0	
GPIO29	J2801	19	P3	IO		
GPIO30	J2801	17	P3	IO		
GPIO31	J2801	13	P3	IO		
GPIO36	J2801	32	P3	IO	QUP13	

QUP Interface						
PIN name	**Location**	**PIN**	**Voltage**	**Typ.**	**Description**	**Notes**
GPIO37	J2801	30	P3	IO		
GPIO38	J2801	59	P3	IO		
GPIO39	J2801	53	P3	IO		
GPIO40	J2801	5	P3	IO	QUP14	
GPIO41	J2801	28	P3	IO		
GPIO42	J2801	26	P3	IO		
GPIO43	J2801	21	P3	IO		
APPS_I2C_SDA	J2801	50	P3	IO	QUP15	GPIO44
APPS_I2C_SCL	J2801	48	P3	IO		GPIO45
GPIO46	J2802	6	P3	IO		
SDM_FAST_BOOT_1	J2801	10	P3	IO		GPIO47
GPIO48	J2801	36	P3	IO	QUP16	
GPIO49	J2801	34	P3	IO		
GPIO50	J2801	61	P3	IO		
GPIO51	J2801	55	P3	IO		
GPIO52	J2801	33	P3	IO	QUP17	
GPIO53	J2801	37	P3	IO		
GPIO54	J2801	39	P3	IO		
GPIO55	J2801	35	P3	IO		
GPIO56	J2801	29	P3	IO	QUP18	
GPIO57	J2801	27	P3	IO		
GPIO58	J2801	25	P3	IO		
GPIO59	J2801	23	P3	IO		
GPIO 115	J2802	21	P3	IO	QUP2	
GPIO 116	J2802	22	P3	IO		
GPIO117	J2802	23	P3	IO		
GPIO118	J2802	24	P3	IO		

2.3.10. Power on interfaces

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device's available power sources, and enable the correct source. It is recommended to press power on key, PHONE_ON_N, longer than 1s for a power on event. Another power on method is to insert battery or power supply when CBL_PWR_N pin connect to ground.

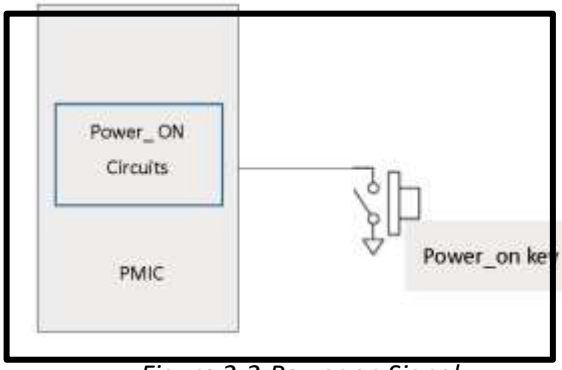

Figure 2-2.Power on Signal

Table 2-16. Power on interface definition

PIN name	Location	PIN	Voltage	Type	Description
PHONE_ON_N	Pad	85	P3	DI	Power-on key (200 kΩ internal PU to 1.8 V) ground switch
CBL_PWR_N	J2800	13	P3	DI	Cable power-on (200 kΩ internal PU to 1.8 V)

2.3.11. Reset interfaces

Extended press of the volume key will initiate a shutdown or reset (software selectable).

Stage 1. Reset – software-configurable bark

PMIC generates interrupt, giving the MSM device the opportunity to fix the problem or gracefully reset the system.

Example events that can cause a bark:

- Over temperature indicates system is getting too hot.
- PMIC watchdog indicates that it has not kicked.

Stage 2. Software-configurable bite

If reset is ignored, PMIC will force a reset event (selectable by software).

Stage 3. Hardware mandatory bite

The user can generate a mandatory reset by a long press of PM_RESIN_N, or PHONE_ON_N, or PM_RESIN_N + PHONE_ON_N in combination.

The standalone or combination of reset triggers can also be selected as SBL by directly writing to the appropriate registers.

Table 2-17. Reset interface definition

PIN name	Location	PIN	Voltage	Type	Description
PM_RESIN_N	J2800	11	P3	DI	Reset input to PM8250 (40 kΩ internal PU to 1.8 V), Low active

2.3.12. Keys interfaces

These interfaces are dedicated for keys.

Table 2-18. Key interface definition

PIN name	Location	PIN	Voltage	Type	Description	Notes
PHONE_ON_N	Pad	85	P3	DI	Power-on key ground switch (200 kΩ internal PU to 1.8 V)	
PM_RESIN_N	J2800	11	P3	DI	Reset input to PM8250 (40 kΩ internal PU to 1.8 V), low active	
SDM_FORCE_USB_BOOT	Pad	86	P3	DI	During development or factory production, a boot from the primary USB 3.1 port can be forced by pulling this pin high to 1.8V.	GPIO132
VOL_UP_N	J2800	7	P3	DI	Volume up key signal, low active	

2.3.13. Debug UART interface

These interfaces are dedicated for debug.

Table 2-19. Debug UART interface definition

PIN name	Location	PIN	Voltage	Type	Description	Notes
SDM_DEBUG_UART_TX	Pad	83	P3	DI	QUP12 UART signals, can be used for debug	
SDM_DEBUG_UART_RX	Pad	84	P3	DO		

2.3.14. Battery interfaces

These interfaces are dedicated for battery, mainly used for monitoring battery status, inserting and voltage detection.

Table 2-20. Battery interface definition

PIN name	Location	PIN	Voltage	Type	Description
VBATT_CONN_VSENSE_P	Pad	141	VBATT	AI	Battery voltage sense positive input signal
VBATT_CONN_VSENSE_M	Pad	140	VBATT	AI	Battery voltage sense negative input signal
BATT_THERM	J2800	25	0~1.875V	AI	Battery temperature sense input signal
BATT_ID	J2800	23	0~1.875V	AI	Battery ID sense input signal

2.3.15. ADCs interfaces

The ADC input signals are used for analog multiplexer function.

Table 2-21. ADC interface definition

PIN name	Location	PIN	Voltage	Type	Description	Notes
PM8150L_GPIO_5	J2800	69	0~1.875V	LV	ADC input, can be configured as 1.8V	-
PM8150L_GPIO_6	J2800	15	0~1.875V	LV	ADC input, can be configured as 1.8V	Or set to provide a PWM, see 2.3.16. PWMs and LED current driver interfaces.
PM8150L_GPIO_7	J2800	19	0~5V	MV	ADC input, can be configured as 1.8V or 5V	-
PM8150L_GPIO_10	J2800	17	0~5V	MV	ADC input, can be configured as 1.8V or 5V	Or set to provide a PWM, see 2.3.16. PWMs and LED current driver interfaces.

2.3.16. PWMs and LED current driver interfaces

C7230C SOM supports dual PWM output and dual LED Current Driver, all PWM output by Light Pulse Generators.

LED Current Driver PINs can be used for different events; they are separate controller. Independently programmable duty cycle and period via LPGs (6-or 9-bit resolution) for digital dimming.

Table 2-22. PWMs and LED Current Driver interface definition

PWMs PINs						
PIN name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PM8150L_GPIO_6	J2800	15	0~1.875V	LV	Can be configured as GPIO and PWM (max. 19.2MHz)	-
PM8150L_GPIO_10	J2800	17	0~5V	MV		-
LED Driver PINs						
PIN name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
R_LED	J2802	9	-	AO	Custom indicator light, connected to positive port	LPG_OUT_1
B_LED	J2802	7	-	AO	Custom indicator light, connected to positive port	LPG_OUT_3
G_LED	J2802	8	-	AO	Custom indicator light, connected to positive port	LPG_OUT_2

2.3.17. Antenna Interfaces

C7230C SOM provides fully-integrated WLAN and Bluetooth function.

The WLAN and Bluetooth share the same antenna port with 50ohm impedance.

- WLAN supports 2 × 2 MIMO (Multiple Input/Multiple Output) with two spatial streams IEEE802.11 a/b/g/n/ac/ax WLAN standards.
- The SOM supports Bluetooth 5.1 + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.

Table 2-23. Antenna interface definition

Name	Location	Type	Description	Notes
Antenna 1	J1501	IO	Antenna 1 supports WI-FI 2.4G/5G &BT	Chain0
Antenna 2	J5907	IO	Antenna 2 supports WI-FI 2.4G/5G	Chain1

Chapter 3. Electrical Characteristics

3.1. Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in 3.2. Operating conditions.

Table 3-1. Absolute rating conditions

Parameter	Min	Max	Units
Input power voltage			
USB_VBUS	-0.3	28	V
VBAT	-0.3	6	V
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M, RSENSE_EXT_M, RSENSE_EXT_P	-0.3	6	V
ESD			
ESD-HBM model rating	-	±2000	V
ESD-CDM model rating	-	±500	V

➲ **NOTE:** ESD rating conditions will be valid only when the module is fully tested and approved in the initial production stage.

3.2. Operating conditions

C7230C SOM needs to be operated under the conditons specified in Table 4-2.

Table 3-2. Operating conditions

Parameters	Min	Typical	Max	Units
Input power voltage				
USB_VBUS	+3.6	5	+13.2	V
VBAT	+3.6	3.8	+4.8	V
VBAT	3	-	-	A
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M,	+3.6	3.8	+4.8	V
Thermal conditions				
Operating temperature	-25	25	75	°C
Storage temperature	-40	-	85	°C

➲ **NOTE:** The min and max operating temperatures specified in the above table shall not exceed those of relevant IC (see Table 3-3).

Table 3-3. IC temperature

Chipset	Thermal Condition (min, °C)	Thermal Condition (max, °C)
QCS7230	Ta=-30	Tj=95
PM8250	Ta=-30	Tj=95
PM8150B	Tc=-30	Tc=85

PM8150L	Ta=-30	Ta=85
PM8009	Tj=-30	Tj=125
PM3003	Ta=-30	Ta=85
PMK8002	Tj=-35	Tj=115
WCD9385	Ta=-30	Tc=85
QCA6391	Ta=-30	Ta=85
LPDDR	Ta=-25	Ta=85
UFS	Ta=-25	Ta=85

➲ **NOTE:**

- Ta: a=ambient, temperature of the working environment.
- Tc: c=case, *surface temperature*, which can be simply understood as ambient temperature + CPU temperature rise. Generally speaking, Tc is slightly higher than the ambient temperature.
- Tj: j=junction, *junction temperature*, which can be simply understood as the chip internal temperature.

3.3. Output power

C7230C SOM provides power supply for external devices, including camera module, SD card, Sensor,etc. Refer to Table 3-3 for details.

Table 3-4. Output power

Function	Default voltage (V)	Programble range (V)	Rated current (mA)	Expected use
VREG_L9C_2P96	+2.96	+2.7--+2.96	600	SD/MMC card or UFS card
VREG_L7F_1P8	+1.808	+1.808	<600	
VREG_S4A_1P8	+1.8	+1.8	1000	Generic 1.8V
VREG_BOB	+3.7	+3.6--+4.0	600	For Codec VDD input, LDO

3.4. Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage. The SOM I/O voltage level is the same as VDDPX_3 except the SD card and analog I/O. The I2C, USB,MIPI and UART comply with the standards.

3.4.1. Digital GPIO characteristics

Table 4-4 shows the digital GPIO characteristics.

Table 3-5. Digital I/O voltage performance

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt	0.7 x VDDPX_3	VDDPX_3+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt	-0.3	0.3 x VDDPX_3	V
VSHYS	Schmitt hysteresis voltage	300	-	mV
VOH	High-level output voltage, CMOS	VDDPX_3 - 0.45	VDDPX_3	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V
RPULL-UP	Pull-up resistance	20 K	60 K	Ω
RPULL-DOWN	Pull-down resistance	60 K	20 K	Ω

3.4.2. SD card digital I/O characteristics

The SD card is powered by P2 supply, 1.8V/2.96V. Table 4-5 shows the SD card digital I/O characteristics.

Table 3-6. SD digital IO voltage performance (1.8V/2.96V)

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27/0.625 x VDDPX_2	-	2/VDDPX_2 + 0.3	V
VIL	Low-level input voltage	-0.3/-0.3	-	0.58/0.25 x VDDPX_2	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/0.75 x VDDPX_2	-	-/VDDPX_2	V
VOL	Low-level output voltage	0/0	-	0.45/0.125 x VDDPX_2	V

3.5. MIPI

C7230C SOM supports the MIPI interface and complies with MIPI standards.

Table 3-7. MIPI_DSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	-
MIPI Alliance Specification for DPHY v1.2	-

MIPI Alliance Specification for CPHY v1.0	-

Table 3-8. MIPI_CSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	• RAW7 not supported • DPCM predictor 2 not supported
MIPI Alliance Specification for DPHY v1.2	-
MIPI Alliance Specification for CPHY v1.0	The maximum supported data rate is 1.5Gsps.

3.6. USB

C7230C SOM supports USB standards and exceptions.

Table 3-9. USB

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
UTMI Specification Version 1.05, released on 3/29/2001	-
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	-

3.7. PCIe

C7230C SOM supports PCIe standards and exceptions.

Table 3-10. PCIe

Applicable standard	Feature exceptions
PCI Express Specification, Revision 3.0	Gen3

3.8. DisplayPort

C7230C SOM supports DisplayPort standards and exceptions.

Table 3-11. DP

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	HBR3

3.9. SLIMbus

C7230C SOM supports SLIMbus HDMI standards and exceptions

Table 3-12. SLIMbus

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	-

3.10. SDIO

C7230C SOM Supports SD standards and exceptions.

Table 3-13. SDIO

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	-
SDIO Card Specification version 3.0	-

3.11. I2S

C7230C SOM I2S standards and exceptions:

- Legacy I2S interfaces for primary and secondary microphones and speakers.
- The multiple I2S (MI2S) interface for microphone and speaker functions.

It supports the following functions:

- Both master and slave modes.
- 16, 24, or 32-bit resolution audio samples.
- 8, 16, 32, 48, 96 and192 kHz sampling rate in Master mode, and all standard sample rates in Slave mode. 16-bit and 24-bit data formats in standard I2S mode, and 24-bit left-justified (24-bit data in 32-bit frame left-justified, LSBs are padded with 0s).
- Maximum clock frequency supported 12.288 MHz.

An additional pin can be used for a master clock, supplied by the MSM device. The master clock is often used in the external devices to drive their oversampling logic. The LPASS clock controller can provide master clocks from independent clock dividers to the I2S bit-clock dividers.

Table 3-14. I2S

Applicable standard	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996	-

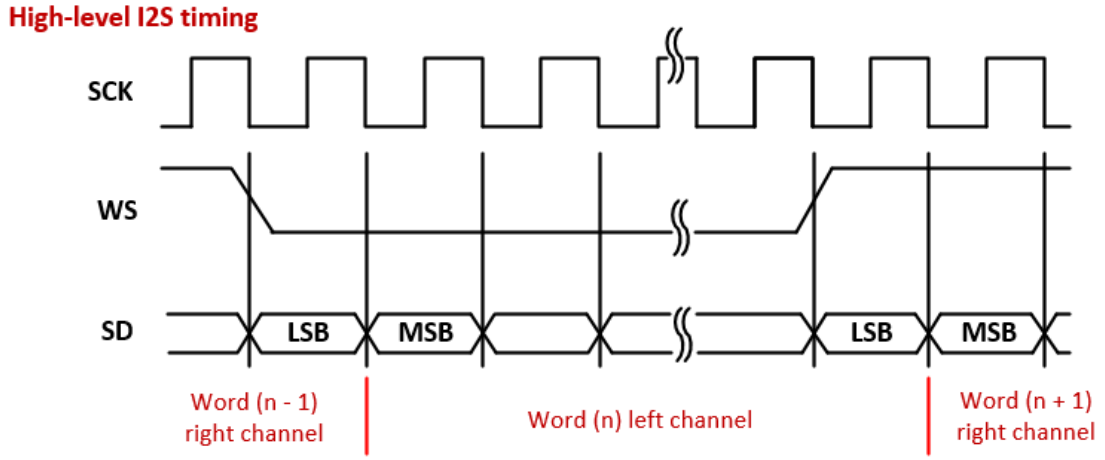

Figure 3-1.High-level I2S Timing

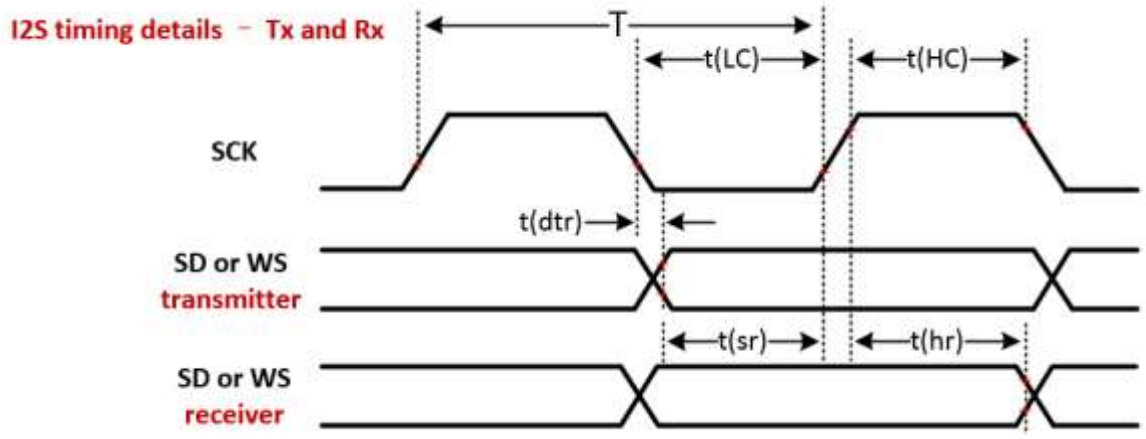

Figure 3-2.I2S Timing Details

The word-select signal is a 50% duty cycle. Signal data is delayed 1 bit-clock, relative to the word select.

Data outputs are launched on the falling edge of the clock, and input data are captured on the rising edge of the clock by the receiver.

I2S samples are 2’s complement values, and the MSB is transmitted first allowing the transmitter and receiver to support different number of bits per sample.

The left channel is transmitted when the word select is low, and the right channel is transmitted when the word select is high

Table 3-15. I2S timing

Parameter		Min	Max	Unit
Using internal SCK				
Frequency		–	24.576	MHz
T	Clock period	40.69	–	ns
t(HC)	Clock high	0.45 × T	0.55 × T	ns
t(LC)	Clock low	0.45 × T	0.55 × T	ns
t(sr)	SD and WS input setup time	8.14	–	ns
t(hr)	SD and WS input hold time	0	–	ns
t(dtr)	SD and WS output delay	–	6.10	ns
Using external SCK				
Frequency		–	24.576	MHz
T	Clock period	40.69	–	ns
t(HC)	Clock high	0.45 × T	0.55 × T	ns
t(LC)	Clock low	0.45 × T	0.55 × T	ns
t(sr)	SD and WS input setup time	8.14	–	ns
t(hr)	SD and WS input hold time	0	–	ns
t(dtr)	SD and WS output delay	–	6.10	ns

3.12. I2C

Refer to Table 3-15 for C7230C SOM I2C standards and exceptions.

Table 3-16. I2C

Applicable standard	Feature exceptions
I2C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.

3.13. SPI

C7230C SOM supports SPI standards as a master only.

3.14. Fuel gauge

The fuel gauge module offers a hardware-based algorithm that is able to accurately estimate the battery's state of charge by using current monitoring and voltage-based techniques. This hybrid approach ensures both excellent short-term linearity and long-term accuracy. Furthermore, neither full battery charge cycling, nor zero-current-load conditions, are required to maintain the accuracy.

The fuel gauge measures the battery pack temperature by sensing the voltage across an external thermistor. Missing battery detection is also incorporated to accurately monitor battery insertion and removal scenarios, while properly updating the state of charge when a battery is reconnected.

Using precise measurements of battery voltage, current, and temperature, the fuel gauging algorithm compensates for the variation in battery characteristics across temperature changes and aging effects. This provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions.

Table 3-17. Fuel gauge

Function	Min	Type	Max	Units	Expected use
VBATT_CONN_VSENSE_P (H47) & VBATT_CONN_VSENSE_M(G47)					
Resolution	-	-	16	bits	Voltage ADC
	1	-	450	Kohm	ID ADC
	-	-	16	bits	Current ADC

3.15. LED current driver

Red, green, and blue RGB drivers, which operate of a dedicated supply voltage, are available.

Table 3-18. LED current driver

Function	Min	Type	Max	Units	Expected use
RGB_LED					
Current per channel (I out)			12	mA	-
Dimming PWM frequency	0.0025		4700	Hz	-
Dimming resolution	6		9	bit	-

3.16. ADC

Refer to Table 3-18 for ADC performance specifications.

Table 3-19. ADC

Specification	Test condition	Min	Typ.	Max	Units	Expected use
1/1 channel end-to-end accuracy	Calibrated data result	-11	±6	11	mV	-
1/1 channel end-to-end accuracy with internal pull-up	Calibrated data result	-12.5	±7	12.5	mV	-
1/3 channel end-to-end accuracy	Calibrated data result	-20	±10	20	mV	-
ADC resolution (LSB)	1/1 channel	-	64.879	-	µV	-
	Scaled to 1/3 channel	-	194.637	-		
ADC conversion time	1K decimation ratio, 4.8MHz sample clock	-	654	700	µs	-
Current consumption	VADC active	-	450	500	µA	-

3.17. Power consumption

Refer to *TurboX C7230C Power Consumption Optimization User Guide*.

3.18. Thermal

T.B.D.

3.19. RF performance

3.19.1.Wi-Fi performance

Wi-Fi supports 2.4G & 5G, below table records the RF performance test result.

Table 3-20. 2.4G CH0 W-iFi performance

2.4G Channel0 RF Performance					
11M					
Test Item		**Expected Result**	**1**	**6**	**11**
11b	Transmit Power(dBm)	16±1.5dBm	16.07	16.34	16.21
	Reference sensitivity (PER＜8%)	11M＜-80dBm	-88	-89	-88
54M					
Test Item		**Expected Result**	**1**	**6**	**11**
11g	Transmit Power(dBm)	15±1.5dBm	14.8	14.76	14.99
	Reference sensitivity (PER＜10%)	54M＜-72dBm	-74	-74	-74
MCS7					
Test Item		**Expected Result**	**1**	**6**	**11**
11n (20)	Transmit Power(dBm)	14±1.5dBm	13.64	13.92	14.08
	Reference sensitivity (PER＜10%)	MCS7＜-69dBm	-73	-73	-73
MCS7					
Test Item		**Expected Result**	**1**	**6**	**11**
11n (40)	Transmit Power(dBm)	14±1.5dBm	14.670	14.140	14.160
	Reference sensitivity (PER＜10%)	MCS7＜-61dBm	-69	-69	-69

Table 3-21. 2.4G CH1 Wi-Fi performance

2.4G Channel1 RF Performance					
11M					
Test Item		**Expected Result**	**1**	**6**	**11**
11b	Transmit Power(dBm)	16±1.5dBm	16.21	16.38	16.43
	Reference sensitivity (PER＜8%)	11M＜-76dBm	-89	-89	-88
54M					
Test Item		**Expected Result**	**1**	**6**	**11**
11g	Transmit Power(dBm)	15±1.5dBm	14.69	14.49	14.76
	Reference sensitivity (PER＜10%)	54M＜-65dBm	-75	-75	-76
MCS7					
Test Item		**Expected Result**	**1**	**6**	**11**
11n (20)	Transmit Power(dBm)	14±1.5dBm	14.06	14.1	13.91
	Reference sensitivity (PER＜10%)	MCS7＜-64dBm	-72	-73	-73
MCS7					
Test Item		**Expected Result**	**1**	**6**	**11**
11n (40)	Transmit Power(dBm)	14±1.5dBm	14.13	14.06	13.92
	Reference sensitivity (PER＜10%)	MCS7＜-61dBm	-68	-68	-68

Table 3-22. 5.8G CH0 Wi-Fi performance

5.8G RF Channel0 Performance									
54M									
Test Item		**Expected Result**	**36 (5180)**	**60 (5300)**	**100 (5500)**	**120 (5600)**	**149 (5745)**	**161 (5805)**	**165 (5825)**
11a	Transmit Power(dBm)	15±1.5dBm	14.28	14.4	14.98	14.34	14.85	15.08	15.05
	Reference sensitivity (PER＜10%)	54M＜-72dBm	-76	-76	-76	-76	-76	-76	-75
MCS7									
Test Item		**Expected Result**	**36 (5180)**	**60 (5300)**	**100 (5500)**	**120 (5600)**	**149 (5745)**	**161 (5805)**	**165 (5825)**
11n (20)	Transmit Power(dBm)	14±1.5dBm	13.53	13.42	13.82	13.23	13.87	13.92	13.91
	Reference sensitivity (PER＜10%)	MCS7≤-69dBm	-73	-73	-73	-73	-73	-73	-73
MCS7									
Test Item		**Expected Result**	**38 (5190)**	**62 (5310)**	**102 (5510)**	**118 (5590)**	**134 (5670)**	**151 (5755)**	**159 (5795)**
11n (40)	Transmit Power(dBm)	14±1.5dBm	13.58	13.61	13.84	13.43	13.63	14.36	14.18
	Reference sensitivity (PER＜10%)	MCS7≤-66dBm	-70	-71	-70	-70	-70	-70	-70
MCS8									
Test Item		**Expected Result**	**36 (5180)**	**60 (5300)**	**100 (5500)**	**120 (5600)**	**149 (5745)**	**161 (5805)**	**165 (5825)**
11ac(20MHz)	Transmit Power(dBm)	14±1.5dBm	13.43	13.46	13.77	13.22	13.94	13.91	13.93
	Reference sensitivity (PER＜10%)	MCS8＜-59dBm	-71	-72	-70	-70	-71	-71	-70
MCS9									
Test Item		**Expected Result**	**38 (5190)**	**62 (5310)**	**102 (5510)**	**118 (5590)**	**134 (5670)**	**151 (5755)**	**159 (5795)**
11ac(40MHz)	Transmit Power(dBm)	13±1.5dBm	12.68	12.75	13.11	12.49	12.64	13.44	13.34
	Reference sensitivity (PER＜10%)	MCS9＜-56dBm	-67	-67	-66	-65	-66	-66	-67

MCS9									
Test Item		**Expected Result**	**46 (5230)**	**58 (5290)**	**110 (5550)**	**122 (5610)**	**130 (5650)**	**155 (5775)**	**159 (5795)**
11ac(80MHz)	Transmit Power(dBm)	12±1.5dBm	11.2	11.12	11.91	11.1	11.75	12.3	12.45
	Reference sensitivity (PER＜10%)	MCS9≤-54dBm	-63	-63	-61	-62	-62	-62	-60
MCS11									
Test Item		**Expected Result**	**38 (5190)**	**62 (5310)**	**102 (5510)**	**118 (5590)**	**134 (5670)**	**151 (5755)**	**159 (5795)**
11ax(20MHz)	Transmit Power(dBm)	12±1.5dBm	12.15	11.12	11.71	11.22	11.51	12.2	12.41
	Reference sensitivity (PER＜10%)	MCS9＜-52dBm	-63	-63	-62	-62	-63	-63	-63
MCS11									
Test Item		**Expected Result**	**46 (5230)**	**58 (5290)**	**110 (5550)**	**122 (5610)**	**130 (5650)**	**155 (5775)**	**159 (5795)**
11ax(40MHz)	Transmit Power(dBm)	12±1.5dBm	11.4	11.39	11.83	11.48	11.4	11.92	12.43
	Reference sensitivity (PER＜10%)	MCS9≤-49dBm	-60	-59	-59	-59	-59	-60	-60
MCS11									
Test Item		**Expected Result**	**38 (5190)**	**62 (5310)**	**102 (5510)**	**118 (5590)**	**134 (5670)**	**151 (5755)**	**159 (5795)**
11ax(80MHz)	Transmit Power(dBm)	12±1.5dBm	10.96	10.98	11.63	10.96	11.14	11.87	12
	Reference sensitivity (PER＜10%)	MCS9＜-46dBm	-58	-57	-56	-56	-56	-56	-56

Table 3-23. 5.8G CH1 Wi-Fi performance

5.8G RF Channel1 Performance									
MCS15									
Test Item		**Expected Result**	**36 (5180)**		**120 (5600)**		**165 (5825)**		
11n (20)	Transmit Power(dBm)	12±1.5dBm	11.05	11.39	11.24	11.14	11.17	12.01	
	Reference sensitivity (PER＜10%)	MCS15≤-69dBm	-74		-74		-73		
MCS15									
Test Item		**Expected Result**	**38 (5190)**		**118 (5590)**		**159 (5795)**		
11n (40)	Transmit Power(dBm)	12±1.5dBm	11.1	11.54	11.44	11.35	11.11	12.26	
	Reference sensitivity (PER＜10%)	MCS15≤-66dBm	-71		-71		-71		

NSS=2, MCS=8 (MCS 17)									
Test Item		**Expected Result**	**36 (5180)**		**120 (5600)**		**165 (5825)**		
11ac (20MHz)	Transmit Power(dBm)	10±1.5dBm	9.1	9.3	9.3	9.19	9.03	10.22	
	Reference sensitivity (PER＜10%)	MCS17＜-59dBm	-71		-71		-71		
NSS=2, MCS=9 (MCS 19)									
Test Item		**Expected Result**	**38 (5190)**		**118 (5590)**		**159 (5795)**		
11ac (40MHz)	Transmit Power(dBm)	10±1.5dBm	9/6	9.51	9.47	9.27	10.56	9.45	
	Reference sensitivity (PER＜10%)	MCS19＜-56dBm	-67		-67		-67		
NSS=2, MCS=9 (MCS 19)									
Test Item		**Expected Result**	**46 (5230)**		**122 (5610)**		**159 (5795)**		
11ac(80MHz)	Transmit Power(dBm)	10±1.5dBm	9.49	9.17	9.33	9.23	9.24	9.33	
	Reference sensitivity (PER＜10%)	MCS19≤-54dBm	-63		-63		-63		
NSS=2, MCS=11 (MCS 23)									
Test Item		**Expected Result**	**36 (5180)**		**120 (5600)**		**165 (5825)**		
11ax(20MHz)	Transmit Power(dBm)	12±1.5dBm	10.93	10.79	10.98	11.23	12.33	11.14	
	Reference sensitivity (PER＜10%)	MCS23＜-52dBm	-64		-63		-63		
NSS=2, MCS=11 (MCS 23)									
Test Item		**Expected Result**	**46 (5230)**		**118 (5590)**		**159 (5795)**		
11ax(80MHz)	Transmit Power(dBm)	12±1.5dBm	11.03	11.26	11.1	11.34	12.09	11.13	
	Reference sensitivity (PER＜10%)	MCS9≤-49dBm	-56		-55		-55		

3.19.2.BT performance

Table 3-24. BT performance

BT RF Performance						
Test Equipment: IQxel/CMW500			RF IN/OUT Offset: 1dB			
Test Item			Expected Result	Channel		
				2402	2440	2480
1	Output Power	Avg(dBm)	-10~10dBm	6	6.46	5.9
2	Initial Carrier Frequency	Offset (KHz)	±75KHz	pass	pass	pass
3	Transmit Spectrum mask	±500KHZ	＜-20dBc	pass	pass	pass
		2MHZ	＜-20dBm	pass	pass	pass
		3MHZ	＜-40dBm	pass	pass	pass
4	Modulation Characteristic	⊿f1 avg	225 kHz ~ 275 kHz	247.8	247.9	247.6
		⊿f2 avg	≥185KHz	221	221.1	220
6	Sensitivity	BER≤0.1%	≤-85dBm	-88	-86	-88

Chapter 4. Packaging

Refer to Figure 4-1 below for single-layer tray packaging. SOM modules shall be chamfered per the tray chamfer and loaded according to the sequence of IMEI number, and one Plastic tray (③) can be loaded with 12 sets of SOM.

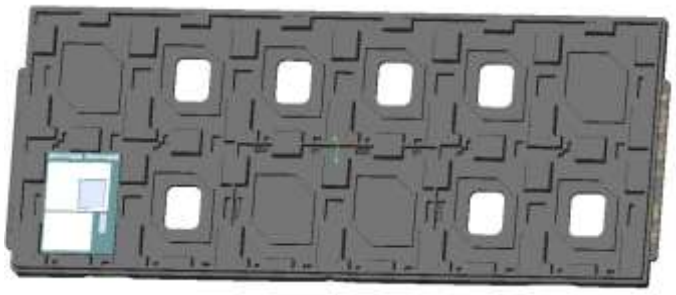

Figure 4-1. Single-layer Tray Packaging

Refer to Figure 4-2 for stacking of trays. Plastic trays (③) are stacked into 11 layers. Put Activated Clay (⑤) at the top and bottom of tray (1 pcs for each), and then put 8 trays into one Foil bag (④). Put the Wet sensitive identification card (⑦) into the Foil bag (④). The packaging capacity of Foil bag (④) is: 12 *7=84 sets of SOM.

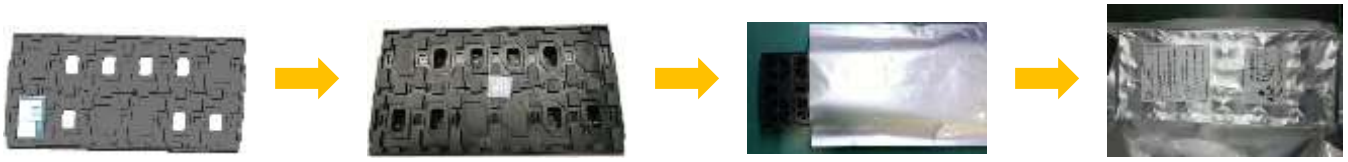

Figure 4-2. Stacking of Trays

The carton packaging is shown as in Figure 4-3. Put two Foil bags (④) into one EPE inner box (②), and then put the EPE inner box (②) and Pearl cotton partition (⑥) into a carton (①). The packaging capacity of a carton is: 84 * 2=168 sets of SOM.

Figure 4-3. Carton Packaging

Table 4-1. BOM list of packaging

Item	PN	Description	Dimensions (mm)	Material	Q'ty
①	TBD	Carton	415*220*210	230/180/120/180/230-BC	1
②	TBD	EPE inner box	400*210*170	20kg/m³, antistatic EPE	1
③	TBD	Plastic tray	322.6x135.9x9.0	PPE(Black)	16
④	TBD	Foil bag	500*300*0.22	Composite of aluminum foil (PET), PE and film	2
⑤	TBD	Activated Clay	40g	N/A	4
⑥	TBD	Pearl cotton partition	400*210*20	20kg/m³, antistatic EPE	1
⑦	TBD	Wet sensitive identification card	75*50	Paper card	2
⑧	TBD	Label	100*80	80g coated paper	1

Refer to Figure 4-4 for the label.

包装标签信息 /Label information			
供应商名称 Vendor		客户名称 Customer	
商品名称 Product Name		型号/Model	
品牌/Brand	TURBOX™	产品编码/TPN	
订单号/Order No.		客户料号 Part No.	
生产日期/MFG Date		箱号/Carton No.	
原产地/Made in		数量/QTY	
毛重/G.W.		净重/N.W.	
检验结果/OQC		备注/Remark	

Figure 4-4. Label

Appendix 1. Compliance and Certificate Information

FCC statements:

Federal Communication Commission (FCC) Radiation Exposure Statement

When using the product, maintain a distance of 20cm from the body to ensure compliance with RF exposure requirements.

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE: The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications or changes to this equipment. Such modifications or changes could void the user's authority to

operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio

communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device is intended only for OEM integrators under the following conditions: 1. The antenna must be installed such that 20 cm is maintained between the antenna and users. 2. The transmitter module may not be co-located with any other transmitter or antenna. As long as the two conditions above are met, additional transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required for the installed module.

Important Note: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the Federal Communications Commission of the U.S. Government (FCC) and the Canadian Government authorizations are no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator shall be responsible for re-evaluating the end-product (including the transmitter)

and obtaining a separate FCC authorization in the U.S. and Canada.

OEM Integrators - End Product Labeling Considerations: This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains, FCC ID: 2AOHHTURBOXC7230C”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

OEM Integrators - End Product Manual Provided to the End User: The OEM integrator shall not provide information to the end user regarding how to install or remove this RF module in end product user manual. The end user manual must include all required regulatory information and warnings as outlined in this document.

Appropriate measurements (e.g. 15 B compliance) and if applicable additional equipment authorizations (e.g. SDoC) of the host product to be addressed by the integrator/manufacturer.

This module is only FCC authorized for the specific rule parts 15.247, 15.407 listed on the grant, and the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host product as being Part 15 Subpart B compliant.

IC statements:

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

(1) This device may not cause interference.

(2) This device must accept any interference, including interference that may cause undesired operation of the device

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1) L'appareil ne doit pas produire de brouillage;

2) L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

The device meets the exemption from the routine evaluation limits in section 2.5 of RSS 102 and compliance with RSS-102 RF exposure, users can obtain Canadian information on RF exposure and compliance.

Le dispositif rencontre l'exemption des limites courantes d'évaluation dans la section 2.5 de RSS 102 et la conformité à l'exposition de RSS-102 rf, utilisateurs peut obtenir l'information canadienne sur l'exposition et la conformité de rf.

the device for operation in the band 5150-5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems

les dispositifs fonctionnant dans la bande 5150-5250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux;

1. the device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;

2. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit;

3. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits specified for point-to-point and non-point-to-point operation as appropriate.

1. les dispositifs fonctionnant dans la bande 5150-5250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux;

2. le gain maximal d'antenne permis pour les dispositifs utilisant les bandes 5250-5350 MHz et 5470-5725 MHz doit se conformer à la limite de p.i.r.e.;

3. le gain maximal d’antenne permis (pour les dispositifs utilisant la bande 5725-5850 MHz) doit se conformer à la limite de p.i.r.e. spécifiée pour l’exploitation point à point et non point à point, selon le cas.

Caution!

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

The final end product must be labelled in a visible area with the following:

“Contains FCC ID: 2AOHHTURBOXC7230C”.

“Contains IC: 23465-TURBOX7230C”.

CE statements:

Do not use the module in the environment at too high or too low temperature, never expose the module under strong sunshine or too wet environment.

RF exposure information: The Maximum Permissible Exposure (MPE) level has been calculated based on a distance of d=20 cm between the device and the human body. To maintain compliance with RF exposure requirement, use product that maintain a 20cm distance between the device and human body.

EU Regulatory Conformance

Hereby, Thundercomm Technology Co., Ltd declares that this device is in compliance with the essential requirements and other relevant provisions of Directive 2014/53/EU.

The device for operation in the band 5150–5350 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

	**AT**	**BE**	**BG**	**CH**	**CY**	**CY**	**DE**	**DK**
	EE	**EL**	**ES**	**FI**	**FR**	**HR**	**HU**	**IE**
	IS	**IT**	**LI**	**LT**	**LU**	**LV**	**MT**	**NL**
	PL	**PT**	**RO**	**SE**	**SI**	**SK**	**TR**	**UK(NI)**

Frequency bands and power

	Bands	**Operation Frequency**	**Max.Power**
Bluetooth	2.4GHz	2402-2480 MHz	EIRP 9.54 dBm
Wi-Fi	2.4GHz	2412-2472MHz	EIRP 19.9 dBm
	5GHz	5180-5240MHz	EIRP 20.32dBm
		5260-5320MHz	EIRP 19.75 dBm
		5500-5700MHz	EIRP 19.94 dBm
		5745-5825MHz	EIRP 13.48 dBm

C7230C model is module without antennas. The following types of antennas are recommended:

Antenna Manufacturer:	Sunnyway
Part No.: 630810000043	SH23129IB77
Antenna Type:	Dipole Antenna
Antenna Gain:	ANT1: WIFI 2.4G/BT:3.35 dBi WIFI 5G:2.08 dBi ANT2: WIFI 2.4G:3.35 dBi WIFI 5G:2.08 dBi

Manufacturer: Thundercomm Technology Co., Ltd

Manufacturer Address: Building 4, No. 99, Data Valley Middle Road, Xiantao District, Yubei District, Chongqing, China.

Signed for and on behalf of: Qiyong Zhou

Chongqing 2022.12.20

Place and date of issue

Name, Function, and signature

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