Thundercomm

Empowering Every IoT Device with Our Technology

Thundercomm C6490

Datasheet

Rev. V1.0
Apr 26, 2022

DN: tc-x1-13110

Revision History

Revision	Date	Description
1.0	Apr 26, 2022	Initial release.

Table List

About This Document

- Illustrations in this documentation might look different from your product.
- Depending on the model, some optional accessories, features, and software programs might not be available on your device.
- Depending on the version of operating systems and programs, some user interface instructions might not be applicable to your device.
- Documentation content is subject to change without notice. Thundercomm makes constant improvements on the documentation of your computer, including this guidebook.

Table of Contents

Chapter 1. Introduction

The TurboX C6490/CT6490 SOM (System on Module) is integrated with Qualcomm® Snapdragon™ 5G QCS6490/QCM6490, a 6 nm processor with superior performance and power efficiency, as well as high AI capability (14 TOPS). It supports Wi-Fi 6E with DBS, Long Range Bluetooth and optional 5G NR connection capabilities and is featured with 5 x 4-lane MIPI CSI D-PHY (2 of them compatible to support 3-lane MIPI CSI C-PHY which is up to 48M camera). It also has a rich set of peripheral interfaces, including both USB 3.1 and USB 2.0 concurrency and PCIE. The CT6490/C6490 SOM is a high performance AIoT SOM for building Handheld Devices, Industrial Robots, Service Robots, Drones and Digital Signage, providing customers with hardware interfaces and software SDK to validate functions and build the prototype quickly.

➲ **NOTE:** "TurboX" referred to herein is the English text of our registered trademark TURBOX.

1.1. Key features

The following table shows the detailed features of QCS6490 and C6490 SOM.

Table 1-1.Key features and performance of TurboX C6490

Item	Description
Applications Processor	Qualcomm® Kryo™ CPU 670 built on Arm v8 Cortex technology • Kryo Gold plus: high-performance core up to 2.7 GHz • Kryo Gold: three high-performance cores at 2.4 GHz • Kryo Silver: four low-power cores at 1.9 GHz
Digital signal processing and AI	Compute Hexagon DSP with dual HVX and Hexagon Co-processor (Hexagon CP) 2.0 and Hexagon Tensor Accelerator • Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, and so on • The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions
Adreno GPU (Graphic Processing Unit)	• Adreno GPU 642L • OpenGL ES 3.2, Vulkan 1.x • OpenCL 2.0, DX FL12
Adreno VPU (Video Processing Unit)	Adreno VPU 633 – fifth-generation UHD video processing unit • Video decode: Up to 4K@60FPS for H.264/H.265/VP9 • Video encode: Up to 4K@30FPS for H.264/H.265 • Video concurrency: 1080P@60FPS decode and 1080P@60FPS encode/4K@30FPS decode + 1080P@30FPS encode • HDR playback: Support for HDR10 and HDR10+ • HFR capture: 720P@480FPS or 1080P@240FPS
Display support	Adreno DPU 1075: • Maximum resolution for internal panel: FHD+ 144 Hz QCLTM, HDR10+, WCG, improved • inline rot, rounded corner, SPR, Demura, CWB-ROI • One 4-lane; DSI D-PHY 1.2 or C-PHY 1.2; VESA DSC 1.2 • 4K@60FPS display support over DisplayPort (USB3 + DisplayPort concurrency)

Item	Description
Camera support	Qualcomm Spectra 570L: 36 + 22MP@30FPS/3x 22MP@30FPS ZSL Qualcomm Spectra 570L ISP supports connectivity to multiple cameras due to five C-PHY/D-PHY interfaces. • Real-time sensor input resolution: 22 + 22 + 22 • Three IFE + two IFE lite, up to eight sensors, five concurrent MIPI CSI configurable in 4 + 4 +4 + 4 + 4 configurations • 5x D-PHY v1.2 /C-PHY v1.2
WLAN/BT	The WCN6856, Tri-band 2x2 MIMO DBS 802.11ax + Bluetooth 5.2 • supports 802.11ax Wi-Fi and Bluetooth 5.2. • supports simultaneous operation on 2.4 GHz and 5 GHz or 6 GHz (DBS).

Table 1-2.Key features and performance of TurboX C6490 SOM

Item	Description
Platform	Snapdragon™ QCS6490 Qualcomm® Kryo™ CPU 670 Qualcomm® Adreno™ GPU 642L, Adreno 633 VPU, Adreno DPU 1075 Qualcomm® Compute Hexagon™ DSP with dual HVX, Hexagon Co-processor (Hexagon CP) 2.0 and Hexagon Tensor Accelerator Qualcomm® Spectra™ 570L image processing
Memory	4GB+64GB or 8GB+128GB (later variant)
Air Interface	NA
Data Rate	NA
Connectivity	802.11 ax over PCIe with DBS, 2x2 MIMO (Wi-Fi 6E), Bluetooth 5.2
Video Encode	4K@30FPS for H.264/H.265
Video Decode	4K@60FPS for H.264/H.265/VP9
Display interfaces	1x MIPI-DSI 4-lane; FHD+ (1080x2520) 8L @120FPS
Camera Interfaces	5 x 4-lane MIPI CSI D-PHY (2 of them compatible with 3-lane MIPI CSI C-PHY up to 48M camera)
Peripherals	1 x USB 3.1 with DP, 1 x USB2.0, 1 x PCIe Gen3 2-lane, 2 x Sound Wire, 1 x SDC for SD card, 3 x DMIC Interfaces, GPIOs, QUPs (UART/I2C/SPI)
Operating Environment	Operation Temperature: -25°C ~ 75°C Operation Humidity: 5%~95%, non-condensing
Form Factor	LGA
Voltage	3.4V~4.5V
Dimensions	42.5mm x 35.5mm x 2.75mm
Operating System	Android 12

1.2. Hardware block diagram

N/A

1.3. Major component location

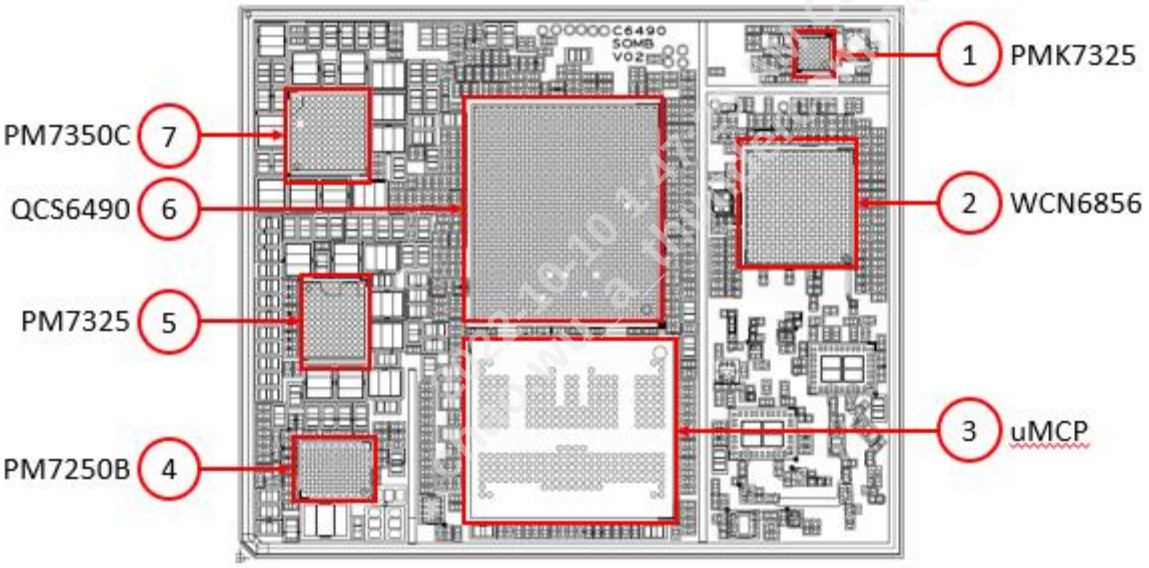

Figure 1-2. TurboX C6490 SOM Key Component Location

1.4. Mechanical size

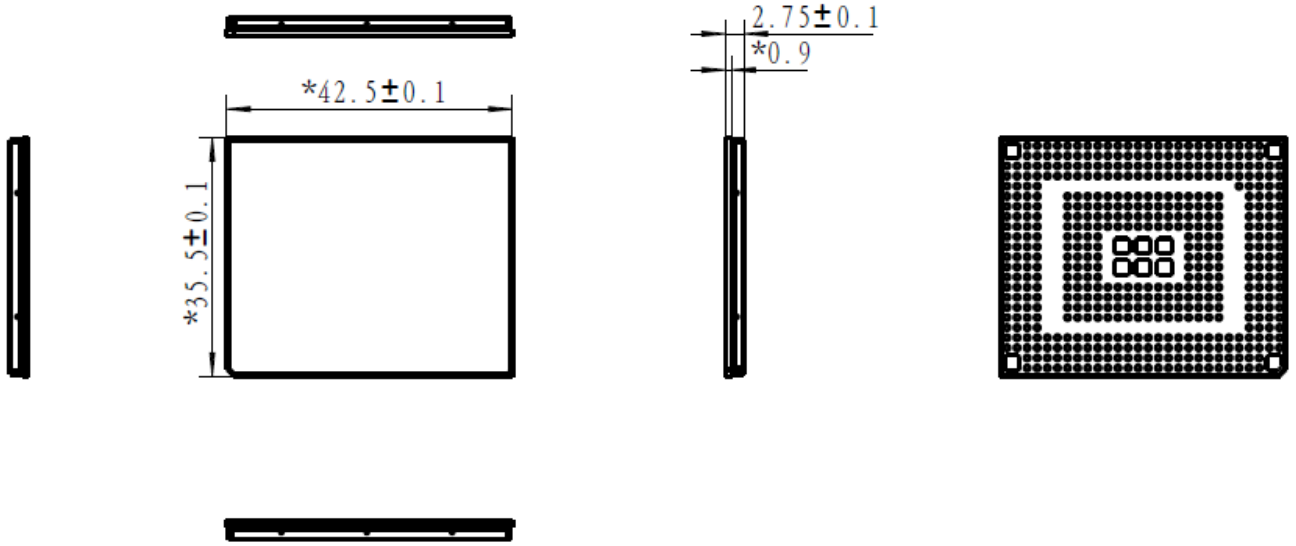

Figure 1-3.TurboX C6490 SOM Mechanical Dimensions

1.5. Package dimensions

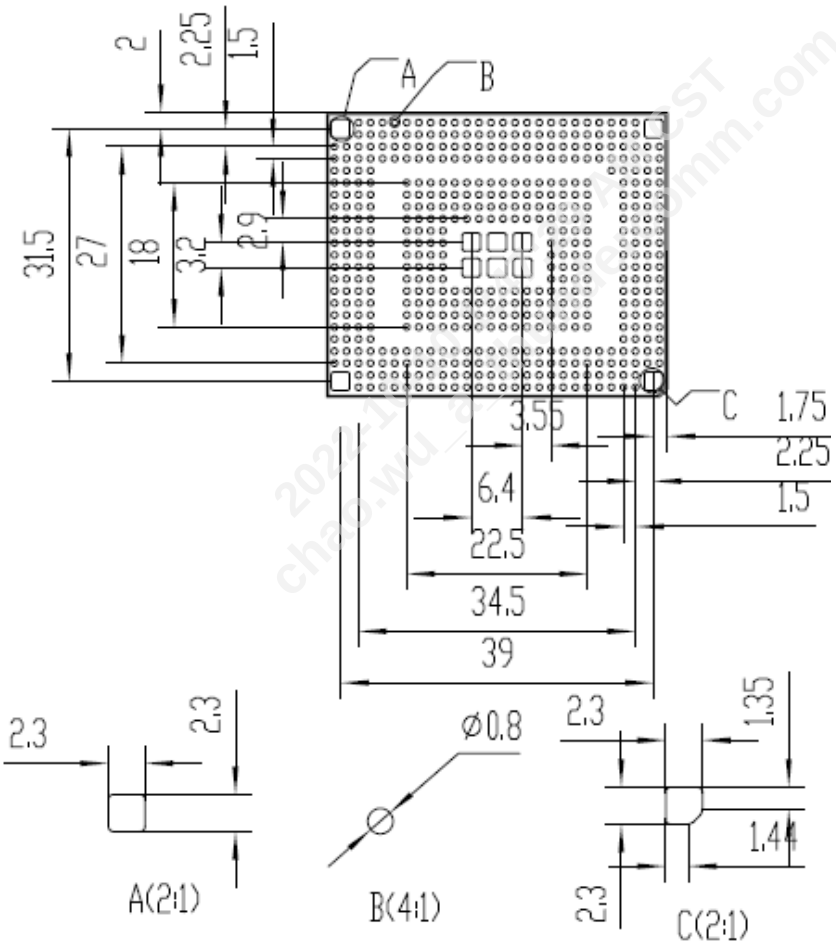

Figure 1-4.TurboX C6490 SOM Package Dimensions

1.6. Stencil design and aperture

To supply sufficient soldering paste and keep reliable soldering joints, add the thickness of stencil partly on the top surface. The stencil aperture for single sheet cannot be greater than 3.0mm×4.0mm and the exceeded part should be divided into smaller apertures with applicable shelves. A clearance of over 2.0mm should be kept between the outward end of the aperture and the component if there are components around the module.

➲ **NOTE**:

- For the convenience of heating and repairing, it is recommended that no components should be placed in the area at the backside of the module on PCB.
- In order to avoid reverse polarity of the module, it is recommended to use asymmetric pads at the bottom of the module to identify the module polarity during module placement.
- It is not recommended to add any silkscreen in the area where the module is mounted to avoid the height that may influence the solder paste printing and soldering quality.
- When there is a need to step-up the stencil, all 01005/0201, 0.4mm-pitch and 0.5mm-pitch components should be kept over 5.0mm away from the stepped-up area to avoid solder bridging that is caused by thicker solder paste.

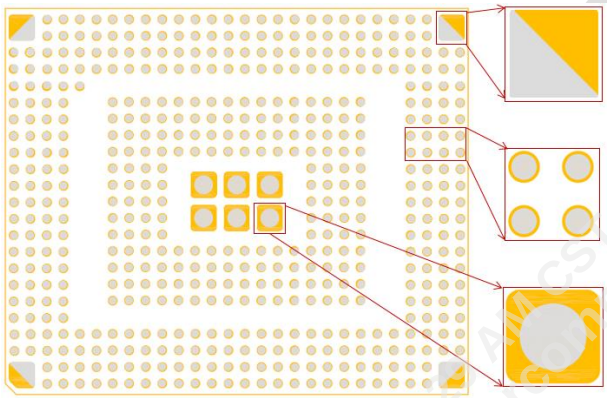

Figure 1-5.Stencil Aperture Diagram

Requirement description

- **Stencil thickness**
  Area of the module should be partly stepped-up to 0.15mm-0.18mm.

- **Pads on four sides**
  The aperture for each single pad should be centered with area reduced to 75%-85%. And the shape should be rectangle with round chamfers (see Figure 1-5).

- **Pads at four corners**
  The stencil aperture should be designed with 60%~65% area of the corresponding pad (see Figure 1-5).

- **Ground pads at the center**
  The stencil aperture should be designed with 60%~65% area of the corresponding pad (see Figure 1-5).

1.7. Module laser marking

Refer to Figure 1-6 for the module laser marking of TurboX C6490.

Figure 1-6.Laser Marking of C6490 SOM

Table 1-3.Module laser marking description

1. Company name/logo	5. Serial number
2. Product name	6. Brand name
3. PCBA version	7. QR code
4. Product number	8. Place of origin

➲ **NOTE**:

- Figure 1-6 is for reference only and may vary with the specific module.
- The part number may be updated. Please confirm with the supplier about the accurate information.

1.8. SMT assembly guide

Refer to *[tc-A-15111]_TurboX Common SMT Assembly Guidelines_V1.1*.

For more information, please contact us at service@thundercomm.com.

Chapter 2. Interface Specifications

This chapter introduces definitions of all the interfaces to facilitate design and verification on Thundercomm TurboX C6490 SOM.

2.1. Interface parameter definition

Table 2-1. Interfaces parameter definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DI	Digital input (CMOS)
DSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DO	Digital output (CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
PX-3	Power group 3, it is 1.8V.
P2	SDC Power group 2, it is 1.8V or 2.95V.

2.2. Interface detailed description

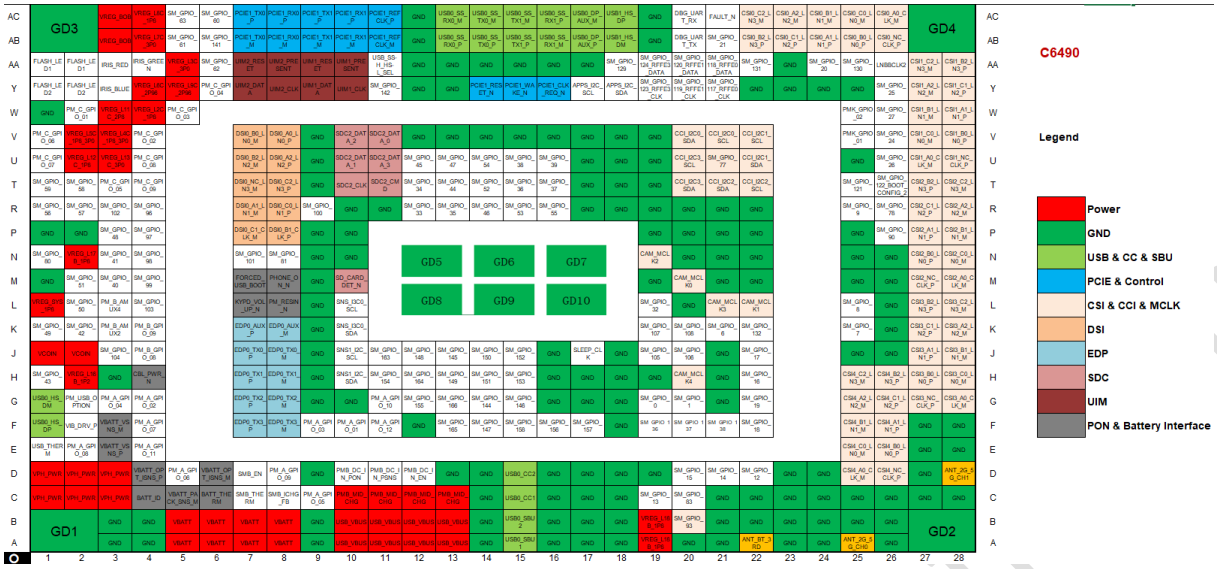

Figure 2-1. TurboX C6490 SOM Pin Location

2.2.1. Power supply interface

Table 2-2 describes all interfaces of SOM power supply.

For the detailed parameter request, refer to Chapter 3. Electrical Characteristics.

Table 2-2. Power supply definition

Pin name	Pin	Type	Description, V_typ@I_rated
VBATT	A5,A6,A7,A8,B5,B6,B7,B8	PI,PO	Power supply input for SOM. Battery voltage node, output for charging, and input for all operations.
VPH_PWR	C1,C2,C3,D1,D2,D3	PO	Primary system supply node
USB_VBUS	A10,A11,A12,A13,B10,B11,B12,B13	PO,PI	Power entry node for the charger. USB output during USB-OTG operation.
VCOIN	J1,J2	PI,PO	Coin-cell charge and supply recommend to use 22uF x 3 for VCOIN
VREG_BOB	AB3,AC3	PO	Buck-boost output 3.3V@1A (will increase to 3.6V during the bootup of the SOM)
VREG_L18B_1P8	A19,B19	PO	PX-3, 1.8V Just for GPIO pull-up
VREG_L2C_1P8	W4	PO	MEMS_DMIC_VDD, 1.62V~1.98V, 1.8V typ
VREG_L3C_3P0	AA5	PO	Touch screen, 2.7V~3.54V, 3V typ
VREG_L7C_3P0	AB4	PO	Sensors, 2.7V~3.54V, 3V typ
VREG_L8C_1P8	AC4	PO	Sensors, 1.62V~2V, 1.8V typ
VREG_L11C_2P8	W3	PO	Connectivity, 1.65V~3.54V, 2.8V typ
VREG_L12C_1P8	U2	PO	OLED VDDIO, 1.62V~1.98V, 1.8V typ
VREG_L13C_3P0	U3	PO	OLED VCI, 2.7V~3.54V, 2.8V typ

Pin name	Pin	Type	Description, V_typ@I_rated
VREG_L16B_1P2	H2	PO	1.2V~1.3V, 1.2V typ
VREG_L17B_1P8	N2	PO	WCD_VDD_BUCK, 1.8V~1.9V, 1.8V typ
VREG_SYS_1P8	L1	PO	System 1.8 V I/O output Reserved for debug, please leave it floating
VIB_DRV_P	F2	PO	Power supply for haptics driver
GND	A3,A4,A9,A14,A16, A17,A18,A20,A21, A23,A24,A26,B3,B4,B9,B14 ,B16,B17,B18,B21,B22,B23 ,B24,B25,B26,C14,C16,C17, C18,C21,C22,C23,C24,C25, C26,C27,C28,D9,D13,D14, D16,D17,D18,D19,D23,D24 ,D27,E27,E28,F12,F18,F27, F28,G9,G10,G16,G17,G18, G21,H3,H9,H16,H17,H18,H 19,H21,J9,J16,Y22,J18,J21,J 25,J26,K9,K26,L9,L20,L26, M1,M9,M19,M21,M22,M2 5,M26,N9,N10,N20,N21,N 22,N25,N26,P9,P10,P19,P2 0,P21,P22,P25,R10,R11,R1 7,R18,R19,R20,R21,R22,T9, T17,T18,T19,U9,U17,U18,U 19,V9,V12,V13,V14,V15,V1 6,V17,V18,V19,W1,Y12,Y13, AA12,AA13,AA14,AA15,AA 16,AA17,AA23,Y25,AB12,A B19,AC12,AC19,U25,P1,P2, Y24,Y23,GD1,GD2,GD3,GD 4,GD5,GD6,GD7,GD8,GD9, GD10	GND	GND

2.2.2. Charger interface

T.B.D.

2.2.3. Camera interfaces

The SOM supports 5x 4-lane camera interfaces.

Table 2-3. Camera interface definition

Pin name	Pin	Volt.	Type	Decription	Notes
CCI_I2C0_SCL	V21	PX-3	DO	Dedicated camera control interface I2C serial data	Pull up needed on Carrier board
CCI_I2C0_SDA	V20	PX-3	B	Dedicated camera control interface I2C serial data	
CAM_MCLK0	M20	PX-3	DO	Camera master clock 0	
CSI0_NC_CLK_P	AB26	CSI	AI	MIPI CSI 0 (D-PHY), differential clock – positive	MIPI signals of Camera0
CSI0_A0_CLK_M	AC26	CSI	AI	MIPI CSI 0 (D-PHY), differential clock – negative	
CSI0_B0_LN0_P	AB25	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 0 – positive	
CSI0_C0_LN0_M	AC25	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 0 – negative	
CSI0_A1_LN1_P	AB24	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – positive	
CSI0_B1_LN1_M	AC24	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – negative	
CSI0_C1_LN2_P	AB23	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 2 – positive	
CSI0_A2_LN2_M	AC23	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 2 – negative	
CSI0_B2_LN3_P	AB22	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 3– positive	
CSI0_C2_LN3_M	AC22	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 3 – negative	
CCI_I2C1_SCL	V22	PX-3	DO	Dedicated camera control interface I2C serial data	Pull up needed on Carrier board
CCI_I2C1_SDA	U22	PX-3	B	Dedicated camera control interface I2C serial data	
CAM_MCLK1	L22	PX-3	DO	Camera master clock 1	
CSI1_NC_CLK_P	U28	CSI	AI	MIPI CSI 1 (D-PHY), differential clock – positive MIPI CSI 1 (C-PHY), no connect	MIPI signals of Camera1
CSI1_A0_CLK_M	U27	CSI	AI	MIPI CSI 1 (D-PHY), differential clock – negative MIPI CSI 1 (C-PHY), trio lane 0 – A	
CSI1_B0_LN0_P	V28	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 0 – positive MIPI CSI 1 (C-PHY), trio lane 0 – B	
CSI1_C0_LN0_M	V27	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 0 – negative MIPI CSI 1 (C-PHY), trio lane 0 – C	
CSI1_A1_LN1_P	W28	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 1 – positive MIPI CSI 1 (C-PHY), trio lane 1 – A	
CSI1_B1_LN1_M	W27	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 1 – negative MIPI CSI 1 (C-PHY), trio lane 1 – B	
CSI1_C1_LN2_P	Y28	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 2 – positive MIPI CSI 1 (C-PHY), trio lane 1 – C	
CSI1_A2_LN2_M	Y27	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 2 – negative MIPI CSI 1 (C-PHY), trio lane 2 – A	
CSI1_B2_LN3_P	AA28	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 3– positive MIPI CSI 1 (C-PHY), trio lane 2 – B	

Pin name	Pin	Volt.	Type	Decription	Notes
CSI1_C2_LN3_M	AA27	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 3 – negative MIPI CSI 1 (C-PHY), trio lane 2 – C	
CCI_I2C2_SCL	T22	PX-3	DO	Dedicated camera control interface IC serial data	Pull up needed on Carrier board
CCI_I2C2_SDA	T21	PX-3	B	Dedicated camera control interface IC serial data	
CAM_MCLK2	N19	PX-3	DO	Camera master clock 2	
CSI2_NC_CLK_P	M27	CSI	AI	MIPI CSI 2 (D-PHY), differential clock – positive	MIPI signals of Camera2
CSI2_A0_CLK_M	M28	CSI	AI	MIPI CSI 2 (D-PHY), differential clock – negative	
CSI2_B0_LN0_P	N27	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 0 – positive	
CSI2_C0_LN0_M	N28	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 0 – negative	
CSI2_A1_LN1_P	P27	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 1 – positive	
CSI2_B1_LN1_M	P28	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 1 – negative	
CSI2_C1_LN2_P	R27	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 2 – positive	
CSI2_A2_LN2_M	R28	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 2 – negative	
CSI2_B2_LN3_P	T27	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 3– positive	
CSI2_C2_LN3_M	T28	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 3 – negative	
CCI_I2C3_SCL	U20	PX-3	DO	Dedicated camera control interface I2C serial data	Pull up needed on Carrier board
CCI_I2C3_SDA	T20	PX-3	B	Dedicated camera control interface I2C serial data	
CAM_MCLK3	L21	PX-3	DO	Camera master clock 3	
CSI3_NC_CLK_P	G27	CSI	AI	MIPI CSI 3 (D-PHY), differential clock – positive MIPI CSI 3 (C-PHY), no connect	MIPI signals of Camera3
CSI3_A0_CLK_M	G28	CSI	AI	MIPI CSI 3 (D-PHY), differential clock – negative MIPI CSI 3 (C-PHY), trio lane 0 – A	
CSI3_B0_LN0_P	H27	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 0 – positive MIPI CSI 3 (C-PHY), trio lane 0 – B	
CSI3_C0_LN0_M	H28	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 0 – negative MIPI CSI 3 (C-PHY), trio lane 0 – C	
CSI3_A1_LN1_P	J27	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 1 – positive MIPI CSI 3 (C-PHY), trio lane 1 – A	
CSI3_B1_LN1_M	J28	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 1 – negative MIPI CSI 3 (C-PHY), trio lane 1 – B	
CSI3_C1_LN2_P	K27	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 2 – positive MIPI CSI 3 (C-PHY), trio lane 1 – C	
CSI3_A2_LN2_M	K28	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 2 – negative MIPI CSI 3 (C-PHY), trio lane 2 – A	
CSI3_B2_LN3_P	L27	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 3– positive MIPI CSI 3 (C-PHY), trio lane 2 – B	
CSI3_C2_LN3_M	L28	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 3 – negative MIPI CSI 3 (C-PHY), trio lane 2 – C	

Pin name	Pin	Volt.	Type	Decription	Notes
CAM_MCLK4	H20	PX-3	DO	Camera master clock 4	
CSI4_NC_CLK_P	D26	CSI	AI	MIPI CSI 4 (D-PHY), differential clock – positive	MIPI signals of Camera4
CSI4_A0_CLK_M	D25	CSI	AI	MIPI CSI 4 (D-PHY), differential clock – negative	
CSI4_B0_LN0_P	E26	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 0 – positive	
CSI4_C0_LN0_M	E25	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 0 – negative	
CSI4_A1_LN1_P	F26	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 1 – positive	
CSI4_B1_LN1_M	F25	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 1 – negative	
CSI4_C1_LN2_P	G26	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 2 – positive	
CSI4_A2_LN2_M	G25	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 2 – negative	
CSI4_B2_LN3_P	H26	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 3– positive	
CSI4_C2_LN3_M	H25	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 3 – negative	

2.2.4. Display interface

The SOM supports 1x 4-lane MIPI_DSI interfaces.

Table 2-4. Display interfaces definition

Pin name	Pin	Volt.	Typ	Description	Notes
MIPI_DSI0_CLK_P	P8	DSI	AO	MIPI DSI 4 (D-PHY), differential clock – positive	MIPI0 signals for MIPI LCM. Compliant with MIPI Alliance Specification for Display Serial Interface.
MIPI_DSI0_CLK_M	P7	DSI	AO	MIPI DSI 4 (D-PHY), differential clock – negative	
MIPI_DSI0_L0_P	V8	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 0 – positive	
MIPI_DSI0_L0_M	V7	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 0 – negative	
MIPI_DSI0_L1_P	R8	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 1 – positive	
MIPI_DSI0_L1_M	R7	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 1 – negative	
MIPI_DSI0_L2_P	U8	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 2 – positive	
MIPI_DSI0_L2_M	U7	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 2 – negative	
MIPI_DSI0_L3_P	T8	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 3– positive	
MIPI_DSI0_L3_M	T7	DSI	AO	MIPI DSI 4 (D-PHY), differential lane 3 – negative	
EDP0_AUX_P	K7	EDP	B	eDP 1.4 auxillary channel – positive	DSI and eDP are mutually exclusive. Concurrent usage of DSI; eDP function is not supported on the current software version.
EDP0_AUX_M	K8	EDP	B	eDP 1.4 auxillary channel – negative	
EDP0_TX0_P	J7	EDP	AO	eDP 1.4 transmit channel 0 – positive	
EDP0_TX0_M	J8	EDP	AO	eDP 1.4 transmit channel 0 – negative	
EDP0_TX1_P	H7	EDP	AO	eDP 1.4 transmit channel 1 – positive	
EDP0_TX1_M	H8	EDP	AO	eDP 1.4 transmit channel 1 – negative	
EDP0_TX2_P	G7	EDP	AO	eDP 1.4 transmit channel 2 – positive	
EDP0_TX2_M	G8	EDP	AO	eDP 1.4 transmit channel 2 – negative	
EDP0_TX3_P	F7	EDP	AO	eDP 1.4 transmit channel 3 – positive	
EDP0_TX3_M	F8	EDP	AO	eDP 1.4 transmit channel 3 – negative	

2.2.5. Touchscreen interface

Touchscreen panels are supported using I2C buses and GPIOs configured as discrete digital inputs.

Table 2-5. Touchscreen interfaces definition

Pin name	Pin	Voltage	Type	Description
SM_GPIO_52	T14	PX-3	OD	TP0_SDA
SM_GPIO_53	R15	PX-3	OD	TP0_SCL
SM_GPIO_81	N8	PX-3	DO	TP0_INT
SM_GPIO_105	J19	PX-3	DI	TP0_RST

2.2.6. Audio interface

The SOM provides Soundwire, DMIC and I2S interfaces for audio. Soundwire interface is special for external codec IC, which can build audio functions of the systeme. DMIC interface can be used to directly connect up to 6 PDM MICs.

Table 2-6. Audio interface definition

Pin name	Pin	Voltage	Type	Description	Notes
WCD_SWR_TX_CLK	G14	PX-3	DO	Soundwire transmit for WCD	SM_GPIO_144
WCD_SWR_TX_DATA0	J13	PX-3	DO		SM_GPIO_145
WCD_SWR_TX_DATA1	G15	PX-3	DO		SM_GPIO_146
WCD_SWR_TX_DATA3	F15	PX-3	DO		SM_GPIO_158
WCD_SWR_RX_CLK	F14	PX-3	DI	Soundwire receive for WCD	SM_GPIO_147
WCD_SWR_RX_DATA0	J12	PX-3	DI		SM_GPIO_148
WCD_SWR_RX_DATA1	H13	PX-3	DI		SM_GPIO_149
WSA_SWR_CLK	H11	PX-3	IO	AUDIO PA Soundwire	SM_GPIO_154
WSA_SWR_DATA	G12	PX-3	IO		SM_GPIO_155
DMIC01_CLK	J14	PX-3	DO	DMIC I/F	SM_GPIO_150
DMIC01_DATA	H14	PX-3	IO		SM_GPIO_151
DMIC23_CLK	J15	PX-3	DO		SM_GPIO_152
DMIC23_DATA	H15	PX-3	IO		SM_GPIO_153
DMIC45_CLK	F16	PX-3	DO		SM_GPIO_156
DMIC45_DATA	F17	PX-3	IO		SM_GPIO_157
PRI_MI2S_MCLK	R4	PX-3	DO	Primary MI²S master clock	SM_GPIO_96
MI2S0_SCK	P4	PX-3	DO	MI2S0	SM_GPIO_97
MI2S0_DATA0	N4	PX-3	B		SM_GPIO_98
MI2S0_DATA1	M4	PX-3	B		SM_GPIO_99
MI2S0_WS	R9	PX-3	B		SM_GPIO_100
MI2S2_SCK	N7	PX-3	B	MI2S2	SM_GPIO_101
MI2S2_DATA0	R3	PX-3	B		SM_GPIO_102
MI2S2_WS	L4	PX-3	B		SM_GPIO_103
MI2S2_DATA1	J3	PX-3	B		SM_GPIO_104
SEC_MI2S_MCLK MI2S1_DATA1	J19	PX-3	DO B	MI2S1	SM_GPIO_105
MI2S1_SCK	J20	PX-3	B		SM_GPIO_106
MI2S1_DATA0	K19	PX-3	B		SM_GPIO_107
MI2S1_WS	K20	PX-3	B		SM_GPIO_108
LPI_QUA_MI2S_SCK	G14	PX-3	B	LPI MI2S 4 lanes	SM_GPIO_144
LPI_QUA_MI2S_WS	J13	PX-3	B		SM_GPIO_145
LPI_QUA_MI2S_DATA0	G15	PX-3	B		SM_GPIO_146

Pin name	Pin	Voltage	Type	Description	Notes
LPI_QUA_MI2S_DATA1	F14	PX-3	B		SM_GPIO_147
LPI_QUA_MI2S_DATA2	J12	PX-3	B		SM_GPIO_148
LPI_QUA_MI2S_DATA3	H13	PX-3	B		SM_GPIO_149
LPI_I2S1_CLK	J14	PX-3	B	LPI I2S1	SM_GPIO_150
LPI_I2S1_WS	H14	PX-3	B		SM_GPIO_151
LPI_I2S1_DATA0	J15	PX-3	B		SM_GPIO_152
LPI_I2S1_DATA1	H15	PX-3	B		SM_GPIO_153
LPI_I2S2_CLK	H11	PX-3	B	LPI I2S2	SM_GPIO_154
LPI_I2S2_WS	G12	PX-3	B		SM_GPIO_155
LPI_I2S2_DATA0	F16	PX-3	B		SM_GPIO_156
LPI_I2S2_DATA1	F17	PX-3	B		SM_GPIO_157

2.2.7. USB & DisplayPort interface

The SOM supports 1x USB 3.1 GEN1, with Type-C with DisplayPort and 1x USB2.0.

Table 2-7. USB &DP interface definition

Pin name	Pin	Type	Description	Notes
PM_USB_OPTION	G2	AI	Used to select different PON options based on pull-down (PD) resistor value Configuration selection for micro USB and Type-C connectors. Float for Type-C and connect to ground with 0 Ohm for micro USB.	
USB_THERM	E1	AI	USB Type-C connector temperature sensor	
USB_SS-H_HS-L_SEL	AA11	DI	Connected to ID Pin of Micro USB. Not supported on SOM by default.	
USB0_CC1	C15	AI, PO	CC1 Pin for the USB Type-C connector or OTG mode enable	
USB0_CC2	D15	AI, PO	CC2 Pin for the USB Type-C connector	
USB0_SBU1	A15	DI	Type-C side band signal SBU1; protected to 22 V max.	
USB0_SBU2	B15	DO	Type-C side band signal SBU2; protected to 22 V max.	
USB0_DP_AUX_P	AB17	AI, AO	DisplayPort auxiliary channel – positive	Native DP
USB0_DP_AUX_M	AC17	AI, AO	DisplayPort auxiliary channel – negative	
USB0_HS_DP	F1	AI, AO	USB 2.0 high-speed data – positive	
USB0_HS_DM	G1	AI, AO	USB 2.0 high-speed data – negative	
USB0_SS_TX0_P	AB14	AO	USB 3.0 Type C PHY transmit 0 – positive	
USB0_SS_TX0_M	AC14	AO	USB 3.0 Type C PHY transmit 0 – negative	
USB0_SS_RX0_P	AB13	AI	USB 3.0 Type C PHY receiver 0 – positive	
USB0_SS_RX0_M	AC13	AI	USB 3.0 Type C PHY receiver 0 – negative	
USB0_SS_TX1_P	AB15	AO	USB 3.0 Type C PHY transmit 1 – positive	
USB0_SS_TX1_M	AC15	AO	USB 3.0 Type C PHY transmit 1 – negative	
USB0_SS_RX1_P	AC16	AI	USB 3.0 Type C PHY receiver 1 – positive	
USB0_SS_RX1_M	AB16	AI	USB 3.0 Type C PHY receiver 1 – negative	
USB1_HS_DP	AC18	AI, AO	USB1_HS – positive	USB1 2.0
USB1_HS_DM	AB18	AI, AO	USB1_HS – negative	

2.2.8. PCIe interface

The SOM supports one Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

Table 2-8. PCIe interface definition

Pin name	Pin	Voltage	Type	Description
PCIE1_REFCLK_P	AC11	-	AI, AO	PCIe 1 Gen 3 reference clock – positive
PCIE1_REFCLK_M	AB11	-	AI, AO	PCIe 1 Gen 3 receive lane 0 – negative
PCIE1_TX0_P	AC7	-	AO	PCIe 1 Gen 3 Transmit lane 0– positive
PCIE1_TX0_M	AB7	-	AO	PCIe 1 Gen 3 Transmit lane 0– negative
PCIE1_RX0_P	AC8	-	AI	PCIe 1 Gen 3 receive lane 0 – positive
PCIE1_RX0_M	AB8	-	AI	PCIe 1 Gen 3 receive lane 0 – negative
PCIE1_TX1_P	AC9	-	AO	PCIe 1 Gen 3 Transmit lane 1– positive
PCIE1_TX1_M	AB9	-	AO	PCIe 1 Gen 3 Transmit lane 1– negative
PCIE1_RX1_P	AC10	-	AI	PCIe 1 Gen 3 receive lane 1 – positive
PCIE1_RX1_M	AB10	-	AI	PCIe 1 Gen 3 receive lane 1 – negative
PCIE1_CLK_REQ_N	Y16	PX-3	DI	PCIE Clock request
PCIE1_RESET_N	Y14	PX-3	DO	PCIe reset signal
PCIE1_WAKE_N	Y15	PX-3	DI	PCIe wake up signal

2.2.9. SDIO interface

The SOM supports 1 x 4-lane SDIO, SDC2 connected to SD card.

The SDIO is a high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 200 MHz.
- The signals routing should be 50Ω ±10% impedance control.
- CLK to DATA/CMD length matching less than 1mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

Table 2-9. SDIO interface definition

Pin name	Pin	Volt.	Type	Description	Notes
VREG_L9C_2P96	Y5	-	DO	SD Card Power Supply	
VREG_L6C_2P96	Y4	-	PO	SD Card pull up power	
SDC2_CLK	T10	P2	PO	Secure digital controller 2 clock	
SDC2_CMD	T11	P2	DO-NP:pdpukp	Secure digital controller 2 command	
SDC2_DATA_0	V11	P2	BH-NP:pdpukp	Secure digital controller 2 data bit 0	
SDC2_DATA_1	U10	P2	BH-NP:pdpukp	Secure digital controller 2 data bit 1	
SDC2_DATA_2	V10	P2	BH-NP:pdpukp	Secure digital controller 2 data bit 2	
SDC2_DATA_3	U11	P2	BH-NP:pdpukp	Secure digital controller 2 data bit 3	
SD_CARD_DET_N	M10	PX-3	BH-NP:pdpukp	Insert detection	SM_GPIO_91

2.2.10. SSC interface

The SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the MSM device is in sleep mode.

The SSC core has dedicated I/O to communicate with the sensors. The I/O scan support I2C and SPI interfaces.

Table 2-10. SSC interface definition

Pin name	Pin	Voltage	Type	Description	Notes
SNS_I3C0_SDA	K10	PX-3	IO	These I3C signals are dedicated to Sensor	SM_GPIO_159
SNS_I3C0_SCL	L10	PX-3	IO		SM_GPIO_160
SNS1_I2C_SDA	H10	PX-3	IO	These I2C signals are dedicated to Sensor	SM_GPIO_161
SNS1_I2C_SCL	J10	PX-3	IO		SM_GPIO_162
SM_GPIO_163	J11	PX-3	IO	Snapdragon™ Sensor Core SPI signals	SM_GPIO_163
SM_GPIO_164	H12	PX-3	IO		SM_GPIO_164
SM_GPIO_165	F13	PX-3	IO		SM_GPIO_165
SM_GPIO_166	G13	PX-3	IO		SM_GPIO_166

2.2.11. QUP interface

These GPIOs are available as QUP (Qualcomm universal peripheral) interface ports that can be configured for UART, SPI, I2C or I3C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus needs to be supplemented by a 2.2 kΩ pull-up resistor.

Table 2-11. QUP interface definition

Pin name	Pin	Voltage	Type	Description	Notes
SM_GPIO_0	G19	PX-3	IO	QUP0 SE0 Lane0/1	
SM_GPIO_1	G20	PX-3	IO		
PCIE1_RESET_N	Y14	PX-3	IO	QUP0 SE0 Lane2/3 QUP0 SE7 Lane4/5	SM_GPIO_2
PCIE1_WAKE_N	Y15	PX-3	IO		SM_GPIO_3
APPS_I2C_SDA	Y18	PX-3	IO	QUP0 SE1 Lane0/1	SM_GPIO_4
APPS_I2C_SCL	Y17	PX-3	IO		SM_GPIO_5
SM_GPIO_6	K21	PX-3	IO	QUP0 SE0 Lane2 QUP0 SE7 Lane6	
SM_GPIO_7	K25	PX-3	IO	QUP0 SE1 Lane3	
SM_GPIO_8	L25	PX-3	IO	QUP0 SE2 Lane0/1	
SM_GPIO_9	R25	PX-3	IO		
SM_GPIO_12	D22	PX-3	IO	QUP0 SE3	
SM_GPIO_13	C19	PX-3	IO		
SM_GPIO_14	D21	PX-3	IO		
SM_GPIO_15	D20	PX-3	IO		
SM_GPIO_16	H22	PX-3	IO	QUP0 SE4	

Pin name	Pin	Voltage	Type	Description	Notes
SM_GPIO_17	J22	PX-3	IO		
SM_GPIO_18	F22	PX-3	IO		
SM_GPIO_19	G22	PX-3	IO		
SM_GPIO_20	AA24	PX-3	IO	QUP0 SE5	
SM_GPIO_21	AB21	PX-3	IO		
DBG_UART_TX	AB20	PX-3	IO		SM_GPIO_22
DBG_UART_RX	AC20	PX-3	IO		SM_GPIO_23
SM_GPIO_24	V26	PX-3	IO	QUP0 SE6	
SM_GPIO_25	Y26	PX-3	IO		
SM_GPIO_26	U26	PX-3	IO		
SM_GPIO_27	W26	PX-3	IO		
SM_GPIO_32	L19	PX-3	IO	QUP1 SE0	
SM_GPIO_33	R12	PX-3	IO		
SM_GPIO_34	T12	PX-3	IO		
SM_GPIO_35	R13	PX-3	IO		
SM_GPIO_36	T15	PX-3	IO	QUP1 SE1	
SM_GPIO_37	T16	PX-3	IO		
SM_GPIO_38	U15	PX-3	IO		
SM_GPIO_39	U16	PX-3	IO		
SM_GPIO_40	M3	PX-3	IO	QUP1 SE2	
SM_GPIO_41	N3	PX-3	IO		
SM_GPIO_42	K2	PX-3	IO		
SM_GPIO_43	H1	PX-3	IO		
SM_GPIO_44	T13	PX-3	IO	QUP1 SE3	
SM_GPIO_45	U12	PX-3	IO		
SM_GPIO_46	R14	PX-3	IO		
SM_GPIO_47	U13	PX-3	IO		
SM_GPIO_48	PX-3	PX-3	IO	QUP1 SE4	
SM_GPIO_49	K1	PX-3	IO		
SM_GPIO_50	L2	PX-3	IO		
SM_GPIO_51	M2	PX-3	IO		
SM_GPIO_52	T14	PX-3	IO	QUP1 SE5	
SM_GPIO_53	R15	PX-3	IO		
SM_GPIO_54	U14	PX-3	IO		
SM_GPIO_55	R16	PX-3	IO		
SM_GPIO_56	R1	PX-3	IO	QUP1 SE6	
SM_GPIO_57	R2	PX-3	IO		
SM_GPIO_58	T2	PX-3	IO		
SM_GPIO_59	T1	PX-3	IO		

Pin name	Pin	Voltage	Type	Description	Notes
SM_GPIO_60	AC6	PX-3	IO	QUP1 SE7 Lane0/1	
SM_GPIO_61	AB5	PX-3	IO		
SM_GPIO_62	AA6	PX-3	IO	QUP1 SE7 Lane2/SE6 Lane4	
SM_GPIO_63	AC5	PX-3	IO	QUP1 SE6 Lane3/SE6 Lane5	

2.2.12. Debug UART interface

Table 2-12. Debug UART interface definition

Pin name	Pin	Voltage	Type	Description	Notes
DBG_UART_TX	AB20	PX-3	DI	QUP0 SE5 UART signals, can use for debug	SM_GPIO_22
DBG_UART_RX	AC20	PX-3	DO		SM_GPIO_23

2.2.13. Power on interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the available power sources of the device, and enable the correct source. Press the KPD_PWR_N for ~2 s to boot the system properly. Power on/off key signal can be connected to ground through SOM Pin M8, PHONE_ON_N (200 kΩ internally pulled up to 1.1 V).

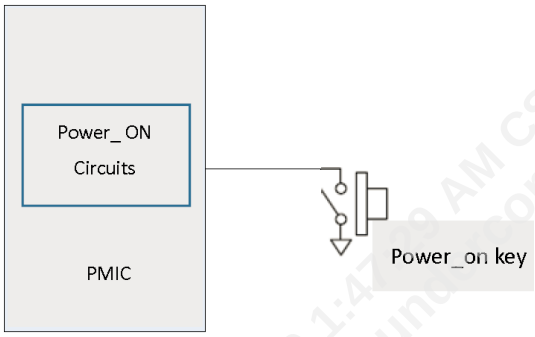

Figure 2-1.Power on Signal

Table 2-13. Power on interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PHONE_ON_N	M8	-	DI	Power-on key ground switch (200 kΩ internal PU to 1.1 V)	

2.2.14. Reset interface

You can generate a mandatory reset by a long key press of RESIN_N, KPD_PWR_N, or RESIN_N plus KPD_PWR_N in combination.

Table 2-14. Reset interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PM_RESIN_N	L8	pulled up internally to 1.8V	DI	Volume down/Reset key signal, Low active	

2.2.15. Keys interface

Table 2-15. Keys interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PHONE_ON_N	M8	200 kΩ internal PU to 1.1 V	DI	Power-on key ground switch	
KYPD_VOL_UP_N	L7	-	DI	Keypad volume up button	
PM_RESIN_N	L8	40 kΩ internal PU to 1.8 V	DI	Reset Keypad volume down button	

2.2.16. Battery interface

Battery interfaces are special for battery interface, major for monitoring battery status, inserting and voltage detection.

Table 2-16. Battery interface definition

Pin name	Pin	Voltage	Type	Description	Notes
BATT_THERM	C6	1.875V max	AI	Battery temperature input to ADC for measuring the pack temperature. Used for charger safe operation and BMS. 100K pull down, or connect to Battery	
BATT_ID	C4	1.875V max	AI	Battery ID input to the ADC interface. Used for missing battery detection. 100K pull down, or connect to Battery	
VBATT_VSNS_P	E3	–	AI	Battery voltage sense input plus. Connect to the battery positive remote sense node or connect this directly to the battery positive node.	
VBATT_VSNS_M	F3	–	AI	Battery voltage sense input minus. Connect to the battery negative remote sense node or connect this directly to the battery negative node.	
VBATT_PACK_SNS_M	C5	–	AI	Battery voltage sense input minus. directly to the battery negative node (pack negative).	
VBATT_OPT_ISNS_P	D4	–	AI	Reserved	
VBATT_OPT_ISNS_M	D6	–	AI	Reserved	

2.2.17. PMIC GPIOs

The PMICs provide GPIO with different functions.

Table 2-17. PMICs and GPIOs

PMIC	Pin name	Pin	Voltage	Description	Notes
PMK7325	PMK_GPIO_01	V25	LV	Configurable; default digital input with 10 µA pull-down	AMUX SMB_SPMI_CLK
	PMK_GPIO_02	W25	LV	Configurable; default digital input with 10 µA pull-down	AMUX SMB_SPMI_DATA
PM7250B	PM_A_GPIO_01	F10	LV	Configurable; default digital input with 10 µA pull-down Interrupt	PM7250B_GPIO_1
	PM_A_GPIO_02	G4	LV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_2
	PM_A_GPIO_03	F9	LV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_3

PMIC	Pin name	Pin	Voltage	Description	Notes
	PM_A_GPIO_04	G3	LV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_4
	PM_A_GPIO_05	C9	MV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_5
	PM_A_GPIO_06	D5	MV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_6
	PM_A_GPIO_07	F4	MV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_7
	PM_A_GPIO_08	E2	MV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_8
	PM_A_GPIO_09	D8	LV	Configurable; default digital output, open drain	PM7250B_GPIO_9
	PM_A_GPIO_10	G11	LV	Configurable; default digital output, open drain	PM7250B_GPIO_10
	PM_A_GPIO_11	E4	LV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_11
	PM_A_GPIO_12	F11	LV	Configurable; default digital input with 10 µA pull-down	PM7250B_GPIO_12
PM7325	PM_B_GPIO_08	J4	MV	Configurable; default digital input with 10 µA pull-down	PM7325_GPIO_08
	PM_B_GPIO_09	K4	MV	Configurable; default digital input with 10 µA pull-down	PM7325_GPIO_09
	PM_B_AMUX2	K3	AI	Analog multiplexer (AMUX) input 2	AMUX_2
	PM_B_AMUX4	L3	AI	Analog multiplexer (AMUX) input 4	AMUX_4
PM7350C	PM_C_GPIO_01	W2	LV	Configurable; default digital input with 10 µA pull-down	
	PM_C_GPIO_02	V4	LV	Configurable; default digital input with 10 µA pull-down	
	PM_C_GPIO_03	W5	LV	Configurable; default digital input with 10 µA pull-down	
	PM_C_GPIO_04	Y6	LV	Configurable; default digital input with 10 µA pull-down	
	PM_C_GPIO_05	T3	MV	Configurable; default digital input with 10 µA pull-down	
	PM_C_GPIO_06	V1	MV	Configurable; default digital input with 10 µA pull-down	
	PM_C_GPIO_07	U1	MV	Configurable; default digital input with 10 µA pull-down	
	PM_C_GPIO_08	U4	MV	Configurable; default digital input with 10 µA pull-down	
	PM_C_GPIO_09	T4	MV	Configurable; default digital input with 10 µA pull-down	

2.2.18. PWMs and LED current driver interface

The SOM has two PWM outputs and three LED Current Drivers.

Table 2-18. PWMs and LED Current Driver interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PWM signals					
PM_C_GPIO_08	U4	MV	DO	Can be configured as GPIO and PWM (only GPIO_08 is available for fixed duty cycle variable frequency mode)	-
PM_C_GPIO_09	T4	MV	DO		-
LED signals					
IRIS_RED	AA3	-	AO	Independent high-side current source brightness control of red, green, and blue channels, 12 mA maximum per channel	-
IRIS_GREEN	AA4	-	AO		-
IRIS_BLUE	Y3	-	AO		-
FLASH LED signals					
FLASH_LED1	AA1,AA2	-	AO	Flash high-side current source	-
FLASH_LED2	Y1,Y2	-	AO		-

2.2.19. RF interface

The SOM provides the fully-integrated WLAN and Bluetooth function.

Table 2-19. Antenna interface definition

Name	Pin	Description	Notes
ANT_2G_5G_CH0	A25	Antenna 1 supports WIFI 2.4G/5G&BT	Chain0
ANT_2G_5G_CH1	D28	Antenna 2 supports WIFI 2.4G/5G&BT (selectable)	Chain1

2.3. Pin summary

Table 2-20. Pin summary

Pin	Pin name	Voltage	Pin type	Notes
A5	VBATT	–	PI, PO	
A6	VBATT	–	PI, PO	
A7	VBATT	–	PI, PO	
A8	VBATT	–	PI, PO	
B5	VBATT	–	PI, PO	
B6	VBATT	–	PI, PO	
B7	VBATT	–	PI, PO	
B8	VBATT	–	PI, PO	
C1	VPH_PWR	–	PI, PO	
C2	VPH_PWR	–	PI, PO	
C3	VPH_PWR	–	PI, PO	
D1	VPH_PWR	–	PI, PO	
D2	VPH_PWR	–	PI, PO	

Pin	Pin name	Voltage	Pin type	Notes
D3	VPH_PWR	–	PI, PO	
A10	USB_VBUS	–	PI, PO	
A11	USB_VBUS	–	PI, PO	
A12	USB_VBUS	–	PI, PO	
A13	USB_VBUS	–	PI, PO	
B10	USB_VBUS	–	PI, PO	
B11	USB_VBUS	–	PI, PO	
B12	USB_VBUS	–	PI, PO	
B13	USB_VBUS	–	PI, PO	
J1	VCOIN	–	PI, PO	
J2	VCOIN	–	PI, PO	
AB3	VREG_BOB	–	PO	
AC3	VREG_BOB	–	PO	
A19	VREG_L18B_1P8	–	PO	
B19	VREG_L18B_1P8	–	PO	
W4	VREG_L2C_1P8	–	PO	
AA5	VREG_L3C_3P0	–	PO	
AB4	VREG_L7C_3P0	–	PO	
AC4	VREG_L8C_1P8	–	PO	
U2	VREG_L12C_1P8	–	PO	
U3	VREG_L13C_3P0	–	PO	
W3	VREG_L11C_2P8	–	PO	
N2	VREG_L17B_1P8	–	PO	
H2	VREG_L16B_1P2	–	PO	
L1	VREG_SYS_1P8	–	PO	
F2	VIB_DRV_P	–	PO	
C6	BATT_THERM	1.875V max	AI	Battery interface
C4	BATT_ID	1.875V max	AI	
E3	VBATT_VSNS_P	–	AI	
F3	VBATT_VSNS_M	–	AI	
C5	VBATT_PACK_SNS_M	–	AI	
D4	VBATT_OPT_ISNS_P	–	AI	
D6	VBATT_OPT_ISNS_M	–	AI	
M8	PHONE_ON_N	–	DI	
L7	KYPD_VOL_UP_N		DI	
L8	PM_RESIN_N		DI	
M7	FORCED_USB_BOOT	PX-3	PD:nppukp DI	
H4	CBL_PWR_N			

Pin	Pin name	Voltage	Pin type	Notes
C10	PMB_MID_CHG		PI	
C11	PMB_MID_CHG			
C12	PMB_MID_CHG			
C13	PMB_MID_CHG			
D10	PMB_DC_IN_PON		AI	
D11	PMB_DC_IN_PSNS		AI	
D12	PMB_DC_IN_EN		DO	
AA26	LNBBCLK2			
J17	SLEEP_CLK			
AA1	FLASH_LED1	–	AO	
AA2	FLASH_LED1	–	AO	
Y1	FLASH_LED2	–	AO	
Y2	FLASH_LED2	–	AO	
AA3	IRIS_RED	–	AO	
AA4	IRIS_GREEN	–	AO	
Y3	IRIS_BLUE	–	AO	
V25	PMK_GPIO_01			
W25	PMK_GPIO_02			
D7	SMB_EN			
C8	SMB_ICHG_FB			
C7	SMB_THERM			
AC21	FAULT_N		DO	
Y5	VREG_L9C_2P96	–	PO	
Y4	VREG_L6C_2P96	–	PO	
T10	SDC2_CLK	PX_2	DO-NP:pdpukp	
T11	SDC2_CMD	PX_2	BH-NP:pdpukp	
V11	SDC2_DATA_0	PX_2	BH-NP:pdpukp	
U10	SDC2_DATA_1	PX_2	BH-NP:pdpukp	
V10	SDC2_DATA_2	PX_2	BH-NP:pdpukp	
U11	SDC2_DATA_3	PX_2	BH-NP:pdpukp	
M10	SD_CARD_DET_N	PX-3	PD:nppukp	
V3	VREG_L4C_1P8_3P0	–	PO	
Y10	UIM1_CLK	PX_6	PD:nppukp DO	
Y9	UIM1_DATA	PX_6	PD:nppukp B	
AA9	UIM1_RESET	PX_6	PD:nppukp DO	
AA10	UIM1_PRESENT	PX_6	PD:nppukp DI	
V2	VREG_L5C_1P8_3P0	–	PO	

Pin	Pin name	Voltage	Pin type	Notes
Y8	UIM2_CLK	PX_6	PD:nppukp DO	
Y7	UIM2_DATA	PX_6	PD:nppukp B	
AA7	UIM2_RESET	PX_6	PD:nppukp DO	
AA8	UIM2_PRESENT	PX_6	PD:nppukp DI	
G2	PM_USB_OPTION		AI	
E1	USB_THERM		AI	
AA11	USB_SS-H_HS-L_SEL	PX-3	DI	
C15	USB0_CC1		AI, PO	
D15	USB0_CC2		AI, PO	
A15	USB0_SBU1		DI	
B15	USB0_SBU2		DO	
AB17	USB0_DP_AUX_P	–	AI, AO	
AC17	USB0_DP_AUX_M	–	AI, AO	
F1	USB0_HS_DP	–	AI, AO	
G1	USB0_HS_DM	–	AI, AO	
AB14	USB0_SS_TX0_P	–	AO	
AC14	USB0_SS_TX0_M	–	AO	
AB13	USB0_SS_RX0_P	–	AI	
AC13	USB0_SS_RX0_M	–	AI	
AB15	USB0_SS_TX1_P	–	AO	
AC15	USB0_SS_TX1_M	–	AO	
AC16	USB0_SS_RX1_P	–	AI	
AB16	USB0_SS_RX1_M	–	AI	
AC18	USB1_HS_DP	–	AI, AO	
AB18	USB1_HS_DM	–	AI, AO	
Y14	PCIE1_RESET_N	PX-3		
Y15	PCIE1_WAKE_N	PX-3		
Y16	PCIE1_CLK_REQ_N	PX-3	DI	
AC11	PCIE1_REFCLK_P	–	AI, AO	
AB11	PCIE1_REFCLK_M	–	AI, AO	
AC7	PCIE1_TX0_P	–	AO	
AB7	PCIE1_TX0_M	–	AO	
AC8	PCIE1_RX0_P	–	AI	
AB8	PCIE1_RX0_M	–	AI	
AC9	PCIE1_TX1_P	–	AO	
AB9	PCIE1_TX1_M	–	AO	
AC10	PCIE1_RX1_P	–	AI	
AB10	PCIE1_RX1_M	–	AI	

Pin	Pin name	Voltage	Pin type	Notes
K7	EDP0_AUX_P	–	B	
K8	EDP0_AUX_M	–	B	
J7	EDP0_TX0_P	–	AO	
J8	EDP0_TX0_M	–	AO	
H7	EDP0_TX1_P	–	AO	
H8	EDP0_TX1_M	–	AO	
G7	EDP0_TX2_P	–	AO	
G8	EDP0_TX2_M	–	AO	
F7	EDP0_TX3_P	–	AO	
F8	EDP0_TX3_M	–	AO	
AB26	CSI0_NC_CLK_P	CSI	AI, AO	
AC26	CSI0_A0_CLK_M	CSI	AI, AO	
AB25	CSI0_B0_LN0_P	CSI	AI, AO	
AC25	CSI0_C0_LN0_M	CSI	AI, AO	
AB24	CSI0_A1_LN1_P	CSI	AI, AO	
AC24	CSI0_B1_LN1_M	CSI	AI, AO	
AB23	CSI0_C1_LN2_P	CSI	AI, AO	
AC23	CSI0_A2_LN2_M	CSI	AI, AO	
AB22	CSI0_B2_LN3_P	CSI	AI, AO	
AC22	CSI0_C2_LN3_M	CSI	AI, AO	
U28	CSI1_NC_CLK_P	CSI	AI, AO	
U27	CSI1_A0_CLK_M	CSI	AI, AO	
V28	CSI1_B0_LN0_P	CSI	AI, AO	
V27	CSI1_C0_LN0_M	CSI	AI, AO	
W28	CSI1_A1_LN1_P	CSI	AI, AO	
W27	CSI1_B1_LN1_M	CSI	AI, AO	
Y28	CSI1_C1_LN2_P	CSI	AI, AO	
Y27	CSI1_A2_LN2_M	CSI	AI, AO	
AA28	CSI1_B2_LN3_P	CSI	AI, AO	
AA27	CSI1_C2_LN3_M	CSI	AI, AO	
M27	CSI2_NC_CLK_P	CSI	AI, AO	
M28	CSI2_A0_CLK_M	CSI	AI, AO	
N27	CSI2_B0_LN0_P	CSI	AI, AO	
N28	CSI2_C0_LN0_M	CSI	AI, AO	
P27	CSI2_A1_LN1_P	CSI	AI, AO	
P28	CSI2_B1_LN1_M	CSI	AI, AO	
R27	CSI2_C1_LN2_P	CSI	AI, AO	
R28	CSI2_A2_LN2_M	CSI	AI, AO	

Pin	Pin name	Voltage	Pin type	Notes
T27	CSI2_B2_LN3_P	CSI	AI, AO	
T28	CSI2_C2_LN3_M	CSI	AI, AO	
G27	CSI3_NC_CLK_P	CSI	AI, AO	
G28	CSI3_A0_CLK_M	CSI	AI, AO	
H27	CSI3_B0_LN0_P	CSI	AI, AO	
H28	CSI3_C0_LN0_M	CSI	AI, AO	
J27	CSI3_A1_LN1_P	CSI	AI, AO	
J28	CSI3_B1_LN1_M	CSI	AI, AO	
K27	CSI3_C1_LN2_P	CSI	AI, AO	
K28	CSI3_A2_LN2_M	CSI	AI, AO	
L27	CSI3_B2_LN3_P	CSI	AI, AO	
L28	CSI3_C2_LN3_M	CSI	AI, AO	
D26	CSI4_NC_CLK_P	CSI	AI, AO	
D25	CSI4_A0_CLK_M	CSI	AI, AO	
E26	CSI4_B0_LN0_P	CSI	AI, AO	
E25	CSI4_C0_LN0_M	CSI	AI, AO	
F26	CSI4_A1_LN1_P	CSI	AI, AO	
F25	CSI4_B1_LN1_M	CSI	AI, AO	
G26	CSI4_C1_LN2_P	CSI	AI, AO	
G25	CSI4_A2_LN2_M	CSI	AI, AO	
H26	CSI4_B2_LN3_P	CSI	AI, AO	
H25	CSI4_C2_LN3_M	CSI	AI, AO	
V21	CCI_I2C0_SCL	PX-3	DO	
V20	CCI_I2C0_SDA	PX-3	B	
V22	CCI_I2C1_SCL	PX-3	DO	
U22	CCI_I2C1_SDA	PX-3	B	
T22	CCI_I2C2_SCL	PX-3	DO	
T21	CCI_I2C2_SDA	PX-3	B	
U20	CCI_I2C3_SCL	PX-3	DO	
T20	CCI_I2C3_SDA	PX-3	B	
M20	CAM_MCLK0	PX-3	DO	
L22	CAM_MCLK1	PX-3	DO	
N19	CAM_MCLK2	PX-3	DO	
L21	CAM_MCLK3	PX-3	DO	
H20	CAM_MCLK4	PX-3	DO	
B20	SM_GPIO_93	PX-3	DO	
AA24	SM_GPIO_20	PX-3	DO	
AB21	SM_GPIO_21	PX-3	DO	
U21	SM_GPIO_77	PX-3	DO	
R26	SM_GPIO_78	PX-3	DO	
P26	SM_GPIO_90	PX-3	DO	

Pin	Pin name	Voltage	Pin type	Notes
T25	SM_GPIO_121	PX-3	DO	
P8	MIPI_DSI0_CLK_P	DSI	AI, AO	
P7	MIPI_DSI0_CLK_M	DSI	AI, AO	
V8	MIPI_DSI0_L0_P	DSI	AI, AO	
V7	MIPI_DSI0_L0_M	DSI	AI, AO	
R8	MIPI_DSI0_L1_P	DSI	AI, AO	
R7	MIPI_DSI0_L1_M	DSI	AI, AO	
U8	MIPI_DSI0_L2_P	DSI	AI, AO	
U7	MIPI_DSI0_L2_M	DSI	AI, AO	
T8	MIPI_DSI0_L3_P	DSI	AI, AO	
T7	MIPI_DSI0_L3_M	DSI	AI, AO	
Y18	APPS_I2C_SDA	PX-3		
Y17	APPS_I2C_SCL	PX-3		
AB20	DBG_UART_TX	PX-3		
AC20	DBG_UART_RX	PX-3		
G19	SM_GPIO_0	PX-3		
G20	SM_GPIO_1	PX-3		
K21	SM_GPIO_6	PX-3		
K25	SM_GPIO_7	PX-3		
L25	SM_GPIO_8	PX-3		
R25	SM_GPIO_9	PX-3		
D22	SM_GPIO_12	PX-3		
C19	SM_GPIO_13	PX-3		
D21	SM_GPIO_14	PX-3		
D20	SM_GPIO_15	PX-3		
H22	SM_GPIO_16	PX-3		
J22	SM_GPIO_17	PX-3		
F22	SM_GPIO_18	PX-3		
G22	SM_GPIO_19	PX-3		
V26	SM_GPIO_24	PX-3		
Y26	SM_GPIO_25	PX-3		
U26	SM_GPIO_26	PX-3		
W26	SM_GPIO_27	PX-3		
L19	SM_GPIO_32	PX-3		
R12	SM_GPIO_33	PX-3		
T12	SM_GPIO_34	PX-3		
R13	SM_GPIO_35	PX-3		
T15	SM_GPIO_36	PX-3		
T16	SM_GPIO_37	PX-3		
U15	SM_GPIO_38	PX-3		
U16	SM_GPIO_39	PX-3		

Pin	Pin name	Voltage	Pin type	Notes
M3	SM_GPIO_40	PX-3		
N3	SM_GPIO_41	PX-3		
K2	SM_GPIO_42	PX-3		
H1	SM_GPIO_43	PX-3		
T13	SM_GPIO_44	PX-3		
U12	SM_GPIO_45	PX-3		
R14	SM_GPIO_46	PX-3		
U13	SM_GPIO_47	PX-3		
P3	SM_GPIO_48	PX-3		
K1	SM_GPIO_49	PX-3		
L2	SM_GPIO_50	PX-3		
M2	SM_GPIO_51	PX-3		
T14	SM_GPIO_52	PX-3		
R15	SM_GPIO_53	PX-3		
U14	SM_GPIO_54	PX-3		
R16	SM_GPIO_55	PX-3		
R1	SM_GPIO_56	PX-3		
R2	SM_GPIO_57	PX-3		
T2	SM_GPIO_58	PX-3		
T1	SM_GPIO_59	PX-3		
AC6	SM_GPIO_60	PX-3		
AB5	SM_GPIO_61	PX-3		
AA6	SM_GPIO_62	PX-3		
AC5	SM_GPIO_63	PX-3		
N1	SM_GPIO_80	PX-3		
N8	SM_GPIO_81	PX-3		
C20	SM_GPIO_83	PX-3		
R4	SM_GPIO_96	PX-3		
P4	SM_GPIO_97	PX-3		
N4	SM_GPIO_98	PX-3		
M4	SM_GPIO_99	PX-3		
R9	SM_GPIO_100	PX-3		
N7	SM_GPIO_101	PX-3		
R3	SM_GPIO_102	PX-3		
L4	SM_GPIO_103	PX-3		
J3	SM_GPIO_104	PX-3		
J19	SM_GPIO_105	PX-3		
J20	SM_GPIO_106	PX-3		
K19	SM_GPIO_107	PX-3		
K20	SM_GPIO_108	PX-3		
AA18	SM_GPIO_129	PX-3		

Pin	Pin name	Voltage	Pin type	Notes
AA25	SM_GPIO_130	PX-3		
AA22	SM_GPIO_131	PX-3		
K22	SM_GPIO_132	PX-3		
F19	SM_GPIO_136	PX-3		
F20	SM_GPIO_137	PX-3		
F21	SM_GPIO_138	PX-3		
AB6	SM_GPIO_141	PX-3		
Y11	SM_GPIO_142	PX-3		
G14	SM_GPIO_144	PX-3		
J13	SM_GPIO_145	PX-3		
G15	SM_GPIO_146	PX-3		
F14	SM_GPIO_147	PX-3		
J12	SM_GPIO_148	PX-3		
H13	SM_GPIO_149	PX-3		
J14	SM_GPIO_150	PX-3		
H14	SM_GPIO_151	PX-3		
J15	SM_GPIO_152	PX-3		
H15	SM_GPIO_153	PX-3		
H11	SM_GPIO_154	PX-3		
G12	SM_GPIO_155	PX-3		
F16	SM_GPIO_156	PX-3		
F17	SM_GPIO_157	PX-3		
F15	SM_GPIO_158	PX-3		
K10	SNS_I3C0_SDA	PX-3		
L10	SNS_I3C0_SCL	PX-3		
H10	SNS1_I2C_SDA	PX-3		
J10	SNS1_I2C_SCL	PX-3		
J11	SM_GPIO_163	PX-3		
H12	SM_GPIO_164	PX-3		
F13	SM_GPIO_165	PX-3		
G13	SM_GPIO_166	PX-3		
F10	PM_A_GPIO_01			
G4	PM_A_GPIO_02			
F9	PM_A_GPIO_03			
G3	PM_A_GPIO_04			
C9	PM_A_GPIO_05			
D5	PM_A_GPIO_06			
F4	PM_A_GPIO_07			
E2	PM_A_GPIO_08			
D8	PM_A_GPIO_09			
G11	PM_A_GPIO_10			

Pin	Pin name	Voltage	Pin type	Notes
E4	PM_A_GPIO_11			
F11	PM_A_GPIO_12			
K3	PM_B_AMUX2			
L3	PM_B_AMUX4			
J4	PM_B_GPIO_08			
K4	PM_B_GPIO_09			
W2	PM_C_GPIO_01			
V4	PM_C_GPIO_02			
W5	PM_C_GPIO_03			
Y6	PM_C_GPIO_04			
T3	PM_C_GPIO_05			
V1	PM_C_GPIO_06			
U1	PM_C_GPIO_07			
U4	PM_C_GPIO_08			
T4	PM_C_GPIO_09			
T26	SM_GPIO_122			
Y21	SM_GPIO_117			
AA21	SM_GPIO_118			
Y20	SM_GPIO_119			
AA20	SM_GPIO_120			
Y19	SM_GPIO_123			
AA19	SM_GPIO_124			
A25	ANT_2G_5G_CH0	–		
D28	ANT_2G_5G_CH1	–		
A22	ANT_BT_3RD	–		
A3	GND	–	–	
A4	GND	–	–	
A9	GND	–	–	
A14	GND	–	–	
A16	GND	–	–	
A17	GND	–	–	
A18	GND	–	–	
A20	GND	–	–	
A21	GND	–	–	
A23	GND	–	–	
A24	GND	–	–	
A26	GND	–	–	
B3	GND	–	–	
B4	GND	–	–	
B9	GND	–	–	
B14	GND	–	–	

Pin	Pin name	Voltage	Pin type	Notes
B16	GND	–	–	
B17	GND	–	–	
B18	GND	–	–	
B21	GND	–	–	
B22	GND	–	–	
B23	GND	–	–	
B24	GND	–	–	
B25	GND	–	–	
B26	GND	–	–	
C14	GND	–	–	
C16	GND	–	–	
C17	GND	–	–	
C18	GND	–	–	
C21	GND	–	–	
C22	GND	–	–	
C23	GND	–	–	
C24	GND	–	–	
C25	GND	–	–	
C26	GND	–	–	
C27	GND	–	–	
C28	GND	–	–	
D9	GND	–	–	
D13	GND	–	–	
D14	GND	–	–	
D16	GND	–	–	
D17	GND	–	–	
D18	GND	–	–	
D19	GND	–	–	
D23	GND	–	–	
D24	GND	–	–	
D27	GND	–	–	
E27	GND	–	–	
E28	GND	–	–	
F12	GND	–	–	
F18	GND	–	–	
F27	GND	–	–	
F28	GND	–	–	
G9	GND	–	–	
G10	GND	–	–	
G16	GND	–	–	
G17	GND	–	–	

Pin	Pin name	Voltage	Pin type	Notes
G18	GND	–	–	
G21	GND	–	–	
H3	GND	–	–	
H9	GND	–	–	
H16	GND	–	–	
H17	GND	–	–	
H18	GND	–	–	
H19	GND	–	–	
H21	GND	–	–	
J9	GND	–	–	
J16	GND	–	–	
Y22	GND	–	–	
J18	GND	–	–	
J21	GND	–	–	
J25	GND	–	–	
J26	GND	–	–	
K9	GND	–	–	
K26	GND	–	–	
L9	GND	–	–	
L20	GND	–	–	
L26	GND	–	–	
M1	GND	–	–	
M9	GND	–	–	
M19	GND	–	–	
M21	GND	–	–	
M22	GND	–	–	
M25	GND	–	–	
M26	GND	–	–	
N9	GND	–	–	
N10	GND	–	–	
N20	GND	–	–	
N21	GND	–	–	
N22	GND	–	–	
N25	GND	–	–	
N26	GND	–	–	
P9	GND	–	–	
P10	GND	–	–	
P19	GND	–	–	
P20	GND	–	–	
P21	GND	–	–	
P22	GND	–	–	

Pin	Pin name	Voltage	Pin type	Notes
P25	GND	–	–	
R10	GND	–	–	
R11	GND	–	–	
R17	GND	–	–	
R18	GND	–	–	
R19	GND	–	–	
R20	GND	–	–	
R21	GND	–	–	
R22	GND	–	–	
T9	GND	–	–	
T17	GND	–	–	
T18	GND	–	–	
T19	GND	–	–	
U9	GND	–	–	
U17	GND	–	–	
U18	GND	–	–	
U19	GND	–	–	
V9	GND	–	–	
V12	GND	–	–	
V13	GND	–	–	
V14	GND	–	–	
V15	GND	–	–	
V16	GND	–	–	
V17	GND	–	–	
V18	GND	–	–	
V19	GND	–	–	
W1	GND	–	–	
Y12	GND	–	–	
Y13	GND	–	–	
AA12	GND	–	–	
AA13	GND	–	–	
AA14	GND	–	–	
AA15	GND	–	–	
AA16	GND	–	–	
AA17	GND	–	–	
AA23	GND	–	–	
Y25	GND	–	–	
AB12	GND	–	–	
AB19	GND	–	–	
AC12	GND	–	–	
AC19	GND	–	–	

Pin	Pin name	Voltage	Pin type	Notes
U25	GND	–	–	
P1	GND	–	–	
P2	GND	–	–	
Y24	GND	–	–	
Y23	GND	–	–	
GD1	GND	–	–	
GD2	GND	–	–	
GD3	GND	–	–	
GD4	GND	–	–	
GD5	GND	–	–	
GD6	GND	–	–	
GD7	GND	–	–	
GD8	GND	–	–	
GD9	GND	–	–	
GD10	GND	–	–	

Chapter 3. Electrical Characteristics

3.1. Absolute maximum ratings

The SOM needs to be designed in the operation conditions which is shown as below table.

Table 3-1. Absolute rating condition

Parameter	Min	Max	Units
Input Power Voltage			
USB_VBUS	-0.3	28	V
VBAT	-0.3	6	V
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M, RSENSE_EXT_M, RSENSE_EXT_P	-0.3	6	V
ESD			
ESD-HBM model rating		±2000	V
ESD-CDM model rating		±500	V

➲ **NOTE:** ESD parameters are valid and available only when the module is fully tested and approved in the Initial Production stage.

3.2. Operating conditions

The SOM needs to be designed in the operation conditons which is shown as below table.

Table 3-2. Operating conditions

Parameters	Min	Typical	Max	Units
Input Power voltage				
USB_VBUS	+3.6	5	+13.2	V
VBAT	+3.6	3.8	+4.8	V
VBAT	3			A
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M, RSENSE_EXT_M, RSENSE_EXT_P	+3.6	3.8	+4.8	V
Thermal conditions				
Operating temperature	-25	25	75	°C
Storage temperature	-40	-	TBD	°C

➲ **NOTE**: For the thermal conditons, operating and storage min and max temperatures are only valid when the module is fully tested and approved in the Initial Production stage.

3.3. Output power

The SOM provide power supply for external device, like camera module, SD card, sensor, and so on.

Table 3-3. Output power

Function	Pin	Default voltage (V)	Range (V)	Expected use
VPH_PWR	C1,C2,C3, D1,D2,D3	-	3.2~4.75	Primary system supply node
VREG_BOB	AB3,AC3	3.3	-	Buck-boost output 3.3V@1A (will increase to 3.6V during the bootup of the SOM)
VREG_L18B_1P8	A19,B19	1.8	1.8~2.0	PX-3, 1.8V Just for GPIO pull-up
VREG_L2C_1P8	W4	1.8	1.62~1.98	MEMS_DMIC_VDD, 1.62V~1.98V, 1.8V typ
VREG_L3C_3P0	AA5	3.008	2.8~3.54	Touch screen, 2.7V~3.54V, 3V typ
VREG_L7C_3P0	AB4	3.008	2.8~3.54	Sensors, 2.7V~3.54V, 3V typ
VREG_L8C_1P8	AC4	1.8	1.8~2	Sensors, 1.62V~2V, 1.8V typ
VREG_L11C_2P8	W3	2.8	2.8~3.54	Connectivity, 1.65V~3.54V, 2.8V typ
VREG_L12C_1P8	U2	1.8	1.8~1.98	OLED VDDIO, 1.62V~1.98V, 1.8V typ
VREG_L13C_3P0	U3	3	2.7~3.54	OLED VCI, 2.7V~3.54V, 2.8V typ
VREG_L16B_1P2	H2	1.2	1.2~1.3	1.2V~1.3V, 1.2V typ
VREG_L17B_1P8	N2	1.8	1.8~1.9	WCD_VDD_BUCK, 1.8V~1.9V, 1.8V typ
VREG_SYS_1P8	L1	-	1.75~1.85	System 1.8 V I/O output Reserved for debug, please leave it floating
VIB_DRV_P	F2	TBD	TBD	Power supply for haptics driver

3.4. Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage. The SOM IO voltage level is the same with VDDPX-3 except the SD card and analog input/output. The I2C, USB, MIPI and UART comply with the standards.

3.4.1. Digital GPIO characteristics

The follow-int table shows the digital GPIO characteristics:

Table 3-4. Digital IO voltage performance

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt	0.7 x VDDPX-3	VDDPX-3+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt	-0.3	0.3 x VDDPX-3	V
VSHYS	Schmitt hysteresis voltage	300	-	mV
VOH	High-level output voltage, CMOS	VDDPX-3 - 0.45	VDDPX-3	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V
RPULL-UP	Pull-up resistance	20 K	60 K	Ω
RPULL-DOWN	Pull-down resistance	60 K	20 K	Ω

3.4.2. SD card digital I/O characteristics

The SD card is powered by P2 supply; the power is 1.8V and 2.96V.the following table shows the SD card digital I/O characteristics:

Table 3-5. SD digital IO voltage performance (1.8V/2.96V)

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27/0.625 x VDDPX_2	-	2/VDDPX_2 + 0.3	V
VIL	Low-level input voltage	-0.3/-0.3	-	0.58/0.25 x VDDPX_2	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/0.75 x VDDPX_2	-	-/VDDPX_2	V
VOL	Low-level output voltage	0/0	-	0.45/0.125 x VDDPX_2	V

3.5. MIPI

The SOM supports the MIPI interface and comply with MIPI standards.

Table 3-6. MIPI_DSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	TBD
MIPI Alliance Specification for DPHY v1.2	TBD
MIPI Alliance Specification for CPHY v1.0	TBD

Table 3-7. MIPI_CSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for DPHY v1.2	TBD
MIPI Alliance Specification for CPHY v1.2	TBD

3.6. USB

The SOM supports USB standards and exceptions.

Table 3-8. USB

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	TBD
UTMI Specification Version 1.05, released on 3/29/2001	TBD
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	TBD

3.7. PCIe

The SOM supports PCIe standards and exceptions

Table 3-9. PCIe

Applicable standard	Feature exceptions
PCI Express Specification, Revision 3.0	Gen3

3.8. DisplayPort

The SOM supports DisplayPort standards and exceptions

Table 3-10. DP

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	TBD

3.9. SLIMbus

The SOM supports SLIMbus HDMI standards and exceptions

Table 3-11. SLIMbus

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	TBD

3.10. SDIO

The SOM Supports SD standards and exceptions

Table 3-12. SDIO

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	TBD
SDIO Card Specification version 3.0	TBD

3.11. I2S

The SOM I2S standards and exceptions:

- Legacy I2S interfaces for primary and secondary microphones and speakers.
- The multiple I2S (MI2S) interface for microphone and speaker functions.

It supports the following functions:

- Both master and slave mode
- 16, 24, or 32-bit resolution audio samples
- 8, 16, 32, 48, 96 and192 kHz sampling rate in Master mode, and all standard sample rates in slave mode.
- 16-bit and 24-bit data formats in standard I2S mode, and 24-bit left-justified (24-bit data in 32-bit frame left-justified, LSBs are padded with 0s)

Maximum clock frequency supported 12.288 MHz.

An additional Pin can be used for a master clock, supplied by the MSM device, the master clock is often used in the external devices to drive their oversampling logic. The LPASS clock controller can provide master clocks from independent clock dividers to the I2S bit-clock dividers.

Table 3-13. I2S

Applicable standard	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996	TBD

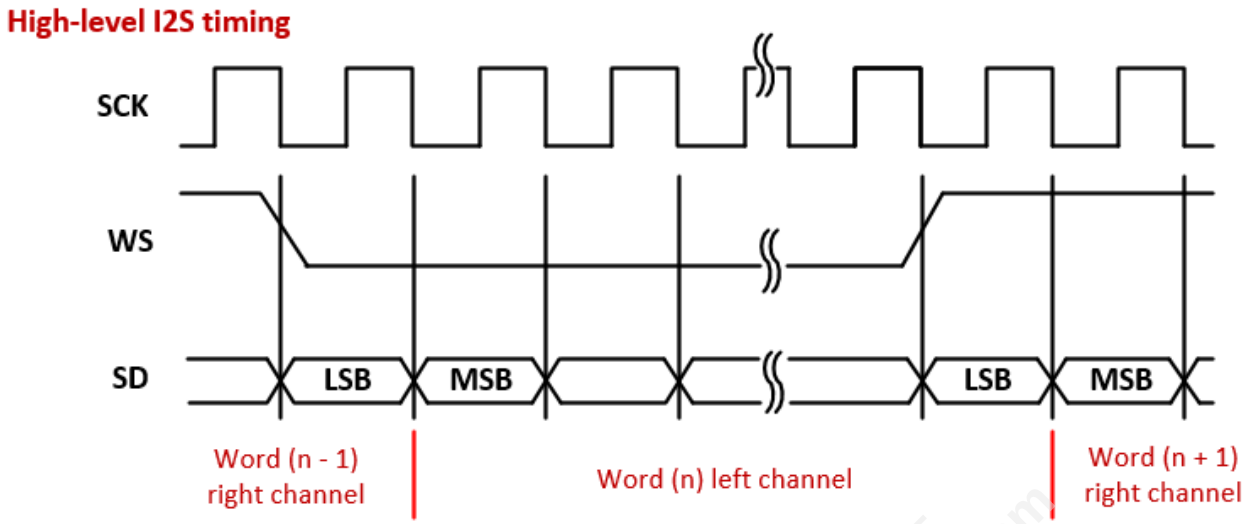

Figure 3-1.I2S Timing Diagram

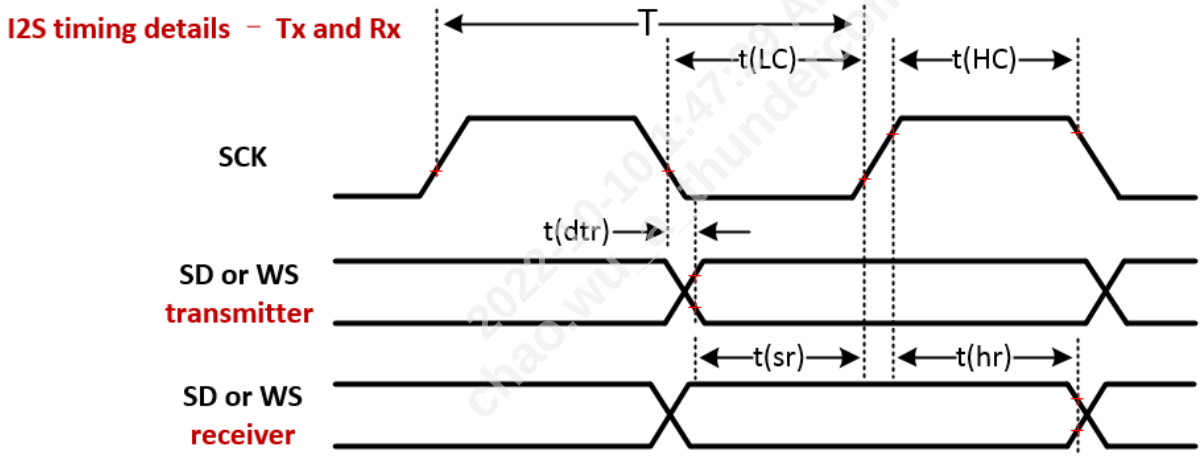

Figure 3-2.I2S Timing Diagram

The word-select signal is a 50% duty cycle signal Data is delayed 1 bit-clock, relative to the word select.

Data outputs are launched on the falling edge of the clock, and inputs data are captured on the rising edge of the clock by the receiver.

I2S samples are 2's complement values, and the MSB is transmitted first allowing the transmitter and receiver to support different number of bits per sample.

The left channel is transmitted when the word select is low, and the right channel is transmitted when the word select is high.

Table 3-14. I2S Timing

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
Using external SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns

3.12. I2C

The SOM I2C standards and exceptions:

Table 3-15. I2C

Applicable standard	Feature exceptions
I2C Specification, version 3.0	TBD

3.13. SPI

The SOM supports SPI standards as a master only.

3.14. Fuel gauge

The fuel gauge module offers a hardware-based algorithm that is able to accurately estimate the Battery's state of charge by using current monitoring and voltage-based techniques. This hybrid approach ensures both excellent short-term linearity and long-term accuracy. Furthermore, neither full battery charge cycling, nor zero-current-load conditions, are required to maintain the accuracy.

The fuel gauge measures the battery pack temperature by sensing the voltage across an external thermistor. Missing battery detection is also incorporated to accurately monitor battery insertion and removal scenarios, while properly updating the state of charge when a battery is reconnected.

Using precise measurements of battery voltage, current, and temperature, the fuel gauging algorithm compensates for the variation in battery characteristics across temperature changes and aging effects. This provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions.

Table 3-16. Fuel Gauge

Function	Min	Type	Max	Units	Expected use
VBATT_CONN_VSENSE_P (H47) & VBATT_CONN_VSENSE_M(G47)					
Resolution	-	-	16	bits	Voltage ADC
	1	-	450	Kohm	ID ADC
	-	-	16	bits	Current ADC

3.15. Power consumption

T.B.D.

3.16. Thermal

T.B.D.

3.17. RF Performance

T.B.D.

Appendix 1. Notices

Thundercomm may have patents or pending patent programs covering subject matter described in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries to service@thundercomm.com.

THUNDERCOMM PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some jurisdictions do not allow disclaimer of express or implied warranties in certain transactions; therefore, this statement may not apply to you.

Changes are made periodically to the information herein; these changes will be incorporated in new editions of the publication. To provide better service, Thundercomm reserves the right to improve and/or modify the products and software programs described in the manuals, and the content of the manual, at any time without additional notice.

The software interface and function and hardware configuration described in the manuals included with your development board or system on module might not match exactly the actual configuration of that you have purchased. For the configuration of the product, refer to the related contract (if any) or product packing list, or consult the distributor for the product sales. Thundercomm may use or distribute any of the information you supply in any way it believes appropriate without incurring any obligation to you.

The products described in this document are not intended for use in implantation or other life support applications where malfunction may result in injury or death to persons. The information contained in this document does not affect or change Thundercomm product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of Thundercomm or third parties. All information contained in this document was obtained in specific environments and is presented as an illustration. The result obtained in other operating environments may vary.

The information of this document should not be as any invitation for offer or any advice to the visitors. Please consult the professional comments from the sales consultant prior to do any actions of invest or purchase.

Thundercomm may use or distribute any of the information you supply in any way it believes appropriate without incurring any obligation to you.

Any references in this publication to non-Thundercomm Web sites are provided for convenience only and do not in any manner serve as an endorsement of those Web sites. The materials at those Web sites are not part of the materials for this Thundercomm product, and use of those Web sites is at your own risk. Thundercomm shall not be responsible for the content of the third party.

Any performance data contained herein was determined in a controlled environment. Therefore, the result obtained in other operating environments may vary significantly. Some measurements may have been made on development-level systems and there is no guarantee that these measurements will be the same on generally available systems. Furthermore, some measurements may have been estimated through extrapolation. Actual results may vary. Users of this document should verify the applicable data for their specific environment.

E-mail messages sent to Thundercomm via the Internet are not guaranteed to be completely secure. Thundercomm shall not be liable for any loss incurred by the surfer when transmitting any information over the Internet or for any loss incurred by Thundercomm when sending any information over the Internet at your request.

Thundercomm has all rights under other relevant exemptions provided by laws and regulations, and Thundercomm's failure to claim or delay in claiming such rights shall not be deemed to be a waiver of such rights by Thundercomm.

Thundercomm reserves the right of final interpretation of this document.

Appendix 2. Trademarks

Thundercomm, Thundercomm TurboX, TURBOX, Thundersoft turbox are trademarks of Thundercomm Corporation or its associate companies in China and/or other countries. Intel, Intel SpeedStep, Optane, and Thunderbolt are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Microsoft, Windows, Direct3D, BitLocker, and Cortana are trademarks of the Microsoft group of companies. Mini DisplayPort (mDP), DisplayPort, and VESA are trademarks of the Video Electronics Standards Association. The terms HDMI and HDMI High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries. Wi-Fi, Wi-Fi Alliance, WiGig, and Miracast are registered trademarks of Wi-Fi Alliance. USB-C is a registered trademark of USB Implementers Forum. All other trademarks are the property of their respective owners.

FCC Caution:

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IMPORTANT NOTE:

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C&E has been investigated. It is applicable to the modular.

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

Operation of 5850-5895MHz, 5925-6425 MHz, 6425-6525MHz, 6525-6875MHz, 6875-7125MHz are restricted to indoor use only.

Operation of transmitters in the 5.925–7.125 GHz band is prohibited for control of or communications with unmanned aircraft systems.

2.4 Limited module procedures

Not applicable

2.5 Trace antenna designs

Not applicable

2.6 RF exposure considerations

To maintain compliance with FCC's RF Exposure guidelines, this equipment should be installed and operated with minimum distance of 20cm from your body.

2.7 Antennas

This module device tested with follow antennas information.

Internal Identification	Antenna Description	Antenna type	Impedance	Maximum antenna gain
Antenna 1	Bluetooth/Wi-Fi Antenna (Antenna on I/O Board)	FPC	50Ω	Bluetooth/2.4G Wi-Fi: 2.5dBi, 5/6G Wi-Fi: 2.6dBi
Antenna 2	Wi-Fi Antenna (Antenna on I/O Board)	FPC	50Ω	2.4G Wi-Fi: 2.5dBi, 5/6G Wi-Fi: 2.6dBi

2.8 Label and compliance information

The module with label, FCC ID: 2AOHHTURBOX-C6490 listed. Please refer to label.

The final end product must be labeled in a visible area with the following" Contains FCC ID: 2AOHHTURBOX-C6490"

2.9 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B