Schneider

865-0329
WiLink™ 8 Single-Band Module – Wi-Fi

1 Device Overview

1.1 Features

- General
  - Integrates RF, Power Amplifiers (PAs), Clock, RF Switches, Filters, Passives, and Power Management
  - Quick Hardware Design With TI Module Collateral and Reference Designs
  - Operating Temperature: –20°C to +70°C
  - Small Form Factor: 13.3 × 13.4 × 2 mm
  - 100-Pin MOC Package
  - FCC, IC, RCM/CE Certified With PCB, Dipole, Chip, and PIFA Antennas
- Wi-Fi®
  - WLAN Baseband Processor and RF Transceiver Support of IEEE Std 802.11b, 802.11g, and 802.11n
  - 20- and 40-MHz SISO and 20-MHz 2 × 2 MIMO at 2.4 GHz for High Throughput: 80 Mbps (TCP), 100 Mbps (UDP)
  - 2.4-GHz MRC Support for Extended Range
  - Fully Calibrated: Production Calibration Not Required
  - 4-Bit SDIO Host Interface Support
  - Wi-Fi Direct Concurrent Operation (Multichannel, Multirole)

1.2 Applications

•Internet of Things (IoT)

•Multimedia

•Home Electronics

•Home Appliances and White Goods

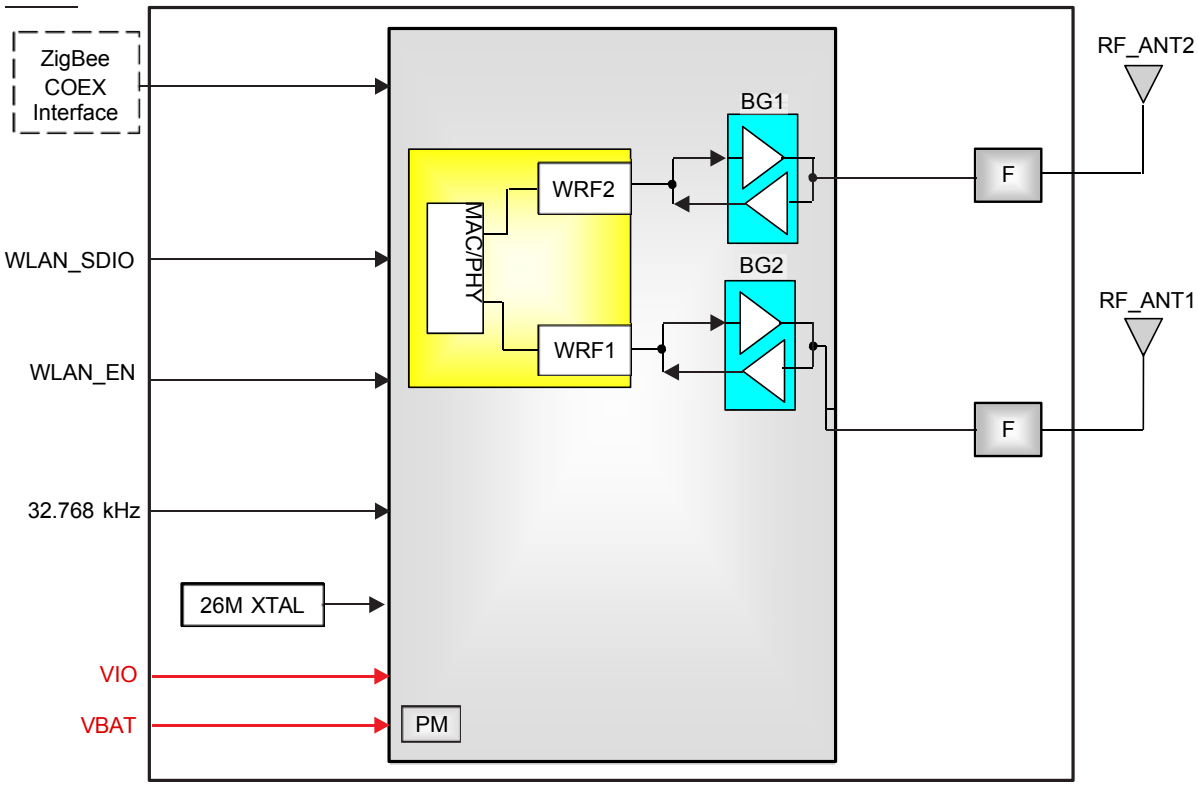
1.3 Description

The 865-0329 device is a 2.4-GHz module, two antenna solution. The device is FCC, IC, ETSI/CE, and RCM certified for AP and client. Compatible with high-level operating systems such as Linux®and Android™. Additional drivers, such as WinCE and RTOS, which includes QNX, Nucleus, ThreadX, and FreeRTOS, are supported through third parties.

PART NUMBER	PACKAGE	BODY SIZE
865-0329	QFM (100)	13.3 mm × 13.4 mm × 2 mm

1.4 Functional Block Diagram

Figure 1-1 shows a functional block diagram of the 865-0329 variant.



NOTE: Dashed lines indicate optional configurations and are not applied by default.

Figure 1-1. 865-0329 Functional Block Diagram

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2 Device Features

The 865 - 0329 module offers four footprint-compatible 2.4-GHz variants providing stand-alone Wi-Fi connectivity. Table 3-1 compares the features of the module.

Table 3-1. 865 - 0329 Module Variants

FEATURE	DEVICE
	865 - 0329
WLAN 2.4-GHZ SISO(1)	√
WLAN 2.4-GHZ MIMO(1)	√
WLAN 2.4-GHZ MRC(1)	√

(1) SISO: single input, single output; MIMO: multiple input, multiple output; MRC: maximum ratio combining, supported at 802.11 g/n.

3 Device Comparison Terminal Configuration and Functions

Figure 1-1 shows the pin assignments for the 100-pin MOC package.

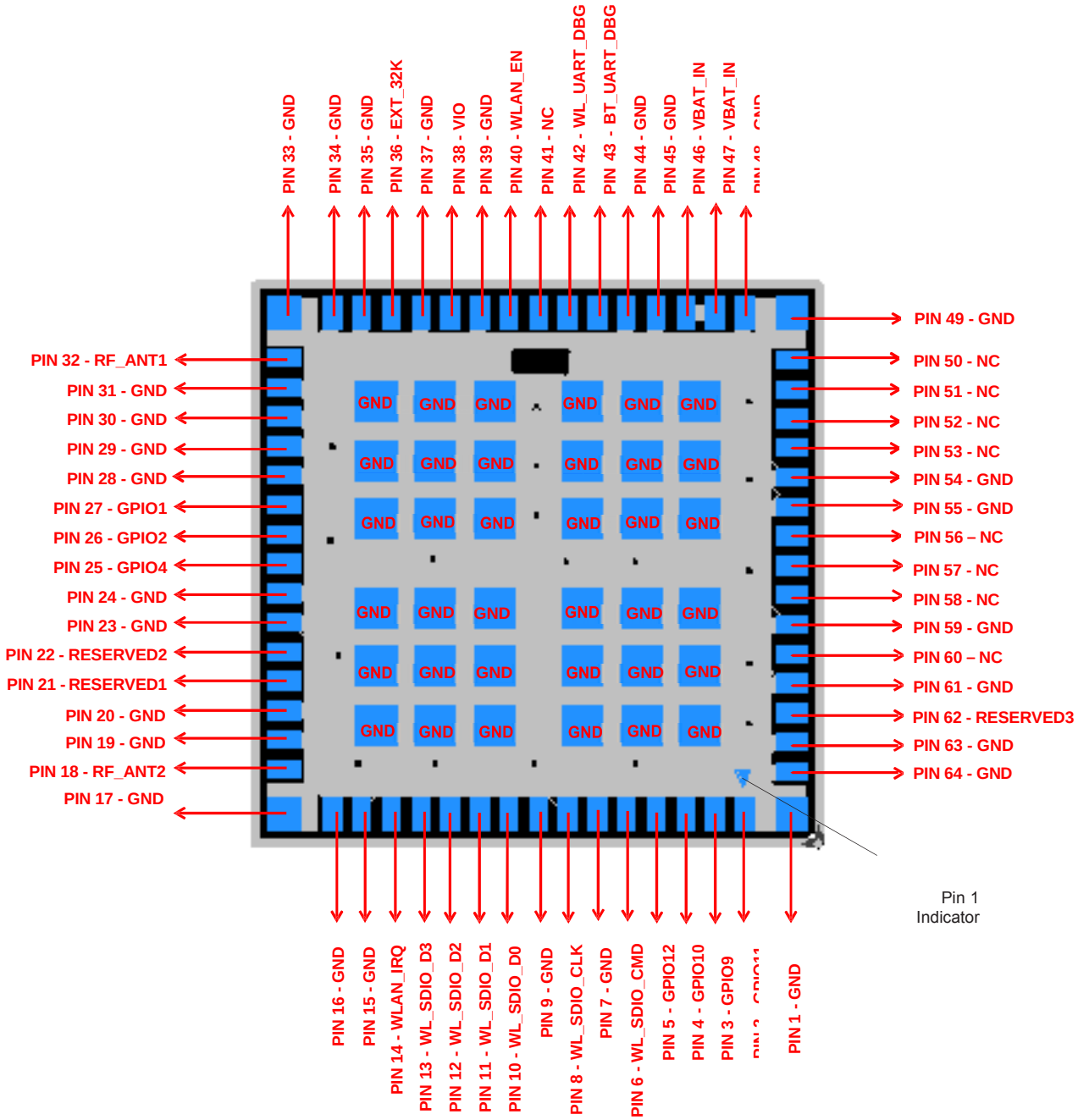


Figure 1-1. 100-Pin MOC Package (Bottom View)

3.1 Pin Attributes

Table 3-1 describes the module pins.

Table 3-1. Pin Attributes

PIN NAME	PIN NO.	TYPE/ DIR	SHUTDOWN STATE	AFTER POWER UP(1)	VOLTAGE LEVEL	CONNECTIVITY	DESCRIPTION
Clocks and Reset Signals							
WL_SDIO_CLK	8	I	Hi-Z	Hi-Z	1.8 V	v	WLAN SDIO clock. Must be driven by the
EXT_32K	36	ANA			–	v	Input sleep clock:
WLAN_EN	40	I	PD	PD	1.8 V	v	Mode setting: high = enable
NC	41	I	PD	PD	–	x	
VIO_IN	38	POW	PD	PD	1.8 V	v	Connect to 1.8-V
VBAT_IN	46	POW			VBAT	v	Power supply input,
VBAT_IN	47	POW			VBAT	v	Power supply input,
GPIO11	2	I/O	PD	PD	1.8 V	v	Reserved for future use. NC
GPIO9	3	I/O	PD	PD	1.8 V	v	Reserved for future use. NC
GPIO10	4	I/O	PU	PU	1.8 V	v	Reserved for future use. NC
GPIO12	5	I/O	PU	PU	1.8 V	v	Reserved for future use. NC
RESERVED1	21	I	PD	PD	1.8 V	x	Reserved for future use. NC
RESERVED2	22	I	PD	PD	1.8 V	x	Reserved for future use. NC
GPIO4	25	I/O	PD	PD	1.8 V	v	Reserved for future use. NC
RESERVED3	62	O	PD	PD	1.8 V	x	Reserved for future use. NC
WL_SDIO_CMD_1V8	6	I/O	Hi-Z	Hi-Z	1.8 V	v	WLAN SDIO command
WL_SDIO_D0_1V8	10	I/O	Hi-Z	Hi-Z	1.8 V	v	WLAN SDIO data bit 0
WL_SDIO_D1_1V8	11	I/O	Hi-Z	Hi-Z	1.8 V	v	WLAN SDIO data bit 1
WL_SDIO_D2_1V8	12	I/O	Hi-Z	Hi-Z	1.8 V	v	WLAN SDIO data bit 2

(1) PU = pullup; PD = pulldown
(2) v = connect; x = no connect
(3) Host must provide PU using a 10-K resistor for all non-CLK SDIO signals.

Table 3-1. Pin Attributes (continued)

PIN NAME	PIN NO.	TYPE/ DIR	SHUTDOWN STATE	AFTER POWER UP(1)	VOLTAGE LEVEL	CONNECTIVITY	DESCRIPTION
WL_SDIO_D3_1V8	13	I/O	Hi-Z	PU	1.8 V	v	WLAN SDIO data bit 3. Changes state to PU at WL_EN or BT_EN assertion for
WL_IRQ_1V8	14	O	PD	0	1.8 V	v	WLAN SDIO out-of- band interrupt line. Set to rising edge (active high) by default. (To extract the debug option WL_RS232_ TX/RX
RF_ANT2	18	ANA			–	v	2.4-GHz ANT2 TX, RX; 2.4-GHz secondary
GPIO2	26	I/O	PD	PD	1.8 V	v	WL_RS232_RX (when WLAN_IRQ =
GPIO1	27	I/O	PD	PD	1.8 V	v	WL_RS232_TX (when WLAN_IRQ =
RF_ANT1	32	ANA			–	v	2.4-GHz WLAN main antenna SISO,
WL_UART_DBG	42	O	PU	PU	1.8 V	v	Option: WLAN
NC	43	O	PU	PU	1.8 V	x	
NC	50	O	PU	PU	1.8 V	x	
NC	51	I	PU	PU	1.8 V	x	
NC	52	O	PU	PU	1.8 V	x	
NC	53	I	PU	PU	1.8 V	x	
NC	56	I	PD	PD	1.8 V	x	
NC	57	O	PD	PD	1.8 V	x	
NC	58	I/O	PD	PD	1.8 V	x	
NC	60	I/O	PD	PD	1.8 V	x	

Table 3-1. Pin Attributes (continued)

PIN NAME	PIN NO.	TYPE/ DIR	SHUTDOWN STATE	AFTER POWER UP(1)	VOLTAGE LEVEL	Connectivity	DESCRIPTION
GND	1	GND			–	v	
GND	7	GND			–	v	
GND	9	GND			–	v	
GND	15	GND			–	v	
GND	16	GND			–	v	
GND	17	GND			–	v	
GND	19	GND			–	v	
GND	20	GND			–	v	
GND	23	GND			–	v	
GND	24	GND			–	v	
GND	28	GND			–	v	
GND	29	GND			–	v	
GND	30	GND			–	v	
GND	31	GND			–	v	
GND	33	GND			–	v	
GND	34	GND			–	v	
GND	35	GND			–	v	
GND	37	GND			–	v	
GND	39	GND			–	v	
GND	44	GND			–	v	
GND	45	GND			–	v	
GND	48	GND			–	v	
GND	49	GND			–	v	
GND	54	GND			–	v	
GND	55	GND			–	v	
GND	59	GND			–	v	
GND	61	GND			–	v	
GND	63	GND			–	v	
GND	64	GND			–	v	
GND	G1 – G36	GND			–	v	

4 Specifications

All specifications are measured at the module pins using the 865-0329 evaluation board. All measurements are performed with V_{BAT} = 3.7 V, V_{IO} = 1.8 V, 25°C for typical values with matched RF antennas, unless otherwise indicated.

4.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{BAT}		4.8(2)	V
V_{IO}	–0.5	2.1	V
Input voltage to analog pins	–0.5	2.1	V
Input voltage limits (CLK_IN)	–0.5	VDD_IO	V
Input voltage to all other pins	–0.5	(VDD_IO + 0.5 V)	V
Operating ambient temperature	–20	70(3)	°C
Storage temperature, T_{stg}	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 4.8 V cumulative to 2.33 years, including charging dips and peaks
(3) In the system, a control mechanism exists to ensure T_j < 125°C. When T_j approaches this threshold, the control mechanism manages the transmitter patterns.

4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{BAT}(1)	DC supply range for all modes		2.9	3.7	4.8	V
V_{IO}	1.8-V I/O ring power supply voltage		1.62	1.8	1.95	V
V_{IH}	I/O high-level input voltage		0.65 × VDD_IO		VDD_IO	V
V_{IL}	I/O low-level input voltage		0		0.35 × VDD_IO	V
V_{IH_EN}	Enable inputs high-level input voltage		1.365		VDD_IO	V
V_{IL_EN}	Enable inputs low-level input voltage		0		0.4	V
V_{OH}	High-level output voltage	@ 4 mA	VDD_IO –0.45		VDD_IO	V
V_{OL}	Low-level output voltage	@ 4 mA	0		0.45	V
T_r,T_f	Input transitions time T_r,T_f from 10% to 90% (digital I/O)(2)		1		10	ns
T_r	Output rise time from 10% to 90% (digital pins)(2)	C_L < 25 pF			5.3	ns
T_f	Output fall time from 10% to 90% (digital pins)(2)	C_L < 25 pF			4.9	ns

(1) 4.8 V is applicable only for 2.33 years (30% of the time). Otherwise, maximum V_{BAT} must not exceed 4.3 V.
(2) Applies to all digital lines except PCM and slow clock lines

Recommended Operating Conditions *(continued)*

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
	Ambient operating temperature		–20		70	ºC
Maximum power	WLAN operation				2.8	W

4.4 External Digital Slow Clock Requirements

The supported digital slow clock is 32.768 kHz digital (square wave). All core functions share a single input.

		CONDITION	MIN	TYP	MAX	UNIT
	Input slow clock frequency		32768			Hz
	Input slow clock accuracy (Initial + temp + aging)	WLAN,			±250	ppm
T_r, T_f	Input transition time (10% to 90%)				200	ns
	Frequency input duty cycle		15%	50%	85%	
V_{IH}, V_{IL}	Input voltage limits	Square wave, DC-coupled	0.65 x VDD_IO		VDD_IO	V_{peak}
			0		0.35 x VDD_IO	
	Input impedance		1			MΩ
	Input capacitance				5	pF

4.5 Thermal Resistance Characteristics for MOC 100-Pin Package

THERMAL METRICS(1)		(°C/W)(2)
θ_{JA}	Junction to free air(3)	16.6
θ_{JB}	Junction to board	6.06
θ_{JC}	Junction to case(4)	5.13

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RΘJC] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.

(3) According to the JEDEC EIA/JESD 51 document

(4) Modeled using the JEDEC 2s2p thermal test board with 36 thermal vias

4.6 WLAN Performance: 2.4-GHz Receiver Characteristics

over operating free-air temperature range (unless otherwise noted). All RF and performance numbers are aligned to the module pin.

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
RF_ANT1 pin 2.4-GHz SISO					
Operation frequency range		2412		2484	MHz
Sensitivity: 20-MHz bandwidth. At < 10% PER limit	1 Mbps DSSS		–96.3		dBm
	2 Mbps DSSS		–93.2		
	5.5 Mbps CCK		–90.6		
	11 Mbps CCK		–87.9		
	6 Mbps OFDM		–92.0		
	9 Mbps OFDM		–90.4		
	12 Mbps OFDM		–89.5		
	18 Mbps OFDM		–87.2		
	24 Mbps OFDM		–84.1		
	36 Mbps OFDM		–80.7		
	48 Mbps OFDM		–76.5		
	54 Mbps OFDM		–74.9		
	MCS0 MM 4K		–90.4		
	MCS1 MM 4K		–87.6		
	MCS2 MM 4K		–85.9		
	MCS3 MM 4K		–82.8		
	MCS4 MM 4K		–79.4		
	MCS5 MM 4K		–75.2		
	MCS6 MM 4K		–73.5		
	MCS7 MM 4K		–72.4		
	MCS0 MM 4K 40 MHz		–86.7		
	MCS7 MM 4K 40 MHz		–67.0		
	MCS0 MM 4K MRC		–92.7		
	MCS7 MM 4K MRC		–75.2		
	MCS13 MM 4K		–73.7		
	MCS14 MM 4K		–72.3		
	MCS15 MM 4K		–71.0		
Maximum input level	OFDM	–20.0	–10.0		dBm
	CCK	–10.0	–6.0		
	DSSS	–4.0	–1.0		
Adjacent channel rejection: Sensitivity level +3 dB for OFDM; Sensitivity level +6 dB for 11b	2 Mbps DSSS	42.0			dB
	11 Mbps CCK	38.0			
	54 Mbps OFDM	2.0			

4.7 WLAN Performance: 2.4-GHz Transmitter Power

over operating free-air temperature range (unless otherwise noted). All RF and performance numbers are aligned to the module pin.

PARAMETER	CONDITION(1)	MIN	TYP	MAX	UNIT
	RF_ANT1 Pin 2.4-GHz SISO				
Output Power: Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM(2)	1 Mbps DSSS		17.3		dBm
	2 Mbps DSSS		17.3		
	5.5 Mbps CCK		17.3		
	11 Mbps CCK		17.3		
	6 Mbps OFDM		17.1		
	9 Mbps OFDM		17.1		
	12 Mbps OFDM		17.1		
	18 Mbps OFDM		17.1		
	24 Mbps OFDM		16.2		
	36 Mbps OFDM		15.3		
	48 Mbps OFDM		14.6		
	54 Mbps OFDM		13.8		
	MCS0 MM		16.1		
	MCS1 MM		16.1		
	MCS2 MM		16.1		
	MCS3 MM		16.1		
	MCS4 MM		15.3		
	MCS5 MM		14.6		
	MCS6 MM		13.8		
	MCS7 MM(3)		12.6		
	MCS0 MM 40 MHz		14.8		
	MCS7 MM 40 MHz		11.3		
	RF_ANT1 + RF_ANT2				
	MCS12 (WL18x5)		18.5		dBm
	MCS13 (WL18x5)		17.4		
	MCS14 (WL18x5)		14.5		
	MCS15 (WL18x5)		13.4		
	RF_ANT1 + RF_ANT2				
Operation frequency range		2412		2484	MHz
Return loss			–10.0		dB
Reference input impedance			50.0		Ω

(1) Maximum transmitter power (TP) degradation of up to 30% is expected, starting from 80°C ambient temperature on MIMO operation

(2) Regulatory constraints limit module output power to the following:
- Channel 14 is used only in Japan; to keep the channel spectral shaping requirement, the power is limited: 14.5 dBm.
- Channels 1, 11 @ OFDM legacy and HT 20-MHz rates: 12 dBm
- Channels 1, 11 @ HT 40-MHz rates: 10 dBm
- Channel 7 @ HT 40-MHz lower rates: 10 dBm
- Channel 5 @ HT 40-MHz upper rates: 10 dBm
- All 11B rates are limited to 16 dBm to comply with the ETSI PSD 10 dBm/MHz limit.
- All OFDM rates are limited to 16.5 dBm to comply with the ETSI EIRP 20 dBm limit.
- For clarification regarding power limitation,

(3) To ensure compliance with the EVM conditions specified in the PHY chapter of IEEE Std 802.11™ – 2012:
- MCS7 20 MHz channel 12 output power is 2 dB lower than the typical value.
- MCS7 20 MHz channel 8 output power is 1 dB lower than the typical value.

4.8 WLAN Performance: Currents

over operating free-air temperature range (unless otherwise noted). All RF and performance numbers are aligned to the module pin.

PARAMETER	SPECIFICATION	TYP (AVG) –25°C	UNIT
Receiver	Low-power mode (LPM) 2.4-GHz RX SISO20 single chain	49	mA
	2.4 GHz RX search SISO20	54	
	2.4-GHz RX search MIMO20	74	
	2.4-GHz RX search SISO40	59	
	2.4-GHz RX 20 M SISO 11 CCK	56	
	2.4-GHz RX 20 M SISO 6 OFDM	61	
	2.4-GHz RX 20 M SISO MCS7	65	
	2.4-GHz RX 20 M MRC 1 DSSS	74	
	2.4-GHz RX 20 M MRC 6 OFDM	81	
	2.4-GHz RX 20 M MRC 54 OFDM	85	
	2.4-GHz RX 40-MHz MCS7	77	
Transmitter	2.4-GHz TX 20 M SISO 6 OFDM 15.4 dBm	285	mA
	2.4-GHz TX 20 M SISO 11 CCK 15.4 dBm	273	
	2.4-GHz TX 20 M SISO 54 OFDM 12.7 dBm	247	
	2.4-GHz TX 20 M SISO MCS7 11.2 dBm	238	
	2.4-GHz TX 20 M MIMO MCS15 11.2 dBm	420	
	2.4-GHz TX 40 M SISO MCS7 8.2 dBm	243	

(1) All RF and performance numbers are aligned to the module pin.
(2) Sensitivity degradation up to –3 dB may occur due to fast clock harmonics with dirty TX on.

4.9 Timing and Switching Characteristics

4.9.1 Power Management

4.19.1.1 Block Diagram – Internal DC-DCs

The device incorporates three internal DC-DCs (switched-mode power supplies) to provide efficient internal supplies, derived from V_{BAT}.

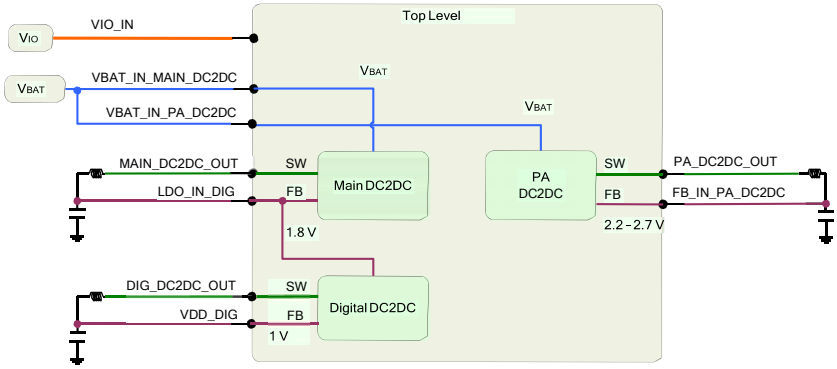


Figure 4-1. Internal DC-DCs

4.9.2 Power-Up and Shut-Down States

The correct power-up and shut-down sequences must be followed to avoid damage to the device.

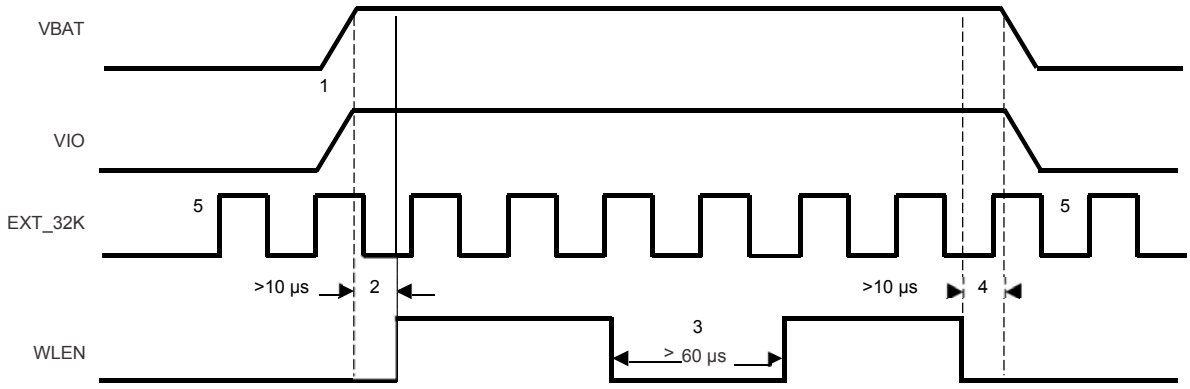
While V_{BAT} or V_{IO} or both are deasserted, no signals should be driven to the device. The only exception is the slow clock that is a fail-safe I/O.

While V_{BAT}, V_{IO}, and slow clock are fed to the device, but WL_EN is deasserted (low), the device is in SHUTDOWN state. In SHUTDOWN state all functional blocks, internal DC-DCs, clocks, and LDOs are disabled.

To perform the correct power-up sequence, assert (high) WL_EN. The internal DC-DCs, LDOs, and clock start to ramp and stabilize. Stable slow clock, V_{IO}, and V_{BAT} are prerequisites to the assertion of one of the enable signals.

To perform the correct shut-down sequence, deassert (low) WL_EN while all the supplies to the device (V_{BAT}, V_{IO}, and slow clock) are still stable and available. The supplies to the chip (V_{BAT} and V_{IO}) can be deasserted only after both enable signals are deasserted (low).

Figure 4-2 shows the general power scheme for the module, including the power-down sequence.



NOTE: 1. Either VBAT or VIO can come up first.
- VBAT and VIO supplies and slow clock (SCLK), must be stable prior to EN being asserted and at all times when the EN is active.
- At least 60 µs is required between two successive device enables. The device is assumed to be in shutdown state during that period, meaning all enables to the device are LOW for that minimum duration.
- EN must be deasserted at least 10 µs before VBAT or VIO supply can be lowered (order of supply turn off after EN shutdown is immaterial).
- EXT_32K - Fail safe I/O

Figure 4-2. Power-Up System

4.9.3 Chip Top-level Power-Up Sequence

Figure 4-3 shows the top-level power-up sequence for the chip.

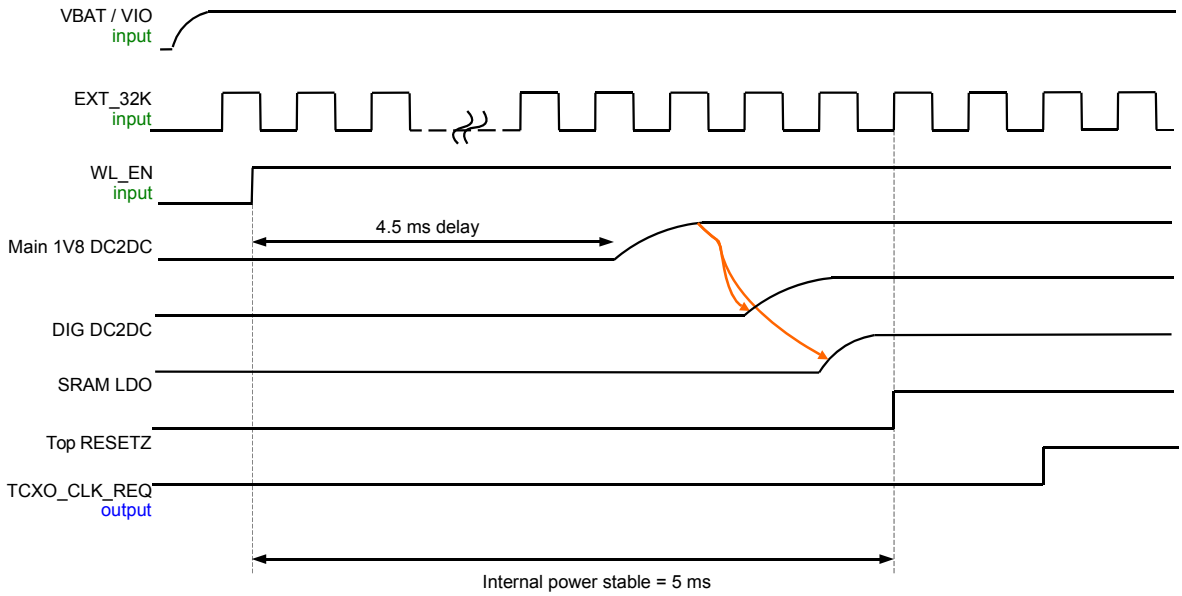


Figure 4-3. Chip Top-Level Power-Up Sequence

4.9.4 WLAN Power-Up Sequence

Figure 4-4 shows the WLAN power-up sequence.

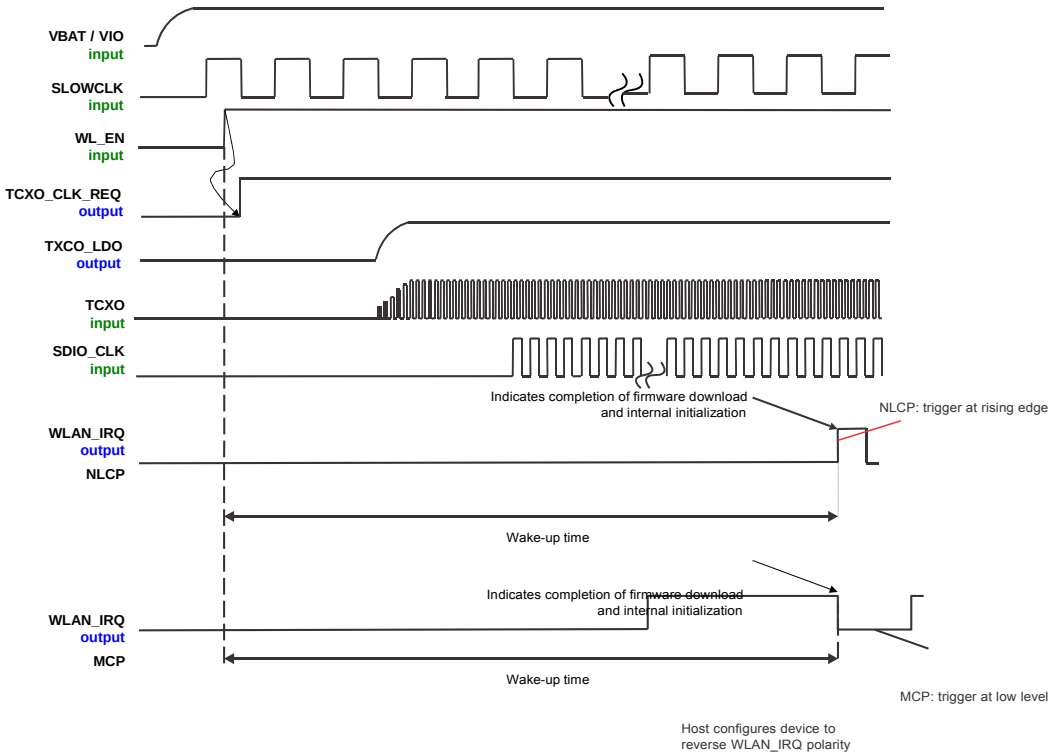


Figure 4-4. WLAN Power-Up Sequence

4.9.5 WLAN SDIO Transport Layer

The SDIO is the host interface for WLAN. The interface between the host and the WL18xx module uses an SDIO interface and supports a maximum clock rate of 50 MHz.

The device SDIO also supports the following features of the SDIO V3 specification:

- 4-bit data bus
- Synchronous and asynchronous in-band interrupt
- Default and high-speed (HS, 50 MHz) timing
- Sleep and wake commands

4.19.6.1 SDIO Timing Specifications

Figure 4-6 and Figure 4-7 show the SDIO switching characteristics over recommended operating conditions and with the default rate for input and output.

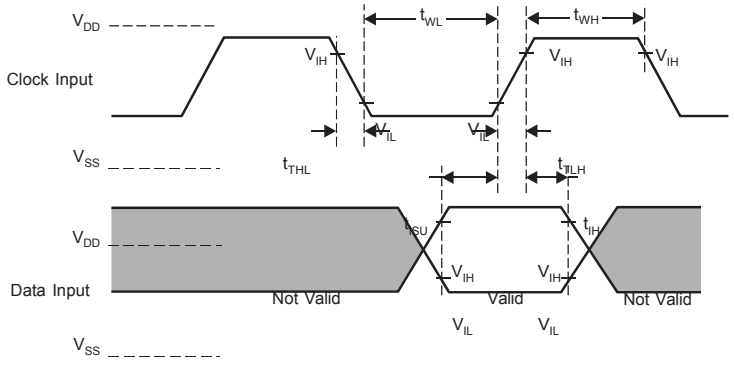


Figure 4-6. SDIO Default Input Timing

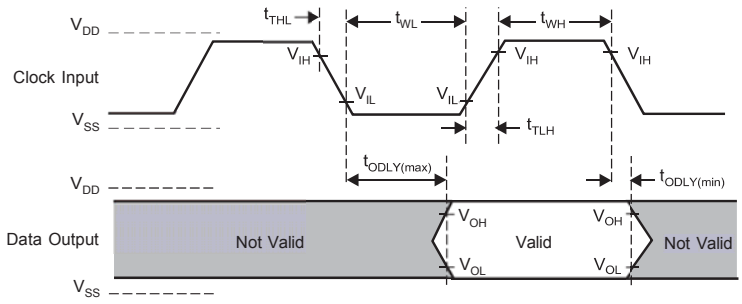


Figure 4-7. SDIO Default Output Timin

Table 4-1 lists the SDIO default timing characteristics.

Table 5-1. SDIO Default Timing Characteristics(1)

		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK(2)	0.0	26.0	MHz
DC	Low, high duty cycle(2)	40.0%	60.0%	
t_{TLH}	Rise time, CLK(2)		10.0	ns
t_{THL}	Fall time, CLK(2)		10.0	ns
t_{ISU}	Setup time, input valid before CLK ↑(2)	3.0		ns
t_{IH}	Hold time, input valid after CLK ↑(2)	2.0		ns
t_{ODLY}	Delay time, CLK ↓ to output valid(2)	7.0	10.0	ns
C_l	Capacitive load on outputs(2)		15.0	pF

(1) To change the data out clock edge from the falling edge (default) to the rising edge, set the configuration bit.
(2) Parameter values reflect maximum clock frequence

4.19.6.2 SDIO Switching Characteristics – High Rate

Figure 4-8 and Figure 4-9 show the parameters for maximum clock frequency.

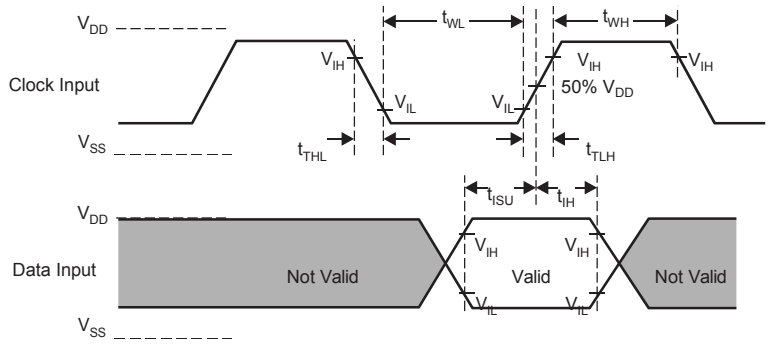


Figure 4-8. SDIO HS Input Timing

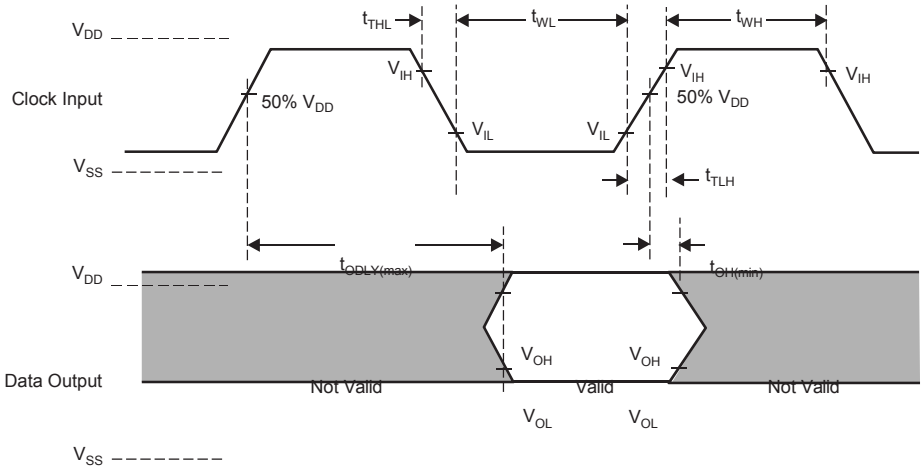


Figure 4-9. SDIO HS Output Timing

Table 4-2 lists the SDIO high-rate timing characteristics.

Table 4-2. SDIO HS Timing Characteristics

		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	0.0	52.0	MHz
DC	Low, high duty cycle	40.0%	60.0%	
t_{TLH}	Rise time, CLK		3.0	ns
t_{THL}	Fall time, CLK		3.0	ns
t_{ISU}	Setup time, input valid before CLK ↑	3.0		ns
t_{IH}	Hold time, input valid after CLK ↑	2.0		ns
t_{ODLY}	Delay time, CLK ↑ to output valid	7.0	10.0	ns
C_l	Capacitive load on outputs		10.0	pF

4.19.7 HCI UART Shared-Transport Layers for All Functional Blocks (Except WLAN)

The device includes a UART module as the host controller interface (HCI) transport layer. The HCI transports commands, events, and ACL between the device and its host using HCI data packets ack as a shared transport for all functional blocks except WLAN. Table 4-3 lists the transport mechanism

Table 4-3. Transport Mechanism

WLAN	SHARED HCI FOR ALL FUNCTIONAL BLOCKS EXCEPT WLAN	
WLAN HS SDIO	Over UART	

The HCI UART supports most baud rates (including all PC rates) for all fast-clock frequencies up to a maximum of 4 Mbps. After power up, the baud rate is set for 115.2 Kbps, regardless of the fast-clock frequency. The baud rate can then be changed using a VS command. The device responds with a Command Complete Event (still at 115.2 Kbps), after which the baud rate change occurs.

HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Receiver-transmitter underflow detection
- CTS, RTS hardware flow control
- 4 wire (H4)

Table 4-4 lists the UART default settings.

Table 4-4. UART Default Setting

PARAMETER	VALUE
Bit rate	115.2 Kbps
Data length	8 bits
Stop-bit	1
Parity	None

4.19.7.1 UART 4-Wire Interface – H4

The interface includes four signals:

- TXD
- RXD
- CTS
- RTS

Flow control between the host and the device is byte-wise by hardware.

When the UART RX buffer of the device passes the flow-control threshold, the buffer sets the UART_RTS signal high to stop transmission from the host. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

Figure 4-10 shows the UART timing.

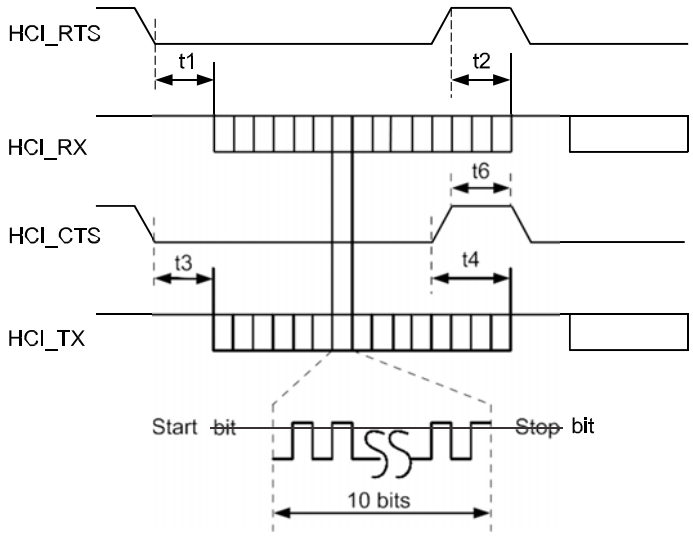


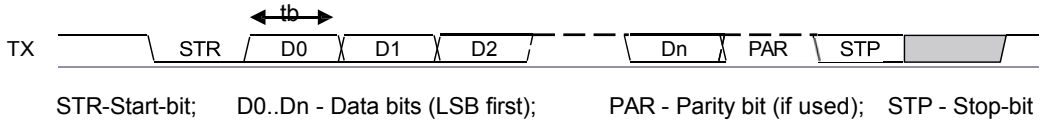
Figure 4-10. UART Timing Diagram

Table 4-5 lists the UART timing characteristics.

Table 4-5. UART Timing Characteristics

	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	Baud rate		37.5		4364	Kbps
	Baud rate accuracy per byte	Receive-transmit	–2.5%		1.5%	
	Baud rate accuracy per bit	Receive-transmit	–12.5%		12.5%	
t3	CTS low to TX_DATA on		0.0	2.0		µs
t4	CTS high to TX_DATA off	Hardware flow control			1.0	Byte
t6	CTS high pulse width		1.0			Bit
t1	RTS low to RX_DATA on		0.0	2.0		µs
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16.0	Bytes

Figure 4-11 shows the UART data frame.



STR-Start-bit; D0..Dn - Data bits (LSB first); PAR - Parity bit (if used); STP - Stop-bit

Figure 4-11. UART Data Frame

5 Detailed Description

The 865-0329 module is a self-contained connectivity solution based on connectivity. The module is based on proven technology.

Figure 5-1 shows a high-level view of the variant.

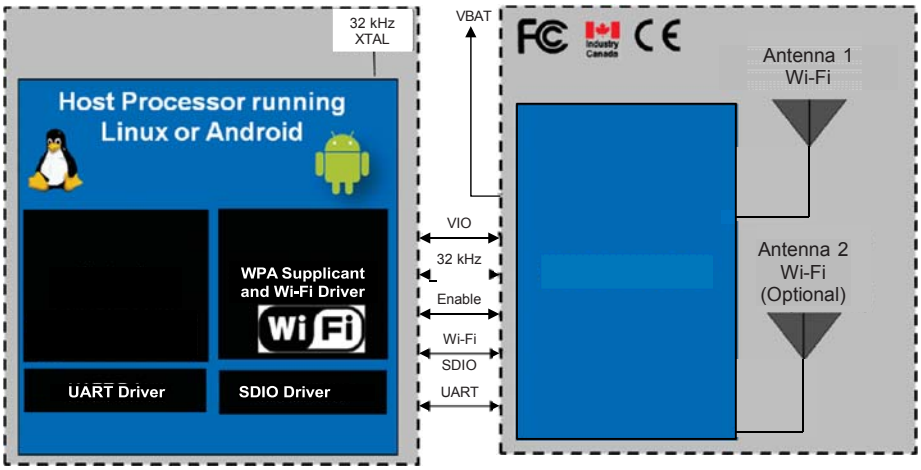


Figure 5-1. High-Level System Diagram

Table 5-1, Table 5-2, and Table 5-3 list performance parameters along with shutdown and sleep currents.

Table 5-1. WLAN Performance Parameters

WLAN(1)	CONDITIONS	SPECIFICATION (TYP)	UNIT
Maximum TX power	1-Mbps DSSS	17.3	dBm
Minimum sensitivity	1-Mbps DSSS	–96.3	dBm
Sleep current	Leakage, firmware retained	160	µA
Connected IDLE	No traffic IDLE connect	750	µA
RX search	Search (SISO20)	54	mA
RX current (SISO20)	MCS7, 2.4 GHz	65	mA
TX current (SISO20)	MCS7, 2.4 GHz, +11.2 dBm	238	mA
Maximum peak current consumption during calibration(2)		850	mA

(1) System design power scheme must comply with both peak and average TX bursts.
(2) Peak current V_{BAT} can hit 850 mA during device calibration.
- At wakeup, the module performs the entire calibration sequence at the center of the 2.4-GHz band.
- Once a link is established, calibration is performed periodically (every 5 minutes) on the specific channel tuned.

- The maximum VBAT value is based on peak calibration consumption with a 30% margin.

Table 5-3. Shutdown and Sleep Currents

PARAMETER	POWER SUPPLY CURRENT	TYP	UNIT
Shutdown mode All functions shut down	VBAT	10	µA
	VIO	2	
WLAN sleep mode	VBAT	160	µA
	VIO	60	

5.1 WLAN Features

- The device supports the following WLAN features:
- Integrated 2.4-GHz power amplifiers (PAs) for a complete WLAN solution
- Baseband processor: IEEE Std 802.11b/g and IEEE Std 802.11n data rates with 20- or 40-MHz SISO and 20-MHz MIMO
- Fully calibrated system (production calibration not required)
- Medium access controller (MAC)
    - Embedded ARM® central processing unit (CPU)
    - Hardware-based encryption-decryption using 64-, 128-, and 256-bit WEP, TKIP, or AES keys
    - Requirements for Wi-Fi-protected access (WPA and WPA2.0) and IEEE Std 802.11i (includes hardware-accelerated Advanced Encryption Standard [AES])
- New advanced coexistence scheme with Bluetooth and Bluetooth low energy wireless technology
- 2.4-GHz radio
    - Internal LNA and PA

– IEEE Std 802.11b, 802.11g, and 802.11n

- 4-bit SDIO host interface, including high speed (HS) and V3 modes

5.2 End Product Labeling

- These modules are designed to comply with the FCC single modular FCC grant, 2AODL-CONEXTGTWY. The host system using this module must display a visible label indicating the following text:
- Contains FCC ID: 2AODL- CONEXTGTWY
- These modules are designed to comply with the IC single modular FCC grant, IC: 24209-CONEXTGTWY. The host system using this module must display a visible label indicating the following text:
- Contains IC: 24209-CONEXTGTWY
- L'étiquette d'homologation d'un module d'Innovation, Sciences et Développement économique Canada devra être posée sur le produit hôte à un endroit bien en vue, en tout temps. En l'absence d'étiquette, le produit hôte doit porter une étiquette sur laquelle figure le numéro d'homologation du module d'Innovation, Sciences et Développement économique Canada, précédé du mot « contient », ou d'une formulation similaire allant dans le même sens et qui va comme suit : Contient IC : 24209-CONEXTGTWY est le numéro d'homologation du module.

5.3 Manual Information to the End User

- The OEM integrator must be aware of not providing information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user's manual must include all required regulatory information and warnings as shown in this manual.

5.4 FCC/ISED Regulatory Compliance

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Warning: changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator and your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

FCC Part 15B Compliance Requirements for End User Device

The OEM integrator is responsible for ensuring that the host product which is installed and operating with the module is in compliant with Part 15B requirements.

Please note that For a Class B digital device or peripheral, the instructions furnished the user manual of the end-user product shall include statement set out in §15.105 Information to the user or such similar statement and place it in a prominent location in the text of the manual.

This device contains licence-exempt transmitter(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s).

Operation is subject to the following two conditions:

This device may not cause interference.

This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

L'appareil ne doit pas produire de brouillage;

L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

RF Exposure Notice

This equipment complies with FCC/ IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

Cet équipement est conforme aux limites d'exposition aux radiations FCC/ IC CNR-102 établies pour un environnement non contrôlé. Cet émetteur ne doit pas être situé ou fonctionner conjointement avec une autre antenne ou un autre émetteur. Cet équipement doit être installé et utilisé avec une distance minimale de 20 cm entre le radiateur et votre corps.

6 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the component specification, and Schneider does not warrant its accuracy or completeness. The customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Design Recommendations

This section describes the layout recommendations for the module, RF trace, and antenna.

Table 6-1 summarizes the layout recommendations.

Table 6-2. Layout Recommendations Summary

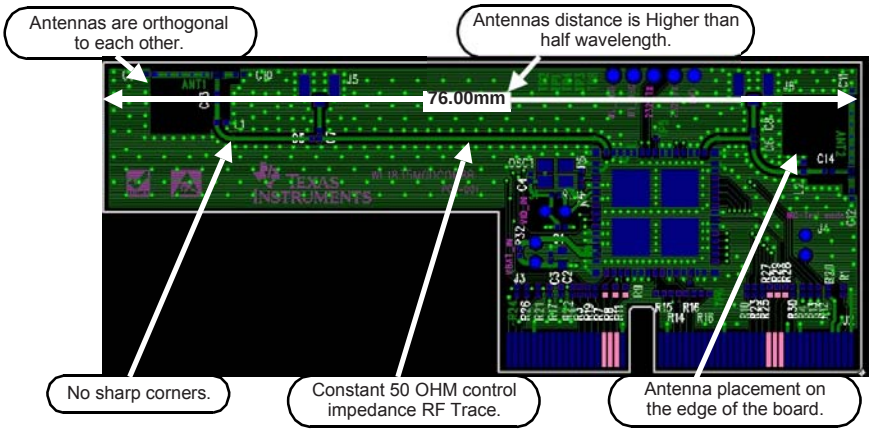
ITEM	DESCRIPTION
Thermal	
1	The proximity of ground vias must be close to the pad.
2	Signal traces must not be run underneath the module on the layer where the module is mounted.
3	Have a complete ground pour in layer 2 for thermal dissipation.
4	Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
5	Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.
6	Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.
RF Trace and Antenna Routing	
7	The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.
8	The RF trace bends must be gradual with an approximate maximum bend of 45° with trace mitered. RF traces must not have sharp corners.
9	RF traces must have via stitching on the ground plane beside the RF trace on both sides.
10	RF traces must have constant impedance (microstrip transmission line).
11	For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
12	There must be no traces or ground under the antenna section.
13	RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.
Supply and Interface	
14	The power trace for V_{BAT} must be at least 40-mil wide.
15	The 1.8-V trace must be at least 18-mil wide.
16	Make VBAT traces as wide as possible to ensure reduced inductance and trace resistance.
17	If possible, shield V_{BAT} traces with ground above, below, and beside the traces.
18	SDIO signals traces (CLK, CMD, D0, D1, D2, and D3) must be routed in parallel to each other and as short as possible (less than 12 cm). In addition, every trace length must be the same as the others. There should be enough space between traces
19	SDIO and digital clock signals are a source of noise. Keep the traces of these signals as short as possible. If possible, maintain a clearance around them.

6.1.2 RF Trace and Antenna Layout Recommendations

Figure 6-2 shows the location of the antenna on board as well as the RF trace routing from the module. The Pulse multilayer antennas are mounted on the board with a specific layout and matching circuit for the radiation test conducted in FCC, CE, and IC certifications.

NOTE

For reuse of the regulatory certification, a trace of 1-dB attenuation is required on the final application board.



Follow these RF trace routing recommendations:

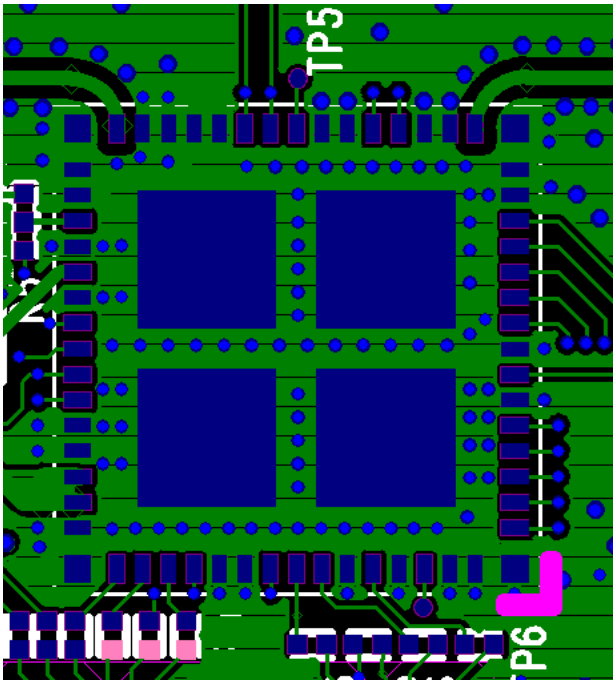
- RF traces must have 50-Ω impedance.
- RF traces must not have sharp corners.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible. The antenna, RF traces, and module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

6.1.3 Module Layout Recommendations

Figure 6-3 shows layer 1 and layer 2 of the module layout.

the

Layer 1



Layer 2(Solid GND)

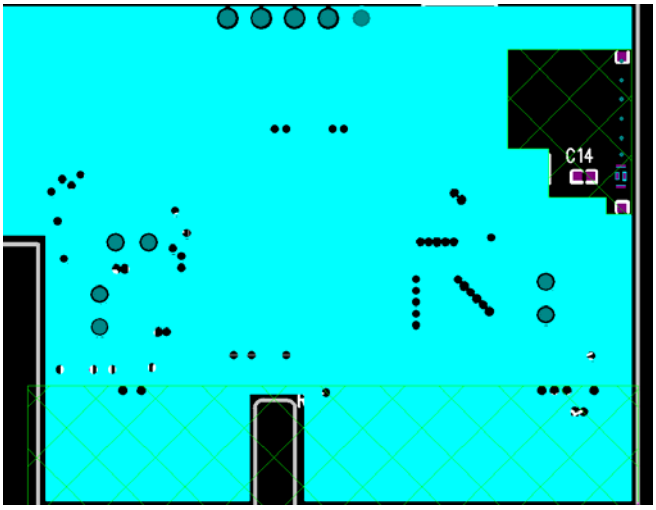


Figure 6-3. The Module Layout

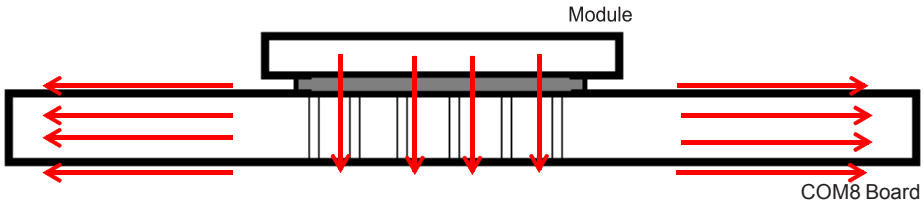
Follow these module layout recommendations:

- Ensure a solid ground plane and ground vias under the module for stable system and thermal dissipation.
- Do not run signal traces underneath the module on a layer where the module is mounted.
- Signal traces can be run on a third layer under the solid ground layer and beneath the module mounting.
- Run the host interfaces with ground on the adjacent layer to improve the return path.
- We recommends routing the signals as short as possible to the host.

6.2 Thermal Board Recommendations

6.2.1 The module uses µvias for layers 1 through 6 with full copper filling, providing heat flow all the way to the module ground pads.

6.2.2 We recommends using one big ground pad under the module with vias all the way to connect the pad to all ground layers (see Figure 6-4).



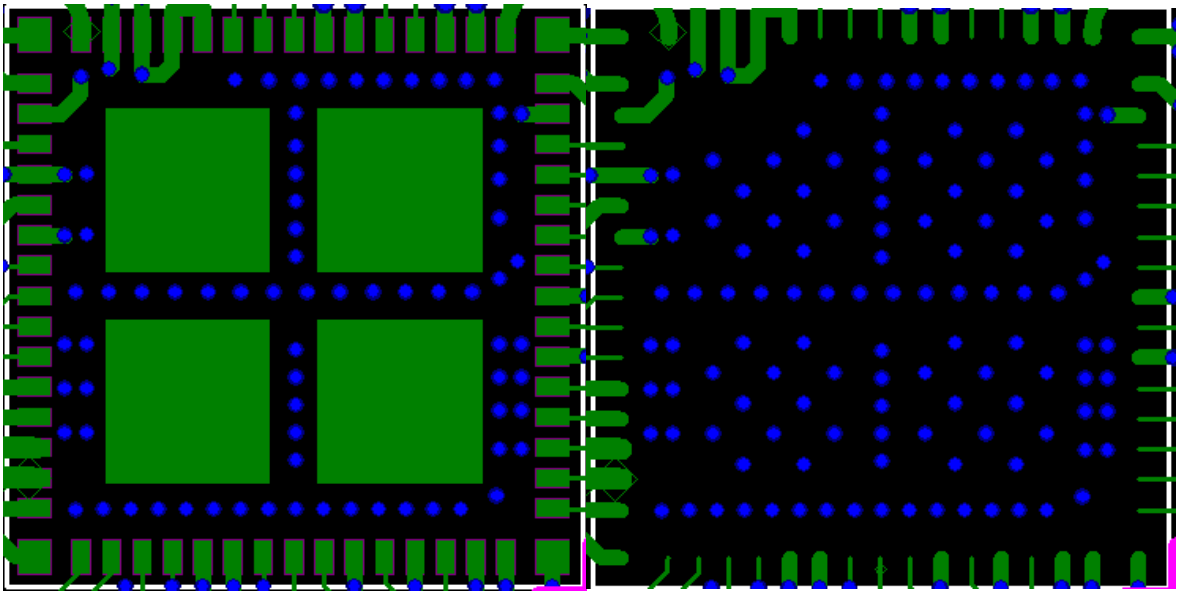


Figure 6-4. Block of Ground Pads on Bottom Side of Package

Figure 6-5 shows via array patterns, which are applied wherever possible to connect all of the layers to the module central or main ground pads.

Figure 6-5. Via Array Patterns

6.2.3 Baking and SMT Recommendations

6.2.3.1 Baking Recommendations

Follow these baking guidelines for the module:

- Follow MSL level 3 to perform the baking process.
- After the bag is open, devices subjected to reflow solder or other high temperature processes must be mounted within 168 hours of factory conditions (< 30°C/60% RH) or stored at <10% RH.
- If the Humidity Indicator Card reads >10%, devices require baking before they are mounted.
- If baking is required, bake devices for 8 hours at 125°C.

6.2.3.2 SMT Recommendations

Figure 6-6 shows the recommended reflow profile for the module.

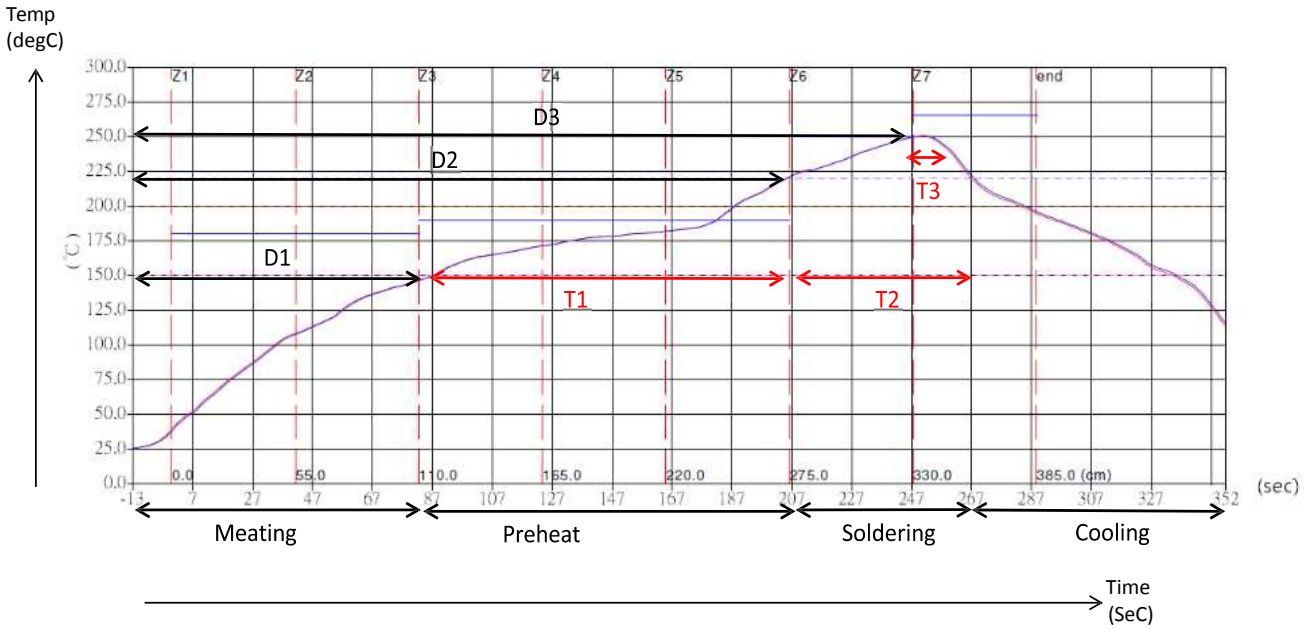


Figure 6-6. Reflow Profile for the Module

Table 6-3 lists the temperature values for the profile shown in Figure 6-6.

Table 6-3. Temperature Values for Reflow Profile

ITEM	TEMPERATURE (°C)	TIME (s)
Preheat	D1 to approximately D2: 140 to 200	T1: 80 to approximately 120
Soldering	D2: 220	T2: 60 ±10
Peak temperature	D3: 250 maximum	T3: 10

NOTE

The manufacturer does not recommend the use of conformal coating or similar material on the module. This coating can lead to localized stress on the WCSP solder connections inside the module and impact the device reliability. Care should be taken during module assembly process to the final PCB to avoid the presence of foreign material inside the module.

7 Mechanical, Packaging, and Orderable Information

7.1 Module Mechanical Outline

Figure 7-1 shows the mechanical outline for the device.

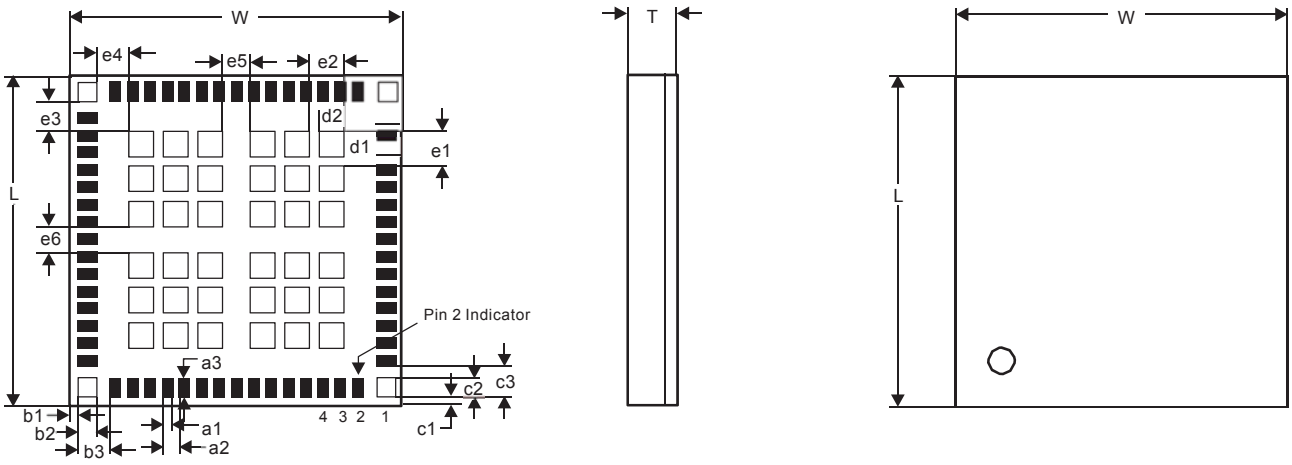


Figure 7-1. Module Mechanical Outline

Table 7-1 lists the dimensions for the mechanical outline of the device.

NOTE

The module weighs 0.684 g typical.

Table 7-1. Dimensions for the Module Mechanical Outline

MARKING	MIN (mm)	NOM (mm)	MAX (mm)	MARKING	MIN (mm)	NOM (mm)	MAX (mm)
L (body size)	13.20	13.30	13.40	c2	0.65	0.75	0.85
W (body size)	13.30	13.40	13.50	c3	1.15	1.25	1.35
T (thickness)	1.80	1.90	2.00	d1	0.90	1.00	1.10
a1	0.30	0.40	0.50	d2	0.90	1.00	1.10
a2	0.60	0.70	0.80	e1	1.30	1.40	1.50
a3	0.65	0.75	0.85	e2	1.30	1.40	1.50
b1	0.20	0.30	0.40	e3	1.15	1.25	1.35
b2	0.65	0.75	0.85	e4	1.20	1.30	1.40
b3	1.20	1.30	1.40	e5	1.00	1.10	1.20
c1	0.20	0.30	0.40	e6	1.00	1.10	1.20

7.2 Tape and Reel Information

Emboss taping specification for MOC 100 pin.

7.2.1 *Tape and Reel Specification*

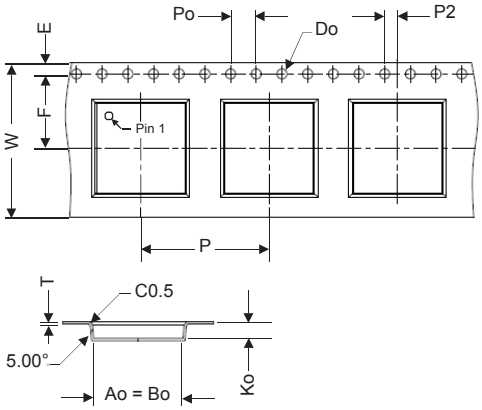


Figure 7-2. Tape Specification

Table 7-2. Dimensions for Tape Specification

ITEM	W	E	F	P	Po	P2	Do	T	Ao	Bo	Ko
DIMENSION (mm)	24.00 (±0.30)	1.75 (±0.10)	11.50 (±0.10)	20.00 (±0.10)	4.00 (±0.10)	2.00 (±0.10)	2.00 (±0.10)	0.35 (±0.05)	13.80 (±0.10)	13.80 (±0.10)	2.50 (±0.10)

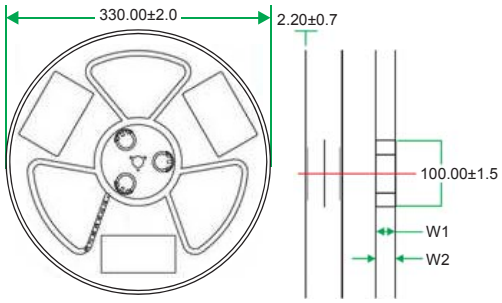


Figure 7-3. Reel Specification

Table 7-3. Dimensions for Reel Specification

ITEM	W1	W2
DIMENSION (mm)	24.4 (+1.5, –0.5)	30.4 (maximum)

7.2.2 *7Packing Specification*

7.2.2.1 Reel Box

The reel is packed in a moisture barrier bag fastened by heat-sealing. Each moisture-barrier bag is packed into a reel box, as shown in Figure 7-4.

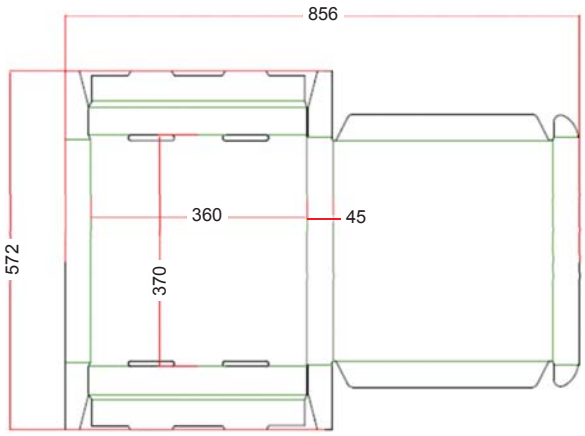


Figure 7-4. Reel Box

The reel box is made of corrugated fiberboard.

7.2.2.2Shipping Box

Figure 7-5 shows a typical shipping box. If the shipping box has excess space, filler (such as cushion) is added.

NOTE

The size of the shipping box may vary depending on the number of reel boxes packed.

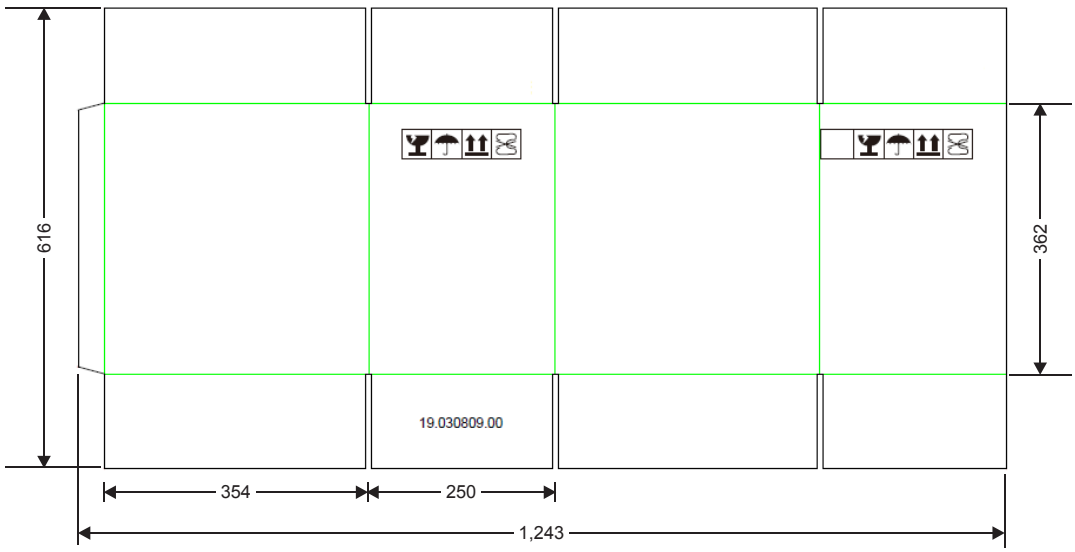


Figure 7-5. Shipping Box

The shipping box is made of corrugated fiberboard.

7.3 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish	MSL Peak Temp (°C) (3)	Op Temp (°C)
865-0329	ACTIVE	QFM	MOC	100	1200	Green	NiPdAu	250	–20 to 70

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: The device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but the manufacturer does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: The manufacture has discontinued the production of the device.

(2) RoHS Compliance: This product has an RoHS exemption for one or more subcomponent(s). The product is otherwise considered Pb-Free (RoHS compatible) as defined above.

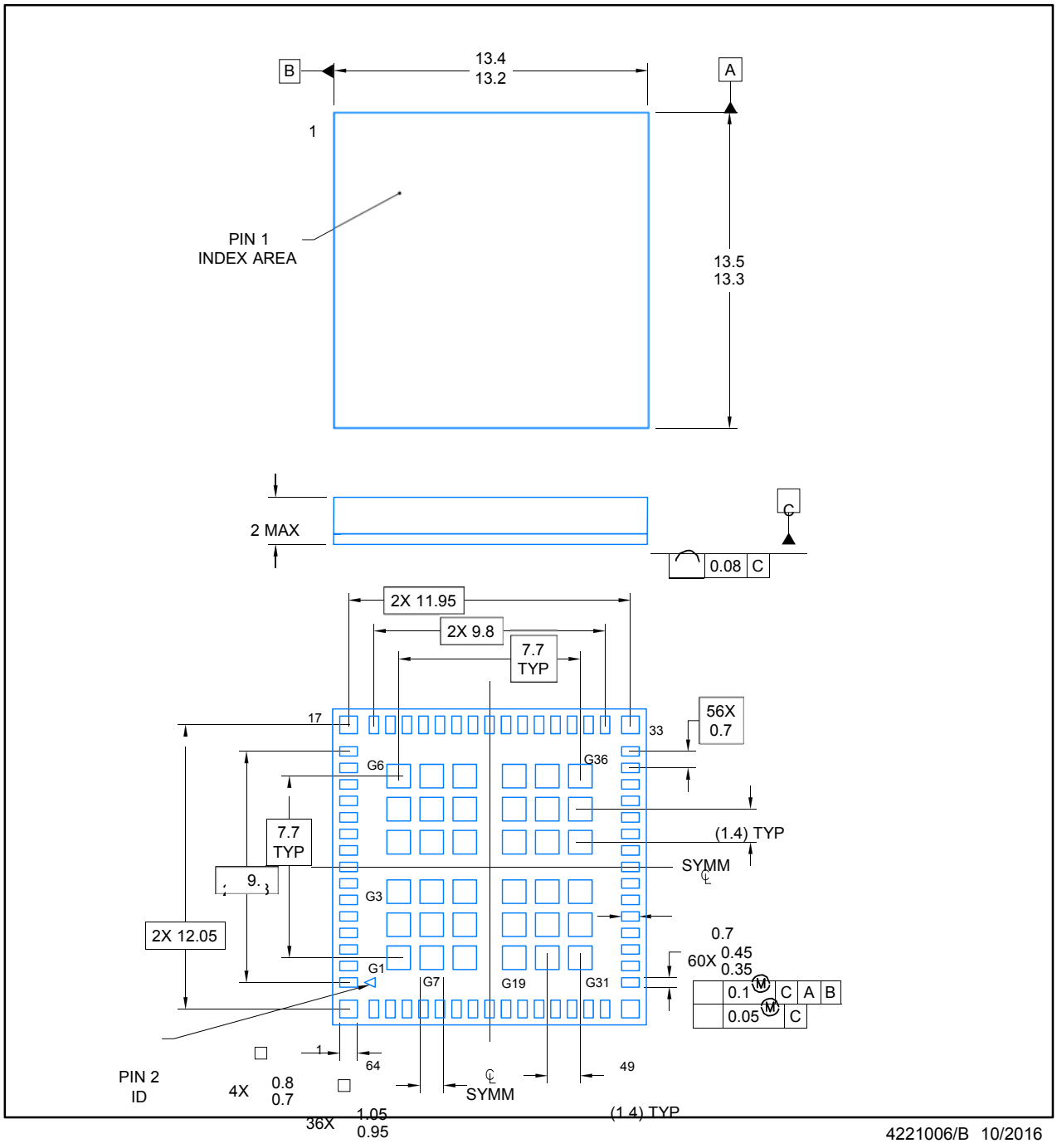
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PACKAGE OUTLINE

MOC0100A

QFM - 2.0 mm max height

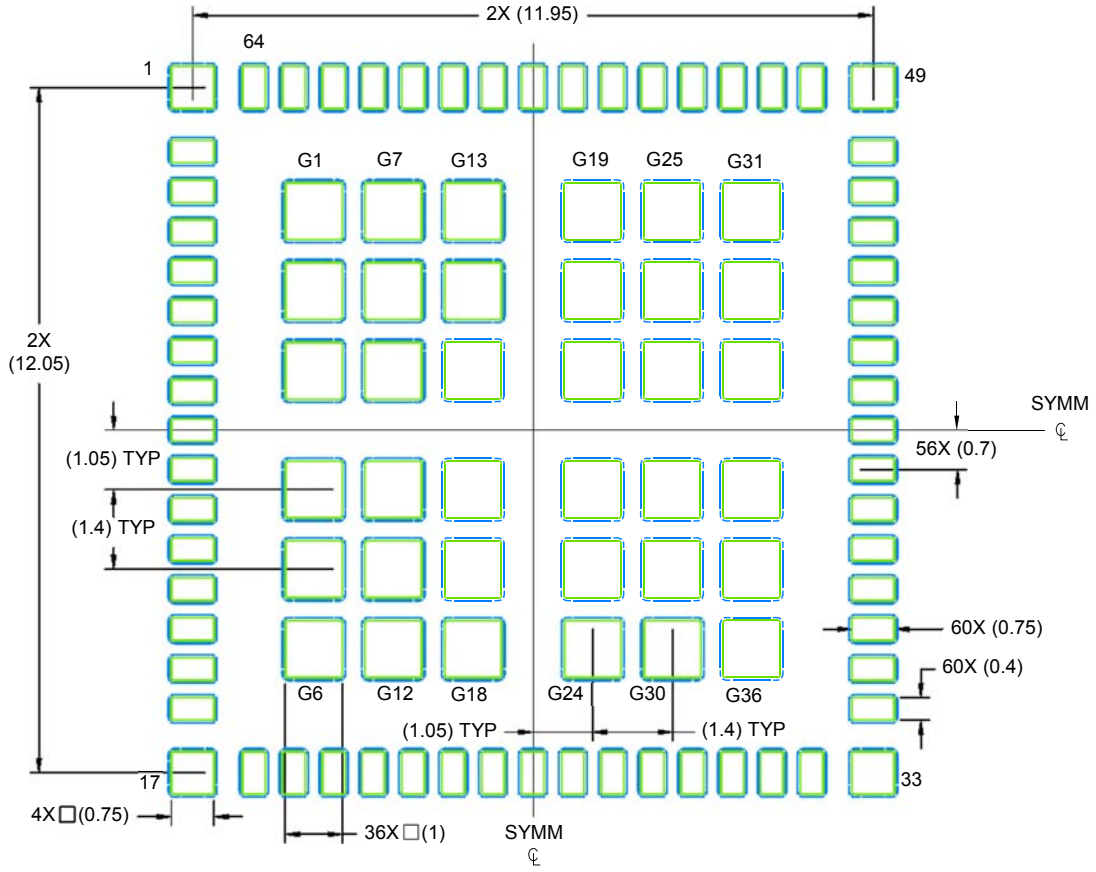
QUAD FLAT MODULE



4221006/B 10/2016

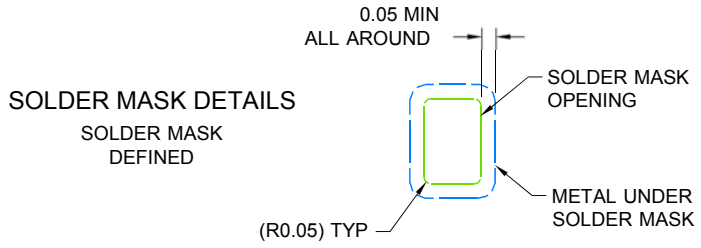
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 8X



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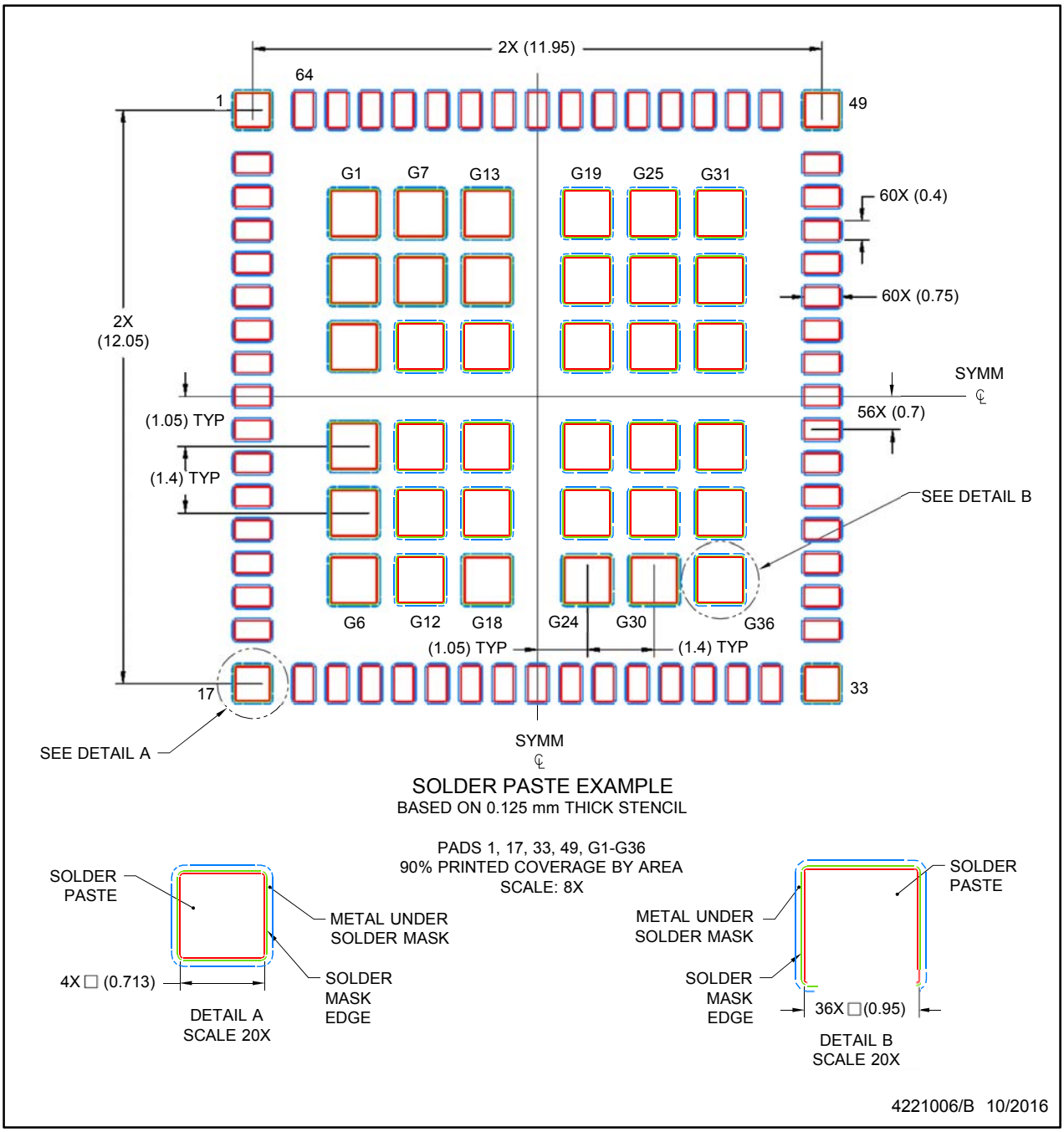
NOTES: (continued)

4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommend。